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**CS223 – Digital Design**

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//Behavioral SystemVerilog module for 2-to-4 decoder and a testbench for it.

module decoder2\_4(input logic [1:0] xin,

output[3:0] yout );

always\_comb

case(xin)

2’b00: yout=4’b0001;

2’b01: yout=4’b0010;

2’b10: yout=4’b0100;

2’b11: yout=4’b1000;

endcase

endmodule

//Testbench

**initial  
begin** // if more than one statement it must be put begin ...end block

A=0; B=0;  
# 10 A=1;  
# 10 A=0; B=1;  
**end**

**initial  
begin**D=3’b000;  
**repeat(7)** // repeat following statement 7 times # 10 D=D+3’b001;

**end**

//////Behavioral SystemVerilog module for 2-to-1 multiplexer.

module mux2 (input data0\_i, data1\_i, select\_i,  
 output data\_o;

assign data\_o = (select\_i ==0) ? data1\_i : data0\_i;

endmodule

//////Behavioral SystemVerilog module for 4-to-1 multiplexer by using three 2-to-1

module mux4 ( input logic [ 3:0] d0, d1, d2, d3,

input logic [ 1:0] s,

output logic [3:0]y);

assign = s[1] ? (s[0] ? d3 : d2 )

: (s[0] ? d1 : d0 );

endmodule

////Structural System Verilog module of 8-to-1 MUX by using two 4-to-1 MUX modules.

module mux2\_8 (input logic [7:0] d0, d1,

input logic s,

output logic [7:0] y;

mux2 lsbmux ( d0 [ 3:0 ] , d1 [ 3: 0 ], s, y[ 3 : 0 ] );

mux2 msbmux ( d0 [ 7 : 4], d1 [ 7 : 4 ], s, y [ 7 : 4 ] );

endmodule