BİLKENT UNIVERSITY

COMPUTER SCIENCER

CS-224 COMPUTER ARTCHITECTURE

DESIGN REPORT

LAB 5

SECTION 1

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23.12.2020

B-C) List of Hazards and Solutions

Control Hazards:

Branch hazard: It generally caused because of branch problems. Branching prediction is done in the Memory stage, which causes lag

Affected Stages: 2 instruction fetched.

When happened : There is needed a branch decision

What is solution: Flushing the fetched instructions and doing branch decision in earlier stages can be solution.

Data Hazards:

Load-use hazard: Instructions that require reading from memory cannot read data.Affected Stages: 2 instruction fetched.

When happened : When we are decoding the using instruction

What is solution: using decoding again,

Compute-use hazard: It can happen when pipeline changes are made when data transactions are read and made.

Affected Stages: The decoding stage of the instruction that follows the instruction that the performed calculation will return an incorrect data value.

When happened : Occurs when there is a request for access to previous instructions that have not yet been written.

What is solution: Problem can actually be solved with Data forwarded to the next instructions Execute stage.

Load-Store hazard: When trying to store data in a memory location immediately after being loaded from memory

Affected Stages: The memory stage of the instruction is affected.

When happened : Usage of lw and sw instructions.

What is solution: This can be solved by, stalling, which allows loading from memory until the next instruction retrieves data from the same record during the decoding phase.

D)

1)Forwarding:

if ((rsE!=0) & (rsE== writeRegW) & RegWriteW)

ForwardAE=01

Else if ((reE!=0) & (rsR== WriteRegM) & RegWriteM)

ForwardAE=10

Else

ForwardAE=00

2)Stallling and Flushing

lwstall = ((rsD == rtE) | (rtD == rtE)) & MemtoRegE

StallD = lwstall = StallF = FlushE