Department of Mechanical Engineering
MECHENG 371 – Digital Circuit Design
Project – Simple Calculator (15%)
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Introduction - Simple calculator

The purpose of this project is to design and implement a simple calculator in FPGA chip that performs four operations: addition, subtraction, multiplication and division of two decimal integers, where each decimal number can be up to two digits (i.e. -99 to 99). The design should show the result of division as an integer quotient and remainder. The implementation uses DE2 FPGA prototyping board with some simple but common interfaces: 4x4 matrix keypad and 7-segment displays, for entering inputs into the chip and displaying outputs from the chip, respectively. The DE2 board also provides light emitting diodes (LEDs), which can be turned on and off and may be used optionally for debugging purposes and understanding the current status of the calculator circuit.

The conceptual illustration of the calculator is presented in Figure 1. The 4x4 matrix keypad consists of 16 keys. Keys 0 to 9 on the keypad are used for entering decimal values, whereas keys A to F can be assigned for different operations as specified by the designer. Users can enter a decimal number of up to two digits by pressing the number keys (0 to 9) one after another. The decimal values of these keys, the decimal digits, will be displayed on the 7-segment display. The entered digits will be stored in a register and always memorises the last two entered digits; hence entering more than two digits will erase the oldest digit. These two digits represent the first operand of the operation, which will be entered next. After entering the first operand, user can press one of the operation keys: C for division, D for multiplication, E for subtraction and F for addition operation. After entering the operation, the second operand can be entered and displayed on the 7-segment display in the same way as the first operand. Once both operands and the operation are entered, user can press the execute key “B (=)” to perform the actual operation and display the result on the 7-segment display. If user wants to perform another operation, clear key “A” should be pressed to clear internal registers and 7-segment display.

Majority of the design components should be implemented in Verilog and only the top level integration can be performed on the block (component) level. A simplified calculator block diagram is shown in Figure 2. This project is marked out of 15%. This project will be done by groups of three students and has the following deliverables and deadlines:

1. Lab interview and demonstration (8% of the final grade), 14th October lab time (3-6pm).
2. The implementation project folder compressed in a ZIP format, containing
    - All the source files that allows us to compile and synthesis your project,
    - An electronic version of the report per group (at most 5 pages),

    The implementation is worth 7% of the final grade (2% code and 5% report).

More details about the deliverables and submission method will be given during the lectures.

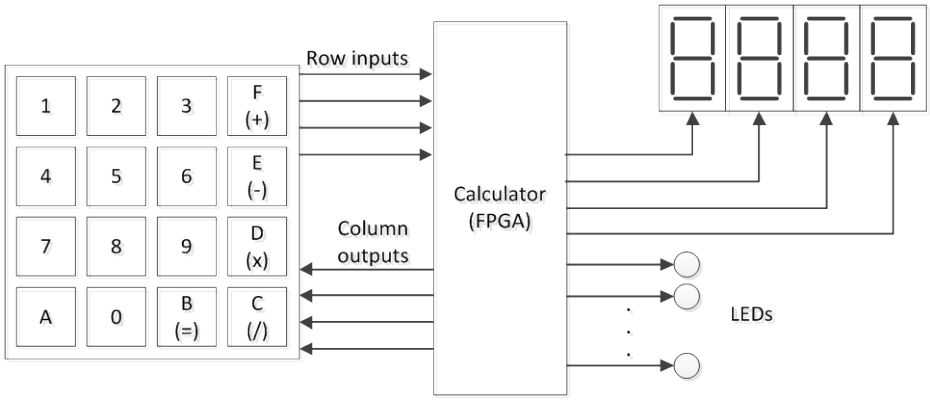

Fig. 1 A conceptual diagram of the simple calculator.

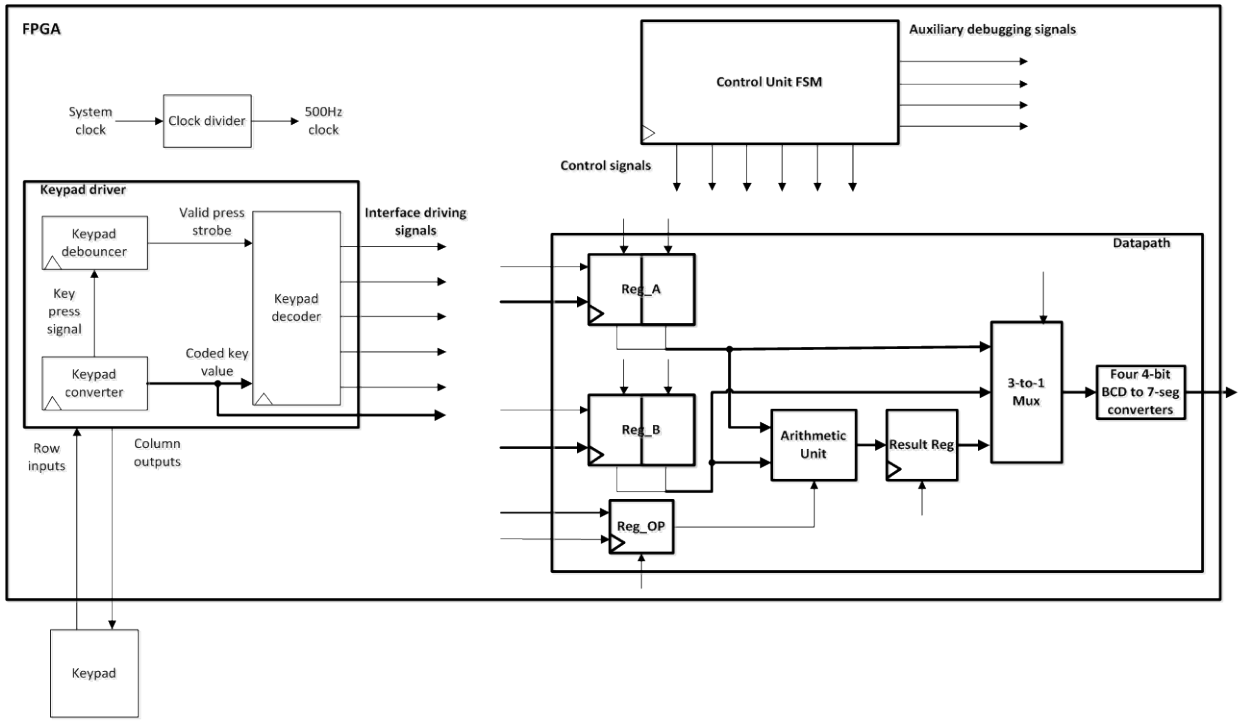

Fig. 2 The simple calculator design overview.