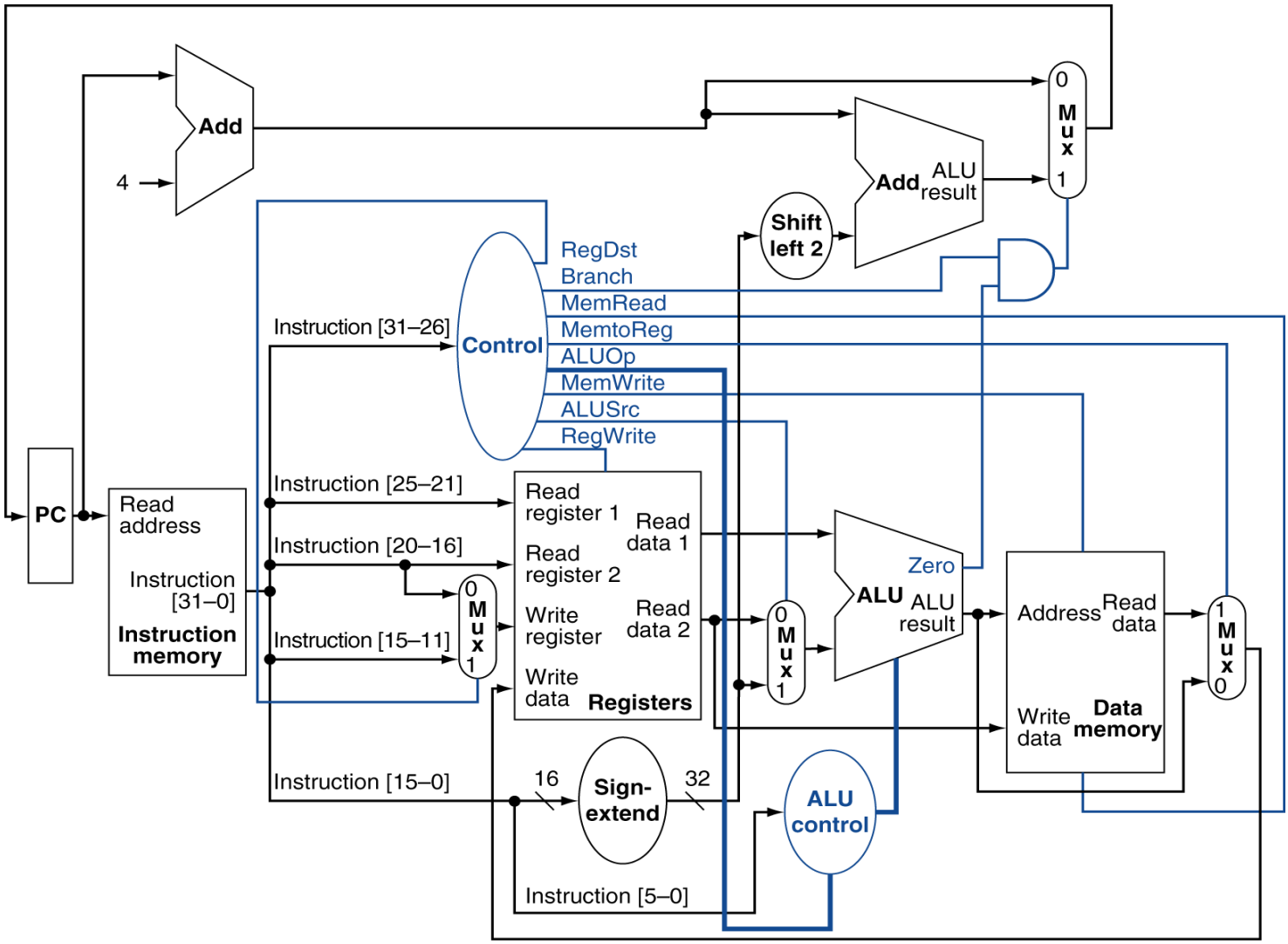
COMP3401 Computer Organization

Fall 2023– HW#4 **Due 20.12.2023**

Hw#4
Datapath&Control

1) Datapath for MIPS single clock cycle processor is shown below:



The memory configuration and register values are given in the following tables.

Registers		Memory	
$t7	101	10000	2
$s2	9	10004	1
$t6	8	10008	6
$s0	10000	1000C	8

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Write the values (decimal) that will be assigned or created during the consecutive executions of the following instructions shown below. (Each space graded 1 pts, no partial)

Instruction	Write Register	Write Data Regfile	ALUSrc	Branch	ALU input 2	MemRead	RegDst	Regwrite	Read Register 2
addi $s0,$s0,4	16	10004	1	0	**4**	**X (dont care)**	0	1	No value
sw $t7, 0($s0)	**No value**	**No value**	1	0	**0**	**0**	**X(dont care)**	**X(dont care)**	15
and $t6,$t6,$s2	18	17	0	0	**9**	**X (dont care)**	1	1	18
add $t7,$t7,$t6	15	109	0	0	**8**	**X(dont care)**	1	1	14
beq $t7,$t6,12	**X(dont care)**	**X(dont care)**	0	1	12	**X(dont care)**	**X(dont care)**	**X(dont care)**	14
lw $s2, 8($s0)	18	6	1	0	8	1	0	1	No value