Due 7.1.2024

Hw#5
Datapath&Control and Pipeline

1) For the following code draw multicycle pipeline diagram, identify hazards, show if there is pipeline stall or forwarding.

$t0 = 10, $t3 = 1016, $t5 = -2

Address	Value
1012	15
1016	47
1020	-5
1024	3

Lw $t5, 4($t3)
Addi $t3, $t5, 13
Sub $t0, $zero, $t3
Sw $t0, 16($t3)
Or $t3, $t0, $t5
And $t5, $t3, $t3

The value of $t5 in **Lw** operation will be used in the **addi** operation.
The value of $t3 in **addi** operation will be used in the **sub** operation.
The value of $t0 in **sub** operation will be used in the **Sw** operation.
The value of $t3 in **or** operation will be used in the **and** operation.

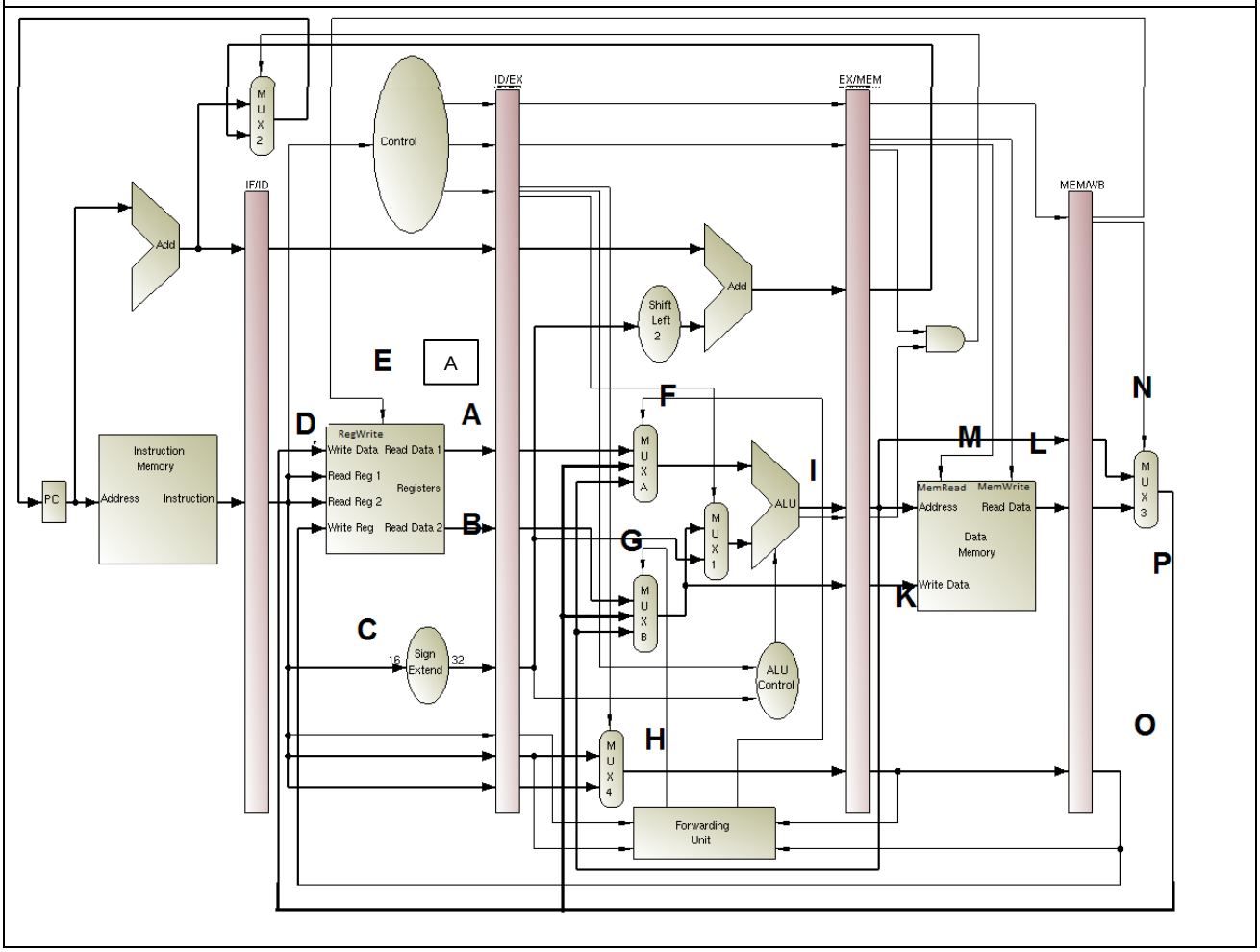
All hazards in this example are data hazards.

a) FIRST DRAW MULTICYCLE PIPELINE DIAGRAM. IDENTIFY DEPENDENCIES. INDICATE IF A REGISTER IS FORWARDED or CAUSES STALL. Example

	Cc 1	Cc 2	Cc 3	Cc 4	CC 5	Cc 6	Cc 7	Cc 8	Cc 9	Cc 10	Cc 11	Cc 12	Write the name of register causing		
Instruction	Pipeline Stages												Stall	Fwd Rs	Fwd Rt
ex $t5,$t1,$t2	IF	ID	EX	M	WB									$t2*	
Lw $t5, 4($t3)	IF	ID	EX	M	WB										
		-	-	-	-	-							$t5		
Addi $t3, $t5, 13			IF	ID	EX	M	WB								$t5*
Sub $t0, $zero, $t3				IF	ID	EX	M	WB							$t3*
Sw $t0, 16($t3)					IF	ID	EX	M	WB						$t0*
Or $t3, $t0, $t5						IF	ID	EX	M	WB					$t0*
And $t5, $t3, $t3							IF	ID	EX	M	WB			$t3*	$t3*

b) Place the instructions below at the forwarding clock cycle:

Instruction				
Sw $t0, 16($t3)	Sub $t0, $zero, $t3	Addi $t3, $t5, 13	empty	Lw $t5, 4($t3)



A (read data 1): **0** **B** (read data 2):**1016** **C**(sign extend input): **X**
D(Write data):**1016(the value of $t0)** **E**(RegWrite):**1**
F(Mux A): **0** **G**(Mux B): **X** **H**(Mux 4 output): **0** **I**(ALU output): **11**
K(Write Data): **empty** **L**(Mem write): **empty** **M**(Mem read): **empty**
N(Mux 3): **1** **P**(Mux 3 output): **-5** **O**(MEM/WB) write reg: **1**