Lab 1

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1. 實作過程

- lab1_1
  In this lab, the goal is to write a 4-bit shifter with 3 inputs a (4-bit), b, dir, and a ouput d (4-bit). If the dir is “0”, then the output will a << b. Otherwise, the output will be a >> b. Therefore, I add those two conditions in the always block directly.

```
1  `timescale 1ns/100ps
2  module lab1_1(a, b, dir, d);
3      input [3:0] a;
4      input [1:0] b;
5      input dir;
6      output reg [3:0] d;
7      always @* begin
8          if(dir == 1'b0) d = a << b;
9          else if(dir == 1'b1) d = a >> b;
10     end
11 endmodule
```

- lab1_1_t
  TODO 1, In order to instantiate the lab1_1 in the testbench, I write the lab1_1 module and give it a name and parameters. Here I write the parameters in order as the lab1_1.
  TODO 2, To increase the counter by one, which is {a, b, dir}, I assign the counter and plus it “1”.
  TODO 3, The condition here is to check when the direction is “0’ and the b is “1” is correct or not. Which mean I need to shift the input to left by one bit. Therefore, I need the last 3 bits of the input to be the front of the output and add “0” bit to the last bits.
  TODO 4, To set the pass signal to be “0”. I directly assign the pass signal equal to 0 bits by using ‘=’ symbol.

- lab1_2
  In this 4-bit ALU module, the goal is to shift the input a by b and also add or substract a by b. The ALU module has a 2-bit input “aluctr”, which is a multiplexer. For the shifter, since we need to reuse the lab1_1 shifter, I instantitate 2 module from the lab1_1, one for the left shift and the other for right shift. Also I make two 4-bit wire outputs for the each module, left and right. Then I assign the wire output to the ALU output. For the add and substract a by b is similar, only the symbol is different. One is ‘+’ and the other is ‘-’ and assign it to the ALU ouput.

```
lab1_1 lshift (a, b, 1'b0, leftshift);
lab1_1 rshift (a, b, 1'b1, rightshift);
always@* begin
    d = 4'd0;
    case(aluctr)
        2'b00 : d = leftshift;
        2'b01 : d = rightshift;
        2'b10 : d = a + b;
        2'b11 : d = a - b;
    endcase
end
```

2. 學到的東西與遇到的困難

For the reason that it has been a few months I didn't write Verilog, plus my understanding to Verilog is not really good when I was taking the Logic Design class before, I need to review it for a couple hours just to recall what I have learned in the past. After review it, I also still need a lot of try and error in order to finish the lab1 completely.

Since this is the first time I am using Vivado, I am not familiar to it and need time to get to use with it. But thanks to the clear guide by the TAs, I can just follow the step and create a project in Vivado. However, the software is somekind of slow to run and sometimes the loading is just like never ending. I keep force stop the software and re-open it which make it takes a lot of time.

3. 想對老師或助教說的話

None