8 *pn* Junction Diode: Transient Response

At the beginning of the *pn* junction diode discussion, we noted that a complete, systematic device analysis was normally divided into four major segments: modeling of the internal electrostatics, steady state response, small-signal response, and transient response. In this chapter we address the final major segment of the *pn* junction diode analysis, the transient or switching response. In a number of applications a *pn* junction diode is used as an electrical switch. A pulse of current or voltage is typically used to switch the diode from forward bias, called the "on" state, to reverse bias, called the "off" state, and vice-versa. Of prime concern to circuit and device engineers is the speed at which the *pn* junction diode can be made to switch states. Generally speaking, it is during the turn-off transient, going from the on to the off state, where speed limitations are most significant. The subsequent development therefore concentrates on the turn-off transient. Moreover, the diode under analysis is assumed to be ideal. This allows us to convey the basic concepts and principles of transient operation with a minimum of mathematical complexity.

8.1 TURN-OFF TRANSIENT

8.1.1 Introduction

Consider the idealized representation of a switching circuit shown in Fig. 8.1(a). Prior to $t = 0$ the diode is taken to be forward-biased with a steady state forward current, I_F, flowing through the diode. At $t = 0$ the switch in the circuit is rapidly moved to the right-hand position. For use in switching applications, one would like the corresponding diode current to decrease instantaneously from I_F to the small steady-state reverse current consistent with the applied reverse voltage. What one actually observes is sketched in Fig. 8.1(b). Instead of a vanishingly small current, the reverse current immediately after switching is comparable in magnitude to the forward current if $V_R/R_R \sim V_F/R_F$. Subsequently, the current through the diode remains essentially constant at the large $-I_R$ for a limited period of time before eventually decaying to the steady state value. The period of time during which the reverse current remains constant is known as the *storage time* or *storage delay time* (t_s). The total time required for the reverse current to decay to 10% of its maximum magnitude is defined to be the reverse recovery time (t_{rr}), while the recovery time (t_r) is the difference between t_{rr} and t_s. The cited times characterizing the transient are also defined graphically in Fig. 8.1(b).

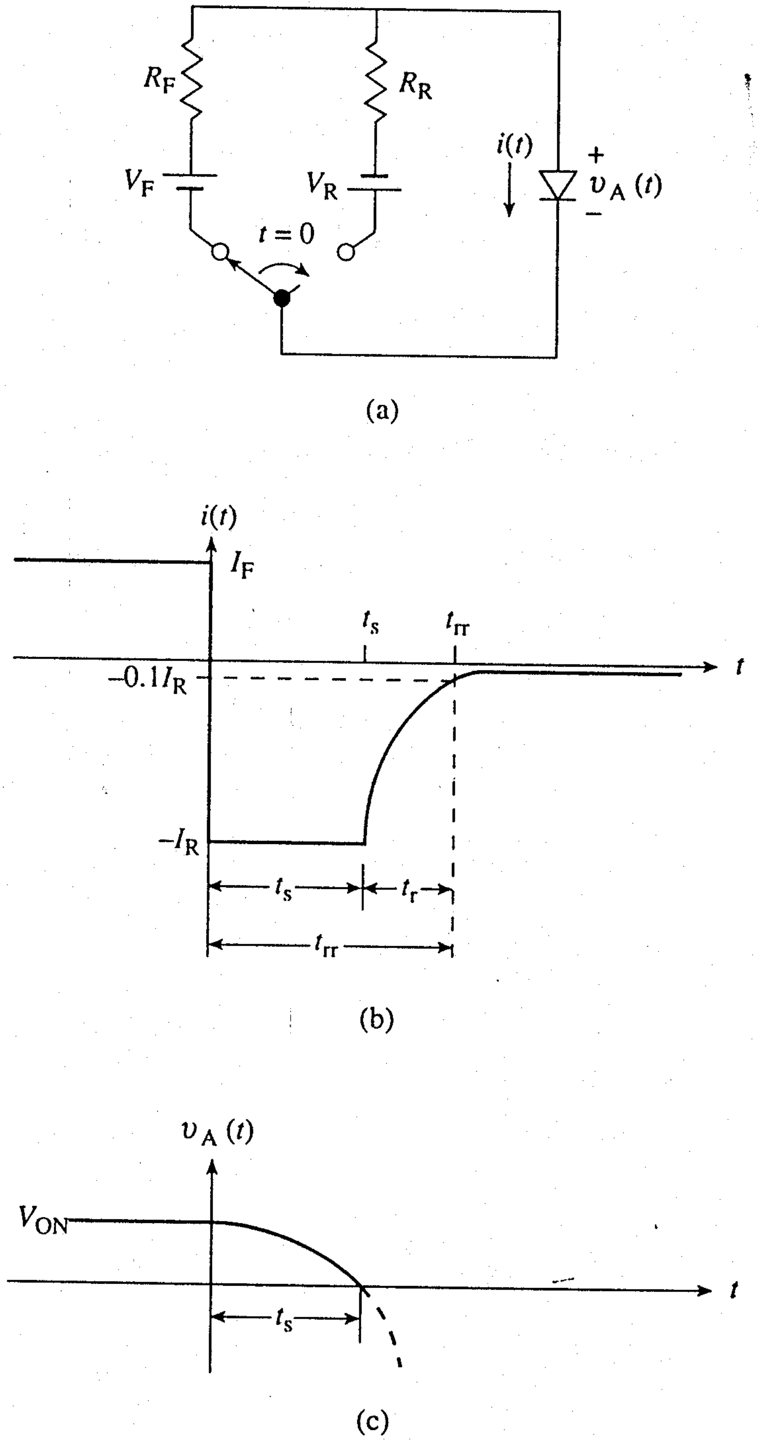


Figure 8.1 The turn-off transient. (a) Idealized representation of the switching circuit. (b) Sketch and characterization of the current-time transient. (c) Voltage-time transient.

The variation of the instantaneous diode voltage (v_A) corresponding to the *i-t* transient is shown in Fig. 8.1(c). Specifically note from the figure that (i) the junction remains forward biased for $0 < t < t_s$ even though the externally applied voltage is such as to reverse-bias the diode, and (ii) the $t = t_s$ point correlates with $v_A = 0$.

In analyzing the transient response, we make the assumption that the battery voltages (V_F and V_R) are large compared to the maximum forward voltage drop (V_{ON}) across the diode. Under the stated assumption

$$I_F = \frac{V_F - V_{ON}}{R_F} \cong \frac{V_F}{R_F} \tag{8.1a}$$

and

$$I_R = \frac{V_R + v_A|_{0<t\leq t_s}}{R_R} \cong \frac{V_R}{R_R} \tag{8.1b}$$

Additionally, the qualitative and quantitative analyses to follow focus on the storage delay portion of the transient. Because the decaying t_r portion is readily distorted by stray capacitance in the measurement circuit, it is t_s that has come to be quoted as the primary figure of merit in characterizing the turn-off transient.

8.1.2 Qualitative Analysis

In looking at the turn-off transient for the first time, a number of questions undoubtedly come to mind. Why is there a delay in going from the on-state to the off-state? Or perhaps better stated, what is the physical cause of the delay? What goes on inside the diode during the transient? How is it the diode remains forward biased for $0 < t < t_s$ even though the applied voltage is such as to reverse bias the diode?

The root cause of the delay in switching between the on and off states is easy to identify. Forward biasing of the diode, as we have noted previously several times, causes a build-up or storage of excess minority carriers in the quasineutral regions immediately adjacent to the depletion region. When the diode is reverse biased, on the other hand, there is a deficit of minority carriers in the near-vicinity of the depletion region. Simply stated, to progress from the on-state to the off-state, the excess minority carriers pictured in Fig. 8.2 must be removed from the two sides of the junction. The storage delay time derives its name from the fact that the majority of the stored charge is being removed from the diode during the t_s portion of the transient.

As the charge control analysis of Subsection 6.3.1 indicated, removal of the excess minority carrier charge in the quasineutral regions can be achieved in two ways. For one, the carriers can be eliminated in place via recombination. Recombination is of course not instantaneous; several minority carrier lifetimes would be required to go from the on-state to the off-state if recombination were the sole means of carrier removal. The other method

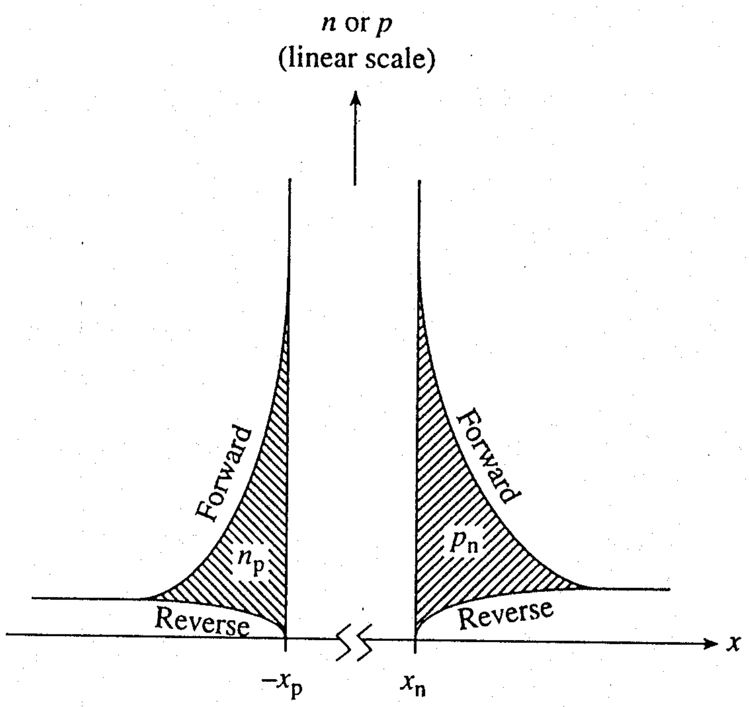


Figure 8.2 Stored minority carrier charge leading to the delay in switching between the on and off states. The reverse and forward minority carrier concentrations are plotted simultaneously on a linear scale with the x coordinates matched at the depletion region edges. The break in the x-axis inside the depletion region acknowledges a difference in the forward-bias and reverse-bias depletion widths. The cross-hatched areas identify minority carriers that must be removed for switching to be complete.

of reducing the carrier excess is by a net carrier flow out of the region. Once the sustaining external bias is removed, the minority carriers can simply flow back to the other side of the junction where they become majority carriers. This reverse injection could conceivably occur at a very rapid rate. The time required to drift back across the depletion region is only $W/\bar{v}_d \sim 10^{-10}$ sec, where $\bar{v}_d$ is the average drift velocity in the depletion region. However, the number of minority carriers removed per second is limited by the switching circuitry. The maximum reverse current that can flow though the diode is approximately $V_R/R_R = I_R$. The smaller I_R, the slower the carrier removal rate. A very rapid transient could be obtained by replacing R_R with a short, but such a procedure would likely lead to a current flow exceeding device specifications and damage to the diode. Summarizing, there are two mechanisms, recombination and reverse current flow, that operate to remove the excess stored charge. Neither mechanism can safely remove the charge at a sufficiently rapid rate to be considered instantaneous. Hence one observes a delay in going from the on to the off state.

We have yet to answer the question how it is the diode remains forward biased during the $0 < t < t_s$ portion of the transient. To answer the question, consider the progressive removal of the hole excess on the n-side of a p^+-n junction as envisioned in Fig. 8.3. Note from the figure that during the $t < t_s$ stages of the decay the minority carrier concentration

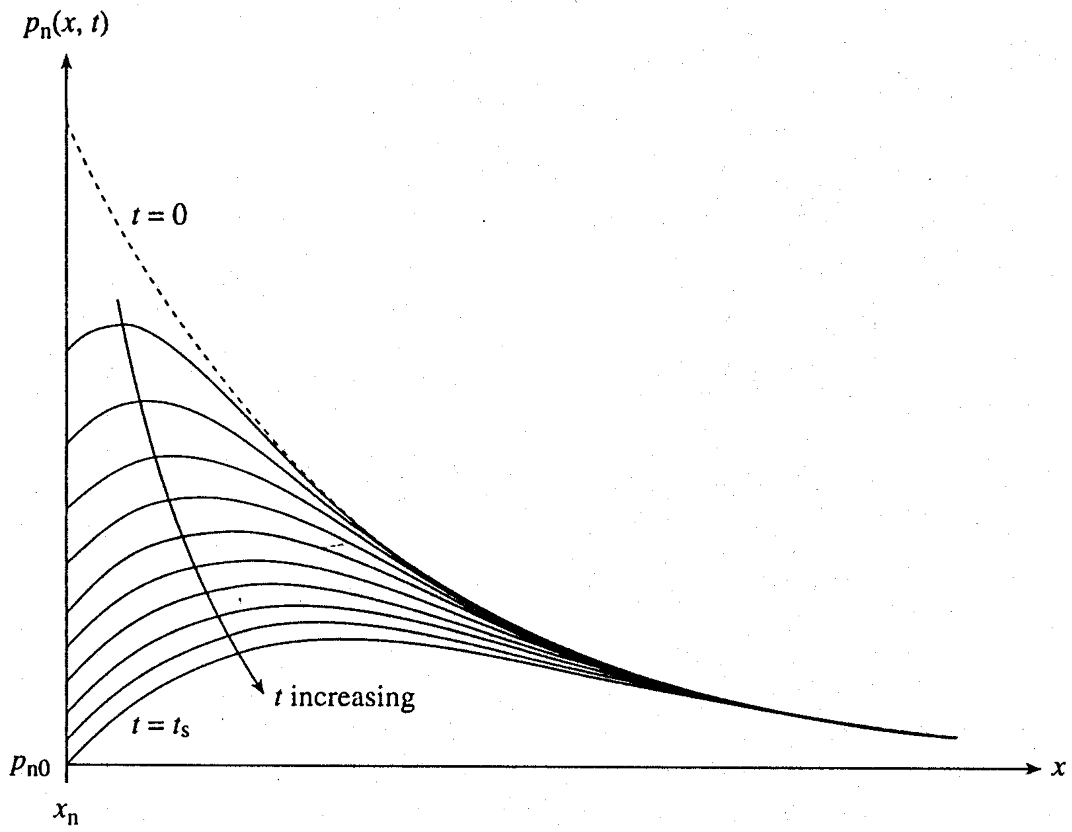


Figure 8.3 Decay of the stored hole charge inside a p^+-n diode as a function of time for $0 \leq t \leq t_s$.

at the edges of the depletion region ($x = x_n$) is greater than the equilibrium value. In Chapter 6 we established depletion edge boundary conditions that tied the minority carrier concentrations at the depletion region edges to the applied voltage. These same boundary conditions apply under transient conditions with $V_A \to v_A$. Thus a $v_A > 0$ indicates there is an excess of minority carriers adjacent to the edges of the depletion region. Pertinent to the present discussion, the reverse is also true—a minority carrier excess above the equilibrium value at the edges of the depletion region implies the junction is forward biased. Or stated another way, it is the residual carrier excess at the edges and inside the depletion region that maintains the forward bias across the junction. It is only when the hole concentration at $x = x_n$ drops below the equilibrium value that the diode becomes reverse biased.

Finally, a comment is in order concerning the slope of the Fig. 8.3 curves at $x = x_n$. In an ideal p^+-n diode, $i = AJ_P(x_n) = -qAD_P d\Delta p_n/dx|_{x=x_n}$ or

$$\left.\frac{d\Delta p_n}{dx}\right|_{x=x_n} = \left\{\begin{array}{c}\text{slope of } \Delta p_n(x) \text{ or } p_n(x) \\ \text{versus } x \text{ plot at } x = x_n\end{array}\right\} = -\frac{i}{qAD_P} \tag{8.2}$$

All $t > 0$ concentration curves must therefore slope upward at $x = x_n$ because $i < 0$. Moreover, the slopes at $x = x_n$ must be the same for all $t > 0$ curves in Fig. 8.3 because $i = -I_R$ = constant during the $0 < t \le t_s$ portion of the transient.

Exercise 8.1

P: Use the qualitative insight gained into the diode response to predict how key factors are expected to affect the observed i–t transient. The accuracy of the predictions will be checked after working out the quantitative theory.

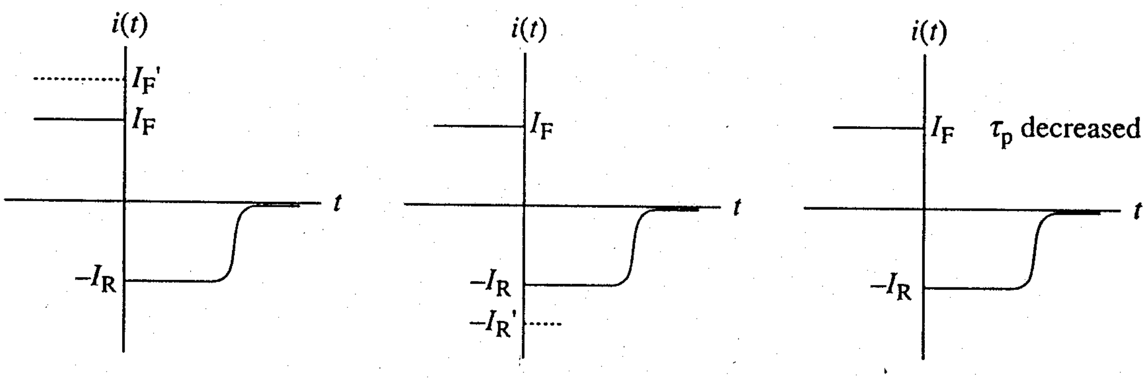
The figures after the problem statement contain a base-line sketch of an i–t transient. Using a dashed line, sketch the expected modification to the base-line transient if as indicated on the figures:

(a) I_F is increased to I_F'.

(b) I_R is increased to I_R'.

(c) τ_p is decreased (made shorter).

Explain how you arrived at the modified i–t sketches.



(a) (b) (c)

S: The reasoning leading to the graphical answers presented in Fig. E8.1 are as follows:

(a) Increasing I_F increases the stored charge inside the diode. Since the stored charge is increased and the removal rate is unchanged, it will take longer to remove the stored charge. t_s is expected to increase.

(b) Increasing I_R increases the rate at which the stored charge is removed by the reverse current flow. Thus in this case the storage delay time is reduced.

(c) A shorter minority carrier lifetime increases the carrier recombination rate and will therefore decrease t_s.

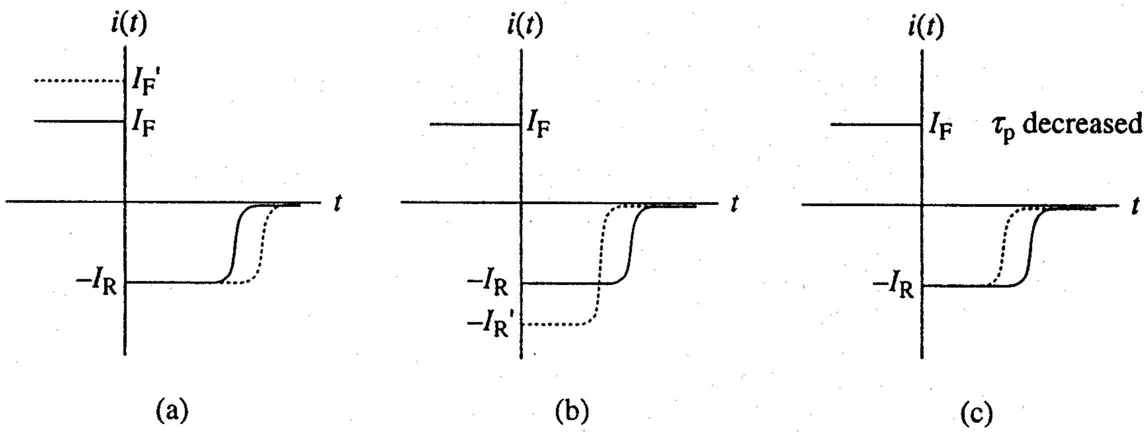


Figure E8.1

8.1.3 The Storage Delay Time

Quantitative Analysis

We seek a quantitative relationship that can be used to predict and compute the storage delay time, t_s. To simplify the analysis, we treat an ideal p^+-n step junction diode and make use of the charge control approach. The electron charge stored on the p-side of a p^+-n junction is of course negligible compared to the hole charge (Q_P) stored on the n-side. We also know that $i = i_{DIFF}$ in an ideal diode and, referring to Eq. (6.56) in Subsection 6.3.1,

$$\frac{dQ_P}{dt} = i - \frac{Q_P}{\tau_p} \tag{8.3}$$

Working toward a solution, we note that $i = -I_R =$ constant for times $0^+ \leq t \leq t_s$, where $t = 0^+$ is an instant after switching. Thus Eq. (8.3) simplifies to

$$\frac{dQ_P}{dt} = -\left(I_R + \frac{Q_P}{\tau_p}\right) \qquad \ldots 0^+ \leq t \leq t_s \tag{8.4}$$

The Q_P and t variables in Eq. (8.4) can be separated and an integration performed over time from $t = 0^+$ to $t = t_s$. We obtain

$$\int_{Q_P(0^+)}^{Q_P(t_s)} \frac{dQ_P}{I_R + Q_P/\tau_p} = -\int_{0^+}^{t_s} dt = -t_s \tag{8.5}$$

giving

$$t_s = -\tau_p \ln\left(I_R + \frac{Q_P}{\tau_p}\right)\Bigg|_{Q_P(0^+)}^{Q_P(t_s)} = \tau_p \ln\left[\frac{I_R + Q_P(0^+)/\tau_p}{I_R + Q_P(t_s)/\tau_p}\right] \tag{8.6}$$

The $Q_P(0^+)$ and $Q_P(t_s)$ appearing in Eq. (8.6) must be dealt with to complete the derivation. $Q_P(0^+)$ proves to be readily expressed in terms of known parameters. Because charge cannot be eliminated instantaneously, $Q_P(0^+) = Q_P(0^-)$. However, prior to switching, $dQ_P/dt = 0$ and $i = I_F$. It therefore follows from Eq. (8.3) that

$$I_F = \frac{Q_P(0^-)}{\tau_p} = \frac{Q_P(0^+)}{\tau_p} \tag{8.7}$$

$Q_P(t_s)$, the stored charge remaining at $t = t_s$, poses more of a problem. Wishing to err on the conservative side (i.e., obtain an estimate of t_s that is too large), we take $Q_P(t_s)$ to be approximately zero. Eliminating $Q_P(0^+)$ in Eq. (8.6) using Eq. (8.7) and setting $Q_P(t_s) = 0$, we conclude

$$\boxed{t_s = \tau_p \ln\left(1 + \frac{I_F}{I_R}\right)} \tag{8.8}$$

Equation (8.8) is noted to be in total agreement with the qualitative predictions of Exercise 8.1. t_s increases with increasing I_F, decreases with increasing I_R, and is directly proportional to τ_p. As a point of information, a more precise analysis, based on a complete $\Delta p_n(x, t)$ solution and properly accounting for the residual stored charge at $t = t_s$, gives[4]

$$\boxed{\mathrm{erf}\left(\sqrt{\frac{t_s}{\tau_p}}\right) = \frac{1}{1 + \dfrac{I_R}{I_F}}} \tag{8.9}$$

Although considerably different in appearance, the Eq. (8.9) solution is likewise noted to be in total agreement with the qualitative predictions of Exercise 8.1.

Measurement

In both Eqs. (8.8) and (8.9) t_s is directly proportional to τ_p. Moreover, the only other parameters affecting t_s are the currents I_F and I_R controlled by the switching circuitry. This suggests it should be a relatively simple matter to determine the minority carrier lifetime on the lightly doped side of an asymmetrical junction by measuring the turn-off i–t transient, noting the storage delay time, and computing τ_p from Eq. (8.8) or Eq. (8.9).

A measurement system that can be used to observe the transient response of diodes with lifetimes in the μsec range is pictured in Fig. 8.4. The measurement circuit in combination with the Tektronix PS5004 d.c. power supply and FG5010 function generator simulates the switching circuit of Fig. 8.1(a). To first order, the d.c. bias applied at the power supply node determines I_F. Rapid switching of the voltage applied across the test diode is

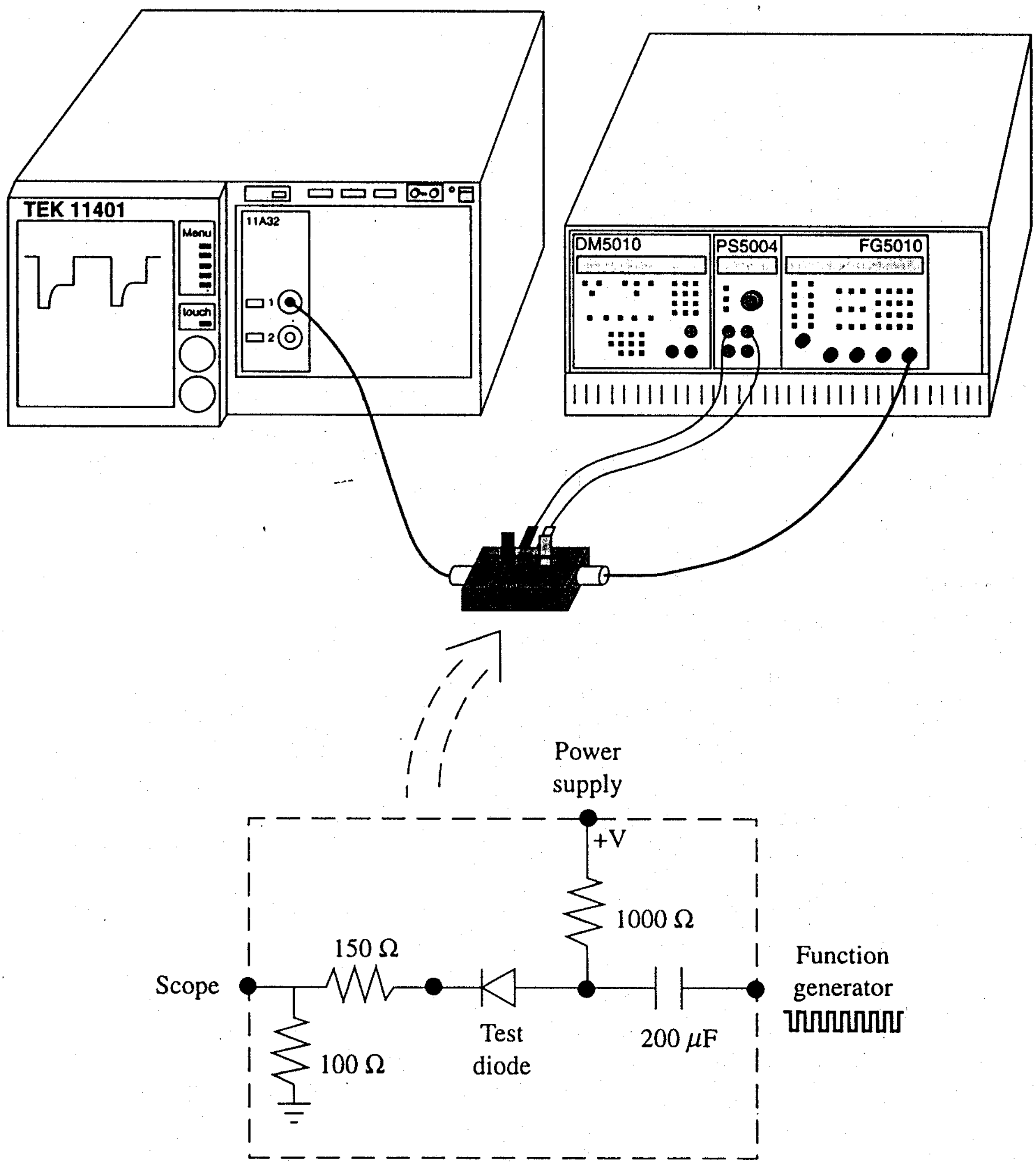


Figure 8.4 Transient response measurement system.

provided by the negative-going square-wave pulse derived from the function generator. Because the charge on the plates of the capacitor cannot change instantaneously, the voltage drop across the capacitor must remain constant as the output of the function generator goes from 0 V to the preselected negative value. This forces the voltage on the diode side of the capacitor to decrease by an amount equal to the peak-to-peak value of the square-wave pulse. Subsequent current flow will tend to discharge the capacitor, but the circuit RC time constants are 10^{-2} seconds or greater, making the discharge negligible during a typical pulsing period. A voltage proportional to the instantaneous current through the test diode,

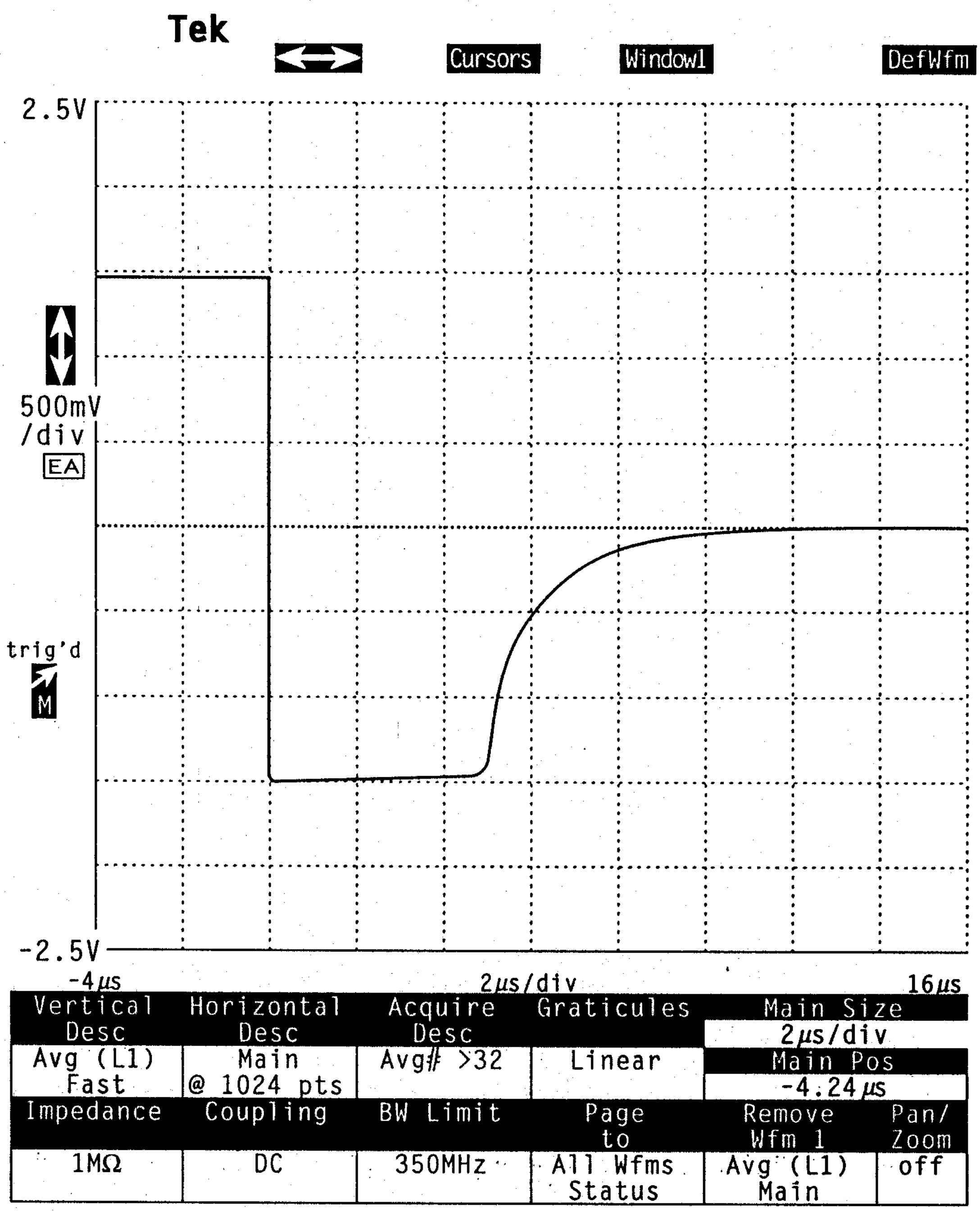


Figure 8.5 Sample current-time turn-off transient. Output derived from the Fig. 8.4 measurement system. (The y-axis display voltage is directly proportional to the instantaneous current through the diode.)

the *i–t* transient, is monitored using the Tektronix 11401 Digitizing Oscilloscope. Waveforms displayed on the 11401 can be analyzed in place, or the screen data can be sent to a printer for subsequent examination.

A sample measured *i–t* transient is reproduced in Fig. 8.5. As extracted from the response curve, $I_R/I_F \cong 1.0$ and $t_s \cong 5.0$ μsec. One deduces a $\tau_p = t_s/\ln(1 + I_F/I_R) =$ 7.2 μsec employing Eq. (8.8) and a $\tau_p = 22$ μsec utilizing Eq. (8.9). A more accurate determination of the lifetime, and a check as to whether the theory properly models the diode under test, is obtained by varying the I_R/I_F ratio and choosing the τ_p yielding the best fit to the normalized t_s/τ_p versus I_R/I_F plot shown in Fig. 8.6. The dashed and solid lines in Fig. 8.6 were computed employing Eqs. (8.8) and (8.9), respectively. Experimental

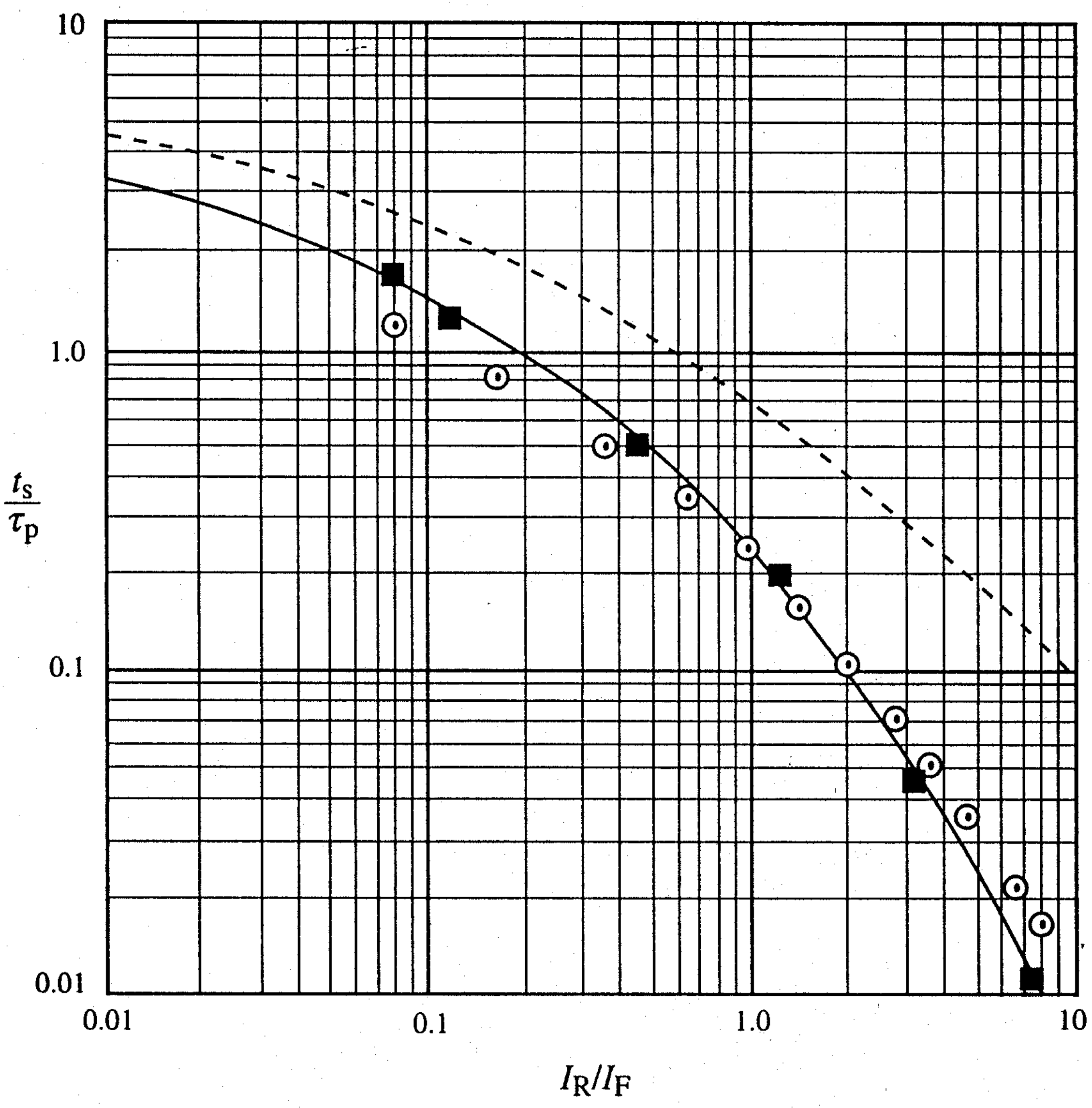


Figure 8.6 Theoretical and measured storage delay times normalized to τ_p versus the reverse to forward current ratio. The dashed line was computed using Eq. (8.8) and the solid line using Eq. (8.9). Experimental data are from a 1N91 Ge diode (■) and a 1N4002 Si diode (⊙).

data from a 1N91 Ge diode and a 1N4002 Si diode have also been added to Fig. 8.6. The Ge diode data can be very closely matched to the more exacting theory if one employs $\tau_p =$ 14.5 μsec. The Si diode data, however, deviates from the predicted dependence. No value of τ_p can be chosen to fit both the upper and lower ends of the curve. Si diodes, it must be remembered, are seldom ideal diodes as assumed in the derivation of Eqs. (8.8) and (8.9).

8.1.4 General Information

We conclude the discussion of the turn-off transient with a few observations of a practical nature. First, as a general rule $t_s \sim \tau_p$ (or τ_n). Increasing the I_R/I_F ratio decreases t_s below τ_p as is obvious from Fig. 8.6, but more often than not there are constraints that limit the size of the I_R/I_F ratio. Another approach to achieve a rapid switching response is to build diodes with short minority carrier lifetimes. Since τ_n and τ_p are proportional to $1/N_T$, where N_T is the R–G center concentration, the minority carrier lifetime can be decreased by the intentional introduction of R–G centers during the fabrication of the diode. The reduction of the minority carrier lifetime in Si devices is typically achieved by diffusing gold into the Si. There is a limit, however, to the R–G center concentration that can be added to a diode. While a shorter lifetime makes for more rapid switching, it also proportionally increases the R–G current ($I_{R\text{-}G} \propto 1/\tau_0$)—a high R–G center concentration may increase the off-state current to unacceptable levels. R–G center concentrations approaching the donor or acceptor concentrations also affect the diode electrostatics. In any event, there is no need for *pn* junction diodes with extremely large R–G center concentrations. Other devices with fewer stored carriers, such as the bipolar junction transistor and the metal-semiconductor diode (both addressed in later chapters), are available for use when the application requires subnanosecond switching times.

Finally, mention should be made of the *step-recovery* or *snap-back* diode. The response of the step-recovery diode is special in that the t_r portion of the transient is very short, ~1 nsec. With a storage delay time ~1 μsec, the reverse current part of the *i–t* transient looks like a step, rapidly "snapping back" to the steady state value after reaching $t = t_s$. Step-recovery diodes are used as pulse generators and high-order, single-stage harmonic generators. In fabricating the diodes, a narrow, lowly doped region is sandwiched between heavily doped *p* and *n* regions. Formed by employing epitaxial techniques, the junctions in this *p-i-n* type structure are required to be very abrupt. The special doping profile causes the minority carrier charge to be stored very close to the edges of the depletion region. This facilitates almost complete removal of the charge by the end of the storage delay time. With little additional charge to be removed after reaching $t = t_s$, the current drops abruptly to the steady state value.

8.2 TURN-ON TRANSIENT

The turn-on transient occurs when the diode is switched from the reverse-bias off-state to the forward-bias on-state. The transition can be accomplished with a current pulse, a voltage pulse, or a mixture of the two pulses. Because of its simplicity and utilization in prac-

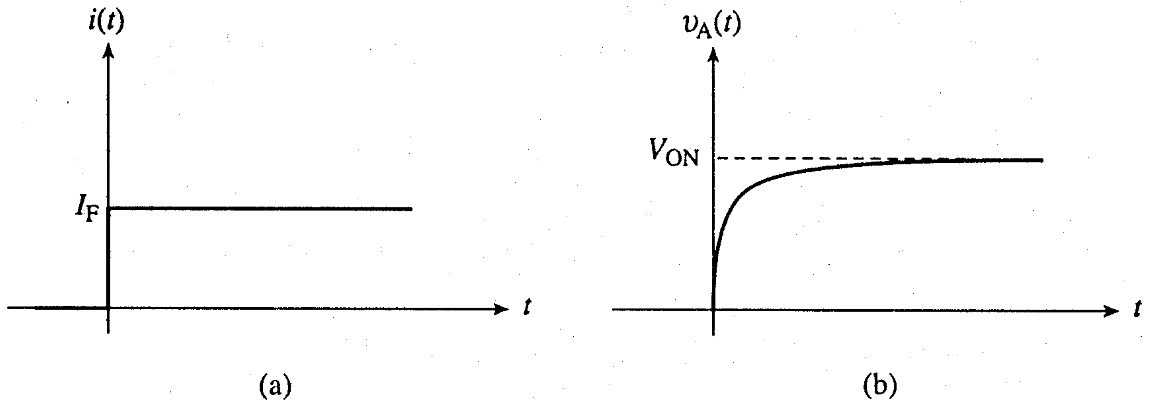


Figure 8.7 Turn-on transient assumed to start from $i = 0$: (a) current pulse; (b) voltage-time response.

tical circuits, we consider herein the case where a current pulse is used to switch the diode into the on state.

When the diode current is changed instantaneously from the prevailing reverse bias value to a constant forward current I_F, the voltage drop across the diode, $v_A(t)$, monotonically increases from the V_{OFF} at $t = 0$ to V_{ON} at $t = \infty$. The first stage of the response from $t = 0$ to the time when $v_A = 0$ is extremely short in duration. The few minority carriers needed to raise the junction voltage to zero are rapidly injected across the depletion region. Majority carrier rearrangement also acts quickly to shrink the depletion width to its zero-bias value. The short duration of the first portion of the transient allows us to act as if the diode were being pulsed from $i = 0$ to $i = I_F$ at $t = 0$ as depicted in Fig. 8.7(a). Figure 8.7(b) shows the corresponding voltage response assumed to start at $v_A = 0$.

In seeking a quantitative solution for $v_A(t) \geq 0$, we again take the device under analysis to be an ideal p^+-n step junction diode and make use of the charge control approach. The envisioned growth of the stored n-side hole charge with time is pictured in Fig. 8.8. Note from the figure that $Q_P = 0$ at $t = 0$ consistent with initiating the transient at $v_A = 0$. Since $i = I_F$ throughout the turn-on transient, the Eq. (8.3) relationship for the stored hole charge reduces to

$$\frac{dQ_P}{dt} = I_F - \frac{Q_P}{\tau_p} \tag{8.10}$$

Separating variables and integrating from $t = 0$ when $Q_P = 0$ to an arbitrary time t yields

$$\int_0^{Q_P(t)} \frac{dQ_P}{I_F - Q_P/\tau_p} = \int_0^t dt' = t \tag{8.11}$$

or upon evaluating the Q_P integral

$$t = -\tau_p \ln\left(I_F - \frac{Q_P}{\tau_p}\right)\Bigg|_0^{Q_P(t)} = -\tau_p \ln\left[1 - \frac{Q_P(t)}{I_F \tau_p}\right] \tag{8.12}$$

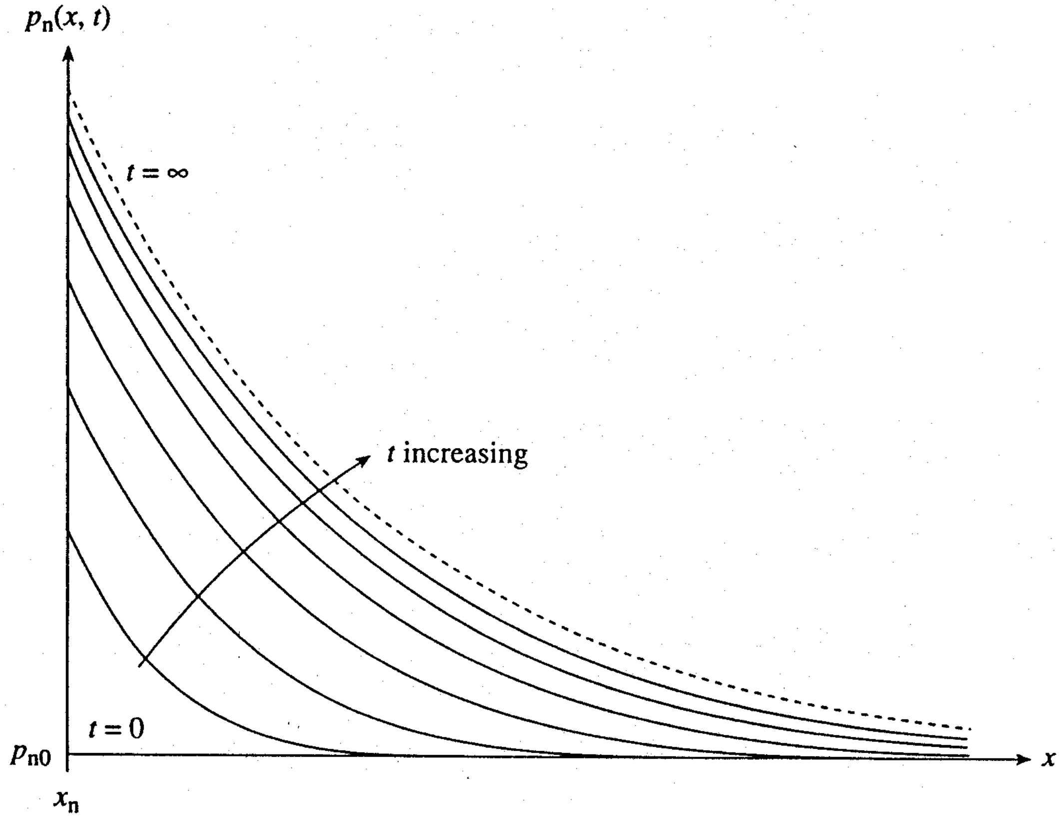


Figure 8.8 Build-up of the stored hole charge inside a p^+-n diode during the turn-on transient.

Solving Eq. (8.12) for $Q_P(t)$ gives

$$Q_P(t) = I_F \tau_p (1 - e^{-t/\tau_p}) \tag{8.13}$$

Under steady state conditions the stored hole charge in an ideal diode is

$$Q_P = I_{DIFF} \tau_p = I_0 \tau_p (e^{qV_A/kT} - 1) \quad \text{. . . steady state} \tag{8.14}$$

As a first-order approximation, let us make the assumption $Q_P(t)$ during the turn-on transient is described by Eq. (8.14) with $V_A \rightarrow v_A$. This is equivalent to assuming the build-up of stored charge occurs quasistatically. One can then write

$$Q_P(t) = I_0 \tau_p (e^{qv_A(t)/kT} - 1) \tag{8.15}$$

Equating the (8.13) and (8.15) expressions for $Q_P(t)$, and solving for $v_A(t)$, we arrive at the solution

$$\boxed{v_A(t) = \frac{kT}{q} \ln\left[1 + \frac{I_F}{I_0}(1 - e^{-t/\tau_p})\right]} \tag{8.16}$$

The turn-on response modeled by Eq. (8.16) is similar to the turn-off response in that the overall length of the transient increases with increasing I_F and τ_p. This is to be more or less expected because the charge required to reach the steady state is directly proportional to I_F and τ_p; i.e., $Q_P(\infty) = I_F\tau_p$ as deduced from either Eq. (8.10) or Eq. (8.13). Perhaps the most interesting feature of the turn-on transient is an initial rapid rise in $v_A(t)$, with $v_A(t)$ increasing to a large fraction of V_{ON} in a very short period of time. If, for example, $T = 300$ K and $V_{ON} = 0.75$ V or $I_F/I_0 = 3.77 \times 10^{12}$, $v_A(t)$ increases to $(0.84)V_{ON}$ after only $t = 0.01\tau_p$. By way of contrast, the final approach to the steady state is considerably slower, requiring a period of time equal to several τ_p.

(C) Exercise 8.2

The CPG (Concentration Plot Generation) program that follows is intended as a visualization and learning aid. The program plots out curves of $\Delta p_n(x', t)/\Delta p_{nmax}$ versus $x'/L_P = (x - x_n)/L_P$ at select t/τ_p for both the turn-off and turn-on transients. The computations are based on the direct solution of the time-dependent minority carrier diffusion equation for an ideal *pn* step junction[4]. The user chooses the type of plot to be displayed from an opening menu. Menu choices are linear or semilog plots of the turn-off transient concentrations and linear or semilog plots of the turn-on transient concentrations. In the turn-off plots t is stepped from $0.1t_s$ to t_s in $0.1t_s$ increments. In the turn-on plots t is stepped from $0.1\tau_p$ to $2\tau_p$ in $0.1\tau_p$ increments. The user must specify the I_R/I_F ratio when a turn-off plot is desired. We should mention that Figs. 8.3 and 8.8 were drawn based on the CPG program output.

Possible uses of the program are:

(1) Visualize the stored-charge decay during turn-off.

(2) Visualize the stored-charge build-up during turn-on.

(3) Examine and compare corresponding linear and semilog plots.

(4) Confirm that the $x = x_n$ slope of the linear turn-off curves are all the same for $0 < t \leq t_s$. (Are the slopes the same on the corresponding semilog plot? Are the $x = x_n$ slopes or curves on a semilog plot related to the current?)

(5) Examine the effect of I_R/I_F on the decay of the stored charge.

(6) Ascertain why the approximate t_s result of Eq. (8.8) becomes less and less accurate as I_R/I_F is increased. (Look at the stored charge remaining at $t = t_s$ as a function of I_R/I_F.)

(7) Check the accuracy of the quasistatic approximation employed in the derivation of Eq. (8.16). (On a semilog plot the turn-on curves should all be parallel to the $t = \infty$ curve if the build-up proceeds quasistatically.)

(8) Compare the turn-on $v_A(t)$ computed employing Eq. (8.16) and the $v_A(t)$ values deduced from the turn-on plot.

Hopefully the user will not be limited by the cited suggestions, but will feel free to experiment on his/her own. The user might also consider modifying the program to better display a given output, to extend the computations, or to obtain a specific output such as $v_A(t)$ versus t.

MATLAB program script...

```
%Exercise 8.2--Turn-off/Turn-on Concentration Plot Generator

%Determine type of desired plot
clear
close
s=menu('Choose the desired plot','OFF-Linear','OFF-Semilog',...
   'ON-Linear','ON-Semilog');

%Compute ts/taup if turn-off plot is desired
if s<=2,
   %Let Iratio=IR/IF and TS=ts/taup
   Iratio=input('Please input the IR/IF ratio: IR/IF= ');
   if Iratio==0, %Catch if IR=0
      TS=1;
   else
      TS=(erfinv(1./(1+Iratio)))^2;
   end
else
end

%Set values of X and T to be computed for desired plot
%X=x'/LP and T=t/taup
if s==1 | s==2,
   X=0:0.03:3;
   T=TS/10:TS/10:TS;
else
   X=0:0.03:3;
   T=[0.1:0.1:2];
end

%Plot steady-state curve, set axes-labels
y0=exp(-X);
if s==1 | s==3,
   plot(X,y0,'g')
   axis([0 3 0 1])
else
   semilogy(X,y0,'g')
   axis([0 3 1.0e-3 1])
```

```
end
xlabel('x`/LP'); ylabel('Δpn(x`,t)/Δpnmax')
grid; hold on

%Primary computations and time-dependent plots
j=length(T);
for i=1:j,
  A=exp(-X).*(1-erf(X./(2*sqrt(T(i)))-sqrt(T(i))));
  B=exp(X).*(1-erf(X./(2*sqrt(T(i)))+sqrt(T(i))));
  yon=(A-B)/2;  %yon=Δpn(x',t)/Δpnmax during turn-on
  if s==3,
    plot(X,yon);
  elseif s==1,
    yoff=exp(-X)-(1+Iratio).*yon;  %yoff=Δpn(x',t)/Δpnmax during turn-off
    plot(X,yoff);
  else
  end
  if s==4,
    semilogy(X,yon);
  elseif s==2,
    yoff=exp(-X)-(1+Iratio).*yon;
    semilogy(X,yoff);
  else
  end
end; hold off
```

8.3 SUMMARY

In this chapter we examined the electrical response and internal carrier response of *pn* junction diodes subjected to a large rapid change in the applied voltage or impressed current, a change intended to switch the diode from the forward-bias on-state to the reverse-bias off-state, or vice-versa. During the turn-off transient the excess minority carriers stored in the quasineutral regions must be removed before steady state conditions can be re-established. The diode initially remains forward biased and a large, constant, reverse current flows through the diode until the carrier concentrations decrease to their equilibrium values at the edges of the depletion region. This takes place in a period of time known as the storage delay time, t_s. t_s is the primary figure of merit used to characterize the transient response of *pn* junction diodes. The storage delay time increases in relation to the initial store of carriers, decreases with the rate of carrier removal by the reverse current, and is directly proportional to the minority carrier lifetime. The storage time is decreased by adding R–G centers to the semiconductor during device fabrication, and step-recovery diodes are produced by properly tailoring the doping profile. Measurement of the turn-off transient can also be used to determine the minority carrier lifetime on the lightly doped side of a junction. Overall, the focus of the chapter has been on establishing a basic understanding of transient operation and providing physical insight, knowledge that will prove very useful in treating one of the pre-eminent switching devices, the bipolar junction transistor.

PROBLEMS

CHAPTER 8 PROBLEM INFORMATION TABLE				
Problem	*Complete After*	*Difficulty Level*	*Suggested Point Weighting*	*Short Description*
8.1	8.3	1–2	15 (a::c-2, d::h-1, i::j-2)	Quick quiz
8.2	8.1.2	1	6 (2 each part)	Interpret $p_n(x, t)$ plot
• 8.3	8.1.3	2	8	Improved $Q_P(t_s)$ approx.
8.4	8.2	2–3	10 (a::c-3, d-1)	Open circuit voltage decay
8.5	"	2	6	Compute turn-on times
8.6	"	2	10 (a-3, b-7)	Pulse I_{F1} to $I_{F2} > I_{F1}$
8.7	"	2–3	10 (a-6, b-4)	Combined turn-off/turn-on
• 8.8	"	3	15 (a-10, b-5)	Compare turn-on $v_A(t)$

8.1 Quick Quiz.

Answer the following questions as concisely as possible.

(a) Define *storage delay time.*

(b) Define *recovery time* (t_r).

(c) Is it possible for the *pn* junction to support a reverse current even though $v_A > 0$? Explain.

(d) What is the root cause of the delay in switching from the on-state to the off-state?

(e) Name the two mechanisms that act to remove the excess stored charge during the turn-off transient.

(f) True or false: If $\Delta p_n(x, t) > 0$, $v_A > 0$.

(g) True or false: If $i > 0$, the slope of a linear $p_n(x, t)$ versus x plot must be positive (p_n increases with x) at $x = x_n$.

(h) What is special about the electrical and physical properties of a step-recovery diode?

(i) True or false: Increasing both I_F and I_R by a factor of 2 will have no effect on the storage delay time. Indicate how you arrived at your answer.

(j) True or false: Recombination actually acts to *retard* the build-up of stored carriers during the turn-on transient.—Indicate how you arrived at your answer.

8.2 The hole concentration on the n-side of a pn step junction diode at a given instant of time is as pictured in Fig. P8.2.

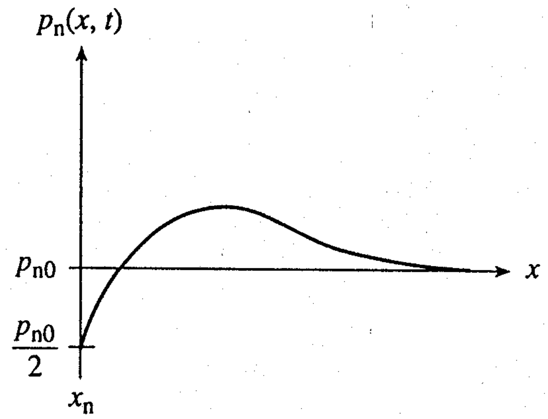


Figure P8.2

(a) Is the junction forward or reverse biased? Explain how you arrived at your answer.

(b) If $p_{n0} = 10^4/\text{cm}^3$ and $T = 300$ K, determine v_A.

(c) Is there a forward or reverse current flowing through the diode? Explain how you arrived at your answer.

• **8.3** The approximation $Q_P(t_s) = 0$ was used in deriving Eq. (8.8). Researchers have suggested the alternative approximation,[5]

$$Q_P(t_s) = \frac{I_F \tau_p}{1 + I_F/I_R}$$

which leads to the revised charge control expression

$$t_s = \tau_p \ln\left[\frac{(1 + I_F/I_R)^2}{1 + 2I_F/I_R}\right]$$

Determine whether the revised t_s expression is a significant improvement. Construct a plot of t_s/τ_p versus I_R/I_F similar to Fig. 8.6 using the revised charge control expression in place of Eq. (8.8). Briefly comment on the result.

8.4 An ideal p^+-n step junction diode carrying a forward current I_F is suddenly open-circuited at $t = 0$.

(a) Sketch the expected variation of $p_n(x, t)$ versus x at progressively increasing times after open-circuiting the diode. (Check your answer using the CPG program in Exercise 8.2.)

(b) Derive an expression for the stored hole charge, $Q_P(t)$, inside the diode at times $t > 0$. Be sure to express $Q_P(0)$ in terms of known parameters.

(c) Assuming a quasistatic decay of the hole charge, derive an expression for $v_A(t)$. Take the v_A voltages of interest to be greater than a few kT/q; i.e., $\exp(qv_A/kT) \gg 1$. Also use the fact that $I_F/I_0 = \exp(qV_{ON}/kT) - 1 \cong \exp(qV_{ON}/kT)$ to simply your result.

(d) Does the part (c) result suggest anything? Explain. (For further information see Subsection 8.5.2 in Schroder[3].)

8.5 An ideal p^+-n step junction diode is switched with a current pulse from $I = 0$ to $I_F = 1$ mA at $t = 0$. Calculate the time necessary for the diode voltage to reach 90% and 95% of its final value. Let $\tau_p = 1\ \mu$sec and $I_0 = 10^{-15}$ A.

8.6 An ideal p^+-n step junction diode initially forward biased at I_{F1} is pulsed to a constant current of $I_{F2} > I_{F1}$ at $t = 0$.

(a) Sketch the expected variation of $p_n(x, t)$ versus x at progressively increasing times after $t = 0$.

(b) Assuming a quasistatic build-up of the stored charge, derive an expression for $v_A(t)$.

8.7 At $t = 0$ the current through a p^+-n diode is switched from $I_F = 1$ mA to $i = -I_R = -1$ mA. After 1 μsec a current pulse is applied to switch the diode back to an $I_F = 1$ mA. Assume the diode to be ideal with $\tau_p = 1\ \mu$sec.

(a) Sketch the $i(t)$ through the diode as a function of time.

(b) Establish an expression for $v_A(t)$ at times $t > 1\ \mu$sec.

• **8.8** (a) The turn-on curves drawn by the CPG program in Exercise 8.2 correspond to t/τ_p values stepped from 0.1 to 2 in 0.1 increments. Noting

$$\frac{\Delta p_n(0,t)}{\Delta p_{nmax}} = \frac{e^{qv_A(t)/kT} - 1}{e^{qV_{ON}/kT} - 1}$$

appropriately modify the program to obtain v_A/V_{ON} at the stepped values of t/τ_p. Let $V_{ON} = 0.5$ V and $T = 300$ K in performing a sample computation.

(b) Compare the $v_A(t)$ derived from the part (a) exact solution with the Eq. (8.16) solution that was obtained by assuming turn-on proceeds quasistatically. The comparison assuming $V_{ON} = 0.5$ V and $T = 300$ K may be presented in either a plot or point-by-point format. Note that $I_F/I_0 = \exp(qV_{ON}/kT) - 1$.