7 *pn* Junction Diode: Small-Signal Admittance

7.1 INTRODUCTION

In this chapter we examine and model the small signal response of the *pn* junction diode. A small sinusoidal voltage (v_a) is taken to be superimposed on the applied d.c. bias giving rise to an a.c. current (i) flowing through the diode, as pictured in Fig. 7.1. The a.c. response of a passive device like the diode is characterized by specifying the small-signal admittance, $Y = i/v_a$. Response information can be alternatively conveyed through the use of a small-signal equivalent circuit. The junction region response of the *pn* diode has capacitive (C) and conductive (G) components and in general exhibits an admittance of the form

$$Y = G + j\omega C \tag{7.1}$$

where $j = \sqrt{-1}$ and ω is the angular frequency of the a.c. signal in radians/sec. The corresponding equivalent circuit, modeling the entire diode and valid for arbitrary d.c. biasing conditions, is shown in Fig. 7.2. The arrows through the capacitance and conductance symbols in the figure indicate that C and G are functions of the applied d.c. bias. R_S, the series resistance introduced in Chapter 6, models the portion of the diode outside the junction region. R_S can limit the performance of the diode in certain applications, but it is normally very small compared to the junction impedance except at large forward biases. Unless stated otherwise, we will henceforth assume R_S to be negligible.

In establishing explicit expressions for the admittance of the junction region, it is convenient to divide the development into two parts. In the first we take the diode to be reverse-biased. When reverse-biased, the diode conductance is small and $Y \cong j\omega C$. Moreover, the reverse-bias capacitance is linked solely to majority carrier oscillations inside the device. The second part treats forward bias where the conductance cannot be neglected and minority carriers contribute to the overall response.

7.2 REVERSE-BIAS JUNCTION CAPACITANCE

7.2.1 General Information

Reiterating the statement in the introduction, when reverse-biased, the *pn* junction diode becomes functionally equivalent to a capacitor. Many "capacitors" in ICs and other circuits are in fact reverse-biased *pn* junction diodes. The *pn* junction diode does differ from

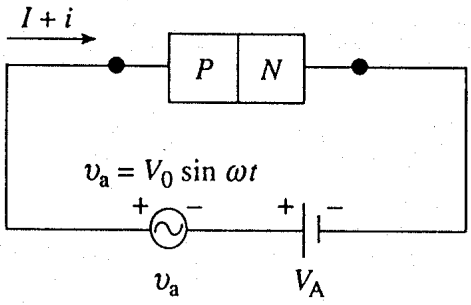

Figure 7.1 Diode biasing circuit. v_a is the applied small-signal voltage; i is the resultant a.c. current.

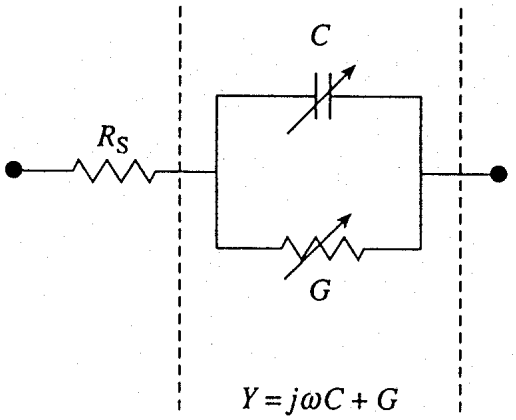

Figure 7.2 General-case small-signal equivalent circuit for a *pn* junction diode. $Y = j\omega C + G$ is the admittance of the junction region; R_S models the series resistance of the contacts and quasineutral regions.

a standard capacitor in that the diode capacitance monotonically decreases with increasing reverse bias. The sample C–V data presented in Fig. 7.3 illustrate the observed dependence.

The general a.c. behavior of the *pn* junction diode under reverse biasing can be explained by examining what happens inside the diode as the a.c. signal runs through a bias cycle. With the a.c. signal superimposed on the d.c. bias, the total voltage drop across the junction becomes $V_A + v_a$. During the positive portion of the v_a cycle, the a.c. signal slightly reduces the reverse bias across the junction, and the depletion width shrinks by a small amount, as envisioned in Fig. 7.4(a). The ρ-plot in Fig. 7.4(b), which was drawn assuming a step junction, emphasizes that there is a corresponding decrease in the charge on the two sides of the depletion region. When the a.c. signal reverses and goes negative, v_a now increases the total reverse bias across the junction to greater than V_A, and the depletion width increases slightly above its steady state value. A depletion width larger than the steady state value in turn gives rise to an increase in the depletion region charge on the two sides of the junction. The overall effect of the a.c. signal may thus be viewed as a small oscillation of the depletion width about its steady state value and an associated $\Delta\rho$ charge density oscillation, as pictured in Figs. 7.4(c) and (d). The $\Delta\rho$-plots were obtained

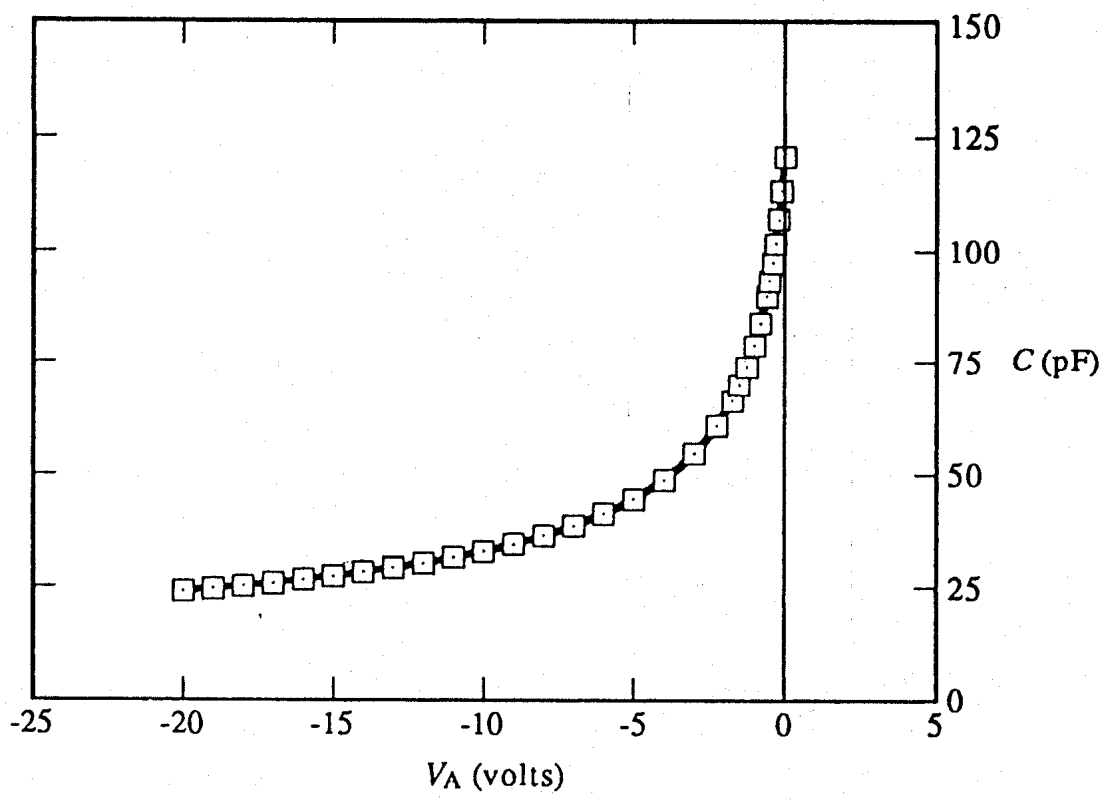

Figure 7.3 Monotonic decrease in the diode capacitance with increasing reverse bias. Sample C–V data derived from a 1N5472A abrupt junction diode.

by subtracting the d.c. charge density distribution in Fig. 7.4(b) from the $V_A \pm v_a$ charge density distributions.

The small size of v_a, typically a few tens of millivolts or less, dictates that the maximum displacement of the $\Delta\rho$ charge from the edges of the steady state depletion region will be extremely small. Effectively, it looks like plus and minus charges are being alternately added and subtracted from two planes inside the diode separated by a width W. The described a.c. situation is physically identical to what takes place inside a parallel plate capacitor. It is well known that the parallel plate capacitor exhibits a capacitance equal to the dielectric permittivity of the material between the plates, times the area of the plates, divided by the distance between the plates. The diode capacitance is concluded by analogy to be

$$C_J = \frac{K_S \varepsilon_0 A}{W} \tag{7.2}$$

The capacitance associated with the depletion width oscillation is known as the *junction* or *depletion-layer capacitance* and is identified by the subscript J. $C = C_J$ if the diode is reverse-biased, since there are no other significant charge oscillations. Also, we know W

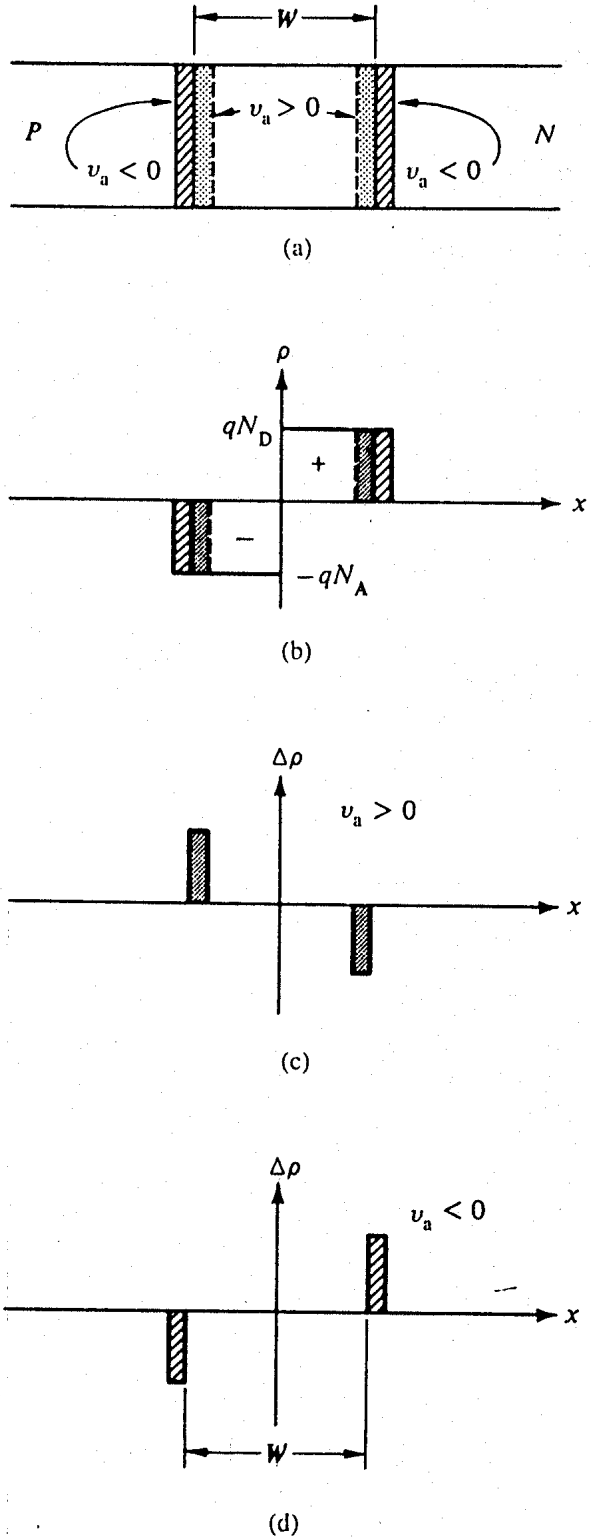

Figure 7.4 Depletion-layer charge considerations. (a) Depletion width and (b) total charge density oscillations in response to an applied a.c. signal. (c) $v_a > 0$ and (d) $v_a < 0$ a.c. charge densities.

increases with increasing reverse bias. C_J being proportional to $1/W$ is therefore expected to decrease with increased reverse biasing, in agreement with experimental (Fig. 7.3) observations.

One point must be clarified concerning the oscillation of the depletion width about its steady state value: To achieve this oscillation, majority carriers must move rapidly into and out of the affected region in sync with the a.c. signal. In other words, the carriers are assumed to respond to the a.c. signal as if it were a d.c. bias. When this happens, the device is said to *follow the a.c. signal quasistatically.* In the discussion of the d.c. response, we noted the majority carriers in the quasineutral regions were capable of a rapid rearrangement, with majority carriers being supplied or eliminated at the contacts as required. The majority carrier response time in Si is typically $\sim 10^{-10}$ sec or less, and the quasistatic assumption made here is routinely valid up to very high signal frequencies.

7.2.2 *C–V* Relationships

The precise capacitance versus voltage dependence expected from a given diode is established by replacing W in Eq. (7.2) by the appropriate expression relating W to the applied voltage. In treating the junction electrostatics in Chapter 5, the W versus V_A relationship was found to vary with the doping profile. The Chapter 5 analysis specifically gave

$$W = \left[\frac{2K_S\varepsilon_0}{qN_B}(V_{bi} - V_A)\right]^{1/2} \quad \ldots \text{ asymmetrical step junction} \tag{7.3}$$

and

$$W = \left[\frac{12K_S\varepsilon_0}{qa}(V_{bi} - V_A)\right]^{1/3} \quad \ldots \text{ linearly graded junction} \tag{7.4}$$

where N_B is the doping (N_A or N_D) on the lightly doped side of the asymmetrical step junction and a is the linear grading constant.

Although Eqs. (7.3) and (7.4) could be separately substituted into Eq. (7.2), it is more convenient to deal with a single generalized relationship valid for a wide range of profiles. Working to develop a generalized W versus V_A relationship, we consider a profile with one side ($x < 0$) heavily doped and the concentration on the lightly doped side described by the power law

$$N_B(x) = bx^m \quad \ldots x > 0 \tag{7.5}$$

where $b > 0$ and m are constants for a given profile. Examples of one-sided power-law profiles for select m-values are displayed in Fig. 7.5. Note that $m = 0$ and $m = 1$ correspond to the asymmetrical step junction and the one-sided linearly graded junction, respectively. Also note that negative m-values are permitted. A profile where $m < 0$ and the doping decreases as one moves away from the junction is said to be *hyperabrupt.* Hyperabrupt junctions can be formed by ion implantation or epitaxy.

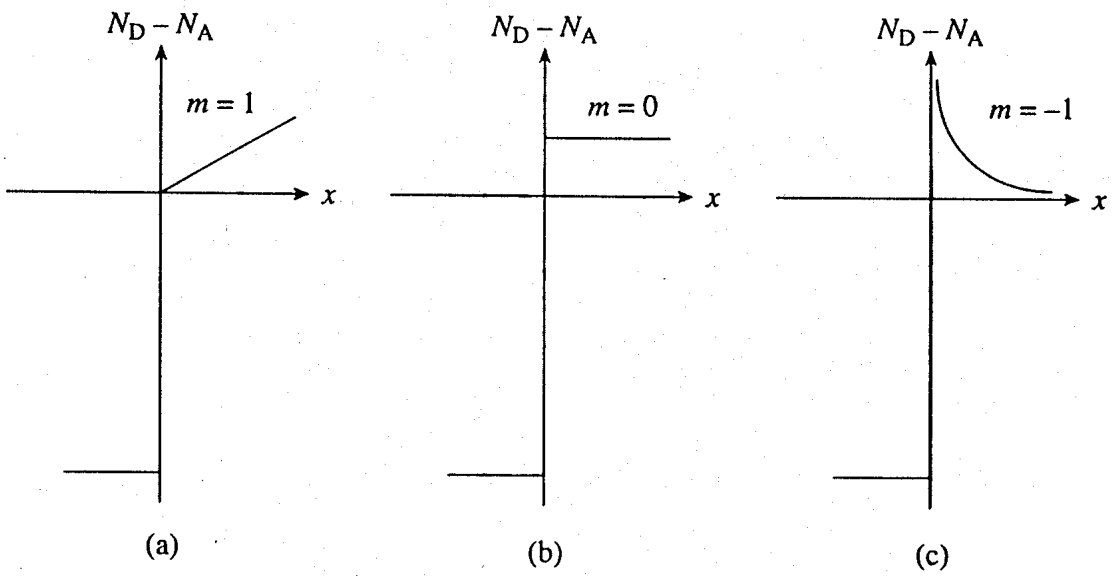

Figure 7.5 Example one-sided power-law profiles: (a) linearly graded, (b) step, and (c) $m = -1$ hyperabrupt.

Inside a *pn* junction with a one-sided power-law profile, the depletion width dependence for $m > -2$ is

$$W = \left[\frac{(m+2)K_S\varepsilon_0}{qb}(V_{bi} - V_A)\right]^{1/(m+2)} \tag{7.6}$$

The derivation of Eq. (7.6) is left as an exercise. For $m = 0$, $b = N_B$—where N_B without a trailing (x) is understood to be a position-independent constant—and Eq. (7.6) reduces to Eq. (7.3). Setting $m = 1$ and $b = a/4$ in Eq. (7.6) yields Eq. (7.4).† Satisfied Eq. (7.6) yields acceptable results, we conclude upon substituting Eq. (7.6) into Eq. (7.2) that

$$\boxed{C_J = \frac{K_S\varepsilon_0 A}{\left[\frac{(m+2)K_S\varepsilon_0}{qb}(V_{bi} - V_A)\right]^{1/(m+2)}}} \tag{7.7}$$

Alternatively, it is sometimes convenient to introduce

$$C_{J0} \equiv C_J|_{V_A=0} = \frac{K_S\varepsilon_0 A}{\left[\frac{(m+2)K_S\varepsilon_0}{qb}V_{bi}\right]^{1/(m+2)}} \tag{7.8}$$

†Equation (7.4) is appropriate for a *two-sided* linearly graded junction. b must be set equal to $a/4$ instead of a to account for the difference in profiles.

where, in terms of the capacitance at $V_A = 0$,

$$C_J = \frac{C_{J0}}{\left(1 - \frac{V_A}{V_{bi}}\right)^{1/(m+2)}} \tag{7.9}$$

A *pn* junction diode that is manufactured to take advantage of the capacitance-voltage variation described by Eqs. (7.7)/(7.9) is called a *varactor. Varactor* is a combination of the words *var*iable and re*actor,* where reactor alludes to the reactance $= 1/j\omega C$ of the device. Varactor diodes are widely used in parametric amplification, harmonic generation, mixing, detection, and voltage-variable tuning. In such applications it is often desirable to employ a diode exhibiting the maximum capacitance ratio over a given voltage range. This figure of merit is called the *tuning ratio* (*TR*). Examining Eq. (7.9) for reverse biases such that $-V_A/V_{bi} \gg 1$, we find

$$TR \equiv \frac{C_J(V_{A1})}{C_J(V_{A2})} \cong \left(\frac{V_{A2}}{V_{A1}}\right)^{1/(m+2)} \tag{7.10}$$

As is obvious from Eq. (7.10), the largest tuning ratios are derived from devices with the smallest m-values—*TR* progressively increases in going from linearly graded ($m = 1$), to step ($m = 0$), to hyperabrupt ($m < 0$) junctions. This should explain the special interest in hyperabrupt profiles and the commercial availability of hyperabrupt varactor diodes.

(C) Exercise 7.1

P: Equation (7.7) can be used to compute and plot fully dimensioned capacitance-voltage characteristics; "universal" normalized C–V curves are readily constructed using Eq. (7.9). To examine the general nature of the predicted C–V characteristics, compute and plot normalized C_J/C_{J0} versus V_A/V_{bi} curves appropriate for linearly graded, step, and $m = -1$ hyperabrupt junction diodes. Limit the voltage axis to $-25 \leq V_A/V_{bi} \leq 0$. Comment on the results.

S: The normalized characteristics were computed using Eq. (7.9). The MATLAB program script and output plot (Fig. E7.1) follow. The step junction curve is noted to provide a fairly good match to the experimental data presented in Fig. 7.3 if one assumes $V_{bi} \sim 1$ V. Also, if $V_A = 0$ is used for V_{A1}, and assuming similar V_{bi} values, the tuning ratio $[C_J(V_{A1})/C_J(V_{A2})]$ employing any V_{A2} is obviously greatest for the hyperabrupt diode and least for the linearly graded diode, in agreement with the text discussion.

MATLAB program script...

```
%Exercise 7.1...Normalized C-V curves

%Computation
clear
m=[1 0 -1];
s=1 ./(m+2);
x=linspace(-25,0);        %x=VA/Vbi
y=[];                     %y=CJ/CJ0
for i=1:3,
y=[y;1 ./(1-x).^s(i)];
end

%Plot
close
plot(x,y,'-'); grid
axis([-25 0 0 1])
xlabel('VA/Vbi'); ylabel('CJ/CJ0')
text(-20,.42,'linear (m=1)')
text(-20,.27,'step (m=0)')
text(-20,.10,'hyperabrupt (m=-1)')
```

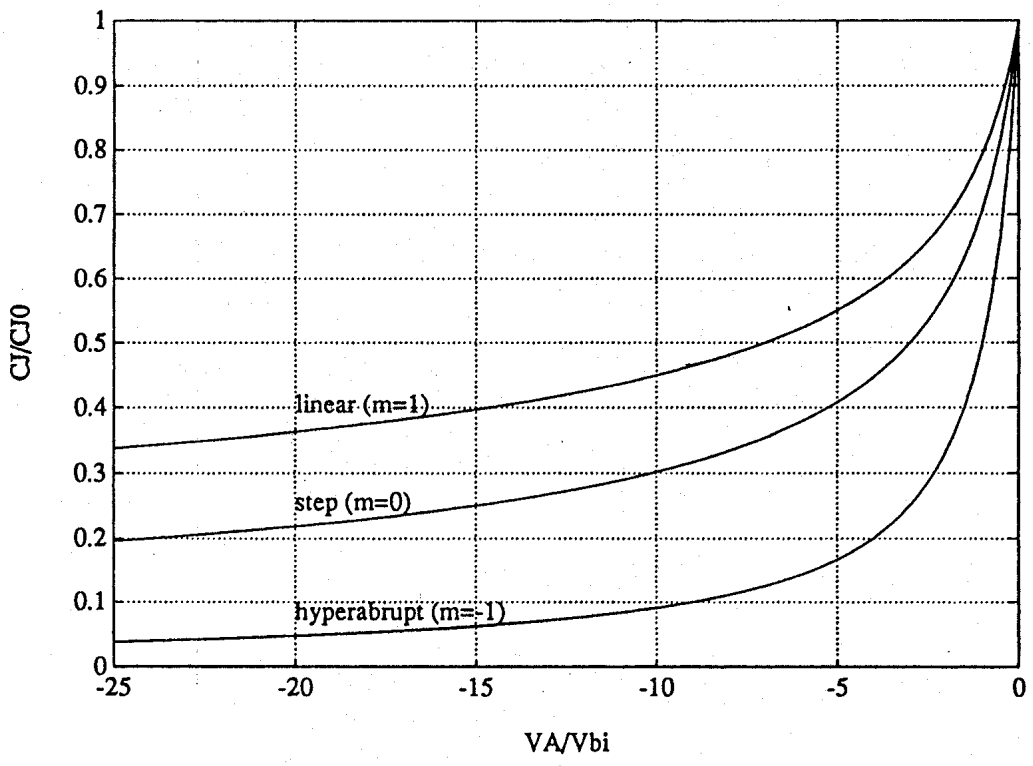

Figure E7.1

7.2.3 Parameter Extraction/Profiling

C–V data from *pn* junction diodes and other devices are routinely used to determine device parameters, notably the average doping or doping profile on the lightly doped side of a junction. *C–V* measurements have become so commonplace in the characterization and testing of devices that automated systems are available for acquiring and analyzing the *C–V* data. Since the measurement is an integral component of parameter extraction, we begin here with a brief description of an automated *C–V* system.

The *C–V* system in the measurements laboratory administered by the author is pictured schematically in Fig. 7.6. The MSI *C–V* meter is the heart of the system, employing a 15 mV rms a.c. signal at a probing frequency of 1 MHz. Four capacitance ranges with a maximum value of 2 pF, 20 pF, 200 pF, and 2000 pF are available for selection from the front panel. A d.c. bias supply inside the meter has two full-scale ranges of ±9.999 V, programmable in 0.001 V increments, and ±99.99 V, programmable in 0.01 V increments. Operator control of the biasing, the data display, data manipulations, and hard-copy output to a printer or plotter are accomplished by software on the personal computer shown to the left of the *C–V* meter in Fig. 7.6. The probe box to the right of the meter is used if the device or devices under test are situated on a wafer. The circular chuck in the probe box provides electrical contact to the back of the wafer and a wire probe contacts the device structure on the top of the wafer. The chuck can be resistance-heated under the local control of the 832 T-Controller. After probe contact, the top of the probe box is typically lowered to keep room light from perturbing the capacitance measurement. If the device under test is encapsulated, the leads to the probe box are removed and the test device is inserted into an adapter connected to the input terminals of the meter. We should mention the meter automatically measures and compensates for the stray capacitance associated with cabling, probe box components, and the encapsulated-device adapter.

Turning to the interpretation of the *C–V* data, suppose the device under test is known to be an asymmetrically doped abrupt junction. (The term *abrupt* is normally used to describe *actual* doping profiles approximately modeled by the idealized step junction.) For the assumed junction profile, $m \to 0$ and $b \to N_B$ in Eq. (7.7). Additionally, if both sides of Eq. (7.7) are inverted and then squared, one obtains

$$\frac{1}{C_J^2} = \frac{2}{qN_B K_S \varepsilon_0 A^2}(V_{bi} - V_A) \tag{7.11}$$

Equation (7.11) indicates that a plot of $1/C_J^2$ versus V_A should be a straight line, with a slope inversely proportional to N_B and an extrapolated $1/C_J^2 = 0$ intercept equal to V_{bi}. Thus, assuming the area A of the diode is known, N_B is readily deduced from the slope of the plot. Although perhaps stating the obvious, a straight line $1/C_J^2$ versus V_A plot is also confirmation that the diode can be modeled as a step junction. A sample analysis of *C–V* data based on the $1/C_J^2$ versus V_A plot is presented in Exercise 7.2.

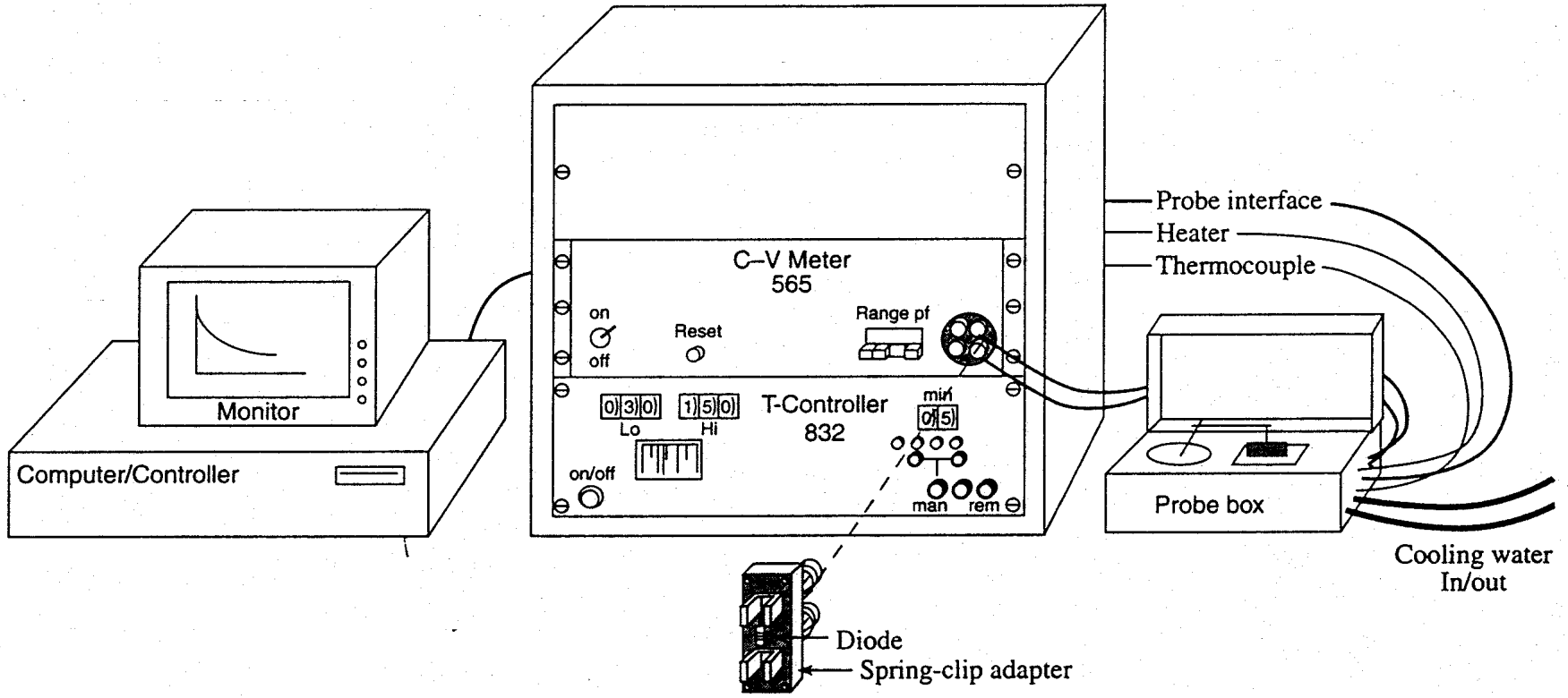

Figure 7.6 Sketch of a capacitance–voltage (C–V) measurement system.

Exercise 7.2

P: The manufacturer indicates the 1N5472A is an n^+-p abrupt junction diode with an area $A = 3.72 \times 10^{-3}$ cm^2. Encapsulation is noted to typically introduce a 2 pF stray capacitance shunting the diode junction. Utilizing the measured 1N5472A C–V data presented in Fig. 7.3, apply the $1/C_J^2$ versus V_A plot technique to confirm the abrupt nature of the junction and to determine the p-side doping concentration. Also quote the deduced value of V_{bi}.

S: A $1/C_J^2$ versus V_A plot of the 1N5472A C–V data is displayed in Fig. E7.2. Prior to constructing the plot, 2 pF was subtracted from all measured capacitance values to correct for the encapsulation-related shunt capacitance ($C_J = C - 2$ pF). The Fig. E7.2 data points are seen to lie in an almost perfect straight line. The junction is definitely abrupt. Performing a least squares fit to the data gives

$$\frac{1}{C_J^2} = (6.89 \times 10^{19}) - (9.78 \times 10^{19})V_A$$

where C_J is in farads and V_A is in volts. Referring to Eq. (7.11), we conclude

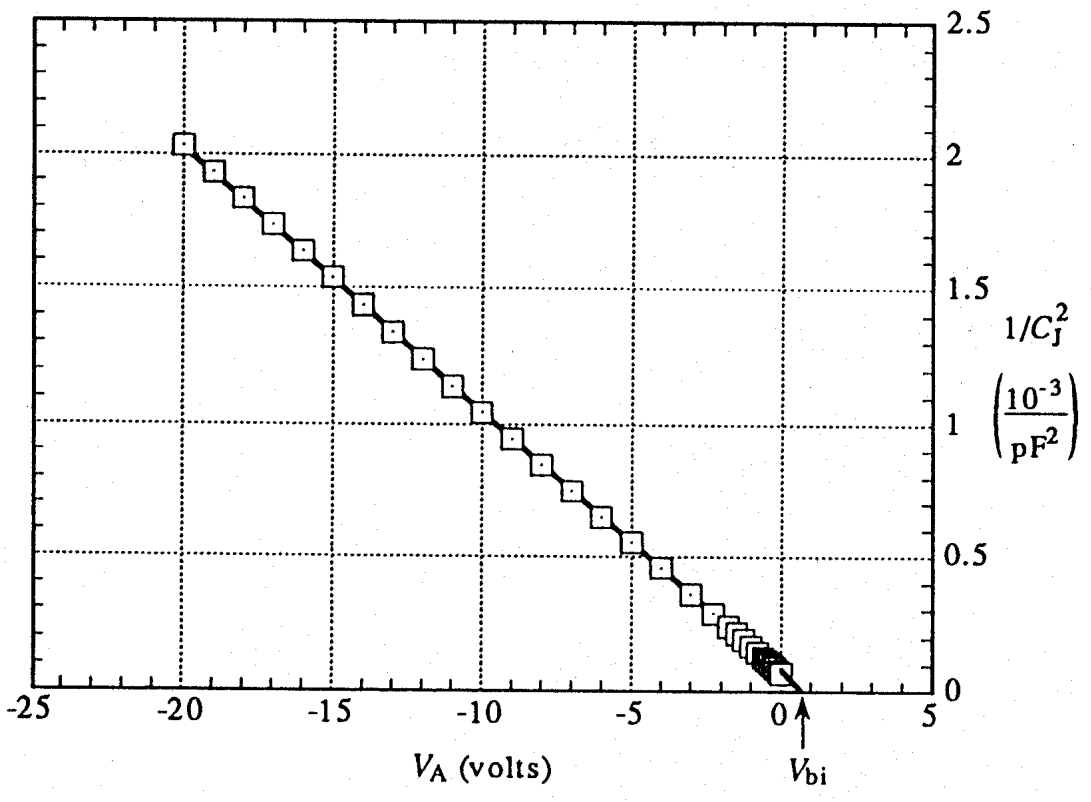

Figure E7.2

$$N_A = \frac{2}{qK_S\varepsilon_0 A^2|\text{slope}|}$$

$$= \frac{2}{(1.6 \times 10^{-19})(11.8)(8.85 \times 10^{-14})(3.72 \times 10^{-3})^2(9.78 \times 10^{19})}$$

$$= \mathbf{8.84 \times 10^{15}/cm^3}$$

and

$$V_{bi} = V_A|_{1/C_j^2=0} = \frac{6.89 \times 10^{19}}{9.78 \times 10^{19}} = \mathbf{0.70\ V}$$

It should be noted that the deduced V_{bi} is lower than one would expect from the $N_A \cong 9 \times 10^{15}/cm^3$ p-side doping. The V_{bi} value deduced from the C–V data is subject to serious extrapolation errors and is sensitive to doping variations in the immediate vicinity of the metallurgical junction.

The foregoing plot approach could obviously be extended to the linearly graded and other profiles. However, this is seldom done. As it turns out, the doping variation with position on the lightly doped side of a junction can be deduced directly from the C–V data without prior knowledge about the nature of the doping profile. Omitting the derivational details, we merely note the doping concentration versus position is computed using[3]

$$N_B(x) = \frac{2}{qK_S\varepsilon_0 A^2|d(1/C_J^2)/dV_A|} \tag{7.12}$$

$$x = \frac{K_S\varepsilon_0 A}{C_J} \tag{7.13}$$

where x is the distance into the lightly doped side of the diode as measured from the metallurgical junction. Note that substituting the Eq. (7.11) step junction relationship into Eq. (7.12) yields the required position-independent result.

The process of determining the doping as a function of position is called *profiling*. The profile determined using Eqs. (7.12)/(7.13) becomes inaccurate if the doping is a rapidly varying function of position, and only a limited portion of the junction can be scanned. Moreover, the result tends to be "noisy" because the slope or derivative of the C–V data is required. Nevertheless, C–V profiling is relatively simple to implement, typically yields useful results, and finds widespread utilization. Software provided with automated C–V systems even performs the (7.12)/(7.13) computations and displays the result graphically. A sample profile, that of a hyperabrupt junction diode automatically processed by the Fig. 7.6 C–V system, is reproduced in Fig. 7.7.

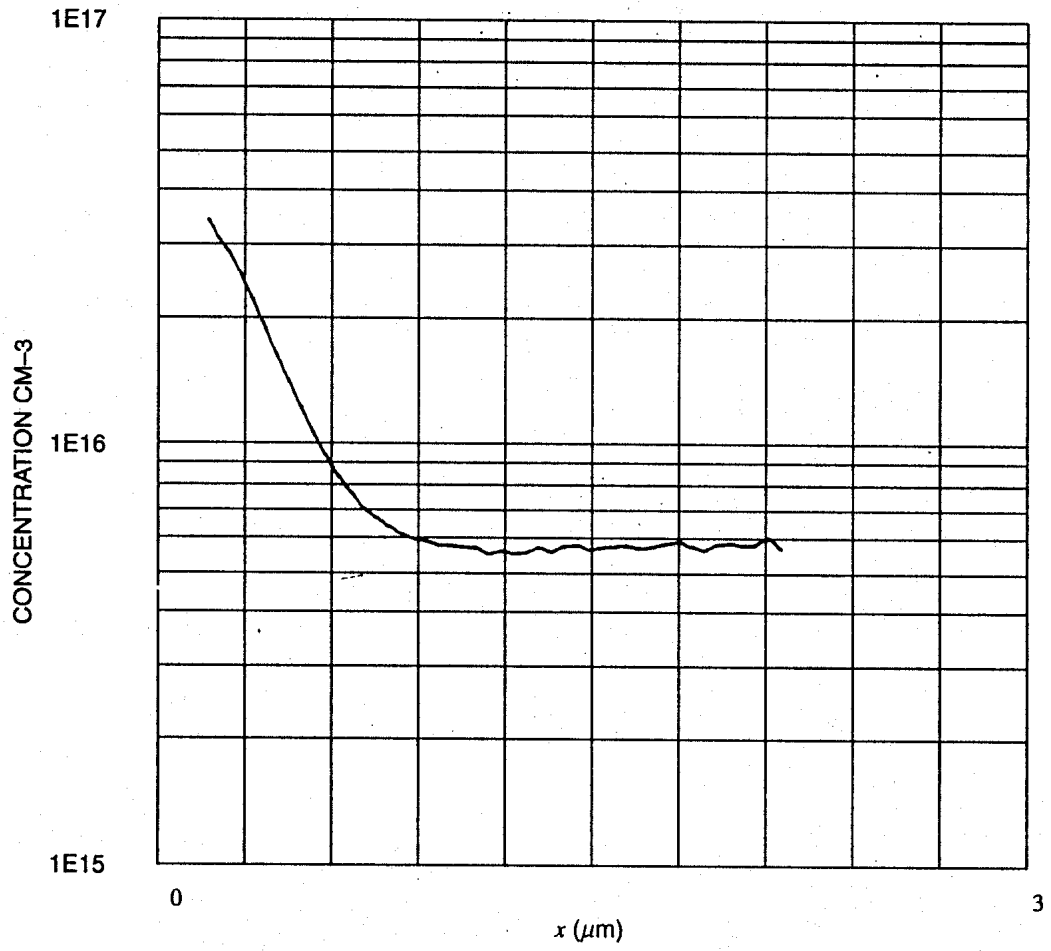

Figure 7.7 Doping profile of a hyperabrupt tuning diode (ZC809). Output from the Fig. 7.6 C–V measurement system. x is the distance from the metallurgical junction into the lightly doped side.

7.2.4 Reverse-Bias Conductance

All standard capacitors exhibit a certain amount of conductance. The same is true of the *pn* junction diode. Although predominantly capacitive, the reverse bias admittance does have a small conductive component. A few words are in order concerning the reverse-bias conductance.

By definition, the differential d.c. conductance of a diode is just the slope of the I–V characteristic, dI/dV, at the d.c. operating point. If the diode is assumed to respond to an a.c. signal quasistatically, then the a.c. conductance $= \Delta I/\Delta V = dI/dV =$ differential d.c. conductance. Limiting our considerations to frequencies where the diode can follow the a.c. signal quasistatically, and introducing the symbol G_0 for the associated low-frequency conductance, we can write

$$G_0 = \frac{dI}{dV_A} \tag{7.14}$$

For an ideal diode where $I = I_0[\exp(qV_A/kT) - 1]$,

$$G_0 = \frac{q}{kT} I_0 e^{qV_A/kT} = \frac{q}{kT}(I + I_0) \quad \ldots \text{ ideal diode} \tag{7.15}$$

When the reverse bias exceeds a few kT/q volts in an ideal diode, $I \to -I_0$ and we see from Eq. (7.15) that $G_0 \to 0$. This is consistent with the fact that the reverse-bias I–V characteristic saturates and the slope of the ideal I–V curve goes to zero. If the d.c. recombination–generation current dominates in the given diode then, for reverse biases greater than a few kT/q volts,

$$G_0 = \frac{d}{dV_A}\left(-\frac{qAn_i}{2\tau_0} W\right) = \frac{qAn_i W/2\tau_0}{(m + 2)(V_{bi} - V_A)} \quad \ldots I_{R\text{–}G} \text{ dominant} \tag{7.16}$$

where use has been made of the Eq. (7.6) relationship for W. When the R–G current dominates, Eq. (7.16) indicates there is a residual conductance at all reverse biases, with the precise voltage dependence varying with the doping profile of the junction.

Regardless of the junction type or dominant current component, it should be emphasized that Eq. (7.14) can always be applied to the measured I–V characteristic to determine G_0.

Exercise 7.3

P: The diode exhibiting the reverse-bias I–V characteristic displayed in Fig. 6.10(b) has a measured junction capacitance of $C_J = 63$ pF at $V_A = -10$ V. The series resistance of the diode was estimated to be 1 ohm in Exercise 6.8. Taking the d.c. operating point to be $V_A = -10$ V and the a.c. frequency to be $f = 100$ kHz, confirm that R_S and $G = G_0$ may be totally neglected in modeling the admittance of the device.

S: Figure 6.10(b) can be used to estimate the low-frequency conductance. We find

$$G_0 = \left.\frac{dI}{dV_A}\right|_{V_A = -10\,V} \cong \frac{40 \text{ pA}}{18 \text{ V}} = 2.22 \times 10^{-12} \text{ S}$$

By way of comparison, at the operational bias and frequency,

$$\omega C_J = (2\pi)(10^5)(6.3 \times 10^{-11}) = 3.96 \times 10^{-5} \text{ S}$$

The capacitive component is clearly much greater than the conductive component and $Y \cong j\omega C_J$.

Next, consider the series resistance. Since R_S is in series with Y, we need to compare $|Z| = 1/|Y|$ with R_S. Here we find

$$R_S \cong 1\ \Omega$$

and

$$\frac{1}{\omega C_J} = 2.52 \times 10^4\ \Omega$$

The reactance of the junction is much greater than the series resistance. For the given operational conditions, the diode may be essentially viewed as a pure capacitor.

7.3 FORWARD-BIAS DIFFUSION ADMITTANCE

7.3.1 General Information

Capacitance arises from charge oscillations inside of a device structure. The junction capacitance introduced in the reverse-bias analysis is caused by the in-and-out movement of majority carriers about the steady state depletion width. The minority carrier concentrations also oscillate about the edges of the depletion width in response to the a.c. signal. The minority carrier numbers are so minuscule under reverse-bias conditions, however, that the contribution to the admittance is negligible. Forward biasing gives rise to nothing new as far as the majority carriers are concerned. These carriers still move back and forth about the edges of the depletion region giving rise to a junction capacitance. In fact, the C_J relationships developed in the previous section can be applied without modification to forward bias. The something new under forward bias is a significant contribution from the minority carrier charge oscillation in response to the a.c. signal.

As noted during the examination of ideal diode results in Subsection 6.1.4, forward biasing of the diode causes a build-up of minority carriers in the quasineutral regions immediately adjacent to the depletion region. The build-up becomes larger and larger with increasing forward bias. In response to an a.c. signal, the voltage drop across the junction is changed to $V_A + v_a$ and the excess minority carrier distributions oscillate about their d.c. values as pictured in Fig. 7.8(a). This results in an additional capacitance. If the minority carriers can follow the signal quasistatically, the carriers move back and forth in unison between the two straight lines in the figure. However, the supply and removal of minority carriers is not as rapid as that of the majority carriers. At angular frequencies approaching the inverse of the minority carrier lifetimes, the minority carrier charge oscillation has difficulty staying in sync with the a.c. signal. The result is an out-of-phase spatial variation of the charge something like the undulating distributions sketched in Fig. 7.8(a). An out-of-phase charge oscillation enhances the observed conductance and reduces the observed

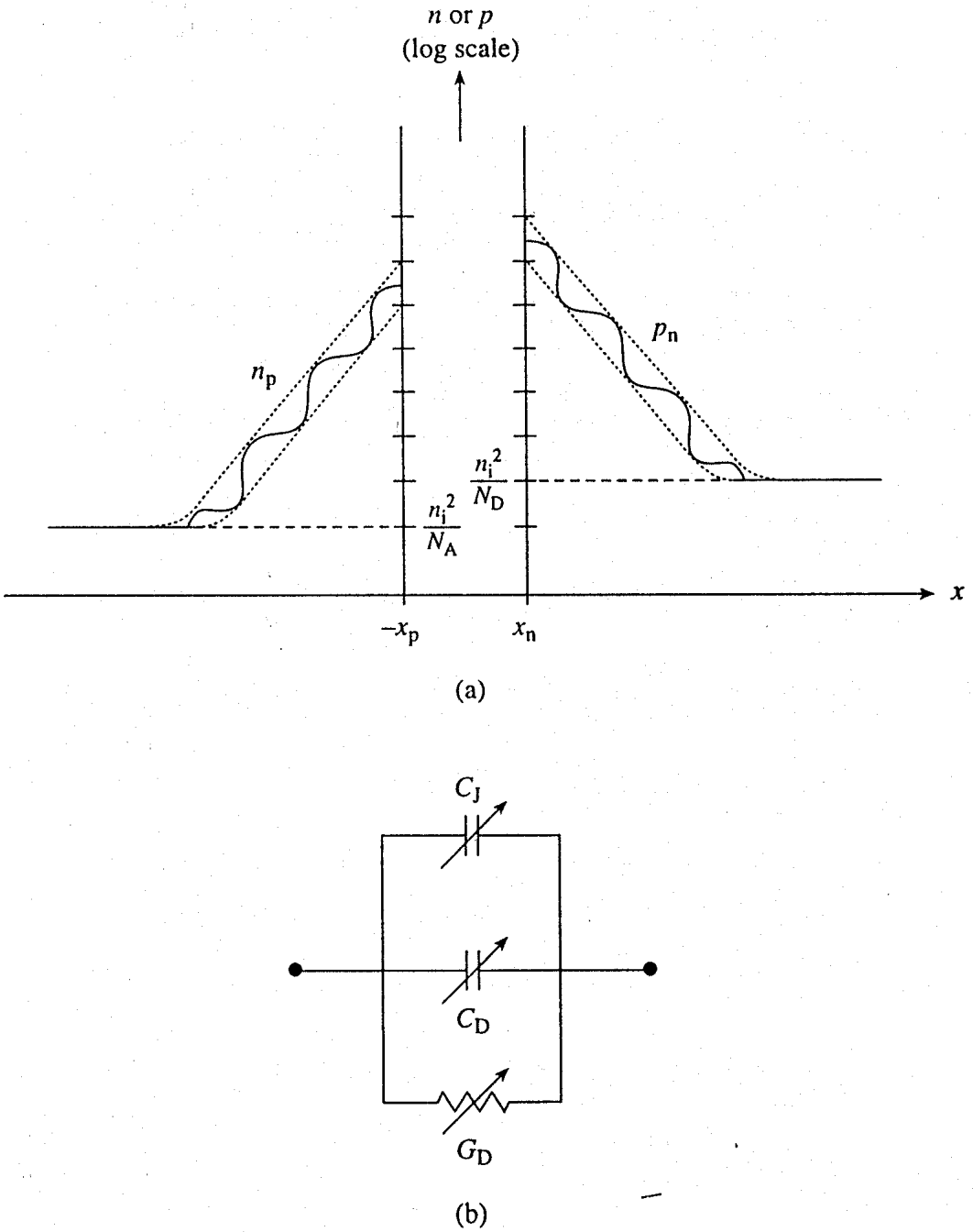

Figure 7.8 The diffusion admittance. (a) Minority carrier charge fluctuation (greatly exaggerated), giving rise to the diffusion admittance. (b) Forward-bias small-signal equivalent circuit for the *pn* junction diode (series resistance assumed to be negligible).

capacitance. In other words, the capacitance and conductance associated with the minority carrier oscillations are expected to be frequency-dependent.

Because the minority carrier build-up about the edges of the depletion region is caused by the diffusion current, the admittance associated with the minority carrier charge oscillation is called the diffusion admittance, Y_D. In general, as we have indicated,

$$Y_D = G_D + j\omega C_D \tag{7.17}$$

where C_D and G_D are the diffusion capacitance and diffusion conductance, respectively. The overall forward-bias admittance is of course the parallel combination of the junction capacitance and the diffusion admittance as noted in Fig. 7.8(b).

Measurement of the forward-bias admittance poses more of a challenge than the reverse-bias capacitance measurement. The larger d.c. current that flows when the diode is forward-biased tends to load down the detection and biasing circuitry in almost all commercially available C–V systems. In measurements on a Si diode at room temperature, a forward bias of only a few tenths of a volt often leads to a fallacious result or automatic termination of the measurement. One instrument that can be used for forward-bias measurements is the HP4284A LCR Meter pictured schematically in Fig. 7.9. The HP4284A with the 001 option installed contains a special isolation circuit that minimizes the loading problem for d.c. currents up to 0.1 A. A very versatile piece of equipment, the HP4284A permits simultaneous capacitance and conductance measurements at frequencies ranging from 20 Hz to 1 MHz, variation of the a.c. signal level from 5 mV to 20 V rms, setting of the d.c. bias between ±40 V, and capacitance detectability claimed to range from 0.01

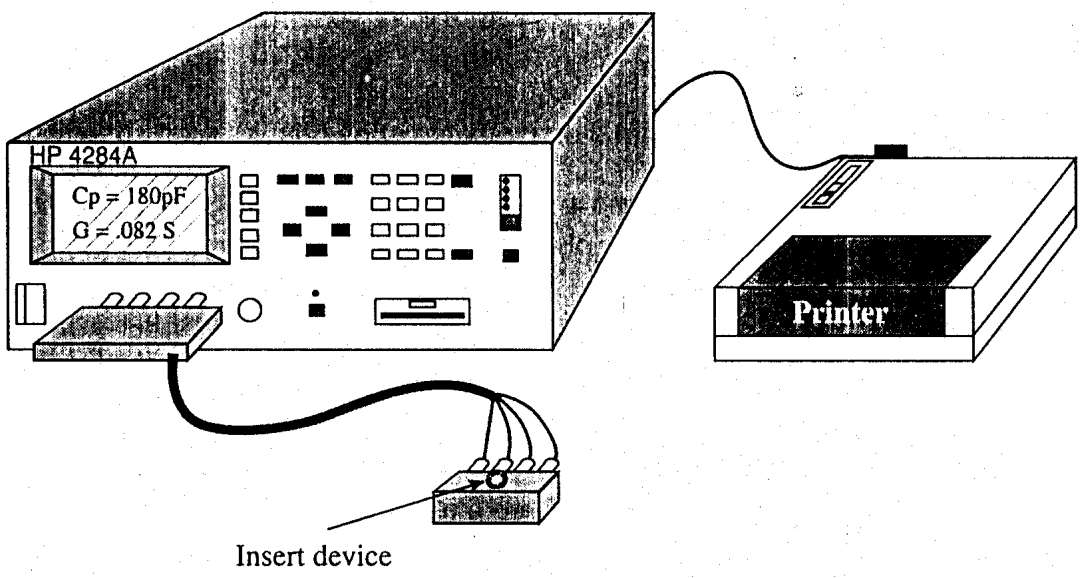

Figure 7.9 The Hewlett-Packard 4284A LCR Meter used for forward-bias measurements. The attached printer conveniently provides a hard-copy record of the display screen data.

femtofarad to 10 farads. The instrument basically performs single-point measurements, but will automatically cycle through ten operator-set values of frequency, d.c. bias, or a.c. signal level.

7.3.2 Admittance Relationships

Obtaining explicit relationships for the diffusion admittance is not difficult, but the mathematical manipulations can become rather tedious. In the straightforward brute-force approach, the ideal diode derivation is simply repeated with the d.c. quantities all replaced by d.c. plus a.c. quantities. Separate solutions are then sought for the a.c. quantities. Once a solution is obtained for the a.c. current as a function of the a.c. voltage, the admittance is computed from $Y = i/v_a$. Alternatively, the a.c. current solution can be obtained from the d.c. current solution by noting equivalencies in the two formulations. We will pursue the latter approach.

The device under analysis is taken to be a p^+-n junction diode. With an a.c. signal superimposed on the d.c. bias, the n-side minority carrier diffusion equation to be solved is

$$\frac{\partial \Delta p_n(x,t)}{\partial t} = D_p \frac{\partial^2 \Delta p_n(x,t)}{\partial x^2} - \frac{\Delta p_n(x,t)}{\tau_p} \tag{7.18}$$

Assuming the a.c. signal is a sine or cosine function, we can write

$$\Delta p_n(x,t) = \overline{\Delta p_n}(x) + \tilde{p}_n(x,\omega)e^{j\omega t} \tag{7.19}$$

where $\overline{\Delta p_n}$ is the time-invariant (d.c.) portion of $\Delta p_n(x, t)$ and $\tilde{p}_n$ is the amplitude of the a.c. component. Substituting the Eq. (7.19) expression for $\Delta p_n(x, t)$ into Eq. (7.18) and explicitly working out the time derivative yields

$$j\omega\tilde{p}_n e^{j\omega t} = D_p \frac{d^2\overline{\Delta p_n}}{dx^2} + D_p \frac{d^2\tilde{p}_n}{dx^2} e^{j\omega t} - \frac{\overline{\Delta p_n}}{\tau_p} - \frac{\tilde{p}_n}{\tau_p} e^{j\omega t} \tag{7.20}$$

The d.c. and a.c. terms in Eq. (7.20) must separately balance. Thus, after collecting like terms and simplifying the a.c. result, one obtains

$$0 = D_p \frac{d^2\overline{\Delta p_n}}{dx^2} - \frac{\overline{\Delta p_n}}{\tau_p} \tag{7.21a}$$

$$0 = D_p \frac{d^2\tilde{p}_n}{dx^2} - \frac{\tilde{p}_n}{\tau_p/(1 + j\omega\tau_p)} \tag{7.21b}$$

Equation (7.21a) is recognized as the usual steady state minority carrier diffusion equation. Note that the a.c. version of the diffusion equation, Eq. (7.21b), has exactly the same form except that τ_p is replaced by $\tau_p/(1 + j\omega\tau_p)$.

In solving Eqs. (7.21) the usual boundary condition applies at $x = \infty$; i.e., $\overline{\Delta p_n}(\infty) = \tilde{p}_n(\infty) = 0$. The boundary condition at $x = x_n$, however, becomes

$$\Delta p_n(x=x_n) = \overline{\Delta p_n}(x_n) + \tilde{p}_n(x_n) = \frac{n_i^2}{N_D}(e^{q(V_A+v_a)/kT} - 1) \tag{7.22}$$

or

$$\overline{\Delta p_n}(x_n) = \frac{n_i^2}{N_D}(e^{qV_A/kT} - 1) \tag{7.23}$$

$$\tilde{p}_n(x_n) = \frac{n_i^2}{N_D} e^{qV_A/kT}(e^{qv_a/kT} - 1) \tag{7.24a}$$

$$\cong \frac{n_i^2}{N_D}\left(\frac{qv_a}{kT} e^{qV_A/kT}\right) \quad \ldots\ v_a \ll kT/q \tag{7.24b}$$

v_a in the foregoing is understood to be the amplitude of the a.c. signal.

At this point we have yet to solve for anything. We have merely established the equation and boundary conditions to be employed in solving for the a.c. variables and current. It is now a simple matter, however, to progress to the desired solution. Since the a.c. minority carrier diffusion equation is identical in form to the d.c. equation except $\tau_p \rightarrow \tau_p/(1 + j\omega\tau_p)$, and since the boundary conditions are identical except $[\exp(qV_A/kT) - 1] \rightarrow [(qv_a/kT)\exp(qV_A/kT)]$, the a.c. and d.c. current solution must likewise be identical except for the cited modifications to τ_p and the voltage factor. For a p^+-n diode we know

$$I_{DIFF} = qA\frac{D_P}{L_P}\frac{n_i^2}{N_D}(e^{qV_A/kT} - 1) = qA\sqrt{\frac{D_P}{\tau_p}}\frac{n_i^2}{N_D}(e^{qV_A/kT} - 1) \tag{7.25}$$

Thus, making the noted τ_p and voltage factor substitutions, we conclude

$$i_{diff} = qA\sqrt{\frac{D_P}{\tau_p}}\sqrt{1 + j\omega\tau_p}\frac{n_i^2}{N_D}\left(\frac{qv_a}{kT} e^{qV_A/kT}\right) = \left(\frac{qv_a}{kT} I_0 e^{qV_A/kT}\right)\sqrt{1 + j\omega\tau_p} \tag{7.26}$$

or in terms of the ideal-diode low-frequency conductance (Eq. 7.15),

$$i_{diff} = G_0\sqrt{1 + j\omega\tau_p}\, v_a \tag{7.27}$$

and

$$\boxed{Y_D = \frac{i_{diff}}{v_a} = G_0\sqrt{1 + j\omega\tau_p}} \quad \ldots\ p^+\text{-}n \text{ diode} \tag{7.28}$$

For an n^+-p diode $\tau_p \rightarrow \tau_n$ in Eq. (7.28). Given a two-sided junction, G_0 must be separated into its n and p components and each multiplied by the appropriate $\sqrt{1 + j\omega\tau}$ factor.

If the Eq. (7.28) diffusion admittance for a p^+-n diode is separated into real and imaginary parts and the result compared with Eq. (7.17), one finds

$$G_D = \frac{G_0}{\sqrt{2}}\left(\sqrt{1 + \omega^2\tau_p^2} + 1\right)^{1/2} \tag{7.29a}$$

$$C_D = \frac{G_0}{\omega\sqrt{2}}\left(\sqrt{1 + \omega^2\tau_p^2} - 1\right)^{1/2} \tag{7.29b}$$

G_D and C_D are noted to be functions of both the d.c. bias (through G_0) and the signal frequency. With G_0 varying as $\exp(qV_A/kT)$, the diffusion components increase very rapidly with increasing forward bias. Whereas C_j dominates the a.c. response at small forward biases, the diffusion capacitance surpasses and eventually overshadows the junction capacitance as the forward bias is progressively increased. Relative to the frequency dependence, at low frequencies where $\omega\tau_p \ll 1$, $\sqrt{1 + \omega^2\tau_p^2} \cong 1 + \omega^2\tau_p^2/2$ and

$$G_D \Rightarrow G_0 \qquad \ldots\ \omega\tau_p \ll 1 \tag{7.30a}$$

$$C_D \Rightarrow G_0\frac{\tau_p}{2} \qquad \ldots\ \omega\tau_p \ll 1 \tag{7.30b}$$

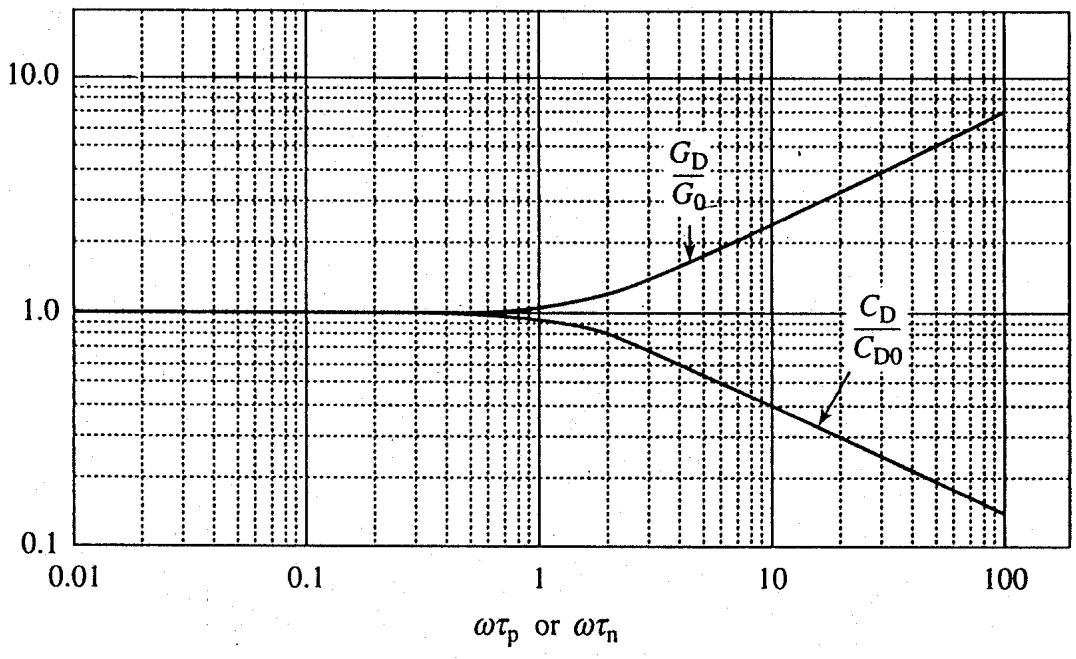

Figure 7.10 Diffusion capacitance and diffusion conductance normalized to their low-frequency values as a function of $\omega\tau_p$ (p^+-n diode) or $\omega\tau_n$ (n^+-p diode). ($C_{D0} = G_0\tau/2$)

If $\tau_p = 10^{-6}$ sec, for example, a frequency independent response described by Eqs. (7.30) is expected for $f \lesssim 1/(20\pi\tau_p) \cong 16$ kHz. For signal frequencies where $\omega\tau_p \gtrsim 1$, the conductance increases while the capacitance decreases with increasing frequency. The relative change in G_D and C_D compared to their low-frequency values is graphed as a function of $\omega\tau_p$ in Fig. 7.10.

(C) Exercise 7.4

P: The 1N5472A n^+-p abrupt junction diode yielding the reverse-bias C–V data plotted in Fig. 7.3 and analyzed in Exercise 7.2 has a zero-bias junction capacitance of $C_{J0} = 120$ pF. The V_{bi} value affording the best fit to junction capacitance data was determined to be 0.7 V in Exercise 7.2. From I–V data following the procedure outlined in Exercise 6.7, one obtains $I_0 = 8 \times 10^{-13}$ A and $n_1 = 1.22$. The p-side minority carrier lifetime is estimated to be $\tau_n = 5 \times 10^{-7}$ sec.

(a) Assuming $\omega\tau_n = 0.01$, but employing relationships valid for arbitrary values of $\omega\tau_n$, compute and plot the expected C_J, C_D, and $C_J + C_D$ versus V_A for the given diode. Restrict V_A to $0 \leq V_A \leq 0.65$ V. Specifically note the approximate voltage where $C_D = C_J$.

(b) Repeat part (a) setting $\omega\tau_n = 0.1$, 1, 10, and 100. Comment on the results.

S: The primary relationships employed in the computation are:

$$C_J = \frac{C_{J0}}{\left(1 - \dfrac{V_A}{V_{bi}}\right)^{1/2}}$$

$$C_D = \frac{\tau_n G_0}{\omega\tau_n\sqrt{2}}\left(\sqrt{1 + \omega^2\tau_n^2} - 1\right)^{1/2}$$

and

$$G_0 = \frac{q}{kT} I_0 e^{qV_A/n_1 kT}$$

The C_J expression is Eq. (7.9) with $m = 0$. The C_D relationship is Eq. (7.29b) with τ_p replaced by τ_n and a τ_n associated with the ω external to the square root. G_0 is the Eq. (7.15) low-frequency conductance with n_1 inserted into the exponent to account for the nonideality of the diode.

The MATLAB program script and the part (a) computational results are reproduced below. Actual forward-bias C–V data derived from the 1N5472A using the

HP4284A LCR Meter (Fig. 7.9) are included on the plot. The junction capacitance is noted to dominate at low forward biases, with the diffusion capacitance rising to $C_D = C_J$ at $V_A \cong 0.545$ V. The same computational results are obtained, as expected, for all $\omega\tau_n < 1$. With increasing $\omega\tau_n$ greater than $\omega\tau_n = 1$, C_D progressively decreases at all biases and the $C_D = C_J$ point shifts to higher and higher voltages. $C_D = C_J$ at $V_A \cong 0.575$ V and 0.62 V when $\omega\tau_n = 10$ and 100, respectively.

MATLAB program script...

```
%Exercise 7.4...Forward-Bias Capacitance

%Computational constants
clear
CJ0=120e-12;        %farads
Vbi=0.7;            %volts
Vth=0.0259;         %Vth=kT/q in volts
taun=5.0e-7;        %seconds
I0=8.0e-13;         %amps
n1=1.22;            %ideality factor
wt=input('input the angular-frequency*lifetime product--');
VA=linspace(0,0.65);

%CJ Computation
CJ=CJ0./sqrt(1-VA./Vbi);

%CD Computation
G0=I0/Vth*exp(VA./(n1*Vth));
CD=taun.*G0./(sqrt(2)*wt)*sqrt(sqrt(1+(wt)^2)-1);

%Measured CD Data
VAm=[0.1 0.2 0.3 0.4 0.42 0.44 0.46 0.48 0.50 0.52 0.54 0.56 0.58];
CDm=[1.31e-10 1.43e-10 1.61e-10 1.88e-10 1.97e-10 2.08e-10 ...
2.23e-10 2.46e-10 2.76e-10 3.46e-10 4.40e-10 6.54e-10 9.38e-10];

%Plot
close
semilogy(VA,CJ,'--r'); axis([0 0.7 1.0e-10 1.0e-9]); grid
hold on; semilogy(VA,CD,'--g'); semilogy(VA,CJ+CD)
semilogy(VAm,CDm-2e-12,'o')
xlabel('VA (volts)'); ylabel('C (farads)')

%Key
semilogy(0.12,7e-10,'o'); text(0.125,7e-10,'...C-V Data')
x=[0.1 0.2];
y1=[6.1e-10 6.1e-10]; semilogy(x,y1,'-y'); text(0.21,6.1e-10,'CJ+CD')
y2=[5.2e-10 5.2e-10]; semilogy(x,y2,'--r'); text(0.21,5.2e-10,'CJ')
y3=[4.3e-10 4.3e-10]; semilogy(x,y3,'-.g'); text (0.21,4.3e-10,'CD')
hold off
```

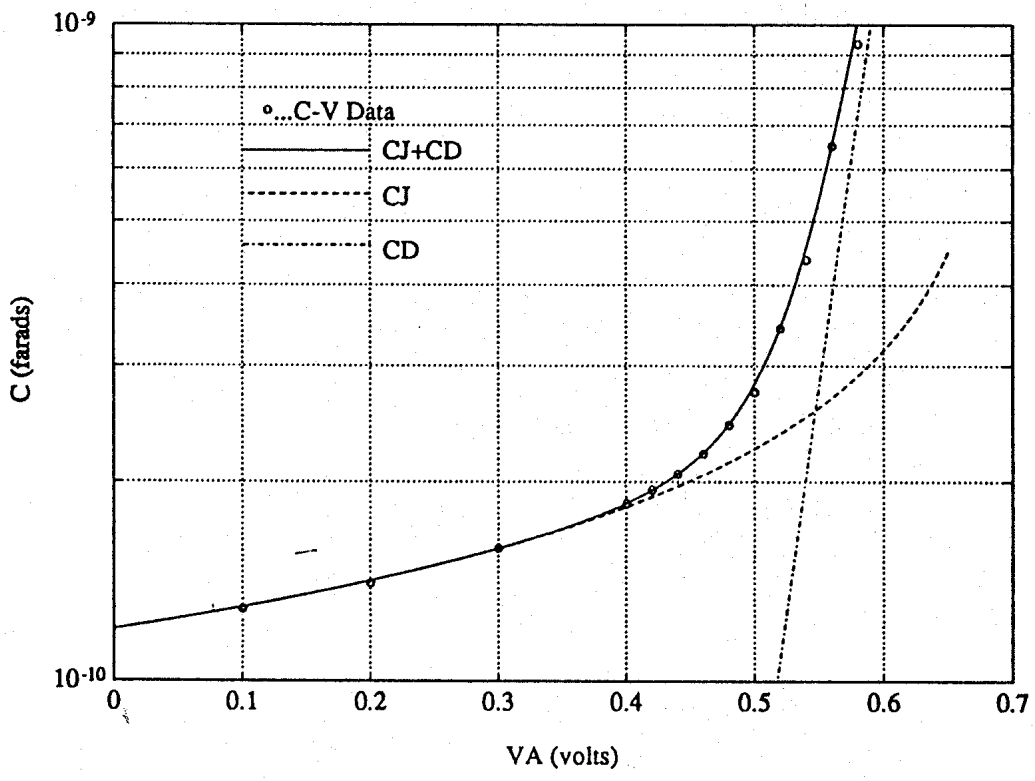

Figure E7.4

7.4 SUMMARY

The chapter was devoted to examining and modeling the small-signal response of the *pn* junction diode. The discussion was divided into two parts corresponding to reverse-biasing and forward-biasing of the diode. When reverse-biased, the *pn* junction diode is functionally equivalent to a capacitor. The capacitance of the diode can in fact be computed using the well-known parallel plate capacitor formula (Eq. 7.2). The *pn* junction diode differs from a standard capacitor in that the diode capacitance monotonically decreases with increasing reverse bias. The reverse-bias junction capacitance arises physically from the in-and-out movement of the majority carriers about the steady state depletion width in response to the a.c. signal. Reverse-bias diodes are employed as capacitors and variable capacitors (varactors) in numerous circuit applications. Capacitance measurements are used extensively in the characterization and testing of devices, particularly in determining the average doping or doping profile on the lightly doped side of a junction. The relevance of the profile to the use of the diode as a varactor, and parameter extraction/profiling procedures, were noted during the course of the discussion.

When the diode is forward-biased, there is a significant build-up of minority carriers in the quasineutral regions immediately adjacent to the depletion region. The oscillation of the minority carrier charge in response to the a.c. signal gives rise to an additional admittance component, the diffusion admittance. An expression for the diffusion admittance was established by appropriately modifying the ideal diode equation. The diffusion admittance

components are strong functions of the d.c. bias, eventually dominating the observed admittance as the forward bias is progressively increased. At signal frequencies where $\omega\tau \gtrsim 1$, the minority carriers have trouble following the a.c. signal and the resulting out-of-phase oscillations enhance the diffusion conductance at the expense of the diffusion capacitance.

PROBLEMS

CHAPTER 7 PROBLEM INFORMATION TABLE				
Problem	*Complete After*	*Difficulty Level*	*Suggested Point Weighting*	*Short Description*
7.1	7.4	1	16 (2 each part)	Quick quiz
7.2	7.2.2	2	10	Derive Eq. (7.6)
•7.3	"	2	12 (a/b-10, c-2)	Dimensioned C–V plot
*7.4	7.2.3	2	15 (plot-5, i-5, ii-5)	Deduce N_B, V_{bi} from C–V
7.5	"	3	10	Derive Eqs. (7.12)/(7.13)
•7.6	"	3	15	$N_B(x)$ versus x
•7.7	7.3.2	1	5	Verify accuracy of Fig. 7.10
•7.8	"	2	10 (prog-8, questions-2)	Relative size of ωC_D, G_D
7.9	"	2	10	τ measurement

7.1 Quick Quiz.

Answer the following questions as concisely as possible.

(a) What is the physical origin of the junction capacitance?

(b) Sketch the $m = -1$ hyperabrupt profile of an n^+-p junction.

(c) Define *quasistatically.*

(d) Define *varactor.*

(e) Define *profiling.*

(f) Make a sketch of the low-frequency conductance of an ideal diode showing both forward and reverse bias. Comment as necessary to forestall a misinterpretation of your sketch.

(g) What is the physical origin of the diffusion admittance?

(h) Why does the diffusion conductance increase with increasing $\omega\tau_p$ when $\omega\tau_p \gtrsim 1$?

7.2 Given the one-sided power-law profile described by Eq. (7.5), and generally following the procedures outlined in Chapter 5, derive Eq. (7.6). Assume a p^+-n junction where $N_B(x) = N_D(x)$. Why is it necessary to specify $m > -2$?

• **7.3** (a) Construct a computer program that yields fully dimensioned reverse-bias C–V curves that can be compared directly with experimental data. The program is to be specifically designed for comparison with the data from Si p^+-n abrupt junction diodes maintained at 300 K. The diode area (A), the lightly doped side concentration (N_B), and the largest reverse-bias voltage of interest ($|V_A|_{max}$) are to be input variables.

(b) Employing $A = 3.72 \times 10^{-3}$ cm^2 and $N_B = 8.84 \times 10^{15}$/cm^3, compare your program output with the experimental data presented in Fig. 7.3. Does the V_{bi} result cited in Exercise 7.2 have any bearing on the agreement between experiment and theory?—Explain.

(c) How does the lightly doped side concentration affect the junction capacitance? Substantiate your answer.

NOTE: Those seeking a greater challenge might consider generalizing the computer program in this problem to handle any one-sided power-law profile.

* **7.4** The 1N4002 is one of the popular 4000-series general-purpose diodes used in automotive and other applications. C–V data from a 1N4002 p^+-n junction diode is listed in Table P7.4. Before analyzing the data, subtract 3pF from each capacitance value to account for the stray capacitance shunting the encapsulated diode. Assuming the diode profile to be abrupt and $A = 6 \times 10^{-3}$ cm^2, apply the plot approach described in the text to determine the lightly doped side concentration and the "best-fit" V_{bi}. Quote the results obtained by (i) "eyeballing" a straight line through the data and (ii) by performing a least squares fit to the data. (NOTE: The 1N4002 is not as ideally abrupt as the 1N5472A of Exercise 7.2. Do not be surprised if your plot points deviate somewhat from a straight line.)

Table P7.4 1N4002 Reverse-Bias C–V Data.

V_A(V)	C(pF)	V_A(V)	C(pF)
0.0	38.709	−5.0	15.548
−0.2	33.717	−6.0	14.599
−0.4	30.567	−7.0	13.834
−0.6	28.319	−8.0	13.189
−0.8	26.598	−9.0	12.639
−1.0	25.170	−10.0	12.163
−1.4	23.060	−11.0	11.746
−1.8	21.490	−12.0	11.373
−2.2	20.254	−13.0	11.037
−2.6	19.248	−14.0	10.734
−3.0	18.405	−15.0	10.458
−4.0	16.762		

7.5 Derive Eqs. (7.12) and (7.13). HINT: See, for example, p. 43 in reference [3].

● **7.6** Construct a computer program that accepts C–V data input and outputs a plot of the $N_B(x)$ versus x profile based on Eqs. (7.12) and (7.13). Test run your program using the 1N4002 data in Table P7.4.

♦ **7.7** Verify the accuracy of Fig. 7.10. Compute and simultaneously plot the diffusion capacitance and diffusion conductance normalized to their low-frequency values as a function of $\omega\tau_p$. Limit the computation to $0.01 \leq \omega\tau_p \leq 100$.

● **7.8** What is the relative size of the capacitive and conductive components of the diffusion admittance at a given d.c. bias and signal frequency? To answer this question, first examine Eqs. (7.29) and (7.30) to determine the limiting values of $\omega C_D/G_D$ when $\omega\tau_p \ll 1$ and $\omega\tau_p \gg 1$. Next, compute and plot $\omega C_D/G_D$ versus $\omega\tau_p$ for $0.01 \leq \omega\tau_p \leq 100$. Does your plot approach the correct limiting values? In words, what is the answer to the original question?

7.9 Forward bias admittance measurements have been used to determine the minority carrier lifetime on the lightly doped side of a junction. Note from Eqs. (7.30) that, given a p^+-n diode, $C_D/G_D = \tau_p/2$ when $\omega\tau_p \ll 1$. Forward bias C–V data from a 1N5472A diode was presented in Exercise 7.4. The corresponding G_D–V_A data for forward biases between 0.50 V and 0.58 V are listed in the following table. Determine the apparent τ_n of the 1N5472A n^+-p diode at each of the listed voltages assuming $\omega\tau_n \ll 1$. Also quote the average τ_n deduced from the data.

V_A(V)	G_D(S)
0.50	2.00×10^{-4}
0.52	3.90×10^{-4}
0.54	7.15×10^{-4}
0.56	1.33×10^{-3}
0.58	2.28×10^{-3}