14 MS Contacts and Schottky Diodes

The metal-semiconductor (MS) contact plays a very important role of one kind or another in all solid-state devices. When in the form of a non-rectifying or ohmic contact, it is the critical link between the semiconductor and the outside world. The rectifying MS contact, referred to as the Schottky diode or the MS diode, is found in a number of device structures and is an important device in its own right. Physically and functionally, there are close similarities between the MS diode and the asymmetrical (p^+-n or n^+-p) step junction diode. Indeed, a large portion of the *pn* diode analysis can be applied directly to the MS diode with only minor modifications.

We initiate the MS analysis by establishing the equilibrium energy band diagram for an ideal contact. With the aid of the diagram, one can readily distinguish between rectifying and ohmic contacts. The next section treats the electrostatics, I–V characteristics, a.c. response, and transient response of the Schottky diode. The chapter concludes with a presentation of select practical information about MS contacts.

14.1 IDEAL MS CONTACTS

An ideal MS contact has the following properties: (1) The metal and semiconductor are assumed to be in intimate contact on an atomic scale, with no layers of any type (such as an oxide) between the components. (2) There is no interdiffusion or intermixing of the metal and semiconductor. (3) There are no adsorbed impurities or surface charges at the MS interface.

The initial task at hand is to construct the energy band diagram appropriate for an ideal MS contact under equilibrium conditions. The surface-included energy band diagrams for the individual, electrically isolated metal and semiconductor components are pictured in Fig. 14.1. Flat band (zero field) conditions are assumed to exist throughout the semiconductor. In both diagrams the vertical line where the energy bands are abruptly terminated is meant to represent a surface. The cross-hatching on the diagrams identifies allowed states that are nearly completely filled with electrons.

Several key energies and energy differences are readily introduced with the aid of Fig. 14.1. The ledge at the top of the vertical line denotes the minimum energy an electron must possess to completely free itself from the material and is called the *vacuum level*, E_0. The energy difference between the vacuum level and the Fermi energy is known as the

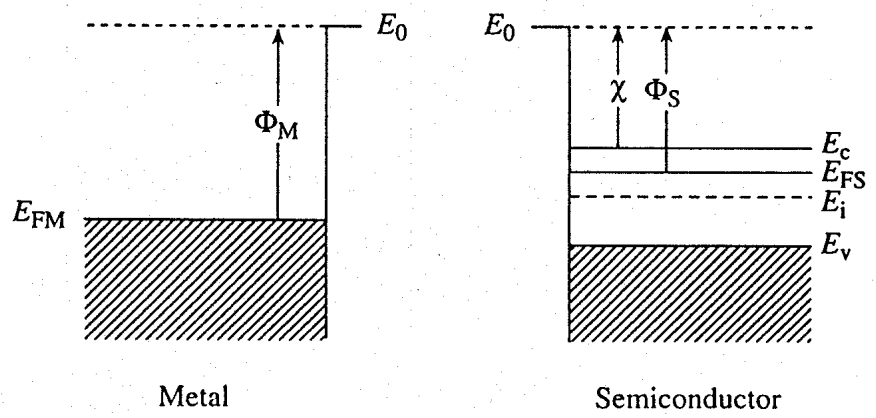


Figure 14.1 Surface-included energy band diagrams for a metal (left) and n-type semiconductor (right).

workfunction (Φ) of the material. The metal workfunction, Φ_M, is an invariant fundamental property of the specified metal. The value of Φ_M ranges from 3.66 eV for magnesium to 5.15 eV for nickel. The semiconductor workfunction, Φ_S, is composed of two distinct parts; that is

$$\Phi_S = \chi + (E_c - E_F)_{FB} \tag{14.1}$$

The *electron affinity*, $\chi \equiv (E_0 - E_c)|_{surface}$, is an invariant fundamental property of the specified semiconductor. χ = 4.0 eV, 4.03 eV, and 4.07 eV for Ge, Si, and GaAs, respectively. Conversely, $(E_c - E_F)_{FB}$, the energy difference between E_c and E_F under flat band or zero field conditions, is a computable function of the semiconductor doping.

Suppose now the $\Phi_M > \Phi_S$ metal and n-type semiconductor of Fig. 14.1 are brought together to form an ideal MS contact. Let us assume the contact formation is accomplished almost instantaneously so that there is negligible electron transfer between the components during the contacting process. If this be the case, then an instant after formation the energy band diagram for the contact will be as pictured in Fig. 14.2(a). In this figure the isolated energy band diagrams are vertically aligned to the common E_0 reference level and simply abutted at the mutual interface. It should be emphasized that Φ_M and χ are material constants and remain unaffected by the contacting process.

Since $E_{FS} \neq E_{FM}$, the MS contact characterized by Fig. 14.2(a) is obviously not in equilibrium. Under equilibrium conditions the Fermi level in a material or a group of materials in intimate contact must be invariant with position (see Subsection 3.2.4). Consequently, a short time after the conceptual contact formation, electrons will begin transferring from the semiconductor to the metal given the situation pictured in Fig. 14.2(a). The net loss of electrons from the semiconductor creates a surface depletion region and a growing barrier to electron transfer from the semiconductor to the metal. This will continue until the transfer rate across the interface is the same in both directions and E_F is the same

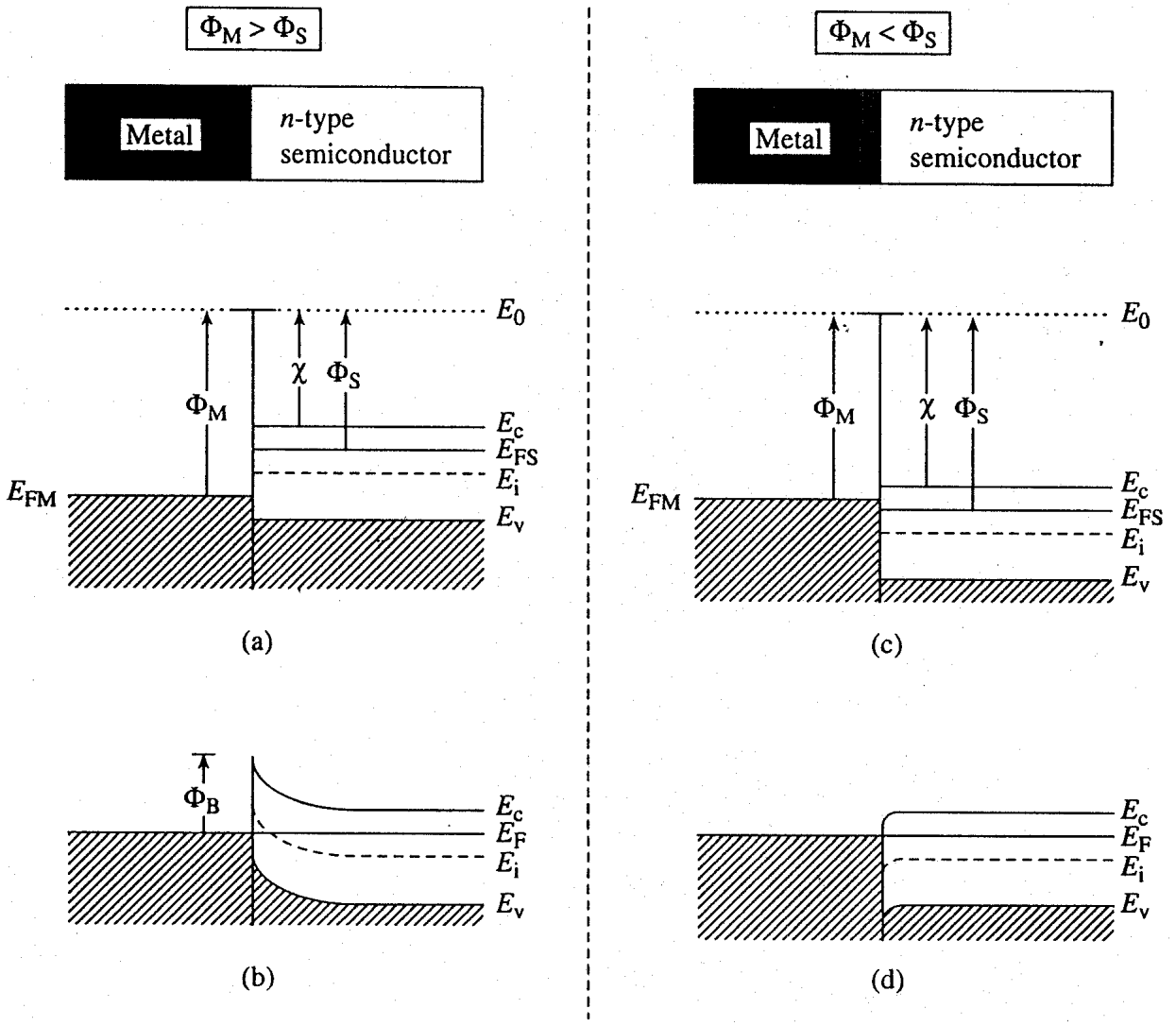


Figure 14.2 Energy band diagrams for ideal MS contacts between a metal and an n-type semiconductor: $\Phi_M > \Phi_S$ system (a) an instant after contact formation and (b) under equilibrium conditions; $\Phi_M < \Phi_S$ system (c) an instant after contact formation and (d) under equilibrium conditions.

throughout the structure. The net result, the equilibrium energy band diagram for an ideal $\Phi_M > \Phi_S$ metal to n-type semiconductor contact, is shown in Fig. 14.2(b). In drawing this figure, extraneous lines such as the E_0 reference level and the portion of the vertical surface line above E_c have been removed. Also note that

$$\Phi_B = \Phi_M - \chi \quad \ldots \text{ ideal MS}(n\text{-type}) \text{ contact} \tag{14.2}$$

where Φ_B is the surface potential-energy barrier encountered by electrons with $E = E_F$ in the metal. Finally, if the entire argument is repeated for a metal and n-type semiconductor where $\Phi_M < \Phi_S$, one obtains the equilibrium energy band diagram shown in Fig. 14.2(d).

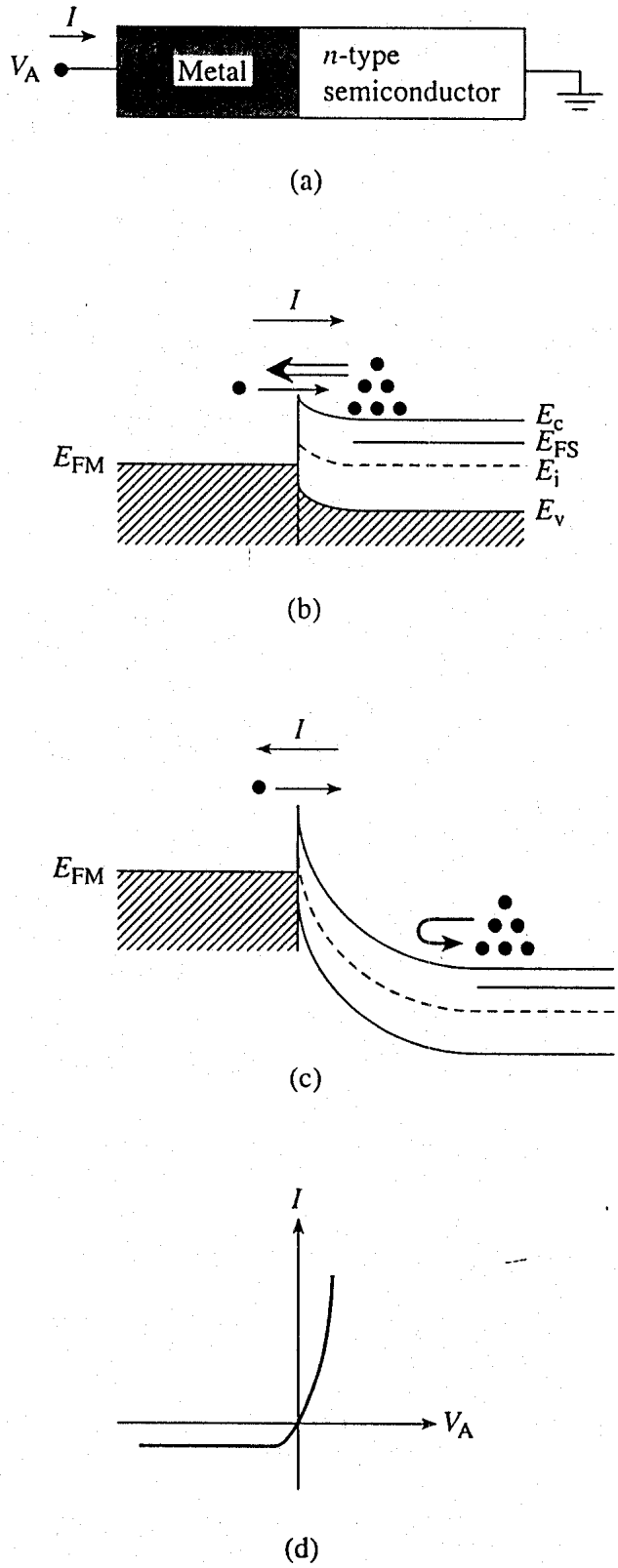


Figure 14.3 Response of the $\Phi_M > \Phi_S$ (n-type) MS contact to an applied d.c. bias. (a) Definition of current and voltage polarities. (b) Energy band diagram and carrier activity when $V_A > 0$. (c) Energy band diagram and carrier activity when $V_A < 0$. (d) Deduced general form of the I–V characteristics.

Let us next qualitatively examine the effect of biasing the two MS structures in Fig. 14.2. As specified in Fig. 14.3(a), the semiconductor is taken to be grounded and V_A applied to the metal. The current I is defined to be positive when current flows from the metal to the semiconductor.

Consider first the $\Phi_M > \Phi_S$ MS contact. Applying a $V_A > 0$ as in Fig. 14.3(b) lowers E_{FM} below E_{FS}, reduces the barrier seen by electrons in the semiconductor, and therefore permits a net flow of electrons from the semiconductor to the metal. Increasing V_A leads to a rapidly rising forward bias current, since an exponentially increasing number of electrons from the semiconductor are able to surmount the surface barrier. On the other hand, applying a $V_A < 0$ raises E_{FM} above E_{FS} as pictured in Fig. 14.3(c). This all but blocks the flow of electrons from the semiconductor to the metal. Some electrons in the metal will be able to surmount the Φ_B barrier, but the associated reverse-bias current should be relatively small. Moreover, since Φ_B is ideally the same for all reverse biases, the reverse current is expected to remain constant after the reverse bias exceeds a few kT/q volts. Clearly, we have just described rectifying characteristics similar to that displayed by a *pn* junction diode. The ideal *n*-type semiconductor to metal contact where $\Phi_M > \Phi_S$ is identified as an MS diode.

The response to an applied bias is considerably different for the $\Phi_M < \Phi_S$ MS contact. There is no barrier of any kind in the Fig. 14.2(d) structure for electron flow from the semiconductor to the metal. Thus even a small $V_A > 0$ gives rise to a large forward bias current. Under reverse biasing there is a small barrier for electron flow from the metal to the semiconductor, but the barrier essentially vanishes if the reverse bias exceeds a few tenths of a volt. Large reverse currents are expected at relatively small reverse biases, and the reverse current definitely does not saturate. The behavior here is obviously nonrectifying or ohmic-like.

The overall conclusion is that an ideal MS contact formed from a metal and an *n*-type semiconductor will be a rectifying contact if $\Phi_M > \Phi_S$ and an ohmic-like contact if $\Phi_M < \Phi_S$. Parallel arguments applied to an ideal MS contact formed from a metal and a *p*-type semiconductor lead to the conclusion that the contact will be rectifying if $\Phi_M < \Phi_S$ and ohmic-like if $\Phi_M > \Phi_S$. These conclusions are summarized in Table 14.1. It should be reemphasized that all results and conclusions in this section are contingent upon the MS contact being ideal. Required modifications imposed by the often nonideal nature of real MS contacts are discussed in Section 14.3.

Table 14.1 Electrical Nature of Ideal MS Contacts.

	n-type Semiconductor	*p-type Semiconductor*
$\Phi_M > \Phi_S$	Rectifying	Ohmic
$\Phi_M < \Phi_S$	Ohmic	Rectifying

Exercise 14.1

P: (a) Construct the equilibrium energy band diagram appropriate for an ideal p-type semiconductor to metal contact where $\Phi_M < \Phi_S$.

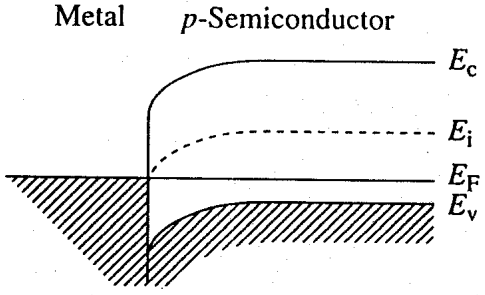
(b) Repeat part (a) when $\Phi_M > \Phi_S$.

(c) Verify that an ideal MS contact formed from a metal and a p-type semiconductor will be rectifying if $\Phi_M < \Phi_S$ and ohmic-like if $\Phi_M > \Phi_S$.

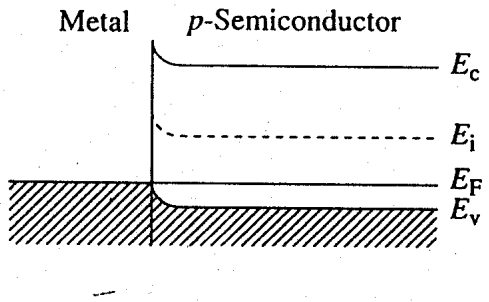
(d) Establish an expression for the barrier height, $\Phi_B \equiv E_{FM} - E_{v|interface}$, of the rectifying p-type contact.

S: (a)/(b) The "prescription" for drawing the equilibrium energy band diagram established in the text can be summarized as follows: (i) Draw the surface-included energy band diagrams for the individual components. (ii) Vertically align the diagrams to the common E_0 reference level, and join the diagrams at the mutual interface. (iii) Without changing the interfacial positioning of the semiconductor bands, move the field-free semiconductor bulk (the region far from the interface) up or down until E_F is constant everywhere. (iv) Appropriately connect up the E_c, E_i, and E_v at the interface with the field-free positioning of the bands in the semiconductor bulk. (v) Eliminate extraneous lines.

Following the cited prescription one obtains the equilibrium energy band diagrams shown below.



(a) $\Phi_M < \Phi_S$



(b) $\Phi_M > \Phi_S$

(c) Hole flow under bias must be examined to determine whether the given MS contacts are rectifying or ohmic. Empty electronic states in the metal, which decrease exponentially with energy below the Fermi level, can be thought of as holes for the purpose of the discussion. For the $\Phi_M < \Phi_S$ contact, there is clearly a barrier to hole flow in both directions under equilibrium conditions. Moving E_{FM} upward relative to E_{FS} reduces the barrier to hole flow from the semiconductor to the metal. The resulting S $\rightarrow$ M hole current is expected to increase exponentially with increased separation between E_{FM} and E_{FS}. Reversing the bias blocks hole flow from the semiconductor to the metal, leaving only a saturating hole current from the metal to the

semiconductor. The $\Phi_M < \Phi_S$ contact is obviously rectifying. For the $\Phi_M > \Phi_S$ contact, there is no barrier to hole flow from the semiconductor to the metal. Moreover, the small barrier to hole flow from the metal to the semiconductor vanishes if E_{FM} is moved only slightly downward relative to E_{FS}. The $\Phi_M > \Phi_S$ contact is concluded to be ohmic-like, thereby completing the required verification.

(d) Since

$$E_{c|interface} - E_{FM} = \Phi_M - \chi$$

it follows that

$$\Phi_B = E_{FM} - E_{v|interface} = (E_c - E_v) - (E_{c|interface} - E_{FM})$$

or

$$\Phi_B = E_G + \chi - \Phi_M \quad \ldots \text{ ideal MS}(p\text{-type}) \text{ contact}$$

14.2 SCHOTTKY DIODE

Having established the basic nature of the rectifying MS contact, we undertake here a more quantitative analysis of the Schottky (MS) diode. Following the usual outline, the analysis includes a survey of the d.c., a.c., and transient characteristics preceded by an examination of the device electrostatics. Strong parallels with the *pn* junction diode permit a relatively condensed presentation. Throughout the discussion we take the semiconductor to be *n*-type and uniformly doped. The assumed current and applied voltage polarities are as specified in Fig. 14.3(a).

14.2.1 Electrostatics

Built-in Voltage

Like in the *pn* junction diode, there is a voltage drop or built-in voltage across the MS diode under equilibrium conditions. Referring to Fig. 14.4(a), the built-in voltage (V_{bi}) is readily deduced to be

$$V_{bi} = \frac{1}{q}\left[\Phi_B - (E_c - E_F)_{FB}\right] \tag{14.3}$$

where as previously noted $\Phi_B = \Phi_M - \chi$ for an ideal MS(*n*-type) contact.

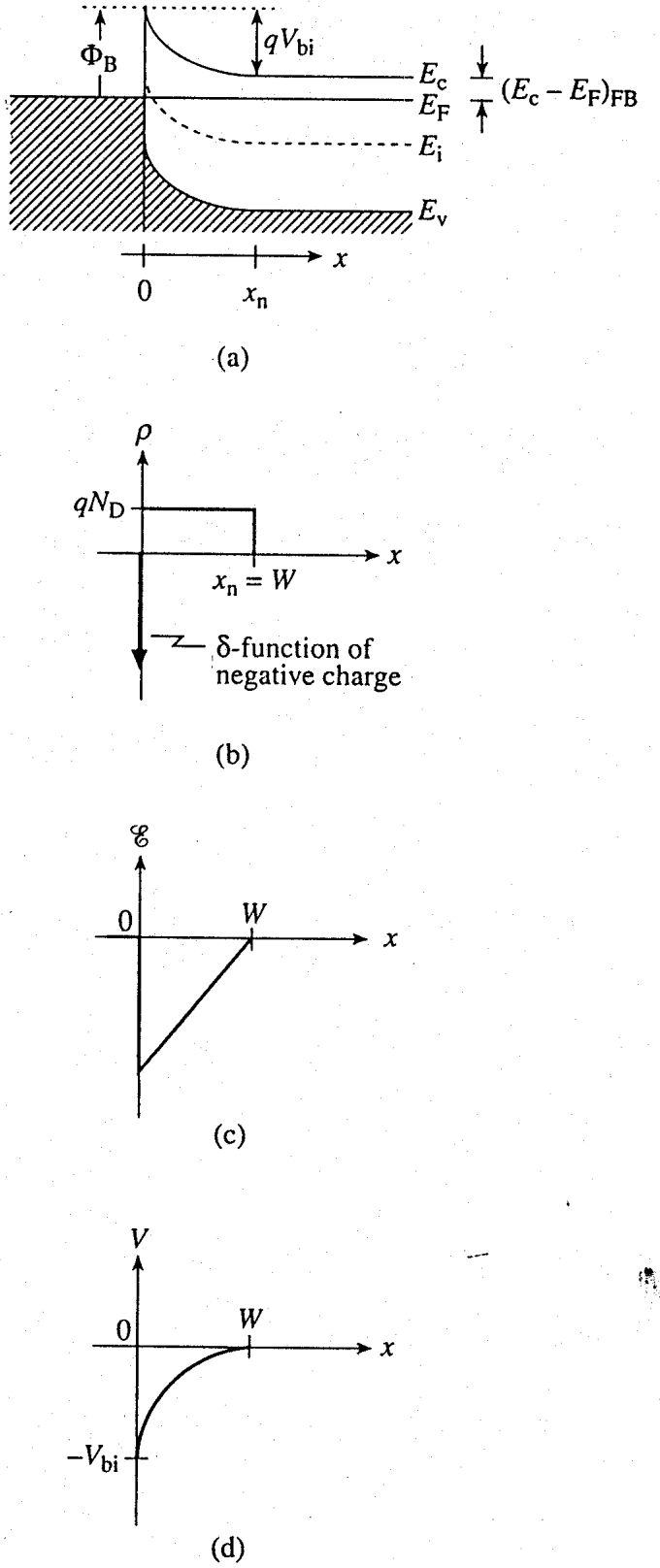


Figure 14.4 Electrostatic variables in an MS (n-type) diode under equilibrium conditions. (a) Equilibrium energy band diagram. (b)–(d) Charge density, electric field, and electrostatic potential as a function of position.

ρ, $\mathscr{E}$, and V

A further examination of Fig. 14.4(a) reveals there is a depletion of electrons in the semiconductor adjacent to the MS interface. Completely analogous to the *pn* junction diode, the depletion region can be viewed as extending a distance x_n into the *n*-type semiconductor, with a net positive charge arising from the donors in the depleted region. Unlike the *pn* junction, however, there is no negative *p*-side acceptor charge to balance the positive *n*-side donor charge. Rather, an essentially δ-function of negative charge (extra electrons) piles up in the metal immediately adjacent to the interface. The charge density inside the structure is therefore concluded to be roughly as pictured in Fig. 14.4(b). Formally invoking the depletion approximation, we can write

$$\rho \cong \begin{cases} qN_D & \ldots 0 \le x \le W \quad (14.4a) \\ 0 & \ldots x > W \quad (14.4b) \end{cases}$$

Note that x_n can be equated to the depletion width W, since the depletion region is totally contained inside the semiconductor.

Given the δ-function nature of the charge on the metal side of the interface, it automatically follows that $\mathscr{E} = 0$ and $V =$ constant inside the metal. Consequently, no further consideration need be given to the metal.

On the semiconductor side of the MS contact, the electric field and charge density are related through Poisson's equation (Eq. 5.2); namely,

$$\frac{d\mathscr{E}}{dx} = \frac{\rho}{K_S \varepsilon_0} \cong \frac{qN_D}{K_S \varepsilon_0} \qquad \ldots 0 \le x \le W \qquad (14.5)$$

Separating variables and integrating Eq. (14.5) from an arbitrary point x in the depletion region to $x = W$ where $\mathscr{E} = 0$, we obtain

$$\int_{\mathscr{E}(x)}^{0} d\mathscr{E}' = \int_{x}^{W} \frac{qN_D}{K_S \varepsilon_0} dx' \qquad (14.6)$$

or

$$\mathscr{E}(x) = -\frac{qN_D}{K_S \varepsilon_0}(W - x) \qquad \ldots 0 \le x \le W \qquad (14.7)$$

Plotted in Fig. 14.4(c), the Eq. (14.7) result is identical to the Eq. (5.21) solution for the $\mathscr{E}$-field on the *n*-side of a p^+-*n* step junction if x_n is equated to W.

Seeking the solution for the electrostatic potential in the semiconductor, we next note

$$\frac{dV}{dx} = -\mathcal{E} = \frac{qN_D}{K_S\varepsilon_0}(W - x) \qquad \ldots 0 \le x \le W \tag{14.8}$$

Once again separating variables and integrating from an arbitrary point x in the depletion region to $x = W$ where the potential is arbitrarily set equal to zero, we obtain

$$\int_{V(x)}^{0} dV' = \int_{x}^{W} \frac{qN_D}{K_S\varepsilon_0}(W - x')\,dx' \tag{14.9}$$

or

$$\boxed{V(x) = -\frac{qN_D}{2K_S\varepsilon_0}(W - x)^2 \qquad \ldots 0 \le x \le W} \tag{14.10}$$

At first glance the solution for $V(x)$ would appear to differ from that in the *pn* junction analysis. Actually, the solutions are totally equivalent. In treating the *pn* junction, the potential was set equal to zero on the far *p*-side of the junction; an MS diode solution of precisely the same form would result if the metal were the $V = 0$ reference. With the analysis focusing on a single semiconductor region as in the MS diode, however, the surface-side edge of the semiconductor bulk is the preferred reference point.

Under equilibrium conditions the potential drop across the depletion region is V_{bi}, $V = -V_{bi}$ at $x = 0$, and the $V(x)$ versus x dependence is as sketched in Fig. 14.4(d). If $V_A \neq 0$, then $V_{bi} \rightarrow V_{bi} - V_A$ and $V = -(V_{bi} - V_A)$ at $x = 0$. The simple $V_{bi} \rightarrow V_{bi} - V_A$ replacement assumes of course that the back contact to the diode is ohmic and that the *IR* potential drop across the semiconductor bulk is negligible.

Depletion Width

Since $V(0) = -(V_{bi} - V_A)$, evaluating Eq. (14.10) at $x = 0$ gives

$$-(V_{bi} - V_A) = -\frac{qN_D}{2K_S\varepsilon_0}W^2 \tag{14.11}$$

Thus, identical to the situation in a p^+-n step junction,

$$\boxed{W = \left[\frac{2K_S\varepsilon_0}{qN_D}(V_{bi} - V_A)\right]^{1/2}} \tag{14.12}$$

Exercise 14.2

P: Copper is deposited on a carefully prepared n-type silicon substrate to form an ideal Schottky diode. $\Phi_M \cong 4.65$ eV, $\chi = 4.03$ eV, $N_D = 10^{16}/\text{cm}^3$, and $T = 300$ K. Determine

(a) Φ_B,

(b) V_{bi},

(c) W if $V_A = 0$, and

(d) $|\mathscr{E}|_{max}$ if $V_A = 0$.

S: (a) $\Phi_B = \Phi_M - \chi = \mathbf{0.62\ eV}$

$$\text{(b) } (E_c - E_F)_{FB} \cong \frac{E_G}{2} - kT \ln\left(\frac{N_D}{n_i}\right) = 0.56 - (0.0259)\ln\left(\frac{10^{16}}{10^{10}}\right) \cong 0.20 \text{ eV}$$

$$V_{bi} = \frac{1}{q}[\Phi_B - (E_c - E_F)_{FB}] = \mathbf{0.42\ V}$$

$$\text{(c) } W = \left[\frac{2K_S\varepsilon_0}{qN_D}(V_{bi} - V_A)\right]^{1/2} = \left[\frac{(2)(11.8)(8.85 \times 10^{-14})}{(1.6 \times 10^{-19})(10^{16})}(0.42)\right]^{1/2}$$

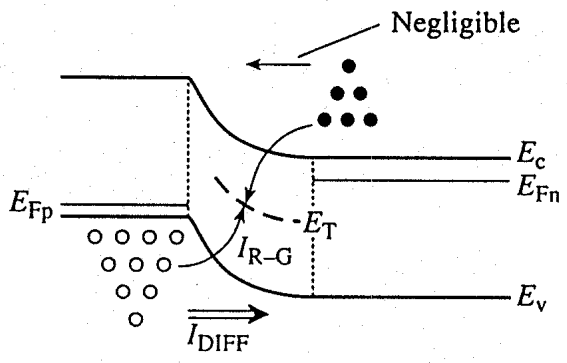
$$= \mathbf{0.234\ \mu m}$$

$$\text{(d) } |\mathscr{E}|_{max} = |\mathscr{E}_{|x=0}| = \frac{qN_D}{K_S\varepsilon_0}W = \frac{(1.6 \times 10^{-19})(10^{16})(2.34 \times 10^{-5})}{(11.8)(8.85 \times 10^{-14})}$$

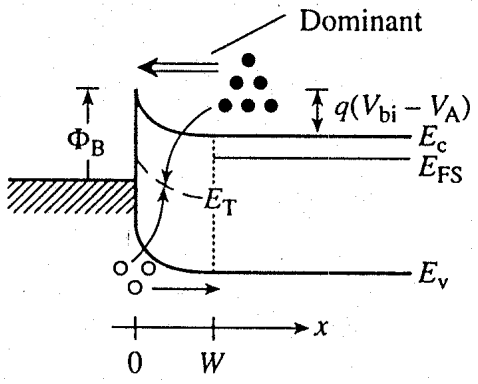
$$= \mathbf{3.59 \times 10^4\ V/cm}$$

14.2.2 *I–V* Characteristics

Whereas the MS diode electrostatics and the general shape of the MS diode I–V characteristics are very similar to those of a pn junction diode, the details of the d.c. current flow are decidedly different. In a p^+-n diode, as reviewed in Fig. 14.5(a), the dominant components of the current typically arise from recombination in the depletion region under small forward biases and hole injection from the p^+ to the n-side of the diode under larger forward biases. The electron injection from the lighter doped n to the p^+-side is always negligible. In an MS(n-type) diode, as pictured in Fig. 14.5(b), the recombination and hole-injection currents still exist. However, because of the relatively low potential barrier seen by electrons in the semiconductor, electron injection from the semiconductor into the metal routinely dominates the observed current. Stated another way, the electron injection leads to a very large forward bias current before the recombination and diffusion (hole-injection) currents become important. The situation under reverse bias is similar. Electron flow from the metal to the semiconductor as previously pictured in Fig. 14.3(c) totally dominates the



(a) p^+–n junction diode



(b) MS diode

Figure 14.5 Negligible and dominant current components in a forward-biased (a) p^+-n junction diode and (b) MS diode.

observed current. The reverse-bias hole diffusion current and the R–G current associated with carrier generation in the depletion region are typically negligible. Reflecting the fact that minority carriers in the semiconductor normally play an insignificant role in determining the I–V and other characteristics, the MS diode is often said to be a "majority carrier device."

The current resulting from majority carrier electron or hole injection over the potential barrier in an MS diode is referred to as the *thermionic emission current.* To establish a quantitative expression for the thermionic emission current, we treat an n-type device and focus initially on electron injection from the semiconductor into the metal. The x-coordinate is assumed to be normal to the MS interface and directed into the semiconductor as shown in Fig. 14.5(b).

Consider an electron entering the depletion region from the semiconductor bulk. The electron is capable of surmounting the surface barrier and crossing into the metal if it has

a v_x velocity directed toward the interface such that

$$\mathrm{KE}_x = \frac{1}{2} m_n^* v_x^2 \geq q(V_{bi} - V_A) \tag{14.13}$$

or

$$|v_x| \geq v_{min} \equiv \left[\frac{2q}{m_n^*}(V_{bi} - V_A)\right]^{1/2} \tag{14.14}$$

Suppose there are $n(v_x)$ electrons/cm^3 in the semiconductor bulk with a negatively directed v_x sufficient to surmount the barrier. Paralleling the drift current derivation in Subsection 3.1.2, the current associated with this set of electrons will be

$$I_{S\bullet\rightarrow M,v_x} = -qAv_x n(v_x) \tag{14.15}$$

Summing over all electrons in the conduction band with v_x velocities capable of surmounting the barrier then gives

$$I_{S\bullet\rightarrow M} = -qA \int_{-\infty}^{-v_{min}} v_x n(v_x)\, dv_x \tag{14.16}$$

For a nondegenerate semiconductor it can be shown that[17]

$$n(v_x) = \left(\frac{4\pi kTm_n^{*2}}{h^3}\right) e^{(E_F - E_c)/kT} e^{-(m_n^*/2kT)v_x^2} \tag{14.17}$$

Substituting Eq. (14.17) into Eq. (14.16), integrating, and simplifying the result, one obtains

$$I_{S\bullet\rightarrow M} = A\mathscr{A}^* T^2 e^{-\Phi_B/kT} e^{qV_A/kT} \tag{14.18}$$

where

$$\mathscr{A}^* \equiv \left(\frac{m_n^*}{m_0}\right)\mathscr{A} \tag{14.19}$$

and

$$\mathscr{A} \equiv \frac{4\pi q m_0 k^2}{h^3} = 120 \text{ amps/(cm}^2 - \text{K}^2) \tag{14.20}$$

The constant $\mathscr{A}$ was introduced in a related analysis of electron emission from metals and has since become known as *Richardson's constant.*

Electrons crossing the interface in the opposite direction from the metal into the semiconductor always see the same potential barrier, Φ_B. Consequently,

$$I_{M\bullet\rightarrow S}(V_A) = I_{M\bullet\rightarrow S}(V_A = 0) \tag{14.21}$$

Moreover, under equilibrium conditions the M●→S and S●→M currents across the barrier must precisely balance, or

$$I_{M\bullet\rightarrow S}(V_A = 0) = -I_{S\bullet\rightarrow M}(V_A = 0) = -A\mathscr{A}^*T^2e^{-\Phi_B/kT} \tag{14.22}$$

The total current at an arbitrary V_A is of course given by

$$I = I_{S\bullet\rightarrow M} + I_{M\bullet\rightarrow S} = I_{S\bullet\rightarrow M} + I_{M\bullet\rightarrow S}(V_A = 0) \tag{14.23}$$

Combining Eqs. (14.18) and (14.22), we therefore conclude

$$\boxed{I = I_s(e^{qV_A/kT} - 1)} \tag{14.24}$$

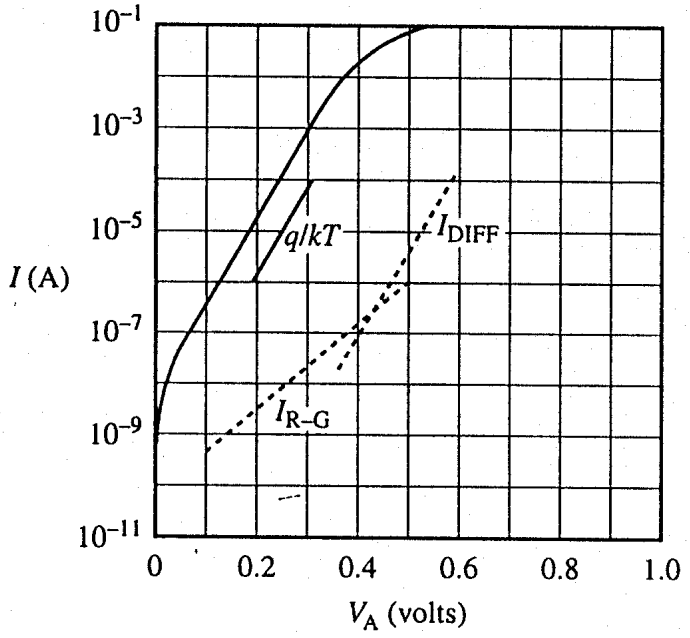
$$I_s \equiv A\mathscr{A}^*T^2e^{-\Phi_B/kT} \tag{14.25}$$

The Eq. (14.24)/(14.25) result is clearly the MS diode version of the ideal diode equation. For forward biases greater than a few kT/q volts, the exponential term in Eq. (14.24) dominates and $I \rightarrow I_s \exp(qV_A/kT)$. For reverse biases greater than a few kT/q volts, the exponential term becomes negligible and the current is predicted to saturate at $I = -I_s$. As formulated, the theory implies I would remain constant at $-I_s$ for reverse biases of unlimited magnitude.

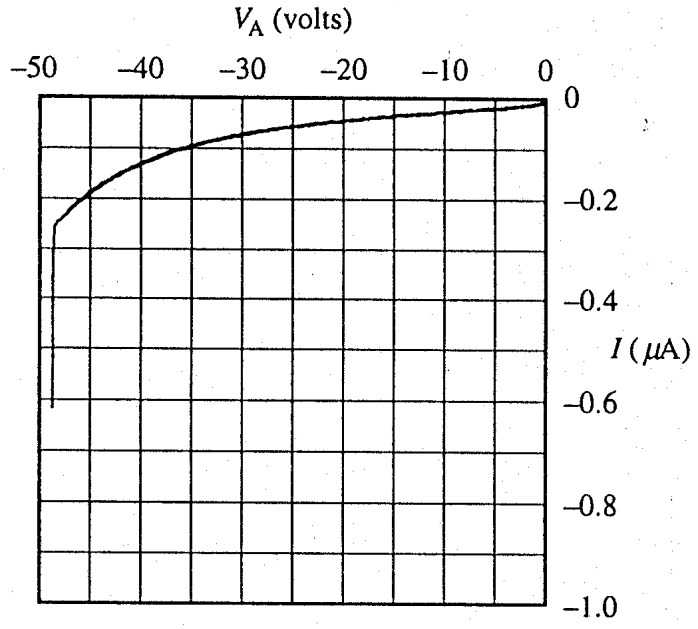
Representative experimental I–V characteristics derived from a MBR040 MS diode are displayed in Fig. 14.6. For forward biases of $V_A \leq 0.35$ V, experiment (the solid line curve in Fig. 14.6a) and theory are in almost perfect agreement. Over the range $0.1\text{ V} \leq V_A \leq 0.35$ V the slope of the forward bias semilog plot is very close to q/kT. Like in the *pn* junction diode, the decrease in slope at larger forward biases is typically caused by an appreciable voltage drop across the bulk series resistance.

Turning to the reverse-bias characteristic in Fig. 14.6(b), we note two significant deviations from the ideal. First, as should have been anticipated, and again paralleling the *pn* junction diode, a breakdown phenomenon limits the maximum magnitude of the reverse bias voltage. In the absence of edge effects, the expected V_{BR} due to avalanching in an MS diode is essentially identical to that of an equivalently doped p^+-n or n^+-p diode. Second, the reverse-bias current does not saturate. Differing from the *pn* junction diode, the observed behavior here cannot be attributed to the recombination–generation current. Rather, the systematic increase in the magnitude of the reverse-bias current is primarily the result of a phenomenon known as *Schottky barrier lowering*. Φ_B is not a bias-independent constant as assumed in the ideal theory, but decreases slightly with reverse biases of increasing magnitude. Specifically,

$$\Phi_B = \Phi_{B0} - \Delta\Phi_B \tag{14.26}$$



(a)



(b)

Figure 14.6 Measured I–V characteristics derived from a MBR040 MS diode: (a) forward bias; (b) reverse bias. The dashed lines in (a) are theoretical estimates of the diffusion (I_{DIFF}) and recombination–generation (I_{R-G}) currents flowing in the diode. The experimental data were obtained employing an HP4145B Semiconductor Parameter Analyzer.

where Φ_{B0} is the barrier height when $\mathscr{E} = 0$ at the MS interface and

$$\Delta\Phi_B = q\left[\frac{q|\mathscr{E}_S|}{4\pi K_S \varepsilon_0}\right]^{1/2} \tag{14.27}$$

$\mathscr{E}_S$, the electric field at the semiconductor surface, is computed using the previously established electrostatic relationships. Since I_s varies as $\exp(-\Phi_B/kT)$, even a small decrease in Φ_B gives rise to a readily noticeable increase in the magnitude of the reverse-bias current. We should point out that, at reverse biases approaching $-V_{BR}$, avalanche multiplication may play a role in enhancing the observed current.

Finally, a comment is in order concerning the dashed lines in Fig. 14.6(a) labeled I_{DIFF} and I_{R-G}. These are theoretical estimates of the diffusion current and recombination current flowing in the given diode. As previously indicated, the I_{DIFF} and I_{R-G} components are seen to be totally negligible compared to the observed thermionic emission current.

(C) Exercise 14.3

P: Assume the 0.1 V $\leq V_A \leq$ 0.35 V portion of the forward-bias characteristic in Fig. 14.6(a) can be modeled by an equation of the form

$$I = I_s e^{qV_A/n_1 kT}$$

where I_s and n_1 are constants. According to Eq. (14.24), the "ideality factor," n_1, should be equal to unity but is usually determined to be slightly greater than unity. Employing the point-by-point data provided in the table below, perform a least squares fit to determine the values of I_s and n_1 that yield an optimum match to the given MS diode characteristics.

V_A (volts)	I (amps)
0.10	4.047×10^{-7}
0.15	2.792×10^{-6}
0.20	1.890×10^{-5}
0.25	1.263×10^{-4}
0.30	8.084×10^{-4}
0.35	4.487×10^{-3}

S: In logarithmic form the fit equation becomes

$$\ln(I) = \ln(I_s) + \frac{q}{n_1 kT} V_A$$

Associating V_A with x and $\ln(I)$ with y, the MATLAB `polyfit` function can be used to perform the required least squares fit to the experimental data. The best fit values derived from the program listed below are $\boxed{n_1 = 1.03}$ and $\boxed{I_s = 1.02 \times 10^{-8} \text{ amps}}$.

MATLAB program script...

```
%Least-Squares fit to MS diode I-V data
%ln(I)=ln(Is)+qVA/n1kT
I=[4.047e-7 2.792e-6 1.890e-5 1.263e-4 8.084e-4 4.487e-3];
VA=[0.1 0.15 0.2 0.25 0.3 0.35];
y=log(I);
c=polyfit(VA,y,1);      %least squares fit function; c(1)=slope, c(2)=ln(Is)
slope=c(1);
format compact
n1=1/(0.0259*slope)     %kT/q=0.0259V
Is=exp(c(2))
```

14.2.3 a.c. Response

A small a.c. signal superimposed on a d.c. reverse bias gives rise to a charge fluctuation inside the diode as pictured in Fig. 14.7. A variation in the depletion width about its equilibrium value and the associated change in charge inside the semiconductor balance fluctuations in the δ-function of charge at the MS interface. Majority carriers move rapidly in and out of the semiconductor to facilitate the variation in the depletion width. With the charge fluctuation taking place along two planes separated by a distance W, the described a.c. situation is physically identical to what takes place inside a parallel plate capacitor. One can therefore write by analogy

$$C = \frac{K_S \varepsilon_0 A}{W} \tag{14.28}$$

or, making use of Eq. (14.12),

$$C = \frac{K_S \varepsilon_0 A}{\left[\dfrac{2K_S \varepsilon_0}{qN_D}(V_{bi} - V_A)\right]^{1/2}} \tag{14.29}$$

for a uniformly doped n-type semiconductor. Also note for future reference that if both sides of Eq. (14.29) are inverted and then squared, one obtains

$$\frac{1}{C^2} = \frac{2}{qN_D K_S \varepsilon_0 A^2}(V_{bi} - V_A) \tag{14.30}$$

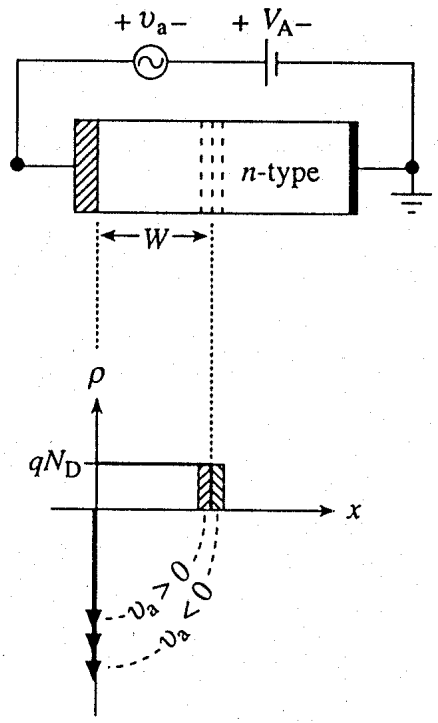


Figure 14.7 Charge fluctuations inside an MS (n-type) diode in response to an applied a.c. signal. $|v_a| \ll V_{bi} - V_A$.

Reverse bias C–V data derived from a commercial MBR040 MS diode are presented in Fig. 14.8(a). The data were obtained using the measurement set-up previously described in Subsection 7.2.3 and schematically pictured in Fig. 7.6. Variation of the capacitance with the applied d.c. bias is generally as expected. Consistent with the predicted $1/\sqrt{V_{bi} - V_A}$ dependence, the capacitance systematically decreases at a slower and slower rate as the reverse bias is increased in magnitude. Figure 14.8(b) provides a more detailed verification of the theory. The $1/C^2$ versus V_A plot of the experimental data exhibits a nearly straight line dependence in agreement with Eq. (14.30). Per Eq. (14.30) the semiconductor doping could be deduced from the slope of the straight line fitted to the plot points and V_{bi} from the extrapolated $1/C^2 = 0$ intercept. In addition, once both the semiconductor doping and V_{bi} are known, Φ_B can be computed employing Eq. (14.3).

Although the reverse bias behavior is essentially identical to that of an asymmetrically doped *pn* junction diode, the forward bias a.c. response of the MS diode is significantly different. In the MS diode the diffusion component of the current is typically negligible. Thus there is very little minority carrier injection and storage within the semiconductor. Since it is stored minority carriers that give rise to the diffusion admittance, *the MS diode does not exhibit a diffusion capacitance or diffusion conductance.* There is of course a forward-bias depletion-region capacitance, a potentially large parallel conductance $G = dI/dV_A$, and a bulk series resistance (R_S) that must be included under certain circumstances. However, even at a.c. frequencies routinely approaching or into the GHz range, C and G remain frequency independent.

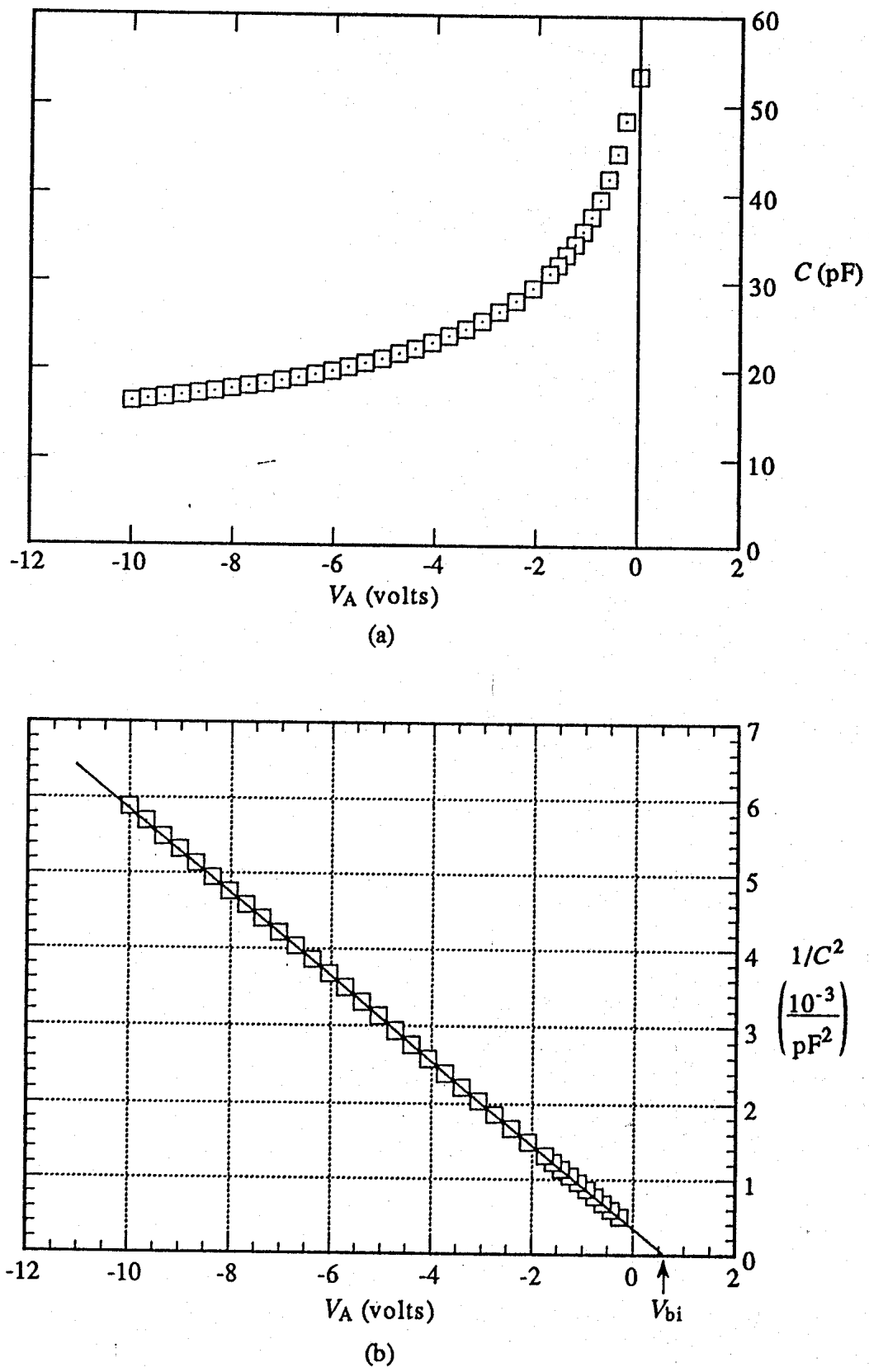


Figure 14.8 (a) Sample C–V data derived from a MBR040 MS diode. (b) $1/C^2$ versus V_A plot constructed from the experimental C–V data. [*Note:* To correct for the encapsulation-related stray capacitance shunting the MS diode, 3.4 pF was subtracted from all measured capacitance values before constructing the part (b) plot.]

Exercise 14.4

P: Working directly with the plotted data in Fig. 14.8(b), estimate the barrier height (Φ_B) inside the MS diode. Assume an n-type device, $A = 1.5 \times 10^{-3}$ cm^2, and room temperature operation.

S: From the extrapolated $1/C^2$ intercept of the straight line drawn through the plot points, we roughly estimate

$$V_{bi} \cong 0.6 \text{ V}$$

The slope of the straight line is approximately

$$\text{slope} = -\frac{6 \times 10^{-3}/\text{pF}^2}{10.3 + 0.6} = -5.5 \times 10^{20}/\text{F}^2\text{-V}$$

and therefore

$$N_D = \frac{2}{qK_S\varepsilon_0 A^2|\text{slope}|}$$

$$\cong \frac{2}{(1.6 \times 10^{-19})(11.8)(8.85 \times 10^{-14})(1.5 \times 10^{-3})^2(5.5 \times 10^{20})}$$

$$= 9.7 \times 10^{15}/\text{cm}^3$$

Noting

$$(E_c - E_F)_{FB} \cong \frac{E_G}{2} - kT \ln\left(\frac{N_D}{n_i}\right) = 0.56 - 0.0259 \ln\left(\frac{9.7 \times 10^{15}}{10^{10}}\right)$$

$$= 0.20 \text{ eV}$$

we conclude, making use of Eq. (14.3),

$$\Phi_B = qV_{bi} + (E_c - E_F)_{FB} \cong 0.6 + 0.2 = \mathbf{0.8 \text{ eV}}$$

14.2.4 Transient Response

A very rapid transient response is the most distinctive characteristic of the MS diode. In *pn* junction devices the excess minority carriers stored in the quasineutral regions of the semiconductor must be removed before the device can be switched from the forward-bias on-

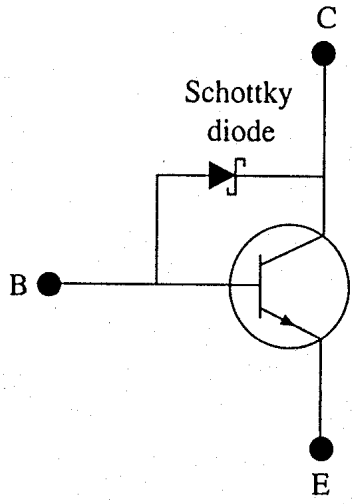


Figure 14.9 Schematic circuit representation of a Schottky-diode-clamped *npn* BJT.

state to the reverse-bias off-state. In an MS diode there is very little minority carrier injection and storage within the semiconductor because the diffusion component of the current is typically negligible. The reverse recovery time of commercial MS diodes is routinely only a few nanoseconds. The MS diode response time can in fact be limited, not by the stored charge, but by the internal *RC* time constant associated with the junction capacitance and the bulk series resistance. Small area devices, sometimes called *hot carrier diodes,* are commercially produced with a maximum $C \lesssim 1$ pF and sub-nanosecond response times.

As first noted in the Chapter 12 discussion of the BJT transient response, the MS diode has been used to speed up the BJT turn-off transient. The arrangement initially pictured in Fig. 12.7(a) and shown again in Fig. 14.9, an arrangement where an MS (Schottky) diode is connected between the base and collector of a BJT, is referred to as a *Schottky diode clamp.* Basically, when the transistor enters the saturation mode during the turn-on transient ($v_{BE} > 0$ and $v_{BC} > 0$), the MS diode begins to conduct and "clamps" the C–B junction at a relatively low forward bias. In other words, use is made of the fact that the MS diode conducts at a lower forward bias than a *pn* junction. Since the C–B junction is held at a relatively low voltage, there is minimal charge storage in the BJT. With less charge to be removed from the BJT and very little charge stored in the Schottky diode, the turn-off time is thereby significantly reduced.

14.3 PRACTICAL CONTACT CONSIDERATIONS

14.3.1 Rectifying Contacts

At the beginning of the chapter, an MS contact was defined to be ideal if the metal and semiconductor were in intimate contact on an atomic scale, there was no intermixing of components, and there were no adsorbed impurities or surface charges at the MS interface. Unfortunately, even though great progress has been made in recent years toward achieving

the ideal MS contact, real MS structures invariably turn out to be nonideal. Silicon devices, for example, are likely to contain a thin (5 Å–25 Å) oxide layer between the metal and semiconductor. A native oxide layer forms almost instantly when Si is exposed to the atmosphere. Arsenic precipitates are believed to form on GaAs surfaces. Allowed electronic states that charge and discharge are known to exist on essentially all semiconductor surfaces. In extreme cases, the cited nonidealities can lead to an ill-functioning or nonfunctioning MS diode. The minimized nonidealities in modern-day structures, however, primarily affect the Φ_B barrier height characterizing the contact.

Contrary to Eq. (14.2), $\Phi_B \neq \Phi_M - \chi$ in most real n-type diodes. A similar statement can be made for p-type diodes. In Si, GaAs, and the majority of other semiconductors, surface charges tend to fix or "pin" the equilibrium Fermi level at a specific energy within the surface band gap. Because of this pinning effect, the observed barrier height normally varies only slightly with the metal used to fabricate the diode. Regardless of the metal employed in forming a GaAs MS diode, for example, $\Phi_B \cong 2E_G/3 = 0.95$ eV for n-type devices and $\Phi_B \cong E_G/3 = 0.47$ eV for p-type devices. Since Φ_B cannot be predicted from a prior knowledge of Φ_M and χ, measurements must be performed to accurately determine Φ_B for a given MS system and fabrication procedure. An C–V based approach similar to that outlined in Exercise 14.4 is one of the more popular measurement techniques. It should be emphasized that the formalism developed in the previous section still applies provided one employs the measured Φ_B in all relevant expressions.

14.3.2 Ohmic Contacts

Metal-semiconductor contacts that have a low impedance regardless of the biasing polarity are an essential part of just about every modern device structure. Although metal-semiconductor combinations where $\Phi_M < \Phi_S$(n-type) and $\Phi_M > \Phi_S$(p-type) ideally yield ohmic contacts, it follows from the barrier height comments in the preceding subsection that the noted metal-semiconductor combinations could produce rectifying contacts in practice. As a case in point, because the surface Fermi level tends to be pinned at $E_c - 2E_G/3$ in GaAs, the deposition of *any* metal on n-type GaAs forms a barrier-type contact. It is reasonable then to ask, "How are ohmic contacts achieved in practice?"

Ohmic contacts are usually produced in practice by heavily doping the surface region of the semiconductor immediately beneath the contact. In Si processing, for example, an n^+ on n region as shown in Fig. 14.10(a) would be created prior to deposition of the metal. The reason this procedure leads to a low-impedance contact can be explained with the aid of Fig. 14.10(b). The equilibrium barrier height is to first order unaffected by an increase in the semiconductor doping. However, the depletion width, and hence the width of the barrier, systematically decrease with increased semiconductor doping. When the semiconductor doping exceeds $\sim 10^{17}/\text{cm}^3$, significant tunneling can take place through the thin upper portion of the barrier. For dopings exceeding $\sim 10^{19}/\text{cm}^3$, the entire barrier becomes so narrow that even low energy majority carriers can readily transfer between the semiconductor and metal via the tunneling process. In other words, although the barrier exists, it effectively becomes transparent to carrier flow when the contact is formed on a heavily doped semiconductor.

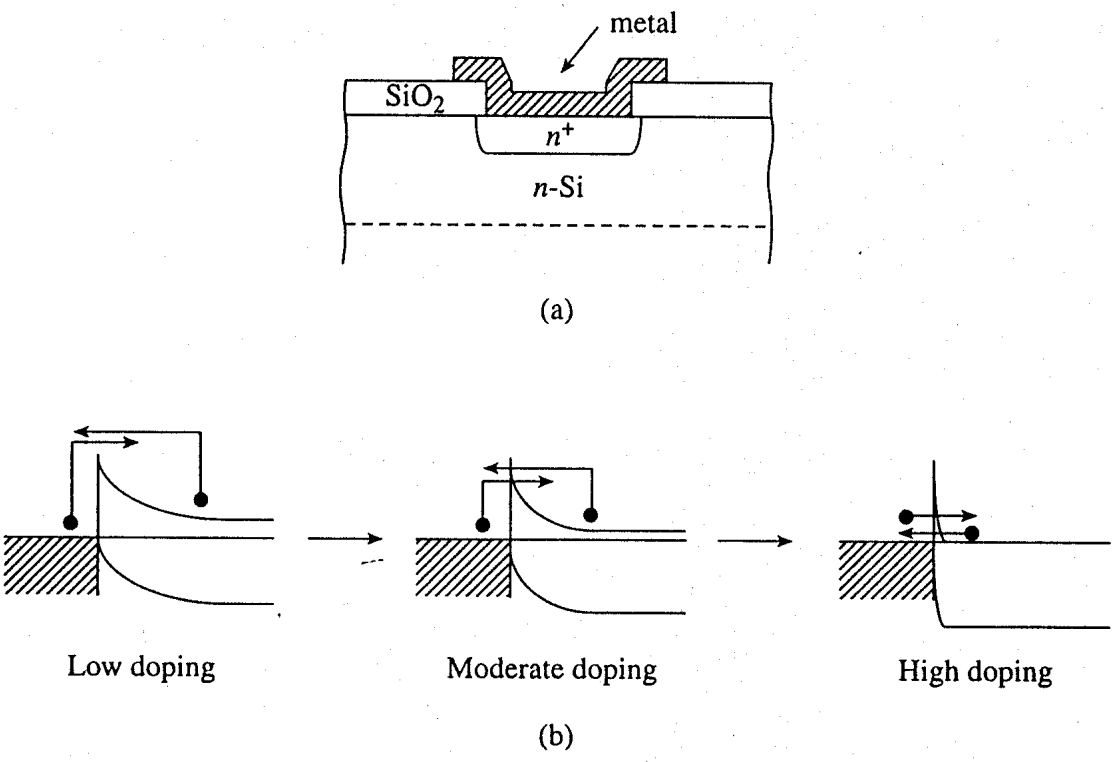
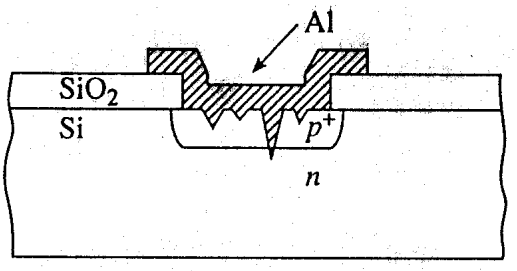


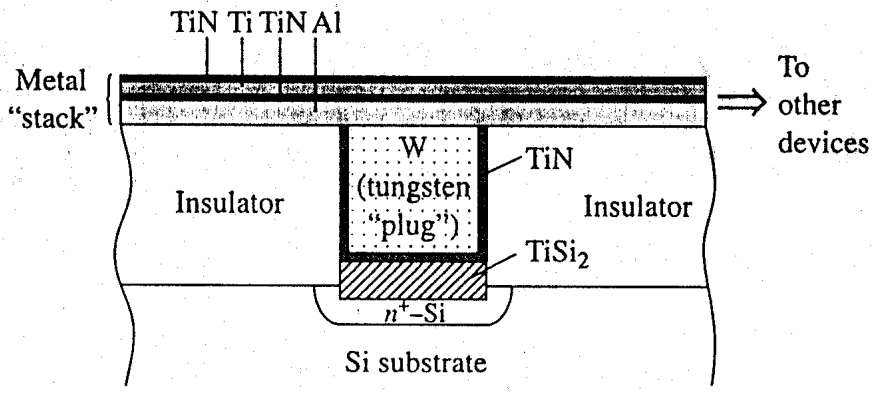
Figure 14.10 Ohmic contact formation. (a) Heavy doping of the semiconductor beneath the MS contact to facilitate ohmic contact formation. (b) Emission currents across a barrier-type contact as a function of doping. The emission is shown varying from solely thermionic emission at low semiconductor dopings to predominantly field emission (tunneling through the barrier) at high semiconductor dopings.

Whereas heavy doping of the underlying semiconductor is a key step in ohmic contact formation, it is seldom the entire story. Annealing or heating the device structure is routinely necessary to minimize the contact resistance. Aluminum is the most widely used contacting metal in the fabrication of discrete Si devices. Heating to approximately 475° C for a few minutes in a nitrogen atmosphere allows the aluminum to penetrate the native oxide layer on the Si surface and facilitates a certain amount of beneficial Al-Si interdiffusion. In contacts formed over shallow p^+-n or n^+-p junctions, however, nonuniform interdiffusion over the contact area can lead to penetration of the aluminum through the junction and junction shorting. Pictured schematically in Fig. 14.11(a), the nonuniform penetration of Al into the Si is called *spiking*. A small percentage of Si is sometimes added to the deposited Al film to inhibit Si diffusion from the substrate and the resultant spiking.

Another consideration is the stability of the ohmic contact during subsequent processing. Aluminum is not an acceptable contact material in complex integrated circuits where additional processing at temperatures in excess of 500° C must be performed after contact formation. Rather, high temperature stability is achieved by employing the metal-like silicon compounds (silicides) formed with members of the refractory metal family (Mo, Ta, Ti, W). Titanium silicide, $TiSi_2$, is presently in widespread use as a contact material. A Ti film deposited over the Si contact area is converted to $TiSi_2$ by heating in an inert atmosphere. Since Si is consumed in the process, the silicide-silicon interface moves a short



(a)



(b)

Figure 14.11 (a) Visualization of spiking beneath an Al-Si contact. (b) Illustration of contact and interconnect metallization representative of that found in modern ICs.

distance into the Si, thereby eliminating surface defects and minimizing contamination. The net result is a clean, planar, temperature-stable, ohmic contact. Figure 14.11(b) illustrates the $TiSi_2$ contact and interconnect metallization representative of that found in modern ICs.

14.4 SUMMARY

The physical properties of an ideal MS contact were specified and the methodology was presented for constructing the energy band diagram characterizing a given metal-semiconductor system. Energy band diagrams corresponding to different combinations of the Φ_M and Φ_S workfunctions were employed to probe the basic nature of the contacts. Ideally, the combinations $\Phi_S(p\text{-type}) > \Phi_M > \Phi_S(n\text{-type})$ and $\Phi_S(p\text{-type}) < \Phi_M < \Phi_S(n\text{-type})$ were concluded to yield rectifying and ohmic contacts, respectively. Operation of the rectifying contact, called a Schottky diode or MS diode when utilized as a device, was next examined in greater detail. The device electrostatics and reverse-bias a.c. response of the MS diode were found to be all but identical to that of a comparably doped p^+-n or n^+-p junction diode. Differing from the pn junction diode, the thermionic emission current associated with majority carrier injection over the surface barrier was identified as the dominant d.c. current component. Because the diffusion current is typically small by compari-

son, the related minority carrier injection and storage are likewise small. As a consequence, the MS diode does not exhibit a significant diffusion admittance and switches between the on- and off-states at an extremely rapid rate. Although the basic description of device operation is unaffected, the Φ_B barrier height in actual Schottky diodes is seldom equal to the ideal device value. Moreover, the ohmic or rectifying nature of an MS contact may be different from that expected from ideal-contact considerations. An ohmic contact is usually produced in practice by heavily doping the surface region of the semiconductor immediately beneath the contact.

PROBLEMS

CHAPTER 14 PROBLEM INFORMATION TABLE

Problem	*Complete After*	*Difficulty Level*	*Suggested Point Weighting*	*Short Description*
14.1	14.4	1	10 (1 each part)	Quick quiz
14.2	14.1	2	10 (5 each part)/comb.	Draw/use band diagram
14.3	14.2.1	2	8 (2 each part)	Parameter computation
• 14.4	"	2	8	W versus N_D plot
• 14.5	"	4	30 (a-18, b-8, c-4)	Autodraw band diagram
14.6	14.2.2	2	8	Confirm Eq. (14.18)
14.7	"	2–3	15 (a-4, b-5, c-4, d-2)	MS photodiode
• 14.8	"	1	8	Effect of R_S on I–V
14.9	"	2	8	Injection ratio
• 14.10	"	3	15 (a-10, b-4, c-1)	Schottky barrier lowering
• 14.11	14.2.3	2	12	C–V data analysis
14.12	"	4	20 (a-12, b-6, c-2)	Linearly graded MS diode

14.1 Quick Quiz

(a) What are the differences between an MS diode, a Schottky diode, and a hot carrier diode?

(b) An ideal MS contact is formed between a metal and a semiconductor with $\Phi_M = \chi$. Under what conditions will the contact be ohmic-like, and under what conditions will the contact be rectifying?

(c) The solutions for the electrostatic variables ρ, $\mathscr{E}$, and V on the lightly doped side of a p^+-n or n^+-p junction diode and inside the semiconductor of a comparably doped MS diode are all but identical. Are there any significant differences in the electrostatic formulations?

(d) Name the dominant current component in MS diodes.

(e) Somehow the $I_{M\bullet\rightarrow S}$ component of the current in an MS(n-type) diode was determined without a detailed mathematical analysis of electron injection from the metal into the semiconductor. How was this accomplished?

(f) Explain why MS diodes do not exhibit a diffusion capacitance or diffusion conductance.

(g) Explain why MS diodes switch very rapidly from the forward-bias on-state to the reverse-bias off-state.

(h) What is a "Schottky diode clamp"?

(i) Describe the usual procedure followed in forming practical ohmic contacts.

(j) What is "spiking"?

14.2 A number of ideal MS contacts are formed on Ge, Si, and GaAs substrates maintained at room temperature. For one or more of the MS parameter combinations listed below,

(a) Draw the equilibrium energy band diagram characterizing the ideal MS contact.

(b) Present an argument similar to the one summarized in Fig. 14.3 to confirm the ohmic or rectifying nature of the contact.

combination A: $\Phi_M = 4.75$ eV, χ(Ge) = 4.00 eV, $N_D = 10^{16}/\text{cm}^3$.
combination B: $\Phi_M = 4.75$ eV, χ(Ge) = 4.00 eV, $N_A = 10^{15}/\text{cm}^3$.
combination C: $\Phi_M = 4.00$ eV, χ(Si) = 4.03 eV, $N_D = 10^{15}/\text{cm}^3$.
combination D: $\Phi_M = 4.25$ eV, χ(Si) = 4.03 eV, $N_A = 10^{16}/\text{cm}^3$.
combination E: $\Phi_M = 4.75$ eV, χ(GaAs) = 4.07 eV, $N_D = 10^{16}/\text{cm}^3$.
combination F: $\Phi_M = 4.75$ eV, χ(GaAs) = 4.07 eV, $N_A = 10^{17}/\text{cm}^3$.

14.3 An ideal rectifying contact is formed by depositing gold ($\Phi_M = 5.10$ eV) on an $N_D = 10^{15}/\text{cm}^3$ doped silicon substrate maintained at room temperature. Calculate

(a) Φ_B,

(b) V_{bi},

(c) W under equilibrium conditions,

(d) $|\mathscr{E}|_{max}$ in the semiconductor under equilibrium conditions.

• **14.4** Construct a plot of the equilibrium depletion width versus the N_D doping concentration in silicon MS diodes maintained at $T = 300$ K. Vary N_D over the range $10^{14}/\text{cm}^3 \leq N_D \leq 10^{17}/\text{cm}^3$ and include curves corresponding to $\Phi_B = 0.5$ eV, 0.6 eV, and 0.7 eV.

• **14.5** (a) Paralleling Exercise 5.4, construct a MATLAB (computer) program that draws the equilibrium energy band diagram for a nondegenerately N_D-doped silicon MS diode maintained at room temperature. Let Φ_B and the N_D doping of the semiconductor be input parameters. Be careful to exclude parameter combinations that would yield a nonrectifying contact.

(b) Generalize the part (a) program so that it also draws the equilibrium energy band diagram for N_A doped silicon diodes.

(c) Revise the (a)/(b) programs so they can be used to generate the equilibrium energy band diagrams for GaAs MS diodes.

14.6 Fill in the missing steps in the derivation of Eq. (14.18). Accepting Eqs. (14.16) and (14.17) to be accurate, perform and record the mathematical manipulations leading to Eq. (14.18).

14.7 MS Photodiode

An N_D-doped silicon MS diode is illuminated, thereby generating electron-hole pairs inside the semiconductor.

(a) If the diode terminals are taken to be *short-circuited,* draw the energy band diagram for the device and picture what happens to the photogenerated carriers created in the semiconductor near the MS interface. With the current and voltage polarities as specified in Fig. 14.3(a), what is the polarity of the short-circuit photocurrent?

(b) If the diode terminals are taken to be *open-circuited,* draw the energy band diagram characterizing the illuminated device. Remember the total current must be identically zero under open-circuit conditions. Explain how you arrived at the form of your diagram.

(c) Assume the light is uniformly absorbed throughout the semiconductor producing a photogeneration rate of G_L electron-hole pairs per cm^3-sec and giving rise to low-level injection. For an arbitrary applied bias, and following the simplified procedure outlined in Subsection 9.2.1, derive an expression for the photocurrent (I_L) flowing in the MS photodiode.

(d) Sketch the expected general form of the $I = I_{dark} + I_L$ versus V_A characteristic exhibited by an illuminated MS photodiode. Is your sketch consistent with the answers to parts (a) and (b)?

• **14.8** The quasineutral portion of the semiconductor and the ohmic back contact of Schottky diodes introduce a resistance R_S in series with the current flowing across the rectifying MS junction. Graphically illustrate the effect of the series resistance on the diode I–V characteristic. Taking $I_s = 10^{-8}$ A, construct a semilog plot of the forward-bias I–V characteristics when $R_S = 0$, 0.1 Ω, 1.0 Ω, and 10 Ω. Limit your plotted output to $0 \leq V_A \leq 0.6$ V and 10^{-9} A $\leq I \leq 10^{-1}$ A.

14.9 The *minority-carrier injection ratio* is often cited as a quantity of interest in characterizing MS diodes. By definition, it is the number of minority carriers injected into the semiconductor per majority carrier injected from the semiconductor into the metal when the device is forward biased. Mathematically, the ratio is just I_{DIFF}/I_{TE}. I_{DIFF} and I_{TE} are respectively the diffusion and thermionic emission currents flowing in the MS diode. Estimate the minority carrier injection ratio in a silicon MS diode where $\mathcal{A}^* = 140$ amps/cm^2-K^2, $\Phi_B = 0.72$ eV, $N_D = 10^{16}/cm^3$, $\tau_p = 10^{-6}$ sec, and $T = 300$ K. I_{DIFF} in the given diode may be equated to the I_{DIFF} flowing in a p^+-n step junction diode with equivalent device parameters.

• **14.10** In this problem we wish to examine the magnitude and effect of Schottky barrier lowering. Parameters will be employed similar to those of the MS diode yielding the Fig. 14.6 characteristics.

(a) Given a silicon MS diode with $N_D = 10^{16}/cm^3$ operating at room temperature, compute and plot $\Delta\Phi_B$ versus V_A for $-50\ V \leq V_A \leq 0$.

(b) Compute and plot $I_s(V_A)/I_s(V_A = 0)$ versus V_A for $-50\ V \leq V_A \leq 0$.

(c) Comment on your results.

• **14.11** A subset of the $1/C^2$ versus V_A data plotted in Fig. 14.8(b) is reproduced in Table P14.11. Analyze the data employing a least squares fit to determine V_{bi}, N_D, and Φ_B. Assume $A = 1.5 \times 10^{-3}\ cm^2$. Compare your results with the approximate values obtained in Exercise 14.4.

Table P14.11

$-V_A$ (volts)	$1/C^2(10^{21}/farad^2)$
1.09	0.953
2.08	1.494
3.07	2.035
4.06	2.579
5.05	3.125
6.04	3.673
7.03	4.217
8.02	4.763
9.01	5.320
10.00	5.890

14.12 The doping profile inside the semiconductor component of an MS diode is linearly graded; i.e., $N_D(x) = ax$.

(a) Derive solutions for ρ, $\mathscr{E}$, V, and W inside the semiconductor.

(b) Indicate how V_{bi} is to be determined and computed.

(c) Establish an expression for the junction (depletion region) capacitance.

R2 Part II
SUPPLEMENT AND REVIEW

ALTERNATIVE / SUPPLEMENTAL READING LIST

Author(s)	*Type (A–Alt., S–Supp.)*	*Level*	*Relevant Chapters*
General References			
Streetman	A	Undergraduate	5–7, 11
Neamen	A	Undergraduate	7–10
Tyagi	A/S	Advanced Undergrad Introductory Grad	6–10, 12–14, 18
For Selected Topics			
Navon	A	Undergraduate	12 (PNPN)
Sah	S	Undergraduate to Graduate (variable)	7 (BJT, HBT and PNPN)
Yang	A/S	Undergraduate	3 (*pn* electrostatics) 6 (BJT technology) 7 (MS diodes)

(1) D. H. Navon, *Semiconductor Microdevices and Materials,* Holt, Rinehart and Winston, New York, © 1986.

(2) D. A. Neamen, *Semiconductor Physics and Devices, Basic Principles,* Irwin, Homewood, IL, © 1992.

(3) C. T. Sah, *Fundamentals of Solid-State Electronics,* World Scientific, Singapore, © 1991.

(4) B. G. Streetman, *Solid State Electronic Devices,* 4th edition, Prentice Hall, Englewood Cliffs, NJ, © 1995.

(5) M. S. Tyagi, *Introduction to Semiconductor Materials and Devices,* John Wiley & Sons, New York, © 1991.

(6) E. S. Yang, *Microelectronic Devices,* McGraw Hill, New York, © 1988.

FIGURE SOURCES / CITED REFERENCES

(1) S. M. Sze, *Physics of Semiconductor Devices,* 2nd edition, John Wiley & Sons, New York, © 1981.

(2) C. T. Sah, R. H. Noyce, and W. Shockley, "Carrier Generation and Recombination in P-N Junctions and P-N Junction Characteristics," Proceedings IRE, **45,** 1228 (Sept. 1957).

(3) D. K. Schroder, *Semiconductor Material and Device Characterization,* John Wiley and Sons, New York, © 1990.

(4) R. H. Kingston, "Switching Times in Junction Diodes and Junction Transistors," Proceedings IRE, **42,** 829–834 (1954).

(5) R. H. Dean and C. J. Neuse, "A Refined Step-Recovery Technique for Measuring Minority Carrier Lifetimes and Related Parameters in Asymmetric *p-n* Junction Diodes," IEEE Transactions on Electron Devices, **ED-18,** 151–158 (March 1971).

(6) E. S. Yang, *Microelectronic Devices,* McGraw Hill, New York, © 1988; page 383.

(7) M. A. Green, A. W. Blakers, J. Zhao, A. M. Milne, A. Wang, and X. Dai, "Characterization of 23-Percent Efficient Silicon Solar Cells," IEEE Transactions on Electron Devices, **37,** 331–336 (Feb. 1990).

(8) Photovoltaics: Program Overview Fiscal Year 1992, report produced by the National Renewable Energy Laboratory, DOE/CH10093-190 DE93000055, March 1993.

(9) M. G. Craford, "LEDs Challenge the Incandescents," IEEE Circuits and Devices, **8,** 24–29 (Sept. 1992).

(10) M. G. Craford, "Recent Developments in Light-Emitting-Diode Technology," IEEE Transactions on Electron Devices, **ED-24,** 935–943 (July 1977).

(11) S. S. Ahmed et al., "A Triple Diffused Approach for High Performance 0.8 μm BiCMOS Technology," Solid State Technology, **35,** 33 (Oct. 1992). Also see the other articles in the special series on BiCMOS Processing, edited by D. Gupta and M. T. Bohr, started in Solid State Technology, June 1992.

(12) M. Lundstrom, "III-V Heterojunction Bipolar Transistors," Chapter 1 in *Heterojunction Transistors and Small Size Effects in Devices,* edited by M. Willander, Studentlitteratur and Chartwell Bratt, © 1992.

(13) I. R. C. Post, P. Ashburn, and G. R. Wolstenholme, "Polysilicon Emitters for Bipolar Transistors: A Review and Re-Evaluation of Theory and Experiment," IEEE Transactions on Electron Devices, **39,** 1717 (July 1992).

(14) For information about MBE, consult the device fabrication references listed in the R1 mini-chapter.

(15) S. Tiwari and D. J. Frank, "Empirical Fit to Band Discontinuities and Barrier Heights in III-V Alloy Systems," Applied Physics Letters, **60,** 630 (Feb. 3, 1992).

(16) D. H. Navon, *Semiconductor Microdevices and Materials,* Holt, Rinehart and Winston, New York, © 1986; pp. 410, 411.

(17) See, for example, S. M. Sze, *Physics of Semiconductor Devices,* 2nd edition, John Wiley and Sons, New York, © 1981; pp. 255, 256.

REVIEW LIST OF TERMS

Defining the following terms using your own words provides a rapid review of the Part II material.

(1) wide-base diode
(2) narrow-base diode
(3) ideal diode
(4) law of the junction
(5) quasineutral region
(6) breakdown
(7) impact ionization
(8) avalanching
(9) multiplication factor
(10) Zener process
(11) tunneling
(12) conductivity modulation
(13) punch-through (in narrow-base diode)
(14) high-level injection
(15) quasistatic
(16) hyperabrupt
(17) varactor
(18) abrupt
(19) profiling
(20) junction capacitance
(21) diffusion admittance
(22) turn-off transient
(23) storage delay time
(24) reverse recovery time
(25) reverse injection
(26) step recovery diode
(27) photodetector
(28) solar cell
(29) LED
(30) *p-i-n* diode
(31) avalanche photodiode
(32) fill factor
(33) shadowing (in solar cells)
(34) texturing (in solar cells)
(35) concentrator solar cells
(36) isoelectronic trap

(37) total internal reflection
(38) BJT
(39) emitter, base, collector
(40) common base
(41) common emitter
(42) active mode
(43) saturation mode
(44) cutoff mode
(45) inverted mode
(46) buried layer
(47) quasineutral base width
(48) emitter efficiency
(49) base transport factor
(50) common base d.c. gain
(51) common emitter d.c. gain
(52) performance parameters
(53) Ebers–Moll equations, model
(54) forward gain
(55) base-width modulation
(56) Early effect
(57) punch-through (in BJT)
(58) regenerative
(59) phototransistor
(60) intrinsic transistor
(61) base series resistance
(62) current crowding
(63) graded base (in BJT)
(64) Gummel plot
(65) BiCMOS
(66) shallow emitter
(67) polysilicon emitter
(68) HBT
(69) heterojunction
(70) band alignment
(71) lattice-matched
(72) graded junction (in HBT)
(73) Hybrid-Pi equivalent circuit
(74) transconductance
(75) base transit time
(76) rise, storage delay, and fall times
(77) Schottky diode clamp
(78) thyristors
(79) SCR
(80) anode, cathode, gate
(81) blocking voltages
(82) two-transistor model
(83) GTO SCR
(84) LAS
(85) *di/dt* burnout
(86) *dv/dt* effect
(87) DIAC, TRIAC
(88) PUT
(89) Schottky diode
(90) vacuum level
(91) metal workfunction
(92) electron affinity
(93) thermionic emission
(94) Richardson's constant
(95) Schottky barrier lowering
(96) hot carrier diode
(97) Fermi-level pinning
(98) field emission
(99) Al spiking
(100) silicide

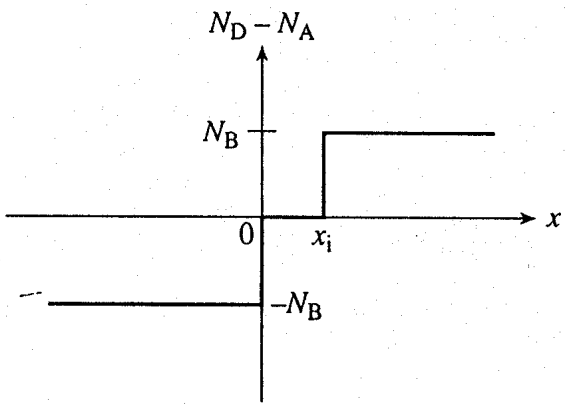
PART II—REVIEW PROBLEM SETS AND ANSWERS

The following problem sets were designed assuming a knowledge—at times an integrated knowledge—of the subject matter in Chapters 5–11 of Part II. The sets could serve as a review or as a means of evaluating the reader's mastery of the subject. Problem Set A is adapted from a one-hour "open-book" examination; Problem Sets B and C are combinations of select problems from "closed-book" examinations. The answers to Problem Sets A and B are included at the end of this section. Answers are not provided for Problem Set C so that it can be used as a homework set with integrated-knowledge-type questions on the *pn* junction diode.

Problem Set A

Problem A1

A *pn* junction has the doping profile sketched below. Throughout this problem, assume the carrier concentrations may be neglected ($n = 0$, $p = 0$) in the $0 \leq x \leq x_i$ region of the diode.



(a) What is the built-in voltage across the junction? Justify your answer.

(b) Invoking the depletion approximation, make a sketch of the charge density inside the diode. Label significant ρ and x values.

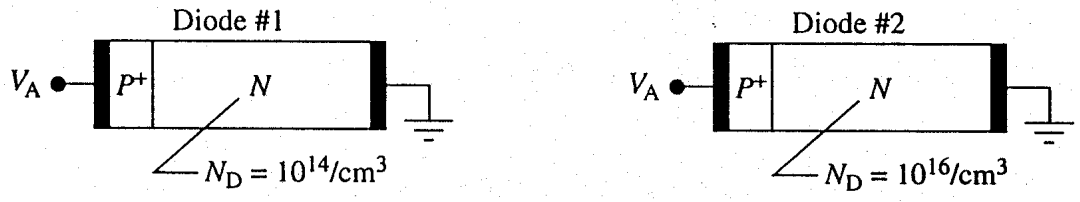
(c) Obtain an analytical solution for the electric field, $\mathscr{E}(x)$, at all points inside the depletion region ($-x_p \leq x \leq x_n$). Show all work and make a sketch of the deduced $\mathscr{E}(x)$ versus x.

(d) In a standard *pn* step junction $N_A x_p = N_D x_n$. How are x_n and x_p related here?

(e) Draw the energy band diagram for the diode under equilibrium conditions. Clearly identify the points $x = 0$ and $x = x_i$ on your diagram. Also indicate how your diagram differs from that of a simple *pn* step junction where $N_A = N_D = N_B$.

Problem A2

Two silicon p^+-n step junction diodes maintained at 300 K are physically identical except for the n-side doping. In diode #1, $N_D = 10^{14}/\text{cm}^3$; in diode #2, $N_D = 10^{16}/\text{cm}^3$. Compare the operation of the two diodes by answering the questions that follow.



(a) Which diode will exhibit the larger built-in voltage (V_{bi})? Explain.

(b) Which diode will exhibit the larger breakdown voltage (V_{BR})? Explain.

(c) Which diode will exhibit the larger junction capacitance (C_J) at a given reverse bias voltage when $|V_A| \gg V_{bi}$? Explain.

(d) If the diodes are assumed to be ideal and reverse biased at a $|V_A| >$ few volts, which diode will support the larger $|I|$? Explain.

(e) If the diodes are *not* assumed to be ideal, which diode will support the larger $|I|$ when reverse biased at a $|V_A| >$ few volts? Explain.

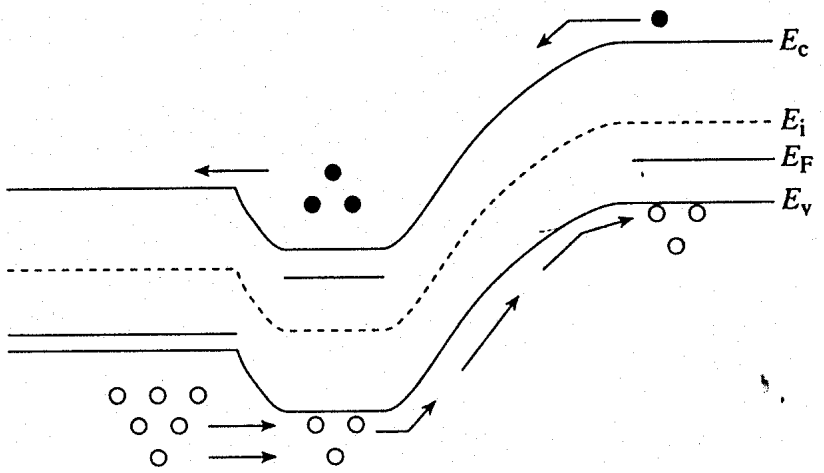
(f) Which diode will exhibit the larger diffusion capacitance (C_D) at a given applied forward bias and frequency? Assume operation in the forward bias "ideal" region. Explain.

(g) Which diode will exhibit the larger storage delay time (t_s) under transient conditions if the I_F/I_R ratio is the same? Explain.

Problem A3

(a) The diagram below pictures the major carrier activity in a *pnp* BJT under active mode biasing. Construct a similar diagram picturing the major carrier activity in the *same pnp* BJT under *inverted* mode biasing. (Include a few words of explanation as necessary to forestall a misinterpretation of your diagram.)

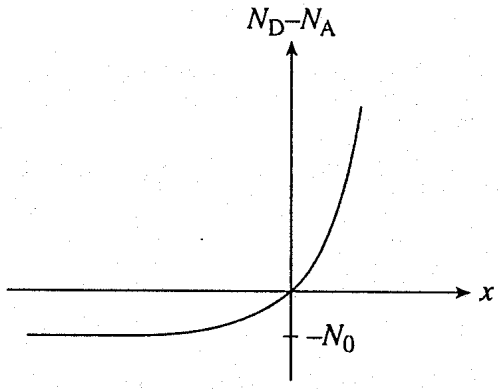
(b) The pictured BJT is accidentally connected up backward so that the collector functions as the emitter and the emitter functions as the collector. In the backward connection with $V_{CB} > 0$ and $V_{EB} < 0$ the device exhibits a lower gain and is more sensitive to base-width modulation. (i) Explain why the backward connection leads to a lower gain. (ii) Explain why the backward connection leads to a greater sensitivity to base-width modulation.



Problem Set B

Problem B1

A *pn* junction diode has the doping profile shown in the following sketch. Mathematically, $N_D - N_A = N_0 [\exp(\alpha x) - 1]$, where N_0 and α are constants.



(a) Give a concise statement of the depletion approximation.

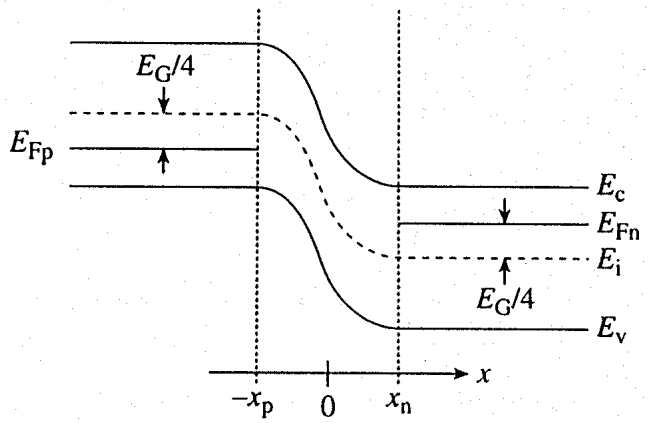
(b) Invoking the depletion approximation, make a sketch of the charge density inside the diode.

(c) Establish an expression for the electric field, $\mathscr{E}(x)$, inside the depletion region.

(d) *Indicate* how you would complete the electrostatic development to eventually obtain an expression for the depletion width, W. Be as specific as possible about the equations to be solved and the boundary conditions to be employed. Don't waste time actually performing the mathematical manipulations. Organize your answer into steps—step 1, step 2, etc.

Problem B2

The energy band diagram given below characterizes a Si step junction diode maintained at room temperature. Note that $E_v(-\infty) = E_c(+\infty)$. Also, $x_n + x_p = 2 \times 10^{-4}$ cm, $A = 10^{-3}$ cm^2, $\tau_n = \tau_p = \tau_0 = 10^{-6}$ sec, $\mu_n(p\text{-side}) = 1352$ cm^2/V-sec, $\mu_p(n\text{-side}) = 459$ cm^2/V-sec, $K_S = 11.8$, and $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm.



(a) What is the magnitude of the reverse-bias voltage (V_A) being applied to the diode? Explain how you arrived at your answer.

(b) Determine V_{bi}, the built-in voltage.

(c) Compute the recombination–generation current flowing through the diode at the pictured bias point.

(d) Compute the diffusion current flowing through the diode at the pictured bias point.

R

(e) What will be the junction capacitance (C_J) exhibited by the diode at the pictured bias point?

(f) On a linear scale, sketch the minority carrier concentrations versus position for the $x \leq -x_p$ and $x \geq x_n$ portions of the diode.

(g) Would you expect the device to exhibit a significant diffusion capacitance (C_D) at the applied bias point? Explain.

(h) If the diode were pulsed from the pictured bias point to a larger reverse bias at $t = 0$, would you expect to observe a current transient characterized by a storage delay time t_s? Explain.

Problem B3

Two Si *pnp* transistors, BJT #1 and BJT #2, are identical except $W_{B1} > W_{B2}$. $N_E \gg N_B > N_C$ and $W \ll L_B$ in both transistors. Under the same active mode biasing conditions, which transistor will exhibit

(a) the larger emitter efficiency? Explain

(b) the larger base transport factor? Explain.

(c) the larger β_{dc}? Explain.

(d) the greater sensitivity to base-width modulation? Explain.

(e) the larger punch-through voltage? Explain.

If the maximum output current is assumed to be limited by carrier multiplication and avalanching, which transistor will exhibit

(f) the larger V_{CB0}? Explain.

(g) the larger V_{CE0}? Explain.

Problem Set C

Problem C1

(a). Which of the following assumptions is *not* invoked in deriving the ideal diode equation?

(i) No recombination–generation in the depletion region.
(ii) Low-level injection.
(iii) Narrow-base diode; i.e., the n and p quasineutral widths are much less than the respective minority carrier diffusion lengths.
(iv) No "other" process; i.e., no photogeneration, avalanching, tunneling, etc.

(b) Under reverse biasing and small forward biasing, the dominant current component in most Si *pn* junction diodes maintained at room temperature is which of the following?

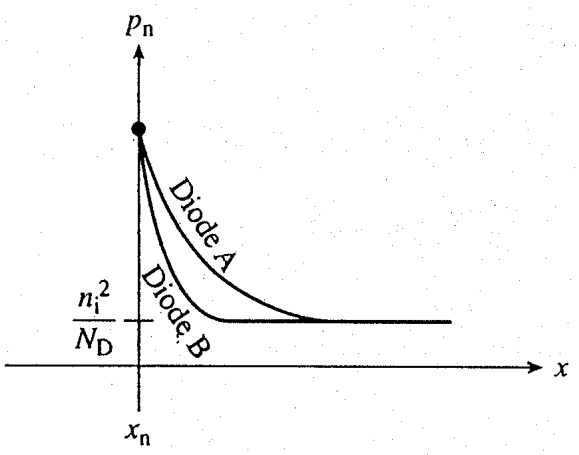
(i) The diffusion current.
(ii) The R–G current.
(iii) The ideal-diode current.
(iv) The drift current.

(c) Which of the following statements is *incorrect?*
  (i) *pn* junction breakdown is a reversible process.
  (ii) For the Zener process to occur in a *pn* junction diode, the depletion width must be very narrow ($\leq 10^{-6}$ cm).
  (iii) The avalanche breakdown voltage varies roughly as the inverse of the doping concentration on the lightly doped side of p^+-n and n^+-p junctions.
  (iv) In Si diodes maintained at room temperature, avalanching is the dominant process causing breakdown if $V_{BR} \lesssim 4.5$ V.

(d) Which of the following statements about the junction capacitance (C_J) is *correct?*
  (i) C_J always varies as $1/\sqrt{V_{bi} - V_A}$.
  (ii) The minimum observable C_J will occur at V_{BR}.
  (iii) C_J vanishes under forward biasing.
  (iv) C_J is associated physically with fluctuations in the minority carrier concentrations at the edges of the depletion region.

Problem C2

Minority carrier concentration versus position plots and sketches are often used to describe the situation inside semiconductor devices. A linear plot of the minority carrier concentration on the n-side of two *ideal* p^+-n *diodes* maintained at room temperature is pictured below. The n-side doping (N_D) and the cross-sectional area (A) are the same in both diodes. Assume low-level injection conditions prevail.



(a) The diodes are [(i) forward biased, (ii) zero biased, (iii) reverse biased].

(b) The magnitude of the bias applied to Diode B is [(i) larger than, (ii) the same as, (iii) smaller than] the magnitude of the bias applied to Diode A.

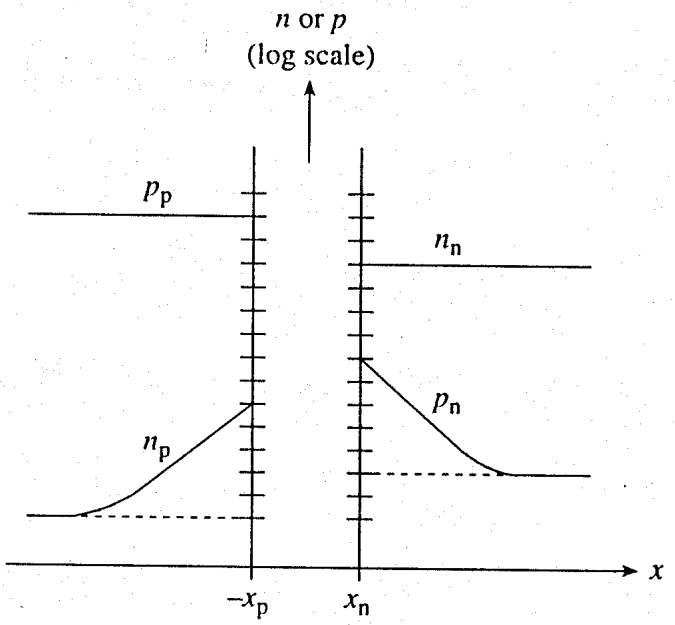
(c) The magnitude of the d.c. current, $|I|$, flowing through Diode B is [(i) significantly larger than, (ii) roughly the same as, (iii) significantly smaller than] the magnitude of the d.c. current flowing through Diode A.

(d) The breakdown voltage (V_{BR}) of Diode B is [(i) significantly larger than, (ii) roughly the same as, (iii) significantly less than] the breakdown voltage of Diode A.

(e) Diodes A and B are tested in the same switching circuit. I_F/I_R is the same for both diodes. Which diode will exhibit the larger storage delay time (larger t_s)? [(i) Diode A; (ii) Diode B; (iii) t_s will be essentially the same for both diodes.]

Problem C3

The steady-state carrier concentrations inside a *pn* junction diode maintained at room temperature are as pictured below.



(a) Is the diode forward or reverse biased? Explain how you arrived at your answer.

(b) Do low-level injection conditions prevail inside the diode? Explain how you arrived at your answer.

(c) *Qualitatively,* what is the physical relationship between the pile-up or store of minority carriers near the depletion region edges and the diffusion capacitance (C_D)?

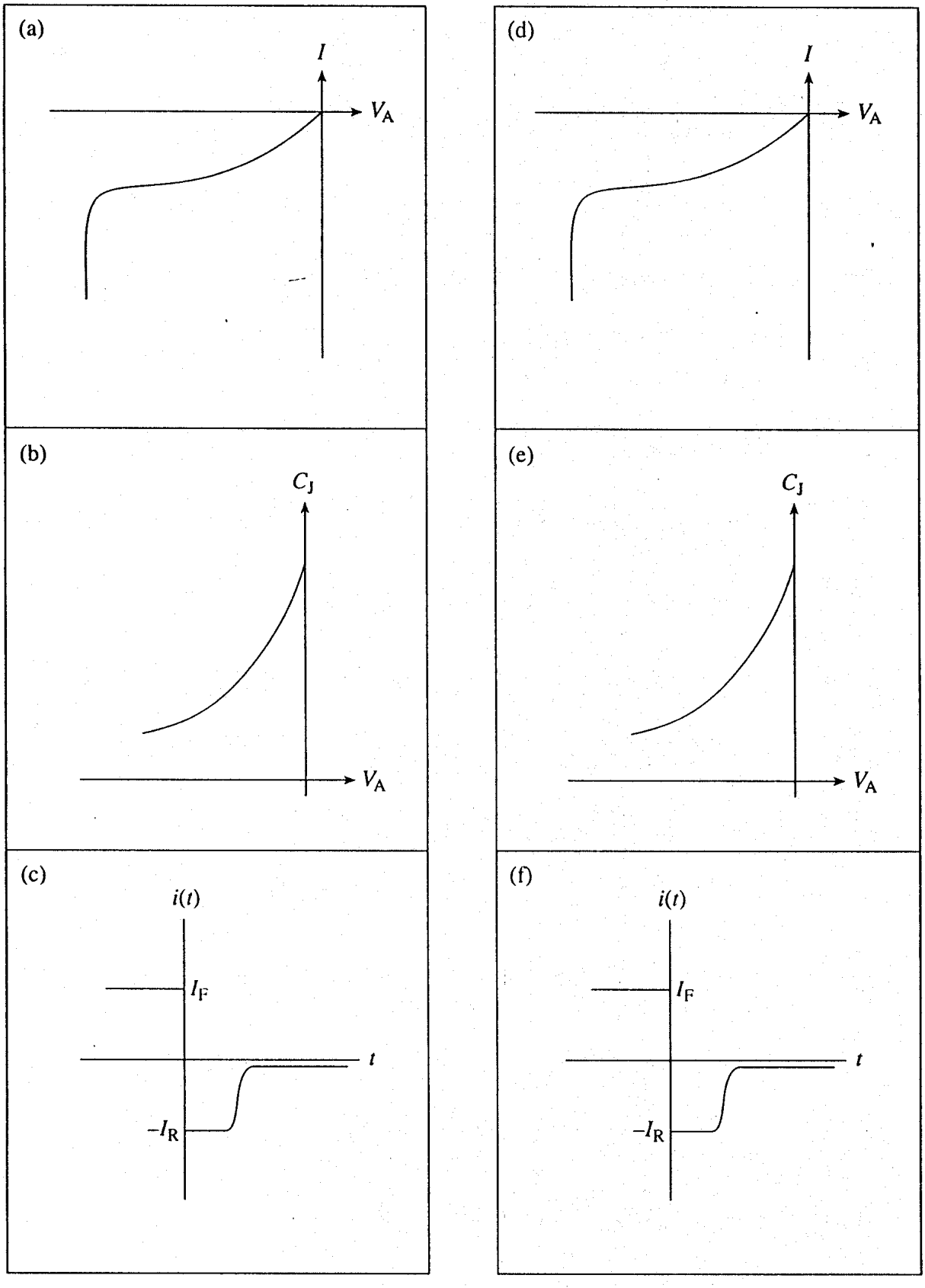
(d) *Qualitatively,* what is the physical relationship between the pile-up or store of minority carriers near the depletion region edges and the storage delay time (t_s) observed during the turn-off transient?

Problem C4

The reverse-bias current–voltage (I–V_A), junction capacitance (C_J–V_A), and turn-off transient (i–t) characteristics derived from a p^+-n Si step junction diode maintained at room temperature are sketched to the right. After reproducing the figures, answer the following questions by adding a *dashed line* to the appropriate characteristic. Note that an answer of *no effect* (a dashed line the same as the given characteristic) is possible. In such cases write *no effect.*

(a–c) *Roughly* indicate how the I–V_A, C_J–V_A, and i–t characteristics are modified if the n-side doping (N_D) is *increased* by a factor of 2. All other parameters remain the same.

(d–f) *Roughly* indicate how the I–V_A, C_J–V_A, and i–t characteristics are modified if the minority carrier lifetime on the n-side (τ_p) and the effective depletion-region generation lifetime (τ_0) are *increased* by a factor of 2. All other parameters remain the same.



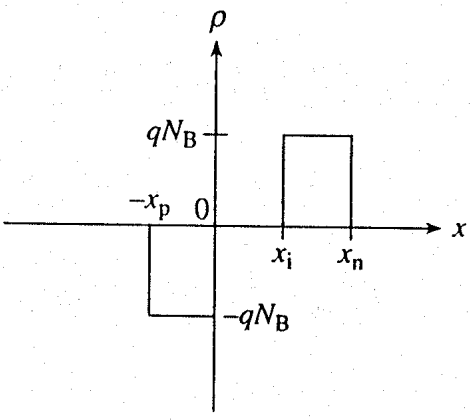
Answers—Set A

Problem A1

(a) Paralleling the derivation in Subsection 5.1.4, one can write $V_{bi} = (kT/q)\ln[n(x_n)/n(-x_p)]$. Here $n(x_n) = n(\infty) = N_B$ and $n(-x_p) = n(-\infty) = n_i^2/N_B$. Thus

$$\boxed{V_{bi} = \frac{kT}{q}\ln\left(\frac{N_B^2}{n_i^2}\right) = \frac{2kT}{q}\ln\left(\frac{N_B}{n_i}\right)}$$

(b)



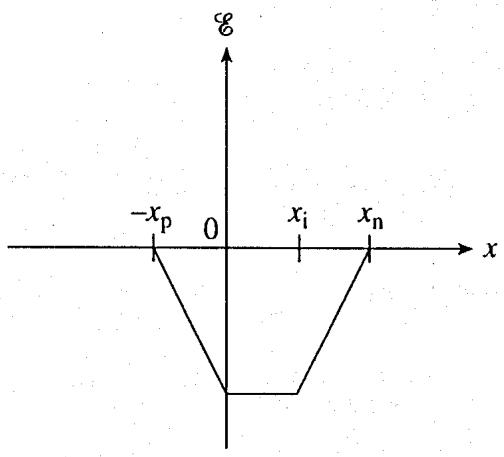
(c)

$$\frac{d\mathscr{E}}{dx} = \frac{\rho}{K_S\varepsilon_0} \cong \begin{cases} \dfrac{-qN_B}{K_S\varepsilon_0} & \ldots -x_p \le x \le 0 \\ 0 & \ldots 0 \le x \le x_i \\ \dfrac{qN_B}{K_S\varepsilon_0} & \ldots x_i \le x \le x_n \end{cases}$$

$$\int_0^{\mathscr{E}(x)} d\mathscr{E}' = -\int_{-x_p}^{x} \frac{qN_B}{K_S\varepsilon_0}\,dx' \Rightarrow \mathscr{E}(x) = -\frac{qN_B}{K_S\varepsilon_0}(x + x_p) \qquad \ldots -x_p \le x \le 0$$

$$\mathscr{E}(x) = \text{constant} = \mathscr{E}(0) = -\frac{qN_B}{K_S\varepsilon_0}x_p \qquad \ldots 0 \le x \le x_i$$

$$\int_{\mathscr{E}(x)}^{\mathscr{E}(x_n)=0} d\mathscr{E}' = \int_x^{x_n} \frac{qN_B}{K_S\varepsilon_0}\,dx' \Rightarrow \mathscr{E}(x) = -\frac{qN_B}{K_S\varepsilon_0}(x_n - x) \qquad \ldots x_i \le x \le x_n$$



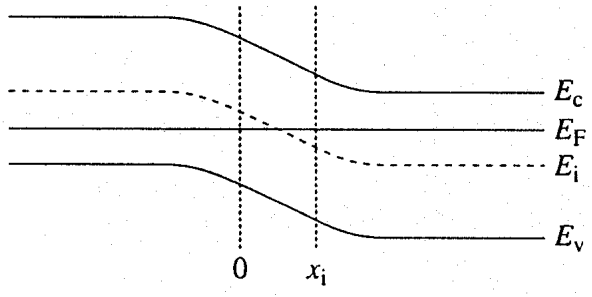
(d) The (+) and (−) charge areas on the part (b) ρ-plot must be equal, or

$$(-qN_B)(-x_p) = qN_B(x_n - x_i) \quad \Rightarrow \quad \boxed{x_p = x_n - x_i}$$

Alternatively, the $\mathscr{E}$-field must be continuous at $x = x_i$, giving

$$-\frac{qN_B}{K_S\varepsilon_0}x_p = -\frac{qN_B}{K_S\varepsilon_0}(x_n - x_i) \quad \Rightarrow \quad x_p = x_n - x_i$$

(e)



A constant energy band slope or straight lines in the $0 \leq x \leq x_i$ region is the only difference. Note that $(E_i - E_F)|_{p\text{-side}} = (E_F - E_i)|_{n\text{-side}}$ since $N_A = N_D = N_B$.

Problem A2

(a) Diode #2

$V_{bi} = (1/q)\,[(E_i - E_F)|_{p\text{-side}} + (E_F - E_i)|_{n\text{-side}}]$. $(E_i - E_F)|_{p\text{-side}}$ is the same for both diodes. $(E_F - E_i)|_{n\text{-side}} = kT\ln(N_D/n_i)$ is larger for the heavier doped diode. Thus $V_{bi2} > V_{bi1}$. Note that p^+ implies degenerate or very heavy doping. Thus the standard relationship, $V_{bi} = (kT/q)\ln(N_A N_D/n_i^2)$ cannot be used to compute V_{bi}.

(b) Diode #1

V_{BR} is roughly proportional to $1/N_D$ in a p^+-n diode. Also, Fig. 6.11 shows $V_{BR} > 1000$ V if $N_D = 10^{14}/\text{cm}^3$, while $V_{BR} \cong 60$ V if $N_D = 10^{16}/\text{cm}^3$.

(c) Diode #2

$$C_J = \frac{K_S \varepsilon_0 A}{W}$$

For a p^+-n step junction

$$W = \left[\frac{2K_S\varepsilon_0}{qN_D}(V_{bi} - V_A)\right]^{1/2} \cong \left[\frac{2K_S\varepsilon_0}{qN_D}(-V_A)\right]^{1/2}$$

where the latter form of the W equation follows from the fact that $|V_A| \gg V_{bi}$. Thus, $W_1 > W_2$ and $C_{J2} > C_{J1}$.

(d) Diode #1

For an ideal p^+-n diode reverse biased to $|V_A| >$ few volts, we can write

$$I \cong -I_0 \cong -qA\frac{D_P}{L_P}\frac{n_i^2}{N_D}$$

Now $1/N_{D1} > 1/N_{D2}$. Also

$$\frac{D_P}{L_P} = \frac{D_P}{\sqrt{D_P\tau_p}} = \sqrt{\frac{D_P}{\tau_p}} = \sqrt{\frac{kT}{q}\frac{\mu_p}{\tau_p}}$$

Since μ_p decreases with increasing N_D, $D_{P1}/L_{P1} > D_{P2}/L_{P2}$. Both of the cited factors in the I expression are such as to make $I_{01} > I_{02}$.

(e) Diode #1

In a real Si diode maintained at 300 K the reverse current is typically dominated by the recombination–generation current component.

$$I_{R\text{-}G} = -qA\frac{n_i}{2\tau_0}W \qquad \ldots \text{ given } -V_A > \text{few volts}$$

From the Eq. (6.44) definition of τ_0 we infer $\tau_0 \propto 1/N_T$ (both τ_n and τ_p are proportional to $1/N_T$). Only the doping is specified as being different in the two diodes, not N_T. Thus τ_0 is the same for both diodes. However, $W_1 > W_2$ from part (c). Consequently, $|I_{R\text{-}G1}| > |I_{R\text{-}G2}|$.

(f) Diode #1

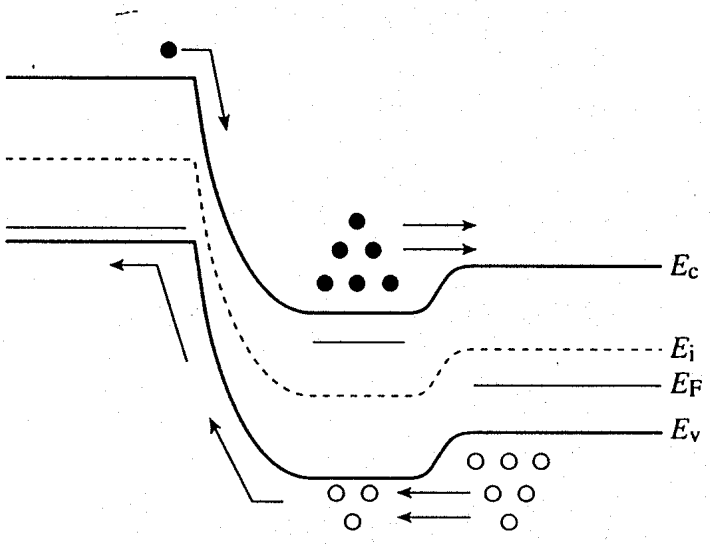
Assuming the diodes are forward biased into the ideal region of operation, $C_D \propto G_0 \propto (I + I_0) \propto I_0$. G_0 is the diode low-frequency conductance. However, $I_{01} > I_{02}$ from part (d). Thus $C_{D1} > C_{D2}$.

(g) Same for both diodes

Examining either the approximate solution [Eq. (8.8)] or the more accurate solution [Eq. (8.9)] for t_s, one concludes $t_{s1} = t_{s2}$ if the I_F/I_R ratio and $\tau_p \propto 1/N_T$ are the same for the two diodes. The I_F/I_R ratio is noted to be the same in the problem statement. N_T and therefore τ_p are also inferred to be the same in the two diodes, since only the N_D doping is specified as being different.

Problem A3

(a)



(b) (i) The efficiency of the injecting collector is far below that of the emitter and $\alpha_{dc} = \gamma a_T$ is thereby degraded. The E–B junction has $N_E \gg N_B$, making hole injection into the base much greater than electron injection from the base into the emitter under active mode biasing. On the other hand, $N_C < N_B$, giving rise to significant electron injection from the base into the collector under "backward" (inverted) operation.

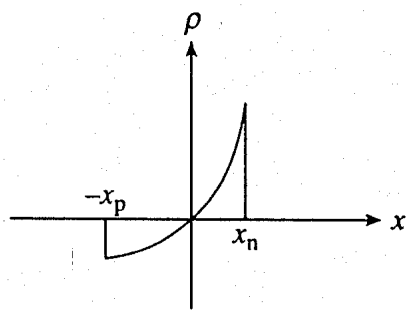
(ii) When used as an amplifier, the larger depletion region is associated with the reverse-biased junction. With the C–B junction reverse biased under active mode operation, most of the depletion region extends into the collector because $N_B > N_C$. However, when the E–B junction is reverse biased, as is the case under "backward" operation, most of the E–B depletion region extends into the *base* because $N_E \gg N_B$. Much larger variations of W for equivalent biasing conditions are expected under backward operation.

Answers—Set B

Problem B1

(a) In the depletion approximation one makes the following simplifying assumptions: (i) p and n are much less than $|N_D - N_A|$ in a $-x_p \leq x \leq x_n$ region about the metallurgical junction. (ii) $\rho = 0$ elsewhere.

(b)



(c) $$\frac{d\mathscr{E}}{dx} = \frac{\rho}{K_S \varepsilon_0} \cong \frac{qN_0}{K_S \varepsilon_0}(e^{\alpha x} - 1) \qquad \ldots -x_p \leq x \leq x_n$$

$$\int_0^{\mathscr{E}(x)} d\mathscr{E}' = \frac{qN_0}{K_S \varepsilon_0} \int_{-x_p}^{x} (e^{\alpha x'} - 1)\, dx' = \frac{qN_0}{K_S \varepsilon_0} [e^{\alpha x'}/\alpha - x']\Big|_{-x_p}^{x}$$

$$\boxed{\mathscr{E}(x) = \frac{qN_0}{K_S \varepsilon_0}\left[\frac{1}{\alpha}(e^{\alpha x} - e^{-\alpha x_p}) - (x + x_p)\right]}$$

(d) Step 1: Solve for $V(x)$ in the $-x_p \leq x \leq x_n$ depletion region.

$$\frac{dV}{dx} = -\mathscr{E}(x); \qquad V = 0 \text{ at } x = -x_p$$

Step 2: Two equations with x_n, x_p, and V_{bi} as unknowns are obtained by imposing the boundary conditions, $\mathscr{E}(x_n) = 0$ and $V(x_n) = V_{bi} - V_A$. Once V_{bi} is known, these two equations can be solved for the x_n, x_p, and $W = x_n + x_p$ resulting from a given V_A. In this particular problem, the solution will have to be obtained numerically.

Step 3: V_{bi} is obtained by a procedure paralleling the linearly graded analysis in Subsection 5.2.5.

Problem B2

(a) $$V_A = -\frac{1}{q}(E_{Fp} - E_{Fn}) = -\frac{E_G}{2q} = \mathbf{-0.56\ V}$$

(b) $V_{bi} = \frac{1}{q}[(E_i - E_F)|_{p\text{-side}} + (E_F - E_i)|_{n\text{-side}}] = \frac{E_G}{2q} = \mathbf{0.56\ V}$

(c) $I_{R\text{-}G} = -qA\frac{n_i}{2\tau_0}W = -(1.6 \times 10^{-19})(10^{-3})\left(\frac{10^{10}}{2 \times 10^{-6}}\right)(2 \times 10^{-4})$

$= \mathbf{-1.6 \times 10^{-10}\ A}$

(d) $D_N = \frac{kT}{q}\mu_n = (0.0259)(1352) = 35.02\ \text{cm}^2/\text{sec}$

$L_N = \sqrt{D_N\tau_n} = [(35.02)(10^{-6})]^{1/2} = 5.92 \times 10^{-3}\ \text{cm}$

$D_P = \frac{kT}{q}\mu_p = (0.0259)(459) = 11.89\ \text{cm}^2/\text{sec}$

$L_P = \sqrt{D_P\tau_p} = [(11.89)(10^{-6})]^{1/2} = 3.45 \times 10^{-3}\ \text{cm}$

$N_A = N_D = n_i e^{E_G/4kT} = (10^{10})(e^{1.12/[4(0.0259)]}) = 4.96 \times 10^{14}/\text{cm}^3$

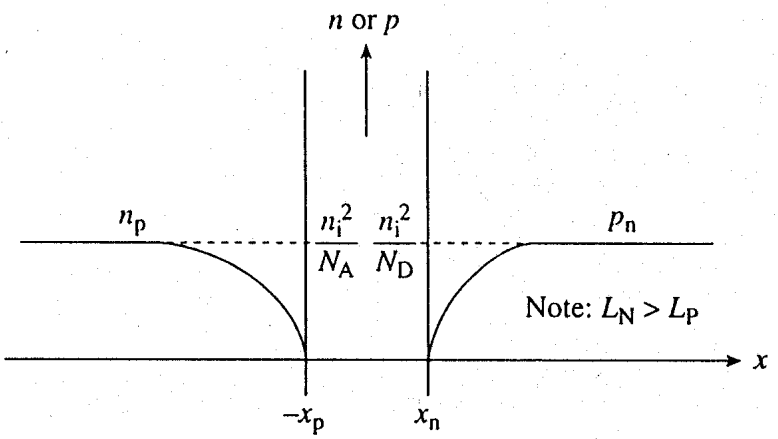
$$I_{Diff} \cong -I_0 = -qA\left(\frac{D_N}{L_N}\frac{n_i^2}{N_A} + \frac{D_P}{L_P}\frac{n_i^2}{N_D}\right)$$

$$= -(1.6 \times 10^{-19})(10^{-3})\left[\left(\frac{35.02}{5.92 \times 10^{-3}}\right)\left(\frac{10^{20}}{4.96 \times 10^{14}}\right) + \left(\frac{11.89}{3.45 \times 10^{-3}}\right)\left(\frac{10^{20}}{4.96 \times 10^{14}}\right)\right]$$

$= \mathbf{-3.02 \times 10^{-13}\ A}$

(e) $C_J = \frac{K_S\varepsilon_0 A}{W} = \frac{K_S\varepsilon_0 A}{x_n + x_p} = \frac{(11.8)(8.85 \times 10^{-14})(10^{-3})}{2 \times 10^{-4}} = \mathbf{5.22\ pF}$

(f)



(g) No. There is no store of minority carriers adjacent to the depletion region.

(h) No. Again, there is no store of minority carriers adjacent to the depletion region. (The device is already reverse biased prior to applying the voltage pulse.)

Problem B3

(a) BJT #2 If $W_{B1} > W_{B2}$, then $W_1 > W_2$ under the same biasing conditions and

$$\gamma_1 = \frac{1}{1 + \dfrac{D_E}{D_B}\dfrac{N_B}{N_E}\dfrac{W_1}{L_E}} < \gamma_2 = \frac{1}{1 + \dfrac{D_E}{D_B}\dfrac{N_B}{N_E}\dfrac{W_2}{L_E}}$$

(b) BJT #2

$$\alpha_{T1} = \frac{1}{1 + \dfrac{1}{2}\left(\dfrac{W_1}{L_B}\right)^2} < \alpha_{T2} = \frac{1}{1 + \dfrac{1}{2}\left(\dfrac{W_2}{L_B}\right)^2}$$

Physically, fewer carriers are lost via recombination in crossing the narrower base.

(c) BJT #2 With $\gamma_1 < \gamma_2$ and $\alpha_{T1} < \alpha_{T2}$, $\alpha_{dc1} < \alpha_{dc2}$ since $\alpha_{dc} = \gamma\alpha_T$. Noting that $\beta_{dc} = \alpha_{dc}/(1 - \alpha_{dc})$, we conclude $\beta_{dc2} > \beta_{dc1}$.

(d) BJT #2 Changes in bias give rise to the same ΔW in the two transistors. However, with $W_1 > W_2$, $\Delta W/W_2 > \Delta W/W_1$, making BJT #2 more sensitive to base width modulation.

(e) BJT #1 Because $W_{B1} > W_{B2}$ and changes in bias give rise to the same ΔW, it will clearly take a larger applied V_{CB} to completely deplete the wider BJT #1 base under active mode biasing.

(f) Same for #1 and #2 V_{CB0} is equal to the V_{BR} of the C–B junction. The avalanche breakdown voltage of the C–B junction should be the same for both transistors since the junction dopings are the same.

(g) BJT #1 According to Eq. (11.54), $V_{CE0} = V_{CB0}/(\beta_{dc} + 1)^{1/m}$, where $3 \leq m \leq 6$. Now, as noted in answering part (c), $\beta_{dc1} < \beta_{dc2}$. Thus, $V_{CE01} > V_{CE02}$.