Chapter

10

Models for Digital Design

In this chapter we develop a digital model for the MOSFET. For a simple logical analysis of a digital circuit we think, Fig. 10.1, of the MOSFETs as simple switches. When the gate of an NMOS device is a logic 1 (*VDD*), the NMOS device is on. When the gate is a logic 0 (ground), the NMOS device is off. The PMOS device operates in a complementary way to the NMOS device. When its gate is a logic zero, it is on (hence why we draw a bubble at its gate). It's important, for a quick logical analysis of a complex digital circuit, to think of the MOSFETs as simple logic-controlled switches.

Figure 10.1 Logical operation of the switches.

Miller Capacitance

One of the important concepts we'll use in this chapter has to do with the "Miller effect" discussed in detail in Ch. 21 (see Fig. 21.5 and the associated discussion). To understand this effect here in our development of digital models, consider the simple schematic in Fig. 10.2. If, initially, the input node is at 0 V and the output node is at *VDD*, the charge on the capacitor is

$$Q_{init} = C \cdot (0 - VDD) = -C \cdot VDD \tag{10.1}$$

If the input node changes to *VDD* and the output node transitions to ground, the charge on the capacitor is

$$Q_{final} = C \cdot (VDD - 0) = C \cdot VDD \tag{10.2}$$

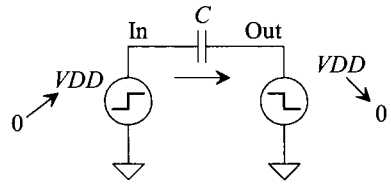


Figure 10.2 Determining the charge through a capacitor.

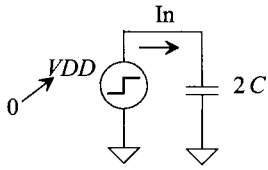
The total charge supplied by the input or output voltage source to the capacitor after the transition is then

$$Q_{tot} = Q_{final} - Q_{init} = 2C \cdot VDD \tag{10.3}$$

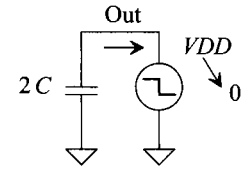
Remembering, in this discussion, that the input source transitions from 0 to *VDD* while, at the same time, the output source transitions from *VDD* to 0, what is the effective capacitance that each source sees? Towards answering this question, consider the models seen in Fig. 10.3. In (a) the input source supplies a charge of

$$Q_{tot} = 2C \cdot VDD \tag{10.4}$$

In (b) the output sinks the same amount of charge. The point here is that the input or output capacitance of the circuits in 10.3a or b is twice the capacitance value connecting the input to the output in Fig. 10.2. We'll use this result in a moment as we develop a digital model for the MOSFET.



(a) Input circuit



(b) Output circuit

Figure 10.3 Splitting the capacitor in Fig. 10.2 up into two equivalent capacitors for developing a model.

10.1 The Digital MOSFET Model

Effective Switching Resistance

Consider the MOSFET circuit shown in Fig. 10.4. Initially, the MOSFET is off, $V_{GS} = 0$, and the drain of the MOSFET is at *VDD*. If the gate of the MOSFET is taken instantaneously from 0 to *VDD*, a current given by

$$I_D = \frac{KP_n}{2} \cdot \frac{W}{L} \cdot (VDD - V_{THN})^2 = \frac{\beta}{2} \cdot (VDD - V_{THN})^2 \tag{10.5}$$

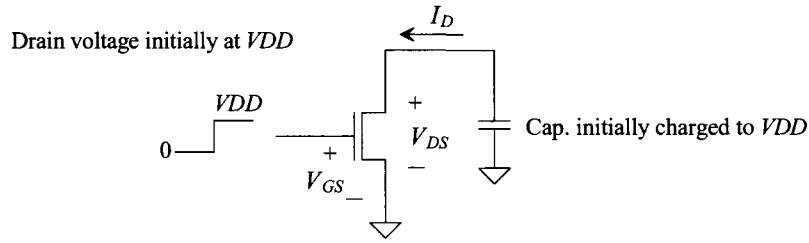


Figure 10.4 MOSFET switching circuit.

initially flows through the MOSFET. Point A in Fig. 10.5 shows the operating point of the MOSFET prior to switching for VDD = 5 V. After switching takes place, the operating point moves to point B and follows the curve $V_{GS} = VDD$ down to $I_D \approx 0$ and $V_{DS} = 0$, point C. At this point, the NMOS switch is on.

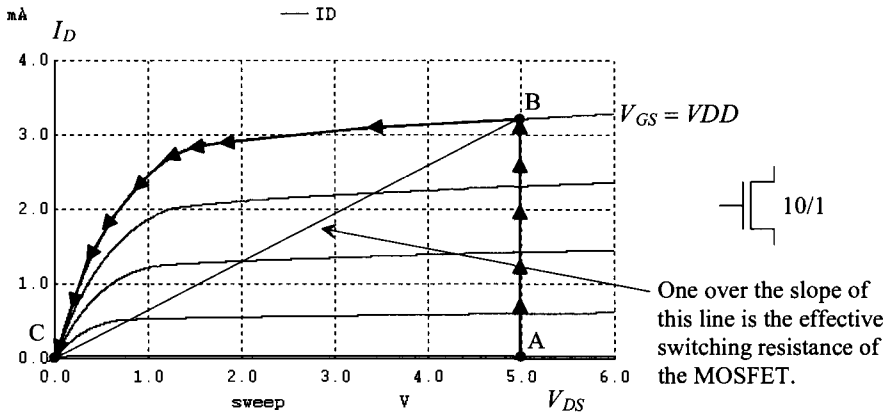


Figure 10.5 IV plot for a 10/1 NMOS device to estimate average switching resistance.

An estimate for the resistance between the drain and source of the MOSFET is given by the reciprocal slope of the line BC in Fig. 10.5, or

$$R_n = \frac{VDD}{\frac{KP_n}{2}\frac{W}{L} \cdot (VDD - V_{THN})^2} = R_n' \cdot \frac{L}{W} \qquad (10.6)$$

The MOSFET is modeled by the circuit shown in Fig. 10.6. When $V_{GS} > VDD/2$, the switch is closed; when $V_{GS} < VDD/2$ the switch is open. In the derivation of this model, we assumed that the input step transition occurred in zero time; that is, that the rise time was zero, so that the point at which the switch was opened or closed was well defined. In practice, we will not encounter a zero rise time pulse; therefore, the model has limitations. Nevertheless, the model works remarkably well in designing and analyzing digital circuits by hand, giving results that are usually within a factor of two of simulation or measurement in general applications.

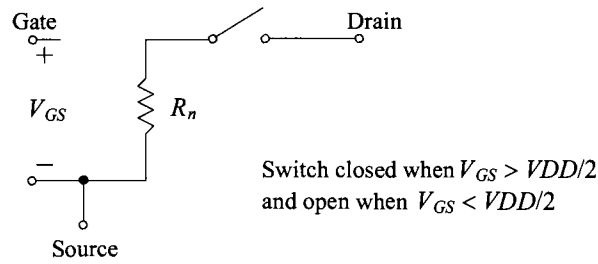


Figure 10.6 Simple digital MOSFET model.

Because the square-law equation used in Eq. (10.6) doesn't model, for example, the reduction in mobility, Sec. 6.5, present in submicron devices it's better to use measured data, via an experimentally-generated SPICE MOSFET model or bench data, to estimate the switching resistances. From Fig. 10.5 we can write

$$R_n = R_n' \cdot \frac{L}{W} = \frac{VDD}{I_{D,sat}} = \frac{5}{3.3\ mA} \rightarrow R_n' \approx 15\ k\Omega \tag{10.7}$$

For an NMOS device with a specific width, W, or length, L, we can estimate the effective switching resistance of the device in the *long-channel CMOS* process in this book (scale factor of 1 μm) as

$$R_n \approx 15k \cdot \frac{L}{W} \tag{10.8}$$

For the PMOS device, the transconductance parameter, KP, is three times smaller than the NMOS's KP (see Table 9.1), so we can write

$$R_p \approx 45k \cdot \frac{L}{W} \tag{10.9}$$

The effective resistance of the PMOS device is three times as large as the NMOS's due to the mobility of the electrons being larger than the mobility of the holes.

Short-Channel MOSFET Effective Switching Resistance

As discussed in Chs. 6 and 9, the short-channel MOSFET doesn't follow the square-law, long-channel, MOSFET models. We can't use Eq. (10.6) to estimate the effective switching resistance. However, we can use the *on current* for the devices (see Sec. 6.5.2). For the *short-channel CMOS* process used in this book (scale factor of 50 nm and a VDD of 1 V), we can write, see Eqs. (6.59), (6.60), and (6.61),

$$R_n = \frac{VDD}{I_{D,n}} = \frac{VDD}{I_{on,n} \cdot W \cdot scale} = \frac{1\ V}{600\ \frac{\mu A}{\mu m} \cdot W \cdot scale} \rightarrow R_n \approx \frac{1.7k \cdot \mu m}{W \cdot scale} \tag{10.10}$$

and

$$R_p = \frac{VDD}{I_{D,p}} = \frac{VDD}{I_{on,p} \cdot W \cdot scale} = \frac{1\ V}{300\ \frac{\mu A}{\mu m} \cdot W \cdot scale} \rightarrow R_p \approx \frac{3.4k \cdot \mu m}{W \cdot scale} \tag{10.11}$$

noting that the effective switching resistance of a short-channel MOSFET is independent of the MOSFET's length. In practice this is true to a point. Increasing the channel length above a certain value, for example $L = 2$, causes the MOSFET's resistance to grow.

Note that in the long-channel equations for switching resistance, Eqs. (10.8) and (10.9), the scale factor doesn't affect the resistance. However, using the short-channel equations the scale factor is important and does affect the switching resistance calculation when using I_{on}. Knowing, for the short-channel process used in this book, that the scale factor is 50 nm, we can rewrite Eqs. (10.10) and (10.11) as

$$R_n = \frac{34k}{W} \text{ and } R_p = \frac{68k}{W} \tag{10.12}$$

where W is the drawn width of the devices. Practically, to model the effects of increasing switching resistance when L is greater than 1 (minimum), we can re-write Eq. (10.12) as

$$R_n = 34k \cdot \frac{L}{W} \text{ and } R_p = 68k \cdot \frac{L}{W} \tag{10.13}$$

noting that now L and W can both be either drawn or actual sizes.

10.1.1 Capacitive Effects

At this point, we need to add the capacitances of the switching MOSFET to our model of Fig. 10.6. Consider the MOSFET circuit shown in Fig. 10.7 with capacitance $\frac{C_{ox}}{2}$ between the gate-drain and the gate-source electrodes. This is the capacitance when the MOSFET is in the triode region and is an *overestimate* for the capacitances of the MOSFET. For example, the capacitance between the gate and drain of the MOSFET is the overlap capacitance from the lateral diffusion when the MOSFET is operating in the saturation region (see Table 6.1). Because of this overestimate, we will neglect the depletion capacitances of the source and drain implants to substrate when doing hand calculations. Simulations using SPICE are required for better estimates of switching behavior (e.g., showing the nonlinearities of a depletion capacitance, see Fig. 2.15 or Eq. [5.17]).

Returning to Fig. 10.7, when the input pulse transitions from 0 to *VDD*, the output transitions from *VDD* to 0 (review Figs. 10.2 and 10.3). The current through C_{gd} (= C_{ox}/2) is given by

$$I = C_{gd} \cdot \frac{dV_{gd}}{dt} = \frac{C_{ox}}{2} \cdot \frac{VDD-(-VDD)}{\Delta t} = C_{ox} \cdot \frac{VDD}{\Delta t} = C_{ox} \cdot \frac{dV_{DS}}{dt} \tag{10.14}$$

The voltage across C_{gd} changes by $2 \cdot VDD$. The current that flows through this capacitance is the drain current of the MOSFET in Fig. 10.7. As seen in Fig. 10.3, we can break C_{gd} into a component from the gate to ground and from the drain to ground of value $2C_{gd}$ or C_{ox}. The complete model of a switching MOSFET is shown in Fig. 10.8.

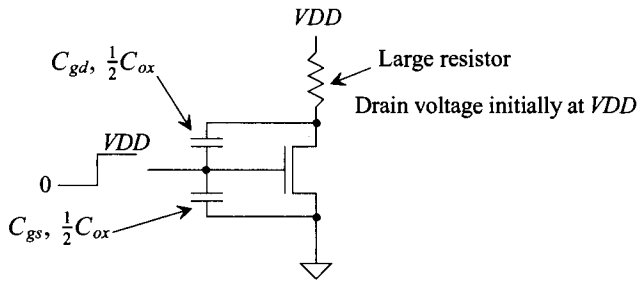


Figure 10.7 MOSFET switching circuit with capacitances.

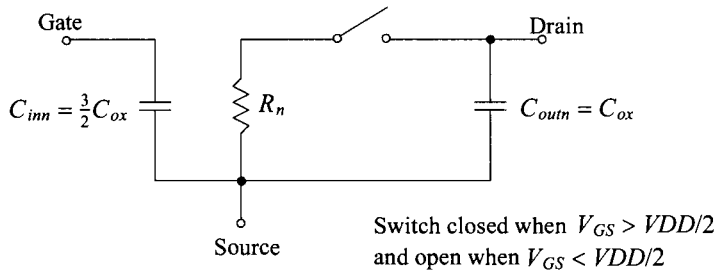


Figure 10.8 Simple digital MOSFET model.

10.1.2 Process Characteristic Time Constant

An important question we can answer at this point is, "What is the intrinsic switching speed of a MOSFET?" Looking at Figs. 10.7 and 10.8, we can see an intrinsic *process characteristic time constant,* τ_n, of R_nC_{ox}. That is, if the drain is charged to *VDD* as in Fig. 10.7 and the input switches from 0 to *VDD*, the output voltage will decay with a time constant of R_nC_{ox}. For an NMOS device in the long-channel process, this is given by

$$\tau_n = R_nC_{ox} = \frac{2L \cdot VDD}{KP_nW(VDD - V_{THN})^2} \cdot C'_{ox}WL \cdot (scale)^2 = \frac{2C'_{ox} \cdot VDD \cdot (L \cdot scale)^2}{KP_n \cdot (VDD - V_{THN})^2} \tag{10.15}$$

Notice that the "speed" of a process increases as the square of the channel length and that the speed is independent of the channel width, *W*. The process characteristic time constant is specified using the process minimum length. Also note that the larger the *VDD,* the faster the process. This is very similar to the unity current gain frequency, f_T, that we discussed in the last chapter. For a short-channel process, Eq. (10.15) can be rewritten as

$$\tau_n = R_nC_{ox} = \frac{VDD}{I_{on,n} \cdot W \cdot scale} \cdot C'_{ox}WL \cdot (scale)^2 = \frac{VDD \cdot C'_{ox} \cdot L \cdot scale}{I_{on,n}} \tag{10.16}$$

For the short-channel process, the time constant decreases linearly with decreasing channel length.

Example 10.1

Estimate the process characteristic time constants for the long- and short-channel CMOS processes used in this book.

For the NMOS device in the long-channel CMOS process, using the data in Table 5.1 and Eq. (10.8),

$$\tau_n = R_nC'_{ox}WL \cdot (scale)^2 = 15k \cdot \frac{L}{W} \cdot 1.75 \frac{fF}{\mu m^2} \cdot LW \cdot (scale)^2 \approx 25\,ps$$

Knowing from Eqs. (10.8) and (10.9) that the effective resistance of the PMOS device is three times as large as the resistance of the NMOS device, we can write

$$\tau_p \approx 75\,ps$$

For the short-channel process, using the data in Table 5.1 and Eq. (10.10), we can write

$$\tau_n = R_n C'_{ox} \cdot WL \cdot (scale)^2 = \frac{1.7k \cdot \mu m}{W \cdot scale} \cdot 25\frac{fF}{\mu m^2} \cdot WL \cdot (scale)^2 = 2.1\ ps$$

and for the PMOS device

$$\tau_p = 4.2\ ps$$

Table 10.1 summarizes the effective switching resistances and oxide capacitances for the long- and short-channel CMOS processes used in this book. ■

Table 10.1 Digital model parameters used for hand calculations in the long- and short-channel CMOS processes used in this book. Note that the widths, W, and lengths, L, seen in this table are drawn lengths (minimum length is 1 while minimum width is 10).

Technology	R_n	R_p	Scale factor	$C_{ox} = C'_{ox} WL \cdot (scale)^2$
1 μm (long-channel)	$15k\frac{L}{W}$	$45k\frac{L}{W}$	1 μm	$(1.75\,fF) \cdot WL$
50 nm (short-channel)	$\frac{34k}{W}$	$\frac{68k}{W}$	50 nm	$(62.5\ aF) \cdot WL$

10.1.3 Delay and Transition Times

Before we go any further in the discussion of the digital models, let's define delays and transition times in logic circuits. Consider Fig. 10.9. The top trace represents the input to a logic gate, while the bottom trace represents the output. Note that there is no logic inversion between the input and output; however, the following definitions apply equally well to the case when there is an inversion. The input rise and fall times are labeled t_r and t_f respectively. The output rise and fall times are labeled t_{LH} and t_{HL}, respectively. The

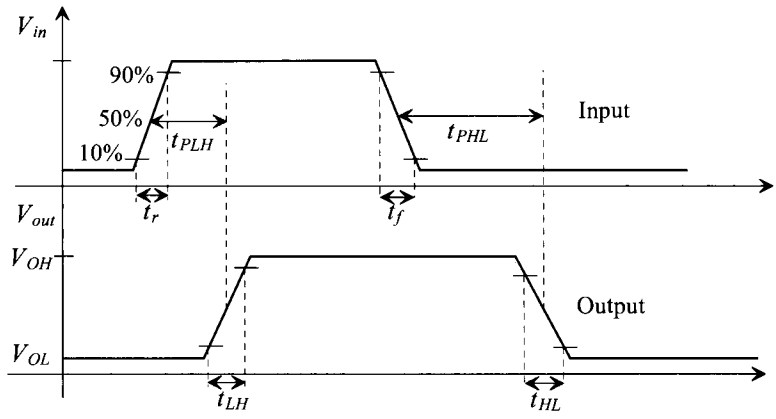


Figure 10.9 Definition of delays and transition times.

delay time between the 50% points of the input and output are labeled t_{PLH} and t_{PHL}, depending on whether the output is changing from a high to a low or from a low to a high. These definitions are extremely important in characterizing the time-domain characteristics of digital circuits.

For the simple *RC* circuit shown back in Fig. 2.21, the delay time is given by

$$t_{delay} = 0.7RC \tag{10.17}$$

and the rise or fall time is given by

$$t_{rise} = 2.2RC \tag{10.18}$$

For our simple digital model of Fig. 10.8, we will assume that the propagation delay time, whether high-to-low or low-to-high, is given by

$$t_{PHL} \approx 0.7 \cdot R_n \cdot C_{tot} \text{ and } t_{PLH} \approx 0.7 \cdot R_p \cdot C_{tot} \tag{10.19}$$

and the output rise and fall times are given by

$$t_{HL} \approx 2.2 \cdot R_n \cdot C_{tot} \text{ and } t_{LH} \approx 2.2 \cdot R_p \cdot C_{tot} \tag{10.20}$$

where C_{tot} is the total capacitance from the drain of the MOSFET to ground. These models for hand calculations **do not give exact results**. The models are useful for determining approximate delay and transition times, usually within a factor of two. They can be used to reveal the location of a speed limitation in a circuit.

Example 10.2

Using hand calculations, estimate the rise, fall, and delay times of the following circuits (Fig. 10.10) in both the long- and short-channel CMOS processes. Compare your results to SPICE simulations.

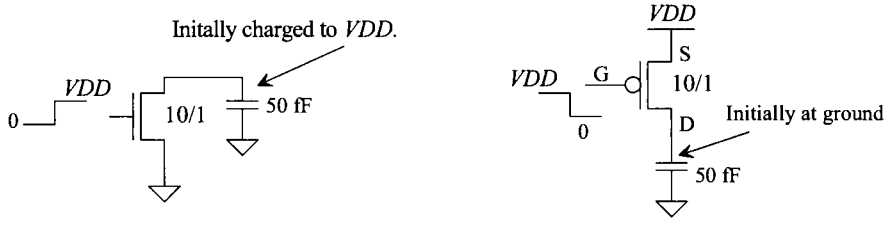


Figure 10.10 Circuits used in Example 10.2.

The models used for calculating delays are seen in Fig. 10.11. The time constant associated with discharging a load capacitor (the NMOS switch) is

$$t_{PHL} = 0.7 \cdot R_n C_{tot} = 0.7 \cdot R_n \cdot (C_{ox} + C_L) \tag{10.21}$$

The time constant associated with charging a load capacitance (the PMOS switch) is

$$t_{PLH} = 0.7 \cdot R_p C_{tot} = 0.7 \cdot R_p \cdot (C_{ox} + C_L) \tag{10.22}$$

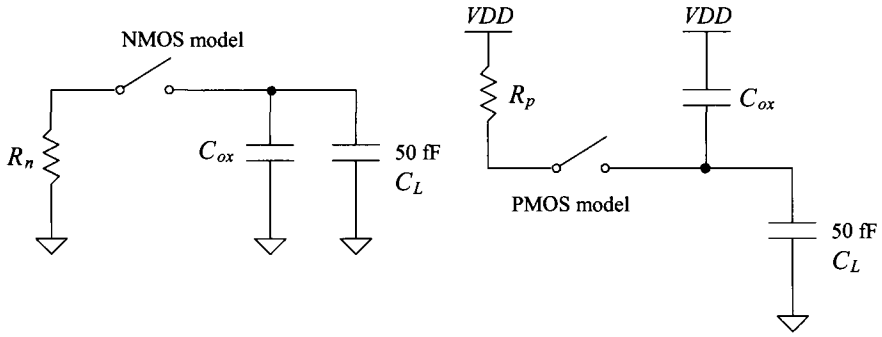


Figure 10.11 Models used to determine switching times in Example 10.2.

In many practical situations the load capacitance is much larger than the output capacitances of the switches. These equations can then be reduced to

$$t_{PHL} = 0.7 \cdot R_n \cdot C_L \text{ and } t_{PLH} = 0.7 \cdot R_p \cdot C_L \text{ for } C_L >> C_{ox} \qquad (10.23)$$

Using Eqs. (10.21) and (10.22) with the parameters in Table 10.1, we can estimate the delays using the long-channel process as

$$t_{PHL} = 0.7 \cdot 15k \cdot \frac{1}{10} \cdot (1.75\,fF \cdot 10 + 50\,fF) = 70\,ps$$

and

$$t_{PLH} = 0.7 \cdot 45k \cdot \frac{1}{10} \cdot (1.75\,fF \cdot 10 + 50\,fF) = 210\,ps$$

For the short-channel process, we get

$$t_{PHL} = 0.7 \cdot \frac{34k}{10} \cdot (62.5\,aF \cdot 10 + 50\,fF) = 120\,ps$$

and

$$t_{PLH} = 0.7 \cdot \frac{68k}{10} \cdot (62.5\,aF \cdot 10 + 50\,fF) = 240\,ps$$

The simulation results are seen in Fig. 10.12. We can also estimate the output rise and fall times using Eqs. (10.19) and (10.20). For the long-channel devices

$$t_{HL} = \frac{2.2}{0.7} \cdot t_{PHL} = 220\,ps$$

and

$$t_{LH} = \frac{2.2}{0.7} \cdot t_{PLH} = 660\,ps$$

For the short-channel devices

$$t_{HL} = 377\,ps \text{ and } t_{LH} = 754\,ps \blacksquare$$

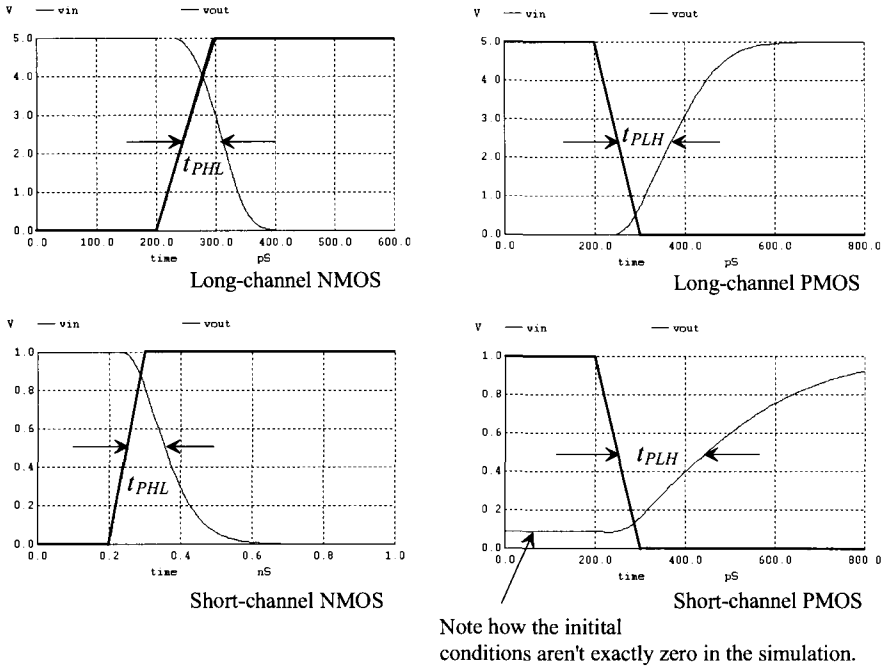


Figure 10.12 Simulating the circuits in Fig. 10.10.

10.1.4 General Digital Design

For general digital design, using the long or short-channel CMOS processes discussed in this book, we can set the drawn size of the NMOS devices to 10/1. To match the effective resistance of the PMOS device to the NMOS device in the long-channel process, Table 10.1, we set the PMOS size to 30/1 (the width of the PMOS is three times the width of the NMOS). For the short-channel process, we use a PMOS device of 20/1 to match the effective switching resistances. Table 10.2 summarizes the parameters for general digital design in the short- and long-channel processes used in this book. For specific digital design solutions we may use a longer device if a higher resistance is needed or a wider device if more drive current through the MOSFET is required.

Table 10.2 Parameters for general digital design using the long-channel (scale factor is 1 μm) or short-channel (scale factor of 50 nm) CMOS process **used in this book.**

Technology	Drawn	Actual size	$R_{n,p}$	$C_{ox,n,p}$
NMOS (long-channel)	10/1	10 μm by 1 μm	1.5k	17.5 *fF*
PMOS (long-channel)	30/1	30 μm by 1 μm	1.5k	52.5 *fF*
NMOS (short-channel)	10/1	0.5 μm by 50 nm	3.4k	625 *aF*
PMOS (short-channel)	20/1	1 μm by 50 nm	3.4k	1.25 *fF*

10.2 The MOSFET Pass Gate

Consider the NMOS device seen in Fig. 10.13a. This is the configuration we are accustomed to looking at, that is, where the NMOS device pulls the output to ground. In (b) we flip the MOSFET in (a) on its side and change the labels from ground to "logic 0" and from *VDD* to "logic 1." Note the locations of the source and drain in these configurations. Also note that in (b) the output is pulled all the way to ground (to a good "0"). It can be said that *an NMOS device is good at passing a* "0."

Next look at the configuration in (c). The configurations in (b) or (c) are sometimes called the *pass gate (PG) configuration.* The MOSFET passes the logic level on its input to its output when its gate is driven to *VDD* (when the PG is enabled). Note that when the PG is disabled (its control gate is driven to ground), the outputs are in a high-impedance state (a *Hi-Z* state). The PG can be useful when sharing a bus or a logic circuit. Also note that the inputs and outputs of the PG can be swapped. Logic flow through the PG can be *bi-directional.*

Returning to (c), we see that if the input to the PG is a "1" we can no longer think of the input as the source of the MOSFET like we did in (a) and (b). If we were to do so, then the V_{GS} of the MOSFET would be zero and the MOSFET would be off. If the NMOS device were off while its gate was driven to *VDD*, then this would contradict our comments at the beginning of the chapter associated with Fig. 10.1. To keep the MOSFET on, we need at least a V_{GS} of V_{THN}. As seen in (d) of the figure, this means that the NMOS PG passes a "1" with a threshold voltage drop. It can be said that *an NMOS device is not good at passing a* "1." Figure 10.14 shows how the output of a PG varies as its input transitions between ground and *VDD* using the 50 nm CMOS process.

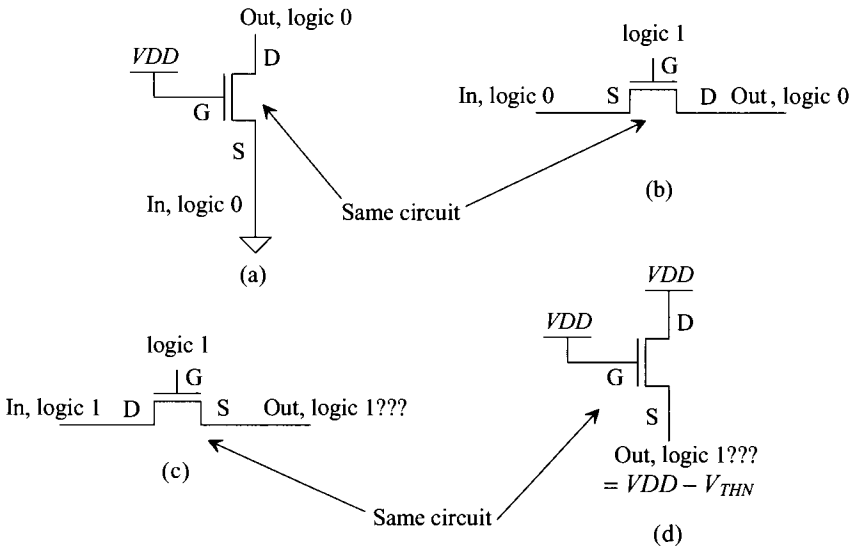


Figure 10.13 Using the NMOS switch as a pass gate.

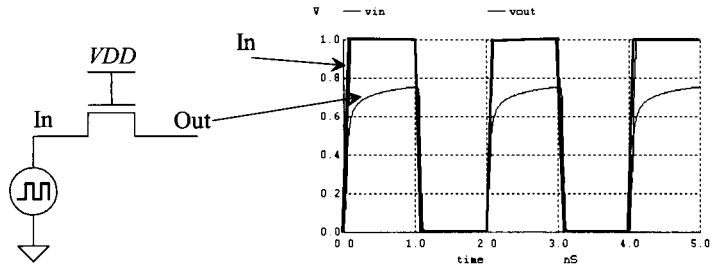


Figure 10.14 The input and output of an NMOS pass gate.

The PMOS Pass Gate

Figure 10.15 shows the operation of the PMOS PG. As expected the operation of the PMOS device is complementary to the NMOS's operation. The PMOS device turns on when its gate is driven to ground. If its gate is pulled to *VDD*, the device is off (and the output is in the Hi-Z state). In Fig. 10.15a the PG is passing a "1" to the output (the V_{SG} is *VDD*). In (b) a "0" is passed to the output. However, noting that the terminals we label drain and source are swapped from (a), the output only gets pulled down to V_{THP}. In (b) the V_{SG} of the MOSFET is V_{THP}. It can be said that a *PMOS PG is good at passing a 1 and bad at passing a 0.*

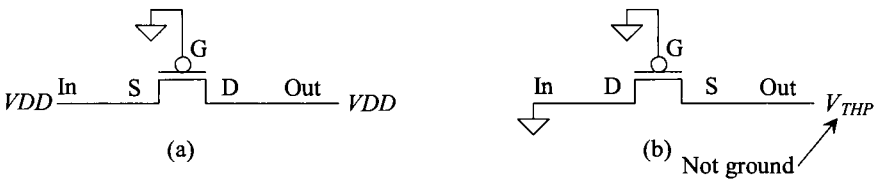


Figure 10.15 How the PMOS device does not pass a logic 0 well.

Example 10.3
Estimate the output voltages in the circuits seen in Fig. 10.16.

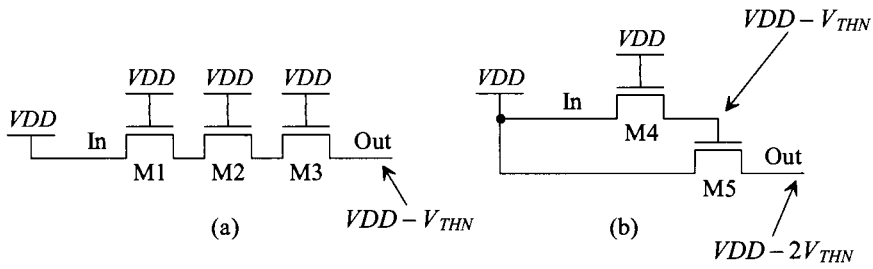


Figure 10.16 Circuits used in Ex. 10.3.

In (a) the output of M1 is $VDD - V_{THN}$. To keep M2 and M3 on, each MOSFET must have a V_{GS} of at least V_{THN}. Because the gates of M2 and M3 are already at VDD, the output of M1 gets passed through M2 and M3 to the final output of the circuit. As seen in the figure this means the overall output is also $VDD - V_{THN}$. We only take one threshold voltage hit.

In (b) the output of the M4 is $VDD - V_{THN}$. This is the gate voltage of M5. For M5 to be on its gate-source voltage must be greater than V_{THN}. The final output is then $VDD - 2V_{THN}$ (again as seen in the figure). ■

10.2.1 Delay through a Pass Gate

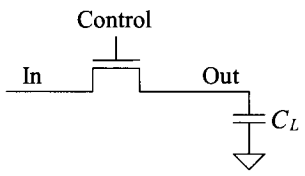
Consider the PG configuration seen in Fig. 10.17a. Let's estimate the delay between the input and the output of the PG. Note that if the input to the circuit is a "0" the PG behaves like the configuration seen in Fig. 10.4 and the output gets pulled all the way down to ground. Let's consider the configuration seen in Fig. 10.17b where the input is transitioning from a "0" to a "1" (VDD). The capacitance that the input sees is $C_{ox}/2$. The total load capacitance is

$$C_{tot} = C_L + \frac{C_{ox}}{2} \tag{10.24}$$

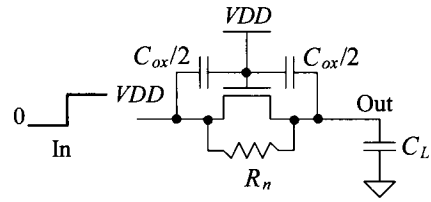
The delay through the PG can be estimated as

$$t_{delay} = 0.7 \cdot R_n C_{tot} = 0.7 \cdot R_n \cdot \left(C_L + \frac{C_{ox}}{2} \right) \tag{10.25}$$

Let's use this result in an example.



(a) Delay from the input to the output through a pass gate.



(b) The capacitances and effective resistance when turning the MOSFET on with an input 1.

Figure 10.17 Estimating the delay through a pass transistor.

Example 10.4

Estimate the delays through the PGs shown in Fig. 10.18. Verify your estimates with simulations. Use the 50 nm (short-channel) CMOS process.

The MOSFETs used in this example have the effective resistances and oxide capacitances listed in Table 10.2. Because the oxide capacitance (the MOSFET's capacitance) is much less than the load capacitance, we can write

$$t_{delay} \approx 0.7 \cdot R_{n,p} C_L \tag{10.26}$$

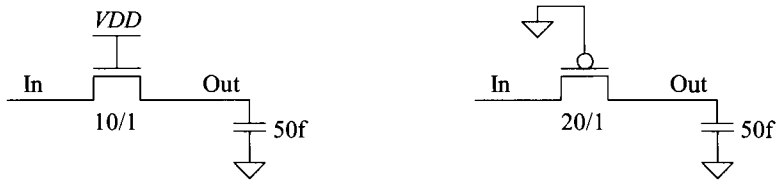


Figure 10.18 Circuits used to calculate delays in Ex. 10.4.

For the NMOS or PMOS PGs in Fig. 10.18 the delays are estimated as

$$t_{delay} \approx 0.7 \cdot 3.4k \cdot 50fF = 120\,ps$$

The simulation results are seen in Fig. 10.19. If we measure the output delays in Fig. 10.19 at 50% of *VDD* (500 mV), as defined in Fig. 10.9, then we get considerably different values from our hand calculations. The fact that the outputs of the PGs don't swing all the way to the power supply rails changes the points where we would measure the delays (to, say, 50% of the output swing). Again, it's important to note that our hand calculations give approximate delays and, more importantly, can indicate the location of a speed limitation in a digital circuit. The hand calculations won't provide exact delay values. Even if they could, the results would be subjective, dependent on the locations (voltage levels) on the input and output waveforms where we measure the delay. ■

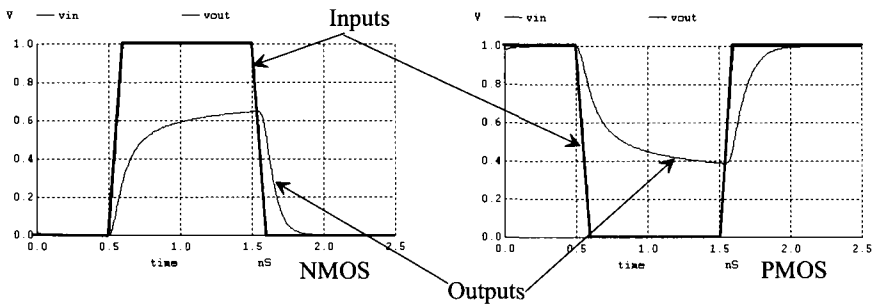


Figure 10.19 The delay through the PGs in Fig. 10.18.

The Transmission Gate (The TG)

The observant reader may be wondering: "If an NMOS PG passes a 0 well and a PMOS PG passes a 1 well, can't we put the two together and pass full logic levels?" The resulting circuit is called a *transmission gate*, *TG*, and is seen in Fig. 10.20. When the select control signal, *S*, is high, the TG is on and the input is passed to the output. The drawbacks of the TG over the PG are increased layout area and the need for two control signals (*S* and its complement). The benefit of using the TG is its rail-to-rail output swing. We'll discuss the TG in more detail in Ch. 13.

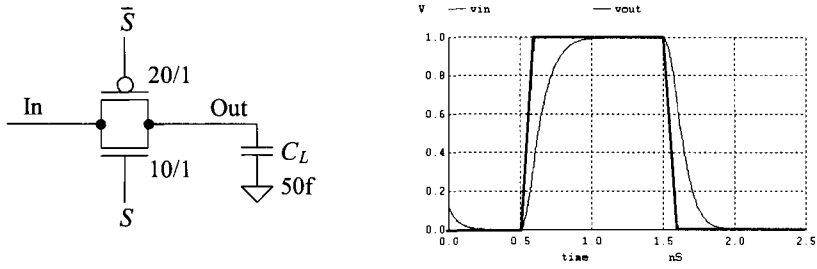


Figure 10.20 Simulating the operation of a transmission gate.

Also seen in Fig. 10.20 are simulation results showing the delay through the TG. For the values seen, the load capacitance is, again, much larger than the oxide capacitances of the MOSFETs, so we can calculate the delay as

$$t_{delay} = 0.7 \cdot (R_n || R_p) \cdot C_L \tag{10.27}$$

Using the results from Ex. 10.4, the delay is estimated as 60 ps (very close to the simulation results).

10.2.2 Delay through Series-Connected PGs

Consider the series connection of (identically sized) NMOS PGs seen in Fig. 10.21. Reviewing Fig. 10.17, we see that capacitance on the internal nodes, in between MOSFETs, is C_{ox} (a contribution of half of C_{ox} from each MOSFET). To approximate the delay through the MOSFETs, we can use Eq. (2.32) or

$$t_{delay} \approx 0.35 \cdot R_n \cdot C_{ox} \cdot l^2 \tag{10.28}$$

Noting $R_n C_{ox}$ is the process characteristic time constant, τ_n , we can quickly estimate delays through series-connected PGs without doing much of a calculation. For example,

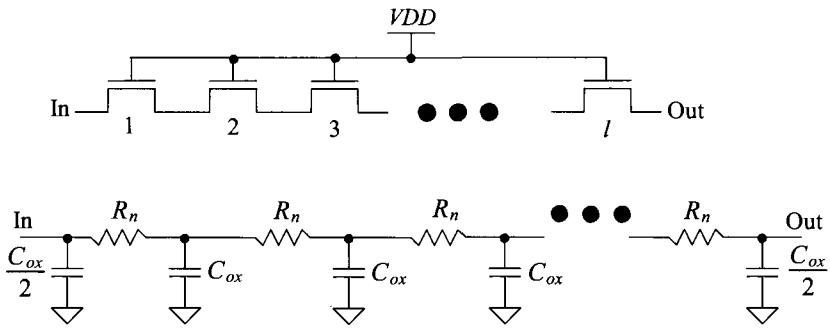


Figure 10.21 How a series connection of MOSFETs behaves like an RC transmission line (see Fig. 2.22).

we know that τ_n, for the 50 nm process, is 2.1 ps from Ex. 10.1. If we have 10 NMOS PGs in a row, the delay through the string is estimated as 73.5 ps.

Example 10.5

Estimate the delay through the circuit in Fig. 10.22. Verify the estimate with a SPICE simulation. Use the 50 nm process with 10/1 NMOS devices.

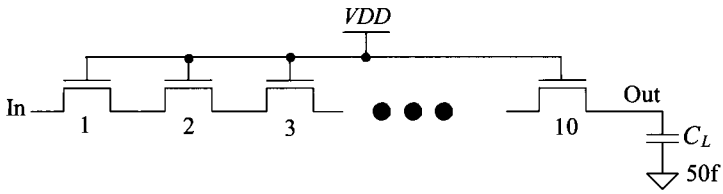


Figure 10.22 Circuit used in Ex. 10.5.

The total delay is the sum of the RC transmission line delay with the delay in charging the load capacitance through the 10 PGs. This delay can be written for the general case as

$$t_{delay} \approx 0.35 \cdot R_n \cdot C_{ox} \cdot l^2 + 0.7 \cdot l \cdot R_n \cdot C_L \qquad (10.29)$$

For the present example, the delay is

$$t_{delay} \approx \overbrace{0.35 \cdot 2.1\,ps \cdot (10)^2}^{73.5\,ps} + 0.7 \cdot 10 \cdot 3.4k \cdot 50f \approx 1.2\,ns \qquad (10.30)$$

The simulation results are seen in Fig. 10.23. ■

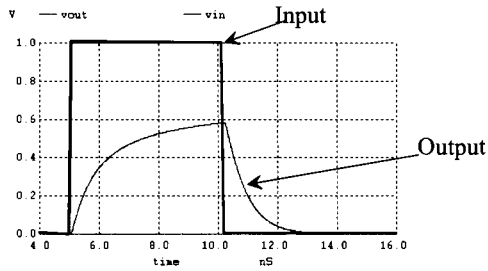


Figure 10.23 Simulating the operation of the circuit in Fig. 10.22.

10.3 A Final Comment Concerning Measurements

Notice that the capacitances we are discussing in this chapter are relatively small. When making measurements it is extremely easy to add a capacitance to the circuit that significantly increases the delays (and may cause circuit failure). Towards understanding this comment in more detail consider the compensated scope probe shown in Fig. 10.24. In (a) we see the input impedance of the oscilloscope (o-scope) is a 1 MΩ resistor in

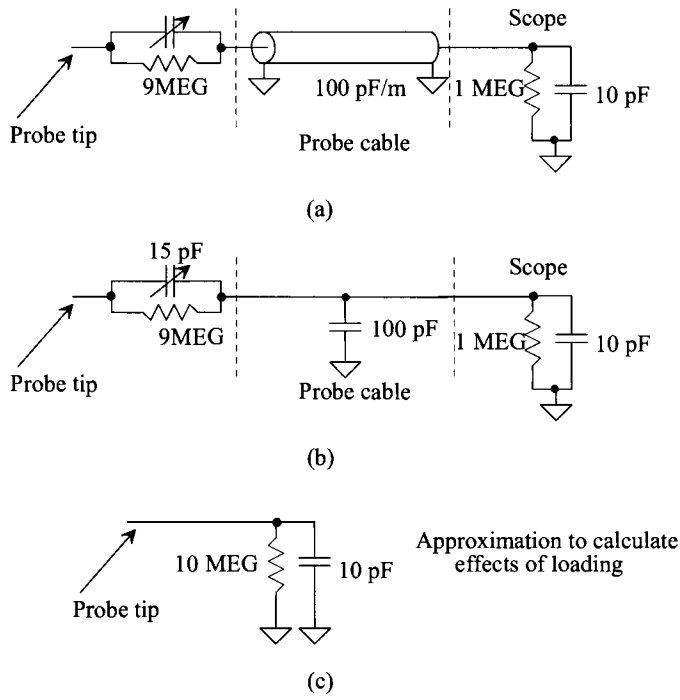


Figure 10.24 Showing how a common scope probe is assembled.

parallel with a 10 pF capacitor. (The actual values are indicated next to the connector on the front of the particular o-scope.) If we connect a piece of cable (co-axial cable or simply coax) from the circuit under test to the input of the scope, we introduce significant capacitance into the circuit. As seen in (a) the cable's capacitance may be as much as 100 pF/meter. Using a piece of coax to probe the circuit (alone) would then add a 110 pF capacitor and a 1 MΩ resistor to ground at each point we probe! **Understanding this is important.** It's common to see new engineering students, in a digital logic lab for example, probing with a cable (that is, without an o-scope probe). They may wonder why their circuits don't work or only work at slow speeds.

To compensate for the cable capacitance, the probe tip has a series resistor and capacitor added in between the cable and the probe tip, (b). This combination of a cable and probe tip RC is called a *compensated scope probe.* The RC in the probe tip is adjusted to have nine times the impedance of the RC from the scope's input to ground (the cable capacitance in parallel with the scope's input impedance) over all frequencies of interest. In other words, a 10:1 voltage divider exists between the probe tip and the input of the scope (and so the minimum signal we can measure increases when using a compensated scope probe). The big benefit, as seen in the approximation for the loading in (c), is that the size of the capacitance introduced into the circuit is reduced. For probing on-chip (or on-wafer), special probes are used with active devices in the probe tips (to reduce the probe's loading on the circuit it is measuring). Active probe tips, called femtoprobes, can be purchased that only have femtofarads amounts of loading.

ADDITIONAL READING

[1] J. P. Uyemura, *Introduction to VLSI Circuits and Systems*, John Wiley and Sons Publishers, 2002. ISBN 0-471-12704-3.

[2] R. L. Geiger, P. E. Allen, and N. R. Strader, *VLSI-Design Techniques for Analog and Digital Circuits,* McGraw-Hill Publishing Company, 1990. ISBN 0-07-023253-9.

PROBLEMS

10.1 Using the parameters in Table 6.2, compare the hand-calculated effective digital switching resistance from Eq. (10.6) to the empircially derived values given in Table 10.1.

10.2 Regenerate Fig. 10.14 for the PMOS device.

10.3 Using SPICE verify the results of Ex. 10.3.

10.4 Replacing the NMOS PGs in Fig. 10.16 with PMOS PGs and changing the *VDD*-connected nodes to ground-connected nodes, show, and verify with simulations, the outputs of the two modified circuits.

10.5 For the following circuits estimate the delay between the input and the output. Use the 50 nm (short-channel CMOS) process. Verify the estimates with SPICE.

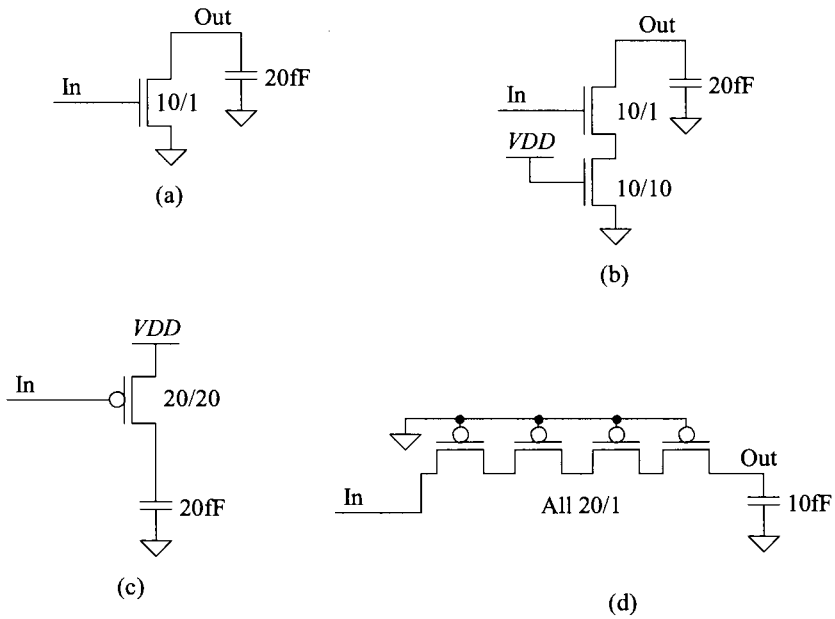


Figure 10.25 Circuits used in Problem 10.5.

Possible Student Projects

This section lists some possible student projects for fabrication through the MOSIS service (see Ch. 1). Generally, two to four student projects should be implemented on one chip. MOSIS will return to the MOSIS liaison (generally, the course instructor) several copies of each chip design submitted.

The design rule-checked designs should be turned in along with (1) one sheet of paper showing the logic level diagrams *and* pin connections so that whoever is evaluating the chip can quickly determine functionality, and (2) final reports that consist of a block diagram, schematic diagram, layout information, hand calculations, SPICE simulations, and clear explanations (and trade-offs) of the operation of the circuit.

1. Quad 2-input MUX
2. Clock-doubling circuit using exclusive OR gate
3. Buffer with tristate outputs
4. SR flipflop with tristate outputs
5. Edge-triggered T flipflop
6. Edge-triggered D flipflop
7. Schmitt trigger
8. 1-of-16 decoder
9. Up counter with asynchrounous reset
10. 4-bit static shift register
11. 4-bit dynamic shift register
12. 2-bit adder with carryout
13. Current-starved VCO with center frequency of 20 MHz
14. 2-bit bidirectional transceiver
15. PE gate to implement $X = \overline{A + BCD + EF}$
16. One-shot whose output pulse width is determined by external RC
17. Buffer for driving a 20 pF load with minimum delay
18. Buffer for driving a 20 pF load with smaller layout area

Advanced projects

19. A 64-bit static RAM including a storage cell, addressing and decoding circuitry, buffers, a write/read enable, and a chip select.
20. Charge pump (voltage generator). The input to the charge pump is *VDD* (= 5 V) and the output is –3 V. The circuit should be fully simulated. The reference, oscillator, and feedback should be fully simulated and discussed in the final report.

21. A 64-bit DRAM, including a storage cell, addressing and decoding circuitry, buffers, a write/read enable, and a chip select.

22. A DPLL which will take a 1 MHz input and generate a 4 MHz output. The output should follow the input for frequency changes from 900 kHz to 1.1 MHz. You should discuss the transient properties of the DPLL, as well as present a detailed design of the phase detector, VCO, and loop filter. The entire design should be monolithic; that is, no external components should be used.