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Team name: Silver Pipelining
ECE 411 MP3, Checkpoint 2

Roadmap:

For Checkpoint 3, we will modify our pipelined processor in order to account for control and data hazards- i.e., instructions whose operands are determined as a result of a previous instruction that has not yet left the pipeline. We already have a paper design implementation of the hazard detection unit, so translating that to SystemVerilog should be reasonably simple.

After this is done, we have a variety of advanced design options to consider and pursue. We will most likely implement some type of branch prediction in order to improve our processor's performance. Other design options that we are considering are leapfrogging and a victim cache. However, we still need to discuss these options more fully- both as a group and with our mentor TA- before we fully commit to implementing them. We will also need to do more research on the subjects involved.