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Team name: Silver Pipelining
ECE 411 MP3, Checkpoint 2

Progress Report:

For Checkpoint 2, our group expanded on our basic pipelined processor design to support all of the instructions in the LC-3b ISA (with the exception of RTI). We also implemented the remaining elements of the memory hierarchy: a split L1 cache connected to an L2 cache, with accesses mediated by an arbiter. The L2 cache interfaces directly with physical memory. This required a solid understanding of pipelined processor design as we had to implement pipeline stalls to account for cache misses. Our first step in this process was to design the L1 cache, arbiter, and L2 cache. We decided to use the 2-way, 8-set cache we implemented in MP2 as our L1 cache- then, since the L2 cache should be larger than the L1, we decided to use an 8-way, 8-set writeback cache to implement that. We used a state-machine-based arbiter design to mediate access between the split L1 cache and L2 cache. Next, we modified our datapath paper design to account for the remaining LC3-b instructions, adding MUXes and control signals when necessary. We utilized a modular testing strategy, ensuring that our pipeline design worked with the dual-port magic memory before attempting to add the split L1 cache. Essentially, we added memory hierarchy components one at a time, debugging the design on each step. This assisted us in debugging as it enabled us to know for sure as to which component had the bug. Throughout the process, we used code with unpadded STIs/LDIs in order to stress-test the design.

So far, work has been divided fairly evenly between the members of our group- Rishi and Nathan implemented the updated pipelined datapath, while Melissa implemented the cache arbiter and L2 cache. The three of us worked together to integrate the components and debug the design using test code that we wrote. As before, we communicated with one another to establish common naming conventions and SystemVerilog coding structures. This minimized the time required to successfully integrate the separate components into a cohesive design.