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ECE 411 MP3, Checkpoint 1

Roadmap:

In future checkpoints, we will continue to add functionality to our basic pipelined processor design. Currently, our design does not account for control or data hazards- i.e., instructions whose operands are determined as a result of a previous instruction that has not yet left the pipeline. We will need to design and implement a hazard detection method that can account for these cases. Furthermore, our design currently uses a dual-port magic memory, which is impossible to implement for a real processor. In future checkpoints, we will implement a two-level cache with separate data and instruction storage. This is necessary to minimize pipeline stalls upon a cache hit caused by a load or store instruction- without a separate I-cache and D-cache, we wouldn't be able to load the next instruction and a data value in the same clock cycle. The two L1 caches will interface with the L2 cache by means of an arbiter, which will decide which L1 cache should interface with the L2 in a given cycle. This L2 cache will then interface with a more realistic physical memory similar to the one used in MP2. Finally, we will need to implement the remaining instructions in the LC-3b instruction set.

Specifically for Checkpoint 2, we will implement the remaining LC-3b instructions, the split L1 caches, and the cache arbiter. Depending on time constraints, we may implement the L2 cache for this checkpoint as well. If we so do, the cache arbiter will interface with this; else, it will simply connect to the physical memory.