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Team name: Silver Pipelining
ECE 411 MP3, Checkpoint 1

Progress Report:

For Checkpoint 1, our group implemented a basic pipelined processor supporting six instructions in the LC-3b ISA (ADD, AND, NOT, LDR, STR, and BR). To do this, our first step was to modify our datapath paper design according to feedback from our mentor TA. Next, we implemented this datapath design in SystemVerilog, creating the appropriate registers and combinational logic for each pipeline stage. Third, we designed the control ROM by tracing the execution of instructions through the datapath and determining what the control signal values needed to be at each stage. In SystemVerilog, our control ROM module was implemented using a simple case statement on the input opcode. Finally, we created a top-level module to interface with our testbench and connect our control ROM and datapath instances.

So far, work has been divided fairly evenly between the members of our group- Rishi and Melissa implemented the datapath, while Nathan implemented the control ROM. The three of us worked together to integrate the components and debug the design using the provided test code. Throughout the entire process, we communicated with one another to establish common naming conventions and SystemVerilog coding structures. This minimized the time required to successfully integrate the separate components into a cohesive design. Following a systematic design approach also enabled us to reduce our debugging time.