

Formal Verification Screenshots

```
op_Module.v'
Setting top design to 'r:/WORK/simple_processor_Top'
Status: Elaborating design controller_new ...
Warning: Variable 'opcode' referenced inside always block which is not in sensitivity list. (Signal: opcode Block
: /controller_new File: /home/userdata/21mvd0086/Simple_Processor_Working/Formal_Verification/fv/controller_12_ap
ril.v Line: 61) (FMR_VLOG-079)
Warning: Variable 'Run' referenced inside always block which is not in sensitivity list. (Signal: Run Block: /con
troller_new File: /home/userdata/21mvd0086/Simple_Processor_Working/Formal_Verification/fv/controller_12_april.v
Line: 99) (FMR_VLOG-079)
Warning: Variable 'DIN' referenced inside always block which is not in sensitivity list. (Signal: DIN Block: /con
troller_new File: /home/userdata/21mvd0086/Simple_Processor_Working/Formal_Verification/fv/controller_12_april.v
Line: 105) (FMR_VLOG-079)
Warning: Variable 'opcode' referenced inside always block which is not in sensitivity list. (Signal: opcode Block
: /controller_new File: /home/userdata/21mvd0086/Simple_Processor_Working/Formal_Verification/fv/controller_12_ap
ril.v Line: 111) (FMR_VLOG-079)
Warning: Variable 'Yreg' referenced inside always block which is not in sensitivity list. (Signal: Yreg Block: /c
ontroller_new File: /home/userdata/21mvd0086/Simple_Processor_Working/Formal_Verification/fv/controller_12_april.
v Line: 117) (FMR_VLOG-079)
Warning: Variable 'Xreg[9:2]' referenced inside always block which is not in sensitivity list. (Signal: Xreg[9:2]
Block: /controller_new File: /home/userdata/21mvd0086/Simple_Processor_Working/Formal_Verification/fv/controller
_12_april.v Line: 119) (FMR_VLOG-079)
Status: Elaborating design dec3to8 ...
Status: Elaborating design dec3to8_3bit ...
Status: Elaborating design datapath_register_array ...
Status: Elaborating design mux_10to1 ...
Status: Elaborating design Add_Sub ...
Status: Elaborating design csa_9bit ...
Status: Elaborating design full_adder ...
Status: Elaborating design half_adder ...
Status: Elaborating design carry_select_adder_4bit_slice ...
Status: Elaborating design ripple_carry_4_bit ...
Status: Elaborating design mux2X1 ...
Status: Elaborating design mux2X1_1 ...
Status: Elaborating design reg_G ...
Status: Elaborating design Register ...
Status: Implementing inferred operators...

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10.10.3.29 (21mvd0086)
Setting top design to 'r:/WORK/simple_processor_Top' with warnings
ATTENTION: RTL interpretation messages were produced during link.
Verification results may disagree with a logic simulator.

***** Library Checking Summary *****
Warning: 186 unlinked power cell(s) with unread pg pins.
Warning: 2535 unlinked power cell(s) with no power down functions on outputs.
Warning: 6 unlinked power cell(s) with unread backup pg pins.
Warning: 714 unlinked power cell(s) with no power down function on an ff or latch.
Use 'report_libraries -defects all' for more details.
*****

Top design set to 'r:/WORK/simple_processor_Top' with warnings
***** RTL Interpretation Summary *****
***** Design: r:/WORK/simple_processor_Top
6 FMR_VLOG-079 messages produced (Incomplete sensitivity list)

Please refer to the Formality log file for more details,
or execute report_hdlin_mismatches.
*****

Reference design set to 'r:/WORK/simple_processor_Top'
No target library specified, default is WORK
Loading verilog file '/home/userdata/21mvd0086/Simple_Processor_Working/Formal_Verification/fv/Simple_Processor_n
etlist.v'
```



The screenshot shows a Windows desktop environment with various application icons in the taskbar. The active window is a terminal titled "10.10.10.529 (21mwx0086)". The terminal output displays the configuration for verification, followed by successful completion messages and a detailed comparison report.

```
set verification_verify_directly_undriven_output false
For details see report_dont_verify_points and report_constants

For further details on Synopsys Auto Setup Mode: Type man synopsys_auto_setup

***** Verification Results *****
Verification SUCCEEDED
ATTENTION: synopsys_auto_setup mode was enabled.
           See Synopsys Auto Setup Summary for details.
ATTENTION: RTL interpretation messages were produced during link
           of reference design.
           Verification results may disagree with a logic simulator.
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Reference design: r:/WORK/simple_processor_Top
Implementation design: i:/WORK/simple_processor_Top
148 Passing compare points
-----
```

	Matched Compare Points	BBDPin	Loop	BBNet	Cut	Port	DFF	LAT	TOTAL
Passing (equivalent)	0	0	0	0	0	10	97	41	148
Failing (not equivalent)	0	0	0	0	0	0	0	0	0

```
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Report      : guidance
              -summary

Reference   : r:/WORK/simple_processor_Top
Implementation : i:/WORK/simple_processor_Top
Version     : 0-2018.06-SP4
Date        : Mon May 2 00:07:39 2022
*****
SVF hasn't been set.
fm_shell (verify)>
```

At the bottom of the terminal window, there is a footer for the MobaXterm software, indicating it is a registered version and providing contact information for support.