**Date:4/5/2022**


VIT®
Vellore Institute of Technology
(Deemed to be University under section 3 of UGC Act, 1956)

**Fall Semester 2021-2022**

**ECE5014 – ASIC Design**

**M.Tech VLSI Design**

**School of Electronics Engineering**

**Vellore Institute of Technology**

**Name: Shreyas S Bagi**

**Register Number: 21MVD0086**

**Slot: L3+L4**

**Date:4/5/2022**

# Lab Task 02

## Architecture Design of Simple Processor

# Section 1 Logic Optimization and Power Optimization

**Aim:** Synopsys Design Complier used for Logic Optimization and Power Optimization of Simple Processor.

**Script used for logic optimization and power optimization of Architecture Design of Simple Processor:**

The SAIF file is generated for Move operation from Logic simulation. This SAIF is included in the script. The Power optimization and Timing Optimization is done based upon this file.

1. **Tickle Script for Multi-Vth of saed14rvt_tt0p8v125c, saed14rvt_ss0p72v125c and saed14rvt_ff0p88v125c. Clock Period = 10ns**

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.

set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.db \
```

```
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db"


##########################################################################
# Logical Library Settings
##########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

set HVT_lib saed14hvt_tt0p8v125c
set LVT_lib saed14lvt_tt0p8v125c
set_attribute [get_libs $HVT_lib]
default_threshold_voltage_group HVt
set_attribute [get_libs $LVT_lib]
default_threshold_voltage_group LVt
set_multi_vth_constraint -lvth_groups {LVt} -lvth_percentage 50 -type hard -
include_blackboxes
#changed this
set_dynamic_optimization true
set_leakage_optimization true

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Top_Module.v
read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top_Top

#Module Name should be written here

######################## Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
```

```
    #   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #       previopus
block.

    #2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
    #   These are defined in libraries set minimum and max temp range value

    #3. Wire Load module.
    #   Estimate Net delay of Interconnecting wire and net.
    #   Estimation of delay using Wire Load module.
    #   Based on 1. transistor size. 2. Fanout
    #   The wire load module varies.
    #    It will take default wire module. It is not accurate delay but it gives   #    some approx
values.
    #

    #4. Drive cell or Input Transistion.

    ##############################################################################
#####

    set_operating_conditions tt0p8v125c
    #set_operating_conditions -min ff0p88v125c -max ss0p6v125c

    link

    ## Generating intermediate technology independet (GTECH) design ###########
    ############### Architecture Mapped File ###################################
    # invoke gui to check what architecture it has done
    write_file -format verilog -output ./Simple_Processor_gtech.vs

    # Like Linting problems.
    # Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
    # check design quality.

    check_design

    ##############################################################################
######
    ########################## Set Design Constraints ############################

    source ./constraints_processor.sdc

    check_timing

    set_wire_load_model -name "8000"
    set_wire_load_mode segmented

    #compile_ultra
    #compile_ultra -no_autoungroup -gate_clock

    #set_fix_multiple_port_nets –all –buffer_constants
    read_saif        -input        ./Simple_Processor_SAIF_Move_Operation.saif        -instance
simple_processor_testbench_mv_op/T3
    #testbench_filename/instance of top_module
```

```
compile_ultra -no_autoungroup
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 2. SDC script for Multi_Vth for Tclk=10ns

```
#set sdc_version 2.1

reset_design

set PERIOD  10.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]
```

```
set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay  -clock "clock" -max $INPUT_DELAY  $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay  -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]

set REFLIB saed14rvt_tt0p8v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN
$INPUTPORTS

#set_driving_cell -library $REFLIB \
            -lib_cell $BUFFER \
            -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
```

```
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

### 3. Report of QOR for Multi_Vth for Tclk=10ns

```
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 01:06:56 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:              10.00
  Critical Path Length:          0.83
  Critical Path Slack:           9.02
  Critical Path Clk Period:     10.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:         -0.08
  Total Hold Violation:         -6.11
  No. of Hold Violations:       96.00
  -----------------------------------

  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:               4.00
  Critical Path Length:          0.15
  Critical Path Slack:           8.70
  Critical Path Clk Period:     10.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:         79
```

```
Hierarchical Port Count:        840
Leaf Cell Count:                532
Buf/Inv Cell Count:              40
Buf Cell Count:                   5
Inv Cell Count:                  35
CT Buf/Inv Cell Count:            0
Combinational Cell Count:       394
Sequential Cell Count:          138
Macro Count:                      0
-----------------------------------


Area
-----------------------------------
Combinational Area:      143.678401
Noncombinational Area:   115.928398
Buf/Inv Area:              7.548000
Total Buffer Area:             1.33
Total Inverter Area:           6.22
Macro/Black Box Area:      0.000000
Net Area:                258.443912
-----------------------------------
Cell Area:               259.606798
Design Area:               518.050710


Design Rules
-----------------------------------
Total Number of Nets:           547
Nets With Violations:             0
Max Trans Violations:             0
Max Cap Violations:               0
-----------------------------------


Hostname: synopsysserver

Compile CPU Statistics
---------------------------------------
Resource Sharing:                 0.17
Logic Optimization:               3.91
Mapping Optimization:            16.98
---------------------------------------
Overall Compile Time:            95.94
Overall Compile Wall Clock Time:    97.07
```

---

Design WNS: 0.00 TNS: 0.00 Number of Violating Paths: 0

Design (Hold) WNS: 0.08 TNS: 6.11 Number of Violating Paths: 96

---

1
dc_shell> exit

Thank you...

## 4. Tickle Script for Multi-Vth of saed14rvt_tt0p8v125c, saed14rvt_ss0p72v125c and saed14rvt_ff0p88v125c. Clock Period = 5ns

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.

set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries
```

```
set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db"


##########################################################################
# Logical Library Settings
##########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


######################## Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #      previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#   It will take default wire module. It is not accurate delay but it gives   #   some approx values.
#

#4. Drive cell or Input Transistion.

##########################################################################
###

set_operating_conditions ss0p72v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c
```

```
link

## Generating intermediate technology independet (GTECH) design ###########
################ Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs

# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
# check design quality.

check_design

#############################################################################
####
########################### Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and
report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
```

```
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 5. SDC Script for Multi_Vth fot Tclk=5ns

```
#set sdc_version 2.1
reset_design

set PERIOD  5.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]
```

```
set_input_delay  -clock "clock" -max $INPUT_DELAY  $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay  -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]

set REFLIB saed14rvt_tt0p8v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
        -lib_cell $BUFFER \
        -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 6. Report of QOR for Multi-Vth for T=5ns

```
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 10:08:18 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:              10.00
  Critical Path Length:          0.83
  Critical Path Slack:           4.02
  Critical Path Clk Period:      5.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:         -0.08
  Total Hold Violation:         -6.11
  No. of Hold Violations:       96.00
```

---

Timing Path Group 'INPUTS'
---
Levels of Logic: 4.00
Critical Path Length: 0.15
Critical Path Slack: 3.70
Critical Path Clk Period: 5.00
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00
---

Cell Count
---
Hierarchical Cell Count: 79
Hierarchical Port Count: 840
Leaf Cell Count: 532
Buf/Inv Cell Count: 40
Buf Cell Count: 5
Inv Cell Count: 35
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 394
Sequential Cell Count: 138
Macro Count: 0
---

Area
---
Combinational Area: 143.678401
Noncombinational Area: 115.928398
Buf/Inv Area: 7.548000
Total Buffer Area: 1.33
Total Inverter Area: 6.22
Macro/Black Box Area: 0.000000
Net Area: 258.443912
---
Cell Area: 259.606798
Design Area: 518.050710

Design Rules
---
Total Number of Nets: 547
Nets With Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0
---

Hostname: synopsysserver

```
 Compile CPU Statistics
 ---------------------------------------
 Resource Sharing:                0.16
 Logic Optimization:              3.91
 Mapping Optimization:            16.48
 ---------------------------------------
 Overall Compile Time:            93.82
 Overall Compile Wall Clock Time:    94.88

 --------------------------------------------------------------------

 Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


 Design (Hold)  WNS: 0.08  TNS: 6.11  Number of Violating Paths: 96

 --------------------------------------------------------------------
1
dc_shell> exit

Thank you...
```

## 7. Tickle Script for Multi-Vth of saed14rvt_tt0p8v125c, saed14rvt_ss0p72v125c and saed14rvt_ff0p88v125c. Clock Period = 1ns

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.
```

```
set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"


##########################################################################
# Logical Library Settings
##########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


######################## Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #      previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#   It will take default wire module. It is not accurate delay but it gives   #   some approx values.
#

#4. Drive cell or Input Transistion.
```

```
################################################################################
###

set_operating_conditions ff0p88v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c

link

## Generating intermediate technology independet (GTECH) design ###########
############### Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs

# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
# check design quality.

check_design

################################################################################
####
########################## Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
```

```
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 8. SDC Script for Multi_Vth for Tclk=1ns

```
#set sdc_version 2.1
reset_design

set PERIOD  1.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1
```

```
group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ff0p88v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
            -lib_cell $BUFFER \
            -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 9. QOR Script for Multi_Vth for Tclk=1ns

```
dc_shell>
****************************************
Report : qor
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 11:24:42 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:              11.00
  Critical Path Length:          0.84
  Critical Path Slack:           0.00
  Critical Path Clk Period:      1.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
```

Worst Hold Violation: -0.09
Total Hold Violation: -6.47
No. of Hold Violations: 97.00
---

Timing Path Group 'INPUTS'
---
Levels of Logic: 5.00
Critical Path Length: 0.34
Critical Path Slack: -0.49
Critical Path Clk Period: 1.00
Total Negative Slack: -29.47
No. of Violating Paths: 95.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00
---

Cell Count
---
Hierarchical Cell Count: 79
Hierarchical Port Count: 840
Leaf Cell Count: 515
Buf/Inv Cell Count: 39
Buf Cell Count: 6
Inv Cell Count: 33
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 377
Sequential Cell Count: 138
Macro Count: 0
---

Area
---
Combinational Area: 141.236401
Noncombinational Area: 116.816398
Buf/Inv Area: 7.459200
Total Buffer Area: 1.60
Total Inverter Area: 5.86
Macro/Black Box Area: 0.000000
Net Area: 256.073023
---
Cell Area: 258.052799
Design Area: 514.125822

Design Rules
---
Total Number of Nets: 538
Nets With Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0
---

Hostname: synopsysserver

Compile CPU Statistics
---
Resource Sharing: 0.15
Logic Optimization: 0.61
Mapping Optimization: 5.03
---
Overall Compile Time: 68.53
Overall Compile Wall Clock Time: 69.30

---

Design WNS: 0.49 TNS: 29.47 Number of Violating Paths: 95

Design (Hold) WNS: 0.09 TNS: 6.47 Number of Violating Paths: 97

---

**Date:4/5/2022**

**Power Optimization Power and Slack Table for RVT with three corners (TT, SS and FF) for Move Operation:**

**Temp = $125^0$C fixed**

| **Constraints** | **MVT @ Tclk = 10ns** | **MVT @ Tclk = 5ns** | **MVT @ Tclk = 1ns** |
|---|---|---|---|
| **Cell Area** | 259 | 259 | 258 |
| **Total Area** | 518 | 518 | 514 |
| **Dynamic Power** | 4.12 nW | 8.24 nW | 41.23 nW |
| **Cell Leakage** | 2.57 uW | 2.57 uW | 2.64 uW |
| **Total Power** | 2.33 uW | 2.33 uW | 2.43 uW |
| **Slack** | 8.7 | 3.7 | -0.49 |

The Process Corners FF is best case because High Vdd and Temp = $125^0$C and RVT library is fixed. The Power consumption is more in case of ff0p88v125c compared to rest.

The speed for process corners.

SS: NMOS slow, PMOS slow.
FF: NMOS fast, PMOS fast.
TT: NMOS typical, PMOS typical.

We observe from the Table that at T=1ns we get setup violation i.e.; we get negative slack values. To remove this, we go for Timing Optimization by varying weight of the path group and minimizing the critical range value we remove the setup violation.

**Date:4/5/2022**

# Section 2 Timing Optimization

**Aim:** Synopsys Design Complier used for Logic Optimization and Power Optimization of Simple Processor.

**Script used for Timing optimization of Architecture Design of Simple Processor:**

1. **Tickle Script for Multi-Vth of saed14rvt_tt0p8v125c, saed14rvt_ss0p72v125c and saed14rvt_ff0p88v125c. Clock Period = 1ns**

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.

set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"


##########################################################################
# Logical Library Settings
```

```
#########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


####################### Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #      previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#   It will take default wire module. It is not accurate delay but it gives   #   some approx values.
#

#4. Drive cell or Input Transistion.

#########################################################################
###

set_operating_conditions ff0p88v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c

link

## Generating intermediate technology independet (GTECH) design ###########
############### Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs
```

```
# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
# check design quality.

check_design

################################################################################
####
########################## Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup -incremental
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and
report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 2. SDC Script for Multi_Vth for Tclk=1ns

```
#set sdc_version 2.1
reset_design

set PERIOD  1.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS
```

```
#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ff0p88v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
            -lib_cell $BUFFER \
            -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 3. QOR Script for Multi_Vth for Tclk=1ns

```
dc_shell>
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 11:24:42 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:              11.00
  Critical Path Length:          0.84
  Critical Path Slack:           0.00
  Critical Path Clk Period:      1.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:         -0.09
  Total Hold Violation:         -6.47
  No. of Hold Violations:       97.00
  -----------------------------------

  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:               5.00
  Critical Path Length:          0.34
  Critical Path Slack:          -0.49
  Critical Path Clk Period:      1.00
```

```
Total Negative Slack:        -29.47
No. of Violating Paths:       95.00
Worst Hold Violation:          0.00
Total Hold Violation:          0.00
No. of Hold Violations:        0.00
----------------------------------


Cell Count
----------------------------------
Hierarchical Cell Count:         79
Hierarchical Port Count:        840
Leaf Cell Count:                515
Buf/Inv Cell Count:              39
Buf Cell Count:                   6
Inv Cell Count:                  33
CT Buf/Inv Cell Count:            0
Combinational Cell Count:       377
Sequential Cell Count:          138
Macro Count:                      0
----------------------------------


Area
----------------------------------
Combinational Area:      141.236401
Noncombinational Area:   116.816398
Buf/Inv Area:              7.459200
Total Buffer Area:             1.60
Total Inverter Area:           5.86
Macro/Black Box Area:      0.000000
Net Area:                256.073023
----------------------------------
Cell Area:               258.052799
Design Area:             514.125822


Design Rules
----------------------------------
Total Number of Nets:           538
Nets With Violations:             0
Max Trans Violations:             0
Max Cap Violations:               0
----------------------------------


Hostname: synopsysserver

Compile CPU Statistics
---------------------------------------
Resource Sharing:                 0.15
Logic Optimization:               0.61
Mapping Optimization:             5.03
---------------------------------------
Overall Compile Time:            68.53
Overall Compile Wall Clock Time:    69.30
```

```
---------------------------------------------------------------

Design  WNS: 0.49  TNS: 29.47  Number of Violating Paths: 95


Design (Hold)  WNS: 0.09  TNS: 6.47  Number of Violating Paths: 97

---------------------------------------------------------------

1
dc_shell> exit

Thank you...
```

## 4. Timing Report for T = 1ns.

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 11:24:05 2022
****************************************

Operating Conditions: tt0p8v125c   Library: saed14hvt_tt0p8v125c
Wire Load Model Mode: segmented

  Startpoint: G8/G2_Datapath/A5/dout_reg[1]
              (rising edge-triggered flip-flop clocked by clock)
  Endpoint: G8/G2_Datapath/g2/Z_reg[6]
            (rising edge-triggered flip-flop clocked by clock)
  Path Group: CLOCK
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  Register_8         ForQA                 saed14hvt_tt0p8v125c
  Register_7         ForQA                 saed14hvt_tt0p8v125c
  Register_6         ForQA                 saed14hvt_tt0p8v125c
  Register_5         ForQA                 saed14hvt_tt0p8v125c
  Register_4         ForQA                 saed14hvt_tt0p8v125c
  Register_3         ForQA                 saed14hvt_tt0p8v125c
  Register_2         ForQA                 saed14hvt_tt0p8v125c
  Register_1         ForQA                 saed14hvt_tt0p8v125c
  Register_0         ForQA                 saed14hvt_tt0p8v125c
  reg_G              ForQA                 saed14hvt_tt0p8v125c
  datapath_register_array
                     8000                  saed14hvt_tt0p8v125c
  controller_new     ForQA                 saed14hvt_tt0p8v125c
  simple_processor_Top_Top
                     8000                  saed14hvt_tt0p8v125c
  simple_processor_Top
```

```
                8000                saed14hvt_tt0p8v125c
  half_adder_32      ForQA                saed14hvt_tt0p8v125c
  half_adder_24      ForQA                saed14hvt_tt0p8v125c
  full_adder_16      ForQA                saed14hvt_tt0p8v125c
  full_adder_12      ForQA                saed14hvt_tt0p8v125c
  ripple_carry_4_bit_3
                ForQA                saed14hvt_tt0p8v125c
  ripple_carry_4_bit_0
                ForQA                saed14hvt_tt0p8v125c
  carry_select_adder_4bit_slice_0
                ForQA                saed14hvt_tt0p8v125c
  csa_9bit           ForQA                saed14hvt_tt0p8v125c
  Add_Sub            ForQA                saed14hvt_tt0p8v125c
  half_adder_23      ForQA                saed14hvt_tt0p8v125c
  half_adder_21      ForQA                saed14hvt_tt0p8v125c
  full_adder_11      ForQA                saed14hvt_tt0p8v125c
  half_adder_19      ForQA                saed14hvt_tt0p8v125c
  full_adder_10      ForQA                saed14hvt_tt0p8v125c
  half_adder_17      ForQA                saed14hvt_tt0p8v125c
  full_adder_9       ForQA                saed14hvt_tt0p8v125c
  mux2X1_1_0         ForQA                saed14hvt_tt0p8v125c
  mux2X1_1           ForQA                saed14hvt_tt0p8v125c
  carry_select_adder_4bit_slice_1
                ForQA                saed14hvt_tt0p8v125c

  Point                                       Incr       Path
  ------------------------------------------------------------------------------
  clock clock (rise edge)                           0.00       0.00
  clock network delay (ideal)                       2.00       2.00
  G8/G2_Datapath/A5/dout_reg[1]/CK (SAEDHVT14_FDP_V2LP_0P5)
                                              0.00       2.00 r
  G8/G2_Datapath/A5/dout_reg[1]/Q (SAEDHVT14_FDP_V2LP_0P5)
                                              0.07       2.07 r
  G8/G2_Datapath/A5/dout[1] (Register_1)            0.00       2.07 r
  G8/G2_Datapath/add_top/A[1] (Add_Sub)             0.00       2.07 r
  G8/G2_Datapath/add_top/add1/a[1] (csa_9bit)       0.00       2.07 r
  G8/G2_Datapath/add_top/add1/csa_slice1/a[0] (carry_select_adder_4bit_slice_0)
                                              0.00       2.07 r
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/a[0] (ripple_carry_4_bit_3)
                                              0.00       2.07 r
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/a (full_adder_12)
                                              0.00       2.07 r
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h1/a (half_adder_24)
                                              0.00       2.07 r
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h1/U1/X
(SAEDHVT14_EO2_V1_0P75)
                                              0.11       2.17 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h1/sum (half_adder_24)
                                              0.00       2.17 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h2/a (half_adder_23)
                                              0.00       2.17 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h2/cout (half_adder_23)
                                              0.00       2.17 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/U1/X (SAEDHVT14_OR2_MM_0P5)
                                              0.06       2.24 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/cout (full_adder_12)
```

```
                                  0.00       2.24 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/cin (full_adder_11)
                                  0.00       2.24 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/h2/b (half_adder_21)
                                  0.00       2.24 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/h2/U2/X
(SAEDHVT14_AN2_MM_0P5)
                                  0.05       2.29 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/h2/cout (half_adder_21)
                                  0.00       2.29 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/U1/X (SAEDHVT14_OR2_MM_0P75)
                                  0.04       2.33 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/cout (full_adder_11)
                                  0.00       2.33 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/cin (full_adder_10)
                                  0.00       2.33 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/h2/b (half_adder_19)
                                  0.00       2.33 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/h2/U2/X (SAEDHVT14_AN2_MM_1)
                                  0.05       2.38 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/h2/cout (half_adder_19)
                                  0.00       2.38 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/U1/X (SAEDHVT14_OR2_MM_0P75)
                                  0.04       2.42 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/cout (full_adder_10)
                                  0.00       2.42 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/cin (full_adder_9)
                                  0.00       2.42 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/h2/b (half_adder_17)
                                  0.00       2.42 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/h2/U2/X (SAEDHVT14_AN2_MM_1)
                                  0.05       2.47 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/h2/cout (half_adder_17)
                                  0.00       2.47 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/U1/X (SAEDRVT14_OR2_0P5)
                                  0.04       2.51 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/cout (full_adder_9)
                                  0.00       2.51 f
  G8/G2_Datapath/add_top/add1/csa_slice1/rca2/cout (ripple_carry_4_bit_3)
                                  0.00       2.51 f
  G8/G2_Datapath/add_top/add1/csa_slice1/mc0/in1 (mux2X1_1_0)
                                  0.00       2.51 f
  G8/G2_Datapath/add_top/add1/csa_slice1/mc0/U1/X (SAEDHVT14_MUX2_1)
                                  0.10       2.60 f
  G8/G2_Datapath/add_top/add1/csa_slice1/mc0/out (mux2X1_1_0)
                                  0.00       2.60 f
  G8/G2_Datapath/add_top/add1/csa_slice1/cout (carry_select_adder_4bit_slice_0)
                                  0.00       2.60 f
  G8/G2_Datapath/add_top/add1/csa_slice2/cin (carry_select_adder_4bit_slice_1)
                                  0.00       2.60 f
  G8/G2_Datapath/add_top/add1/csa_slice2/ms0/sel (mux2X1_1)
                                  0.00       2.60 f
  G8/G2_Datapath/add_top/add1/csa_slice2/ms0/U3/X (SAEDHVT14_MUX2_MM_1)
                                  0.06       2.66 r
  G8/G2_Datapath/add_top/add1/csa_slice2/ms0/out[1] (mux2X1_1)
                                  0.00       2.66 r
```

```
G8/G2_Datapath/add_top/add1/csa_slice2/sum[1] (carry_select_adder_4bit_slice_1)
                                          0.00       2.66 r
G8/G2_Datapath/add_top/add1/sum[6] (csa_9bit)          0.00       2.66 r
G8/G2_Datapath/add_top/ALU_out[6] (Add_Sub)            0.00       2.66 r
G8/G2_Datapath/g2/Sum[6] (reg_G)                       0.00       2.66 r
G8/G2_Datapath/g2/U8/X (SAEDHVT14_AO32_1)              0.17       2.83 r
G8/G2_Datapath/g2/Z_reg[6]/D (SAEDHVT14_FDP_V2_0P5)    0.01       2.84 r
data arrival time                                                 2.84

clock clock (rise edge)                                1.00       1.00
clock network delay (ideal)                            2.00       3.00
clock uncertainty                                     -0.15       2.85
G8/G2_Datapath/g2/Z_reg[6]/CK (SAEDHVT14_FDP_V2_0P5)
                                          0.00       2.85 r
library setup time                                    0.00       2.85
data required time                                               2.85
--------------------------------------------------------------------------------
data required time                                               2.85
data arrival time                                               -2.84
--------------------------------------------------------------------------------
slack (MET)                                                      0.00


Startpoint: Resetn (input port clocked by clock)
Endpoint: G8/G2_Datapath/g2/Z_reg[2]
        (rising edge-triggered flip-flop clocked by clock)
Path Group: INPUTS
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
datapath_register_array
                   8000                  saed14hvt_tt0p8v125c
controller_new     ForQA                 saed14hvt_tt0p8v125c
simple_processor_Top_Top
                   8000                  saed14hvt_tt0p8v125c
simple_processor_Top
                   8000                  saed14hvt_tt0p8v125c
Register_5         ForQA                 saed14hvt_tt0p8v125c
Register_2         ForQA                 saed14hvt_tt0p8v125c
reg_G              ForQA                 saed14hvt_tt0p8v125c

Point                                             Incr       Path
--------------------------------------------------------------------------------
clock clock (rise edge)                           0.00       0.00
clock network delay (ideal)                       2.00       2.00
input external delay                              1.00       3.00 r
Resetn (in)                                       0.00       3.00 r
G8/Resetn (simple_processor_Top)                  0.00       3.00 r
G8/G2_Datapath/rst (datapath_register_array)      0.00       3.00 r
G8/G2_Datapath/U3/X (SAEDHVT14_BUF_S_0P5)         0.08       3.08 r
G8/G2_Datapath/g2/rst (reg_G)                     0.00       3.08 r
G8/G2_Datapath/g2/U9/X (SAEDHVT14_BUF_U_0P5)      0.06       3.14 r
G8/G2_Datapath/g2/U12/X (SAEDHVT14_ND2B_U_0P5)    0.08       3.23 f
G8/G2_Datapath/g2/U11/X (SAEDHVT14_INV_0P5)       0.07       3.29 r
G8/G2_Datapath/g2/U4/X (SAEDHVT14_AO32_1)         0.04       3.33 r
```

G8/G2_Datapath/g2/Z_reg[2]/D (SAEDHVT14_FDP_V2_0P5) 0.01 3.34 r
data arrival time 3.34

clock clock (rise edge) 1.00 1.00
clock network delay (ideal) 2.00 3.00
clock uncertainty -0.15 2.85
G8/G2_Datapath/g2/Z_reg[2]/CK (SAEDHVT14_FDP_V2_0P5)
0.00 2.85 r
library setup time 0.00 2.85
data required time 2.85
---
data required time 2.85
data arrival time -3.34
---
slack (VIOLATED) -0.49

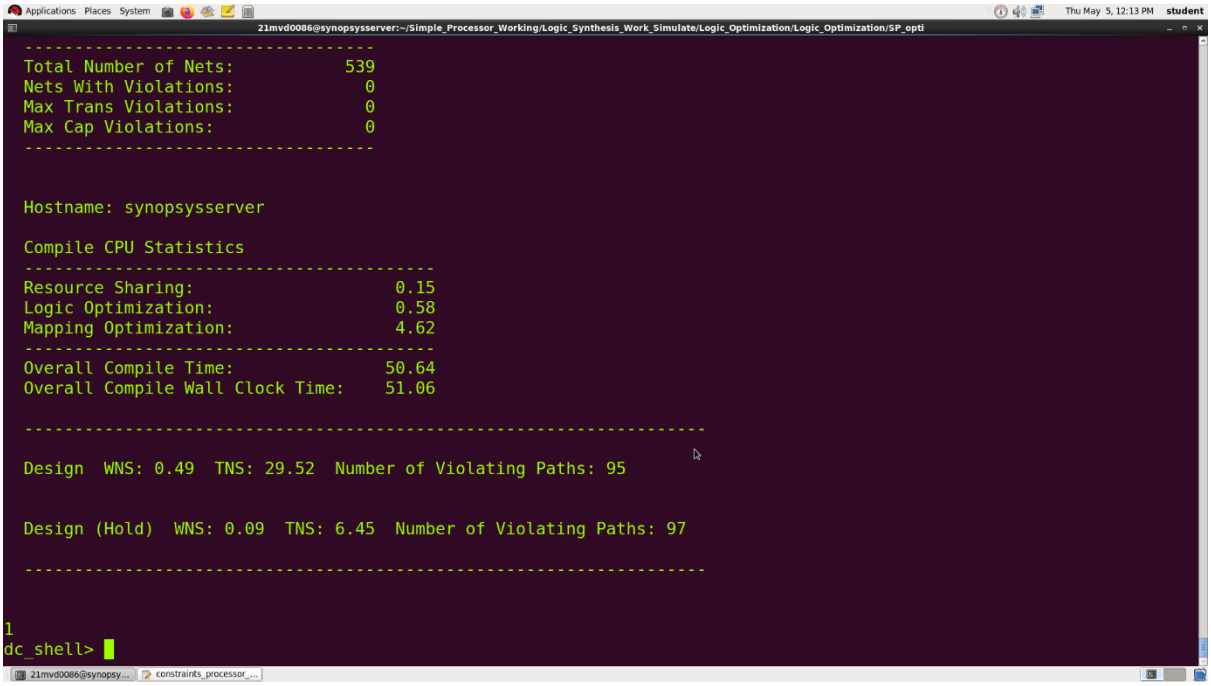


**Figure 2.1** The figure represents the Number of Setup and Hold violation path for T=1ns before Timing Optimization.

The Timing Optimization is done by changing the Weight of the path group of INPUT and changing the critical range value.

## 5. Tickle Script for Multi-Vth of saed14rvt_tt0p8v125c, saed14rvt_ss0p72v125c and saed14rvt_ff0p88v125c. Clock Period = 1ns

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.

set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"


##########################################################################
# Logical Library Settings
##########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3
```

```
set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


######################## Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #       previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#   It will take default wire module. It is not accurate delay but it gives   #   some approx values.
#

#4. Drive cell or Input Transistion.

#########################################################################
###

set_operating_conditions ff0p88v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c

link

## Generating intermediate technology independet (GTECH) design ###########
############### Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs

# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
```

```
# check design quality.

check_design

################################################################################
####
########################## Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup -incremental
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and
report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 6. SDC Script for Multi_Vth for Tclk=1ns

```
#set sdc_version 2.1
reset_design

set PERIOD  1.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5
set_critical_range 0.1 $current_design


## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 50

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS
```

```
#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ff0p88v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
        -lib_cell $BUFFER \
        -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 7. QOR Script for Multi_Vth for Tclk=1ns

```
dc_shell>
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 11:24:42 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:              11.00
  Critical Path Length:          0.84
  Critical Path Slack:           0.00
  Critical Path Clk Period:      1.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:         -0.09
  Total Hold Violation:         -6.47
  No. of Hold Violations:       97.00
  -----------------------------------

  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:              5.00
  Critical Path Length:         0.34
  Critical Path Slack:         -0.49
  Critical Path Clk Period:     1.00
```

```
Total Negative Slack:        -29.47
No. of Violating Paths:       95.00
Worst Hold Violation:          0.00
Total Hold Violation:          0.00
No. of Hold Violations:        0.00
----------------------------------


Cell Count
----------------------------------
Hierarchical Cell Count:         79
Hierarchical Port Count:        840
Leaf Cell Count:                515
Buf/Inv Cell Count:              39
Buf Cell Count:                   6
Inv Cell Count:                  33
CT Buf/Inv Cell Count:            0
Combinational Cell Count:       377
Sequential Cell Count:          138
Macro Count:                      0
----------------------------------


Area
----------------------------------
Combinational Area:      141.236401
Noncombinational Area:   116.816398
Buf/Inv Area:              7.459200
Total Buffer Area:             1.60
Total Inverter Area:           5.86
Macro/Black Box Area:      0.000000
Net Area:                256.073023
----------------------------------
Cell Area:               258.052799
Design Area:             514.125822


Design Rules
----------------------------------
Total Number of Nets:           538
Nets With Violations:             0
Max Trans Violations:             0
Max Cap Violations:               0
----------------------------------


Hostname: synopsysserver

Compile CPU Statistics
---------------------------------------
Resource Sharing:                 0.15
Logic Optimization:               0.61
Mapping Optimization:             5.03
---------------------------------------
Overall Compile Time:            68.53
Overall Compile Wall Clock Time:    69.30
```

```
---------------------------------------------------------------

Design  WNS: 0.49  TNS: 29.47  Number of Violating Paths: 95


Design (Hold)  WNS: 0.09  TNS: 6.47  Number of Violating Paths: 97

---------------------------------------------------------------

1
dc_shell> exit
```

## 8. Report Timing

```
****************************************
Report : timing
-path full
-delay max
-max_paths 1
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 14:57:33 2022
****************************************

Operating Conditions: tt0p8v125c   Library: saed14hvt_tt0p8v125c
Wire Load Model Mode: segmented

Startpoint: Run (input port clocked by clock)
Endpoint: G8/G1_Controller/PS_reg[0]
(rising edge-triggered flip-flop clocked by clock)
Path Group: INPUTS
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
controller_new     ForQA                 saed14hvt_tt0p8v125c
simple_processor_Top_Top
8000               saed14hvt_tt0p8v125c
simple_processor_Top
8000               saed14hvt_tt0p8v125c
```

| Point | Incr | Path |
|---|---|---|
| clock clock (rise edge) | 0.00 | 0.00 |
| clock network delay (ideal) | 2.00 | 2.00 |
| input external delay | 1.00 | 3.00 f |
| Run (in) | 0.00 | 3.00 f |
| G8/Run (simple_processor_Top) | 0.00 | 3.00 f |
| G8/G1_Controller/Run (controller_new) | 0.00 | 3.00 f |
| G8/G1_Controller/U51/X (SAEDHVT14_ND2_CDC_0P5) | 0.04 | 3.04 r |
| G8/G1_Controller/U58/X (SAEDHVT14_INV_0P5) | 0.04 | 3.08 f |

| | | |
|---|---|---|
| G8/G1_Controller/U60/X (SAEDHVT14_NR2_MM_0P5) | 0.03 | 3.12 r |
| G8/G1_Controller/U62/X (SAEDHVT14_OR4_1) | 0.03 | 3.14 r |
| G8/G1_Controller/PS_reg[0]/D (SAEDHVT14_FDP_V2LP_0P5) | 0.01 | 3.15 r |
| data arrival time | | 3.15 |
| | | |
| clock clock (rise edge) | 1.00 | 1.00 |
| clock network delay (ideal) | 2.00 | 3.00 |
| clock uncertainty | -0.15 | 2.85 |
| G8/G1_Controller/PS_reg[0]/CK (SAEDHVT14_FDP_V2LP_0P5) | 0.00 | 2.85 r |
| library setup time | 0.00 | 2.85 |
| data required time | | 2.85 |
| --- | | |
| data required time | | 2.85 |
| data arrival time | | -3.15 |
| --- | | |
| slack (VIOLATED) | | -0.30 |

Startpoint: G8/G2_Datapath/A5/dout_reg[5]
(rising edge-triggered flip-flop clocked by clock)
Endpoint: G8/G2_Datapath/g2/Z_reg[8]
(rising edge-triggered flip-flop clocked by clock)
Path Group: CLOCK
Path Type: max

Des/Clust/Port Wire Load Model Library
---
Register_7 ForQA saed14hvt_tt0p8v125c
Register_6 ForQA saed14hvt_tt0p8v125c
Register_5 ForQA saed14hvt_tt0p8v125c
Register_4 ForQA saed14hvt_tt0p8v125c
Register_3 ForQA saed14hvt_tt0p8v125c
Register_2 ForQA saed14hvt_tt0p8v125c
Register_1 ForQA saed14hvt_tt0p8v125c
Register_0 ForQA saed14hvt_tt0p8v125c
Register_8 ForQA saed14hvt_tt0p8v125c
reg_G ForQA saed14hvt_tt0p8v125c
datapath_register_array
8000 saed14hvt_tt0p8v125c
controller_new ForQA saed14hvt_tt0p8v125c
simple_processor_Top_Top
8000 saed14hvt_tt0p8v125c
simple_processor_Top
8000 saed14hvt_tt0p8v125c
half_adder_15 ForQA saed14hvt_tt0p8v125c
half_adder_7 ForQA saed14hvt_tt0p8v125c
full_adder_7 ForQA saed14hvt_tt0p8v125c
full_adder_3 ForQA saed14hvt_tt0p8v125c
ripple_carry_4_bit_1
ForQA saed14hvt_tt0p8v125c
ripple_carry_4_bit_0
ForQA saed14hvt_tt0p8v125c
carry_select_adder_4bit_slice_0
ForQA saed14hvt_tt0p8v125c

```
csa_9bit          ForQA              saed14hvt_tt0p8v125c
Add_Sub           ForQA              saed14hvt_tt0p8v125c
half_adder_6      ForQA              saed14hvt_tt0p8v125c
half_adder_4      ForQA              saed14hvt_tt0p8v125c
full_adder_2      ForQA              saed14hvt_tt0p8v125c
half_adder_2      ForQA              saed14hvt_tt0p8v125c
full_adder_1      ForQA              saed14hvt_tt0p8v125c
half_adder_0      ForQA              saed14hvt_tt0p8v125c
full_adder_0      ForQA              saed14hvt_tt0p8v125c
mux2X1_0          ForQA              saed14hvt_tt0p8v125c

Point                                   Incr       Path
---------------------------------------------------------------------------
clock clock (rise edge)                 0.00       0.00
clock network delay (ideal)             2.00       2.00
G8/G2_Datapath/A5/dout_reg[5]/CK (SAEDHVT14_FDP_V2LP_0P5)
0.00       2.00 r
G8/G2_Datapath/A5/dout_reg[5]/Q (SAEDHVT14_FDP_V2LP_0P5)
0.06       2.06 f
G8/G2_Datapath/A5/dout[5] (Register_0)          0.00       2.06 f
G8/G2_Datapath/add_top/A[5] (Add_Sub)           0.00       2.06 f
G8/G2_Datapath/add_top/add1/a[5] (csa_9bit)     0.00       2.06 f
G8/G2_Datapath/add_top/add1/csa_slice2/a[0] (carry_select_adder_4bit_slice_0)
0.00       2.06 f
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/a[0] (ripple_carry_4_bit_0)
0.00       2.06 f
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/a (full_adder_3)
0.00       2.06 f
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/h1/a (half_adder_7)
0.00       2.06 f
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/h1/U1/X (SAEDHVT14_AN2_MM_0P5)
0.08       2.14 f
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/h1/U2/X (SAEDHVT14_OA21B_1)
0.03       2.17 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/h1/sum (half_adder_7)
0.00       2.17 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/h2/a (half_adder_6)
0.00       2.17 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/h2/cout (half_adder_6)
0.00       2.17 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/U2/X (SAEDRVT14_OR2_0P5)
0.05       2.23 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa0/cout (full_adder_3)
0.00       2.23 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa1/cin (full_adder_2)
0.00       2.23 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa1/h2/b (half_adder_4)
0.00       2.23 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa1/h2/U1/X (SAEDHVT14_AN2_MM_0P5)
0.05       2.28 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa1/h2/cout (half_adder_4)
0.00       2.28 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa1/U1/X (SAEDRVT14_OR2_0P5)
0.03       2.31 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa1/cout (full_adder_2)
0.00       2.31 r
```

```
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa2/cin (full_adder_1)
0.00       2.31 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa2/h2/b (half_adder_2)
0.00       2.31 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa2/h2/U1/X (SAEDHVT14_AN2_MM_0P5)
0.05       2.36 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa2/h2/cout (half_adder_2)
0.00       2.36 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa2/U1/X (SAEDRVT14_OR2_0P5)
0.03       2.39 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa2/cout (full_adder_1)
0.00       2.39 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa3/cin (full_adder_0)
0.00       2.39 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa3/h2/b (half_adder_0)
0.00       2.39 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa3/h2/U1/X (SAEDHVT14_EO2_V1_0P75)
0.12       2.51 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa3/h2/sum (half_adder_0)
0.00       2.51 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/fa3/sum (full_adder_0)
0.00       2.51 r
G8/G2_Datapath/add_top/add1/csa_slice2/rca2/sum[3] (ripple_carry_4_bit_0)
0.00       2.51 r
G8/G2_Datapath/add_top/add1/csa_slice2/ms0/in1[3] (mux2X1_0)
0.00       2.51 r
G8/G2_Datapath/add_top/add1/csa_slice2/ms0/U4/X (SAEDHVT14_MUX2_U_0P5)
0.13       2.64 r
G8/G2_Datapath/add_top/add1/csa_slice2/ms0/out[3] (mux2X1_0)
0.00       2.64 r
G8/G2_Datapath/add_top/add1/csa_slice2/sum[3] (carry_select_adder_4bit_slice_0)
0.00       2.64 r
G8/G2_Datapath/add_top/add1/sum[8] (csa_9bit)          0.00       2.64 r
G8/G2_Datapath/add_top/ALU_out[8] (Add_Sub)            0.00       2.64 r
G8/G2_Datapath/g2/Sum[8] (reg_G)                       0.00       2.64 r
G8/G2_Datapath/g2/U11/X (SAEDHVT14_OA221_U_0P5)        0.17       2.81 r
G8/G2_Datapath/g2/Z_reg[8]/D (SAEDHVT14_FDP_V2LP_0P5)
0.01       2.82 r
data arrival time                                      2.82

clock clock (rise edge)                        1.00       1.00
clock network delay (ideal)                    2.00       3.00
clock uncertainty                             -0.15       2.85
G8/G2_Datapath/g2/Z_reg[8]/CK (SAEDHVT14_FDP_V2LP_0P5)
0.00       2.85 r
library setup time                             0.00       2.85
data required time                                        2.85
---------------------------------------------------------------------------
data required time                                        2.85
data arrival time                                        -2.82
---------------------------------------------------------------------------
slack (MET)                                               0.03
```

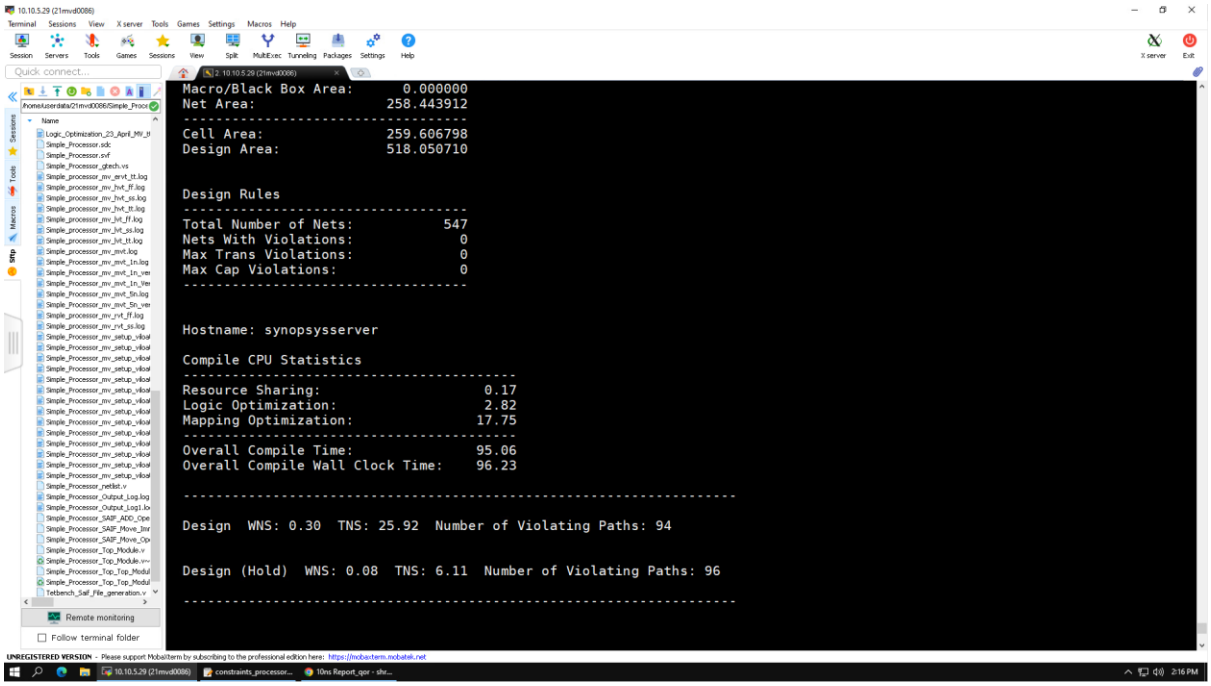


**Figure 2.2** The figure represents the Number of Setup and Hold violation path for T=1ns after Timing Optimization with vary in weight value and critical range value.

The changing of Input delay, Output delay Source Latency, Clock latency, Weight of INPUT path group, setting Critical range to 0.0 by doing these changes eliminated the Whole Setup Violation.

## 9. Tickle Script for Multi-Vth of saed14rvt_tt0p8v125c, saed14rvt_ss0p72v125c and saed14rvt_ff0p88v125c. Clock Period = 1ns

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
```

```
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.

set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"


##########################################################################
# Logical Library Settings
##########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


######################## Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #      previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
```

```
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#   It will take default wire module. It is not accurate delay but it gives   #   some approx values.
#

#4. Drive cell or Input Transistion.

################################################################################
###

set_operating_conditions ff0p88v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c

link

## Generating intermediate technology independet (GTECH) design ###########
############### Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs

# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
# check design quality.

check_design

################################################################################
####
########################### Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup -incremental
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
```

```
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 10. SDC Script for Multi_Vth for Tclk=1ns

```
#set sdc_version 2.1
reset_design

set PERIOD  1.0
set INPUT_DELAY  0.5
set OUTPUT_DELAY  0.5
set CLOCK_LATENCY 0.5
set SOURCE_LATENCY 0.5
set UNCERTAINTY 0.10
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5
set_critical_range 0.0 $current_design


## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]
```

```
set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
          -to clock\
          -weight 1

group_path  -name INPUTS\
          -through [all_inputs]\
          -weight 50
          -critical_range 0.0

group_path  -name OUTPUTS\
          -to [all_outputs]\
          -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ff0p88v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
              -lib_cell $BUFFER \
              -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 11. QOR Script for Multi_Vth for Tclk=1ns

dc_shell>

```
dc_shell>
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 11:44:17 2022
****************************************


  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:              5.00
  Critical Path Length:         0.33
  Critical Path Slack:          0.06
  Critical Path Clk Period:     1.00
  Total Negative Slack:         0.00
  No. of Violating Paths:       0.00
  Worst Hold Violation:         0.00
  Total Hold Violation:         0.00
  No. of Hold Violations:       0.00
  -----------------------------------

  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:             11.00
  Critical Path Length:         0.88
  Critical Path Slack:          0.02
  Critical Path Clk Period:     1.00
  Total Negative Slack:         0.00
  No. of Violating Paths:       0.00
  Worst Hold Violation:        -0.04
  Total Hold Violation:        -1.94
  No. of Hold Violations:      85.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:        79
  Hierarchical Port Count:       840
  Leaf Cell Count:               529
  Buf/Inv Cell Count:             43
  Buf Cell Count:                  6
  Inv Cell Count:                 37
  CT Buf/Inv Cell Count:           0
  Combinational Cell Count:      391
  Sequential Cell Count:         138
  Macro Count:                     0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      145.632001
```

```
Noncombinational Area:   120.679201
Buf/Inv Area:            8.169600
Total Buffer Area:           1.60
Total Inverter Area:         6.57
Macro/Black Box Area:     0.000000
Net Area:              267.932246
-----------------------------------
Cell Area:             266.311202
Design Area:           534.243448


Design Rules
-----------------------------------
Total Number of Nets:          549
Nets With Violations:           0
Max Trans Violations:           0
Max Cap Violations:             0
-----------------------------------


Hostname: synopsysserver

Compile CPU Statistics
---------------------------------------
Resource Sharing:                0.15
Logic Optimization:              0.71
Mapping Optimization:            4.62
---------------------------------------
Overall Compile Time:           66.73
Overall Compile Wall Clock Time:    67.58

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.04  TNS: 1.94  Number of Violating Paths: 85

--------------------------------------------------------------------


1
dc_shell> exit

Thank you...
```

## 12. Timing Optimization Script for Multi_Vth for Tclk=1ns

```
****************************************
Report : timing
        -path full
        -delay max
        -max_paths 1
Design : simple_processor_Top_Top
Version: O-2018.06-SP4
Date   : Thu May  5 11:43:30 2022
****************************************

Operating Conditions: tt0p8v125c   Library: saed14hvt_tt0p8v125c
Wire Load Model Mode: segmented

  Startpoint: Resetn (input port clocked by clock)
  Endpoint: G8/G2_Datapath/g2/Z_reg[0]
          (rising edge-triggered flip-flop clocked by clock)
  Path Group: INPUTS
  Path Type: max

  Des/Clust/Port     Wire Load Model       Library
  ------------------------------------------------
  datapath_register_array
                 8000                  saed14hvt_tt0p8v125c
  controller_new     ForQA                 saed14hvt_tt0p8v125c
  simple_processor_Top_Top
                 8000                  saed14hvt_tt0p8v125c
  simple_processor_Top
                 8000                  saed14hvt_tt0p8v125c
  Register_8         ForQA                 saed14hvt_tt0p8v125c
  Register_1         ForQA                 saed14hvt_tt0p8v125c
  reg_G              ForQA                saed14hvt_tt0p8v125c

  Point                                        Incr       Path
  ---------------------------------------------------------------------------
  clock clock (rise edge)                                0.00       0.00
  clock network delay (ideal)                            1.00       1.00
  input external delay                                   0.50       1.50 r
  Resetn (in)                                            0.00       1.50 r
  G8/Resetn (simple_processor_Top)                       0.00       1.50 r
  G8/G2_Datapath/rst (datapath_register_array)           0.00       1.50 r
  G8/G2_Datapath/U1/X (SAEDHVT14_BUF_S_0P5)              0.07       1.57 r
  G8/G2_Datapath/g2/rst (reg_G)                          0.00       1.57 r
  G8/G2_Datapath/g2/U14/X (SAEDHVT14_BUF_U_0P5)          0.06       1.64 r
  G8/G2_Datapath/g2/U12/X (SAEDHVT14_ND2B_U_0P5)         0.08       1.72 f
  G8/G2_Datapath/g2/U11/X (SAEDHVT14_INV_0P5)            0.07       1.79 r
  G8/G2_Datapath/g2/U2/X (SAEDHVT14_AO32_1)              0.04       1.83 r
  G8/G2_Datapath/g2/Z_reg[0]/D (SAEDHVT14_FDPCBQ_V2LP_0P5)
                                                         0.01       1.83 r
  data arrival time                                                 1.83

  clock clock (rise edge)                                1.00       1.00
  clock network delay (ideal)                            1.00       2.00
  clock uncertainty                                     -0.10       1.90
  G8/G2_Datapath/g2/Z_reg[0]/CK (SAEDHVT14_FDPCBQ_V2LP_0P5)
                                                         0.00       1.90 r
```

```
library setup time                          -0.01      1.89
data required time                                     1.89
-----------------------------------------------------------------------------
data required time                                     1.89
data arrival time                                     -1.83
-----------------------------------------------------------------------------
slack (MET)                                            0.06


Startpoint: G8/G2_Datapath/A5/dout_reg[1]
          (rising edge-triggered flip-flop clocked by clock)
Endpoint: G8/G2_Datapath/g2/Z_reg[5]
         (rising edge-triggered flip-flop clocked by clock)
Path Group: CLOCK
Path Type: max

Des/Clust/Port     Wire Load Model       Library
------------------------------------------------
Register_8         ForQA                 saed14hvt_tt0p8v125c
Register_7         ForQA                 saed14hvt_tt0p8v125c
Register_6         ForQA                 saed14hvt_tt0p8v125c
Register_5         ForQA                 saed14hvt_tt0p8v125c
Register_4         ForQA                 saed14hvt_tt0p8v125c
Register_3         ForQA                 saed14hvt_tt0p8v125c
Register_2         ForQA                 saed14hvt_tt0p8v125c
Register_1         ForQA                 saed14hvt_tt0p8v125c
Register_0         ForQA                 saed14hvt_tt0p8v125c
reg_G              ForQA                 saed14hvt_tt0p8v125c
datapath_register_array
                   8000                  saed14hvt_tt0p8v125c
controller_new     ForQA                 saed14hvt_tt0p8v125c
simple_processor_Top_Top
                   8000                  saed14hvt_tt0p8v125c
simple_processor_Top
                   8000                  saed14hvt_tt0p8v125c
half_adder_32      ForQA                 saed14hvt_tt0p8v125c
half_adder_24      ForQA                 saed14hvt_tt0p8v125c
full_adder_16      ForQA                 saed14hvt_tt0p8v125c
full_adder_12      ForQA                 saed14hvt_tt0p8v125c
ripple_carry_4_bit_3
                   ForQA                 saed14hvt_tt0p8v125c
ripple_carry_4_bit_0
                   ForQA                 saed14hvt_tt0p8v125c
carry_select_adder_4bit_slice_0
                   ForQA                 saed14hvt_tt0p8v125c
csa_9bit           ForQA                 saed14hvt_tt0p8v125c
Add_Sub            ForQA                 saed14hvt_tt0p8v125c
half_adder_23      ForQA                 saed14hvt_tt0p8v125c
half_adder_21      ForQA                 saed14hvt_tt0p8v125c
full_adder_11      ForQA                 saed14hvt_tt0p8v125c
half_adder_19      ForQA                 saed14hvt_tt0p8v125c
full_adder_10      ForQA                 saed14hvt_tt0p8v125c
half_adder_17      ForQA                 saed14hvt_tt0p8v125c
full_adder_9       ForQA                 saed14hvt_tt0p8v125c
mux2X1_1_0         ForQA                 saed14hvt_tt0p8v125c
mux2X1_1           ForQA                 saed14hvt_tt0p8v125c
```

```
carry_select_adder_4bit_slice_1
                ForQA               saed14hvt_tt0p8v125c

Point                                       Incr       Path
---------------------------------------------------------------------------
clock clock (rise edge)                     0.00       0.00
clock network delay (ideal)                 1.00       1.00
G8/G2_Datapath/A5/dout_reg[1]/CK (SAEDHVT14_FDPCBQ_V2LP_0P5)
                                            0.00       1.00 r
G8/G2_Datapath/A5/dout_reg[1]/Q (SAEDHVT14_FDPCBQ_V2LP_0P5)
                                            0.07       1.07 r
G8/G2_Datapath/A5/dout[1] (Register_1)      0.00       1.07 r
G8/G2_Datapath/add_top/A[1] (Add_Sub)       0.00       1.07 r
G8/G2_Datapath/add_top/add1/a[1] (csa_9bit) 0.00       1.07 r
G8/G2_Datapath/add_top/add1/csa_slice1/a[0] (carry_select_adder_4bit_slice_0)
                                            0.00       1.07 r
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/a[0] (ripple_carry_4_bit_3)
                                            0.00       1.07 r
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/a (full_adder_12)
                                            0.00       1.07 r
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h1/a (half_adder_24)
                                            0.00       1.07 r
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h1/U1/X
(SAEDHVT14_EO2_V1_0P75)
                                            0.11       1.18 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h1/sum (half_adder_24)
                                            0.00       1.18 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h2/a (half_adder_23)
                                            0.00       1.18 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/h2/cout (half_adder_23)
                                            0.00       1.18 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/U1/X (SAEDHVT14_OR2_0P5)
                                            0.07       1.25 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa0/cout (full_adder_12)
                                            0.00       1.25 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/cin (full_adder_11)
                                            0.00       1.25 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/h2/b (half_adder_21)
                                            0.00       1.25 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/h2/U2/X
(SAEDHVT14_AN2_MM_0P5)
                                            0.05       1.30 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/h2/cout (half_adder_21)
                                            0.00       1.30 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/U1/X (SAEDHVT14_OR2_0P5)
                                            0.04       1.34 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa1/cout (full_adder_11)
                                            0.00       1.34 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/cin (full_adder_10)
                                            0.00       1.34 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/h2/b (half_adder_19)
                                            0.00       1.34 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/h2/U2/X (SAEDHVT14_AN2_1)
                                            0.05       1.39 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/h2/cout (half_adder_19)
                                            0.00       1.39 f
```

```
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/U1/X (SAEDHVT14_OR2_0P5)
                                  0.04       1.44 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa2/cout (full_adder_10)
                                  0.00       1.44 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/cin (full_adder_9)
                                  0.00       1.44 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/h2/b (half_adder_17)
                                  0.00       1.44 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/h2/U2/X (SAEDHVT14_AN2_1)
                                  0.05       1.49 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/h2/cout (half_adder_17)
                                  0.00       1.49 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/U1/X (SAEDHVT14_OR2_0P5)
                                  0.04       1.53 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/fa3/cout (full_adder_9)
                                  0.00       1.53 f
G8/G2_Datapath/add_top/add1/csa_slice1/rca2/cout (ripple_carry_4_bit_3)
                                  0.00       1.53 f
G8/G2_Datapath/add_top/add1/csa_slice1/mc0/in1 (mux2X1_1_0)
                                  0.00       1.53 f
G8/G2_Datapath/add_top/add1/csa_slice1/mc0/U1/X (SAEDHVT14_MUX2_MM_0P5)
                                  0.10       1.64 f
G8/G2_Datapath/add_top/add1/csa_slice1/mc0/out (mux2X1_1_0)
                                  0.00       1.64 f
G8/G2_Datapath/add_top/add1/csa_slice1/cout (carry_select_adder_4bit_slice_0)
                                  0.00       1.64 f
G8/G2_Datapath/add_top/add1/csa_slice2/cin (carry_select_adder_4bit_slice_1)
                                  0.00       1.64 f
G8/G2_Datapath/add_top/add1/csa_slice2/ms0/sel (mux2X1_1)
                                  0.00       1.64 f
G8/G2_Datapath/add_top/add1/csa_slice2/ms0/U4/X (SAEDHVT14_MUX2_MM_0P5)
                                  0.06       1.70 r
G8/G2_Datapath/add_top/add1/csa_slice2/ms0/out[0] (mux2X1_1)
                                  0.00       1.70 r
G8/G2_Datapath/add_top/add1/csa_slice2/sum[0] (carry_select_adder_4bit_slice_1)
                                  0.00       1.70 r
G8/G2_Datapath/add_top/add1/sum[5] (csa_9bit)          0.00       1.70 r
G8/G2_Datapath/add_top/ALU_out[5] (Add_Sub)            0.00       1.70 r
G8/G2_Datapath/g2/Sum[5] (reg_G)                       0.00       1.70 r
G8/G2_Datapath/g2/U7/X (SAEDHVT14_AO32_1)              0.17       1.87 r
G8/G2_Datapath/g2/Z_reg[5]/D (SAEDHVT14_FDPCBQ_V2LP_0P5)
                                  0.01       1.88 r
data arrival time                                    1.88

clock clock (rise edge)                    1.00       1.00
clock network delay (ideal)                1.00       2.00
clock uncertainty                         -0.10       1.90
G8/G2_Datapath/g2/Z_reg[5]/CK (SAEDHVT14_FDPCBQ_V2LP_0P5)
                                  0.00       1.90 r
library setup time                        -0.01       1.89
data required time                                   1.89
--------------------------------------------------------------------------------
data required time                                   1.89
data arrival time                                   -1.88
--------------------------------------------------------------------------------
slack (MET)                                          0.02
```

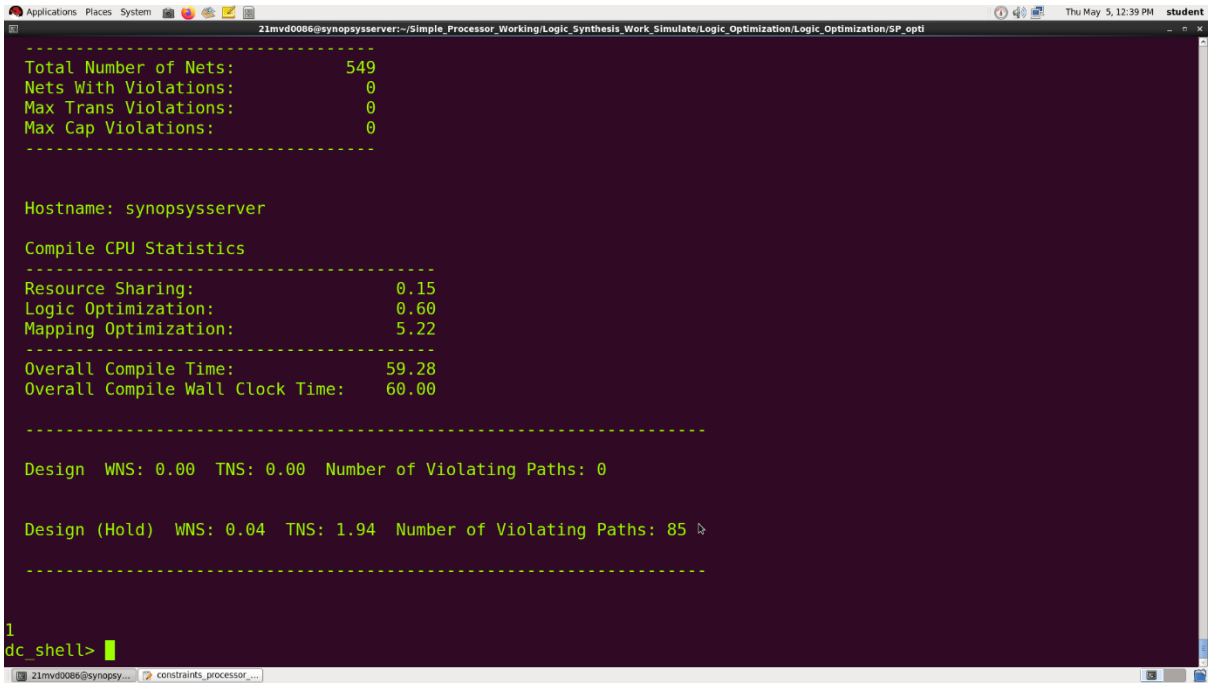


**Figure 2.3** The figure represents the Number of Setup and Hold violation path for T=1ns after Timing Optimization.

## Inference:

1. The Simple Processor 9 bit was designed using Verilog code. The Logic synthesis was done using Synopsys Design Complier tool.
2. The Power Optimization and Timing Optimization is done for 14nm FinFET and target library is for only rvt, lvt and hvt library with TT.
3. The Table represents the variation in power consumption for tt0p8v125c, ss0p72v125c and ff0p88v125c.
4. The Screenshot of report_qor reports Number of path violation and how many paths are reduced by varying the weights of path group. By this we achieving Timing Optimization.