**Date:25/4/2022**


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**ECE5014 – ASIC Design**

**M.Tech VLSI Design**

**School of Electronics Engineering**

**Vellore Institute of Technology**

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# Lab Task 02

## Architecture Design of Simple Processor

# Section 1 Logic Synthesis

**Aim:** Synopsys Design Complier used for Logic Synthesis of Simple Processor.

### Script used for logic synthesis of Architecture Design of Simple Processor:

### 1. Tickle Script for saed14rvt_tt0p8v125c

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory./ ----> Where Verilog Files available
# lvt, hvt and rvt library

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.

set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db"


#########################################################################
```

```
# Logical Library Settings
#############################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


######################## Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#    2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #       previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#    It will take default wire module. It is not accurate delay but it gives    #    some approx values.
#

#4. Drive cell or Input Transistion.

#############################################################################
#####

set_operating_conditions tt0p8v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c

link

## Generating intermediate technology independet (GTECH) design ###########
```

```
################ Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs

# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
# check design quality.

check_design

#############################################################################
######
########################### Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and
report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]
```

```
#to optimize the paths
#compile_ultra -incremental
```

## 2. SDC script for saed14rvt_tt0p8v125c

```
#set sdc_version 2.1
reset_design

set PERIOD  10.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
```

```
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_tt0p8v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN
$INPUTPORTS

#set_driving_cell -library $REFLIB \
        -lib_cell $BUFFER \
        -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 3. Report of QOR for saed14rvt_tt0p8v125c

```
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top
Version: O-2018.06-SP4
Date   : Sun May  1 12:11:23 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:              10.00
  Critical Path Length:          0.82
  Critical Path Slack:           9.03
  Critical Path Clk Period:     10.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:         -0.09
  Total Hold Violation:         -6.80
  No. of Hold Violations:       96.00
  -----------------------------------
```

Timing Path Group 'INPUTS'
---
Levels of Logic: 4.00
Critical Path Length: 0.14
Critical Path Slack: 8.71
Critical Path Clk Period: 10.00
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00
---

Cell Count
---
Hierarchical Cell Count: 78
Hierarchical Port Count: 818
Leaf Cell Count: 535
Buf/Inv Cell Count: 43
Buf Cell Count: 5
Inv Cell Count: 38
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 397
Sequential Cell Count: 138
Macro Count: 0
---

Area
---
Combinational Area: 143.412001
Noncombinational Area: 115.928398
Buf/Inv Area: 8.080800
Total Buffer Area: 1.33
Total Inverter Area: 6.75
Macro/Black Box Area: 0.000000
Net Area: 255.574103
---
Cell Area: 259.340398
Design Area: 514.914501

Design Rules
---
Total Number of Nets: 552
Nets With Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0
---

Hostname: synopsysserver

Compile CPU Statistics
---

```
Resource Sharing:                0.13
Logic Optimization:              0.24
Mapping Optimization:            1.81
-----------------------------------------
Overall Compile Time:            17.51
Overall Compile Wall Clock Time:    17.94

--------------------------------------------------------------------

Design WNS: 0.00 TNS: 0.00 Number of Violating Paths: 0


Design (Hold) WNS: 0.09 TNS: 6.80 Number of Violating Paths: 96

--------------------------------------------------------------------


1
dc_shell> exit

Thank you...
```

## 4. Tickle Script for saed14rvt_ss0p72v125c

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm

#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.
```

```
set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db"


##########################################################################
# Logical Library Settings
##########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


######################## Environment Variables ##############################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #      previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#   It will take default wire module. It is not accurate delay but it gives   #   some approx values.
#

#4. Drive cell or Input Transistion.
```

```
################################################################################
###

set_operating_conditions ss0p72v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c

link

## Generating intermediate technology independet (GTECH) design ###########
############### Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs

# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
# check design quality.

check_design

################################################################################
####
########################## Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
```

```
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 5. SDC Script for saed14rvt_ss0p72v125c

```
#set sdc_version 2.1
reset_design

set PERIOD  10.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1
```

```
group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ ss0p72v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
            -lib_cell $BUFFER \
            -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 6. Report of QOR for saed14rvt_ss0p72v125c

```
Loading db file '/home/synopsys/installs/syn/O-2018.06-SP4/libraries/syn/generic.sdb'
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top
Version: O-2018.06-SP4
Date   : Sun May  1 12:25:47 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:            12.00
```

Critical Path Length: 0.88
Critical Path Slack: 8.97
Critical Path Clk Period: 10.00
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: -0.08
Total Hold Violation: -5.60
No. of Hold Violations: 96.00
---

Timing Path Group 'INPUTS'
---
Levels of Logic: 4.00
Critical Path Length: 0.16
Critical Path Slack: 8.69
Critical Path Clk Period: 10.00
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: 0.00
Total Hold Violation: 0.00
No. of Hold Violations: 0.00
---

Cell Count
---
Hierarchical Cell Count: 78
Hierarchical Port Count: 818
Leaf Cell Count: 530
Buf/Inv Cell Count: 41
Buf Cell Count: 5
Inv Cell Count: 36
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 392
Sequential Cell Count: 138
Macro Count: 0
---

Area
---
Combinational Area: 142.879200
Noncombinational Area: 115.839598
Buf/Inv Area: 7.725600
Total Buffer Area: 1.33
Total Inverter Area: 6.39
Macro/Black Box Area: 0.000000
Net Area: 254.741660
---
Cell Area: 258.718798
Design Area: 513.460458

Design Rules
---
Total Number of Nets: 547

```
Nets With Violations:            0
Max Trans Violations:            0
Max Cap Violations:              0
----------------------------------


Hostname: synopsysserver

Compile CPU Statistics
-----------------------------------------
Resource Sharing:                0.14
Logic Optimization:              0.21
Mapping Optimization:            1.62
-----------------------------------------
Overall Compile Time:            18.14
Overall Compile Wall Clock Time:    18.63

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.08  TNS: 5.60  Number of Violating Paths: 96

--------------------------------------------------------------------


1
dc_shell> exit

Thank you...
```

## 7. Tickle Script for saed14rvt_ff0p88v125c

```
set_svf "Simple_Processor.svf"
# Serial vector Format .svf file is an ASCII text file that stores programming data for programming, verfying and blank checking.

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

# Current Working Directory ./ ----> Where Verilog Files available
# lvt, hvt and rvt library ------> Read on this

set SEARCH_PATH      " ./ \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "

# Link Library -----> Check for refernce for all cells are available or not.

#14nm tech rvt library two types:
#1) ccs
#2) nldm
```

```
#Atleast one library should be available and that should aslo be there in Target library
#1. nldm---Non linear delay Model
#ccs is more accurate than nldm.
#saed14rvt_tt0p6v125c.db.
#tt----for nmos pmos.
#0p6----0.6.
#125----operating temparture.
#Multi Vt then include many libraries.

set LINK_LIBRARY_FILES   " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"

# Target Library choose cells from targeted i.e, with specific library
# slack, speed, area, power varies with lvt and hvt libraries

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"


##########################################################################
# Logical Library Settings
##########################################################################
# set_app_var -----> tool variable
# Tool goes and searches for these variable and file_location pointed by it.
# set_app_var search_path $DIR1 $DIR2 $DIR3


set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "

#read_verilog tool set as top_module of alu.v
#at the end file will be top_level_module ------> Testbench module
#or use current_design testbench_module_name -------> Setting for Top Module

read_verilog Simple_Processor_Top_Module.v
read_verilog Decoders.v
read_verilog controller_12_april.v
read_verilog Datapath_path_work_version_2.v


current_design simple_processor_Top
#Module Name should be written here


######################## Environment Variables ################################
#1. Output Load.
#   tdelay(rise) = f(load cap from next block, I/p transition time)
#   Provide some value. How to set load cap?
#   1. like 10fF
#   2. Drive some 10 buffers all i/p cap of buffer becomes as load cap for #      previopus block.

#2. Operating Condition. (Temperature: 1.Industrial 2.Military 3.Automobile)
#   These are defined in libraries set minimum and max temp range value

#3. Wire Load module.
```

```
#   Estimate Net delay of Interconnecting wire and net.
#   Estimation of delay using Wire Load module.
#   Based on 1. transistor size. 2. Fanout
#   The wire load module varies.
#   It will take default wire module. It is not accurate delay but it gives   #   some approx values.
#

#4. Drive cell or Input Transistion.

################################################################################
###

set_operating_conditions ff0p88v125c
#set_operating_conditions -min ff0p88v125c -max ss0p6v125c

link

## Generating intermediate technology independet (GTECH) design ###########
############### Architecture Mapped File ###################################
# invoke gui to check what architecture it has done
write_file -format verilog -output ./Simple_Processor_gtech.vs

# Like Linting problems.
# Instatntaion problems or missed any constaraints or some mapping is wrong or not mapped
according to us.
# check design quality.

check_design

################################################################################
####
########################### Set Design Constraints ############################

source ./constraints_processor.sdc

check_timing

set_wire_load_model -name "8000"
set_wire_load_mode segmented

#compile_ultra
#compile_ultra -no_autoungroup -gate_clock

set_fix_multiple_port_nets –all –buffer_constants

compile_ultra -no_autoungroup
#compile -ungroup_all
#set_donot_touch


# Report gives number of details
report_area
report_power
report_timing
report_constraint -verbose
report_qor
```

```
report_clock_gating

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./Simple_Processor_netlist.v
write_sdc ./Simple_Processor.sdc

#Reporting reg2reg timing path
#set_false_path -to [all_outputs]
#set_false_path -from [all_inputs]
#Above command will disable timing paths from input ports and to output ports and report_timing will give reg2reg path
#report_timing

#Reporting more than one timing paths and setup slack less than 0
#report_timing -max_paths 10 -slack_lesser_than 0
#report_timing -max_paths 10 -delay_type min -slack_lesser_than 0

#set_fix_hold [all_clocks]

#to optimize the paths
#compile_ultra -incremental
```

## 8. SDC Script for saed14rvt_ff0p88v125c

```
#set sdc_version 2.1
reset_design

set PERIOD  10.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
```

```
group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1


## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ff0p88v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
            -lib_cell $BUFFER \
            -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 9. QOR Script for saed14rvt_ff0p88v125c

```
dc_shell>
dc_shell> report_qor

****************************************
Report : qor
Design : simple_processor_Top
Version: O-2018.06-SP4
Date   : Sun May  1 12:31:37 2022
****************************************


  Timing Path Group 'CLOCK'
  -----------------------------------
  Levels of Logic:              10.00
  Critical Path Length:          0.80
  Critical Path Slack:           9.05
  Critical Path Clk Period:     10.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:         -0.10
  Total Hold Violation:         -7.69
  No. of Hold Violations:       97.00
  -----------------------------------

  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:               4.00
  Critical Path Length:          0.13
  Critical Path Slack:           8.71
  Critical Path Clk Period:     10.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:         78
  Hierarchical Port Count:        818
  Leaf Cell Count:                530
  Buf/Inv Cell Count:              41
  Buf Cell Count:                   5
  Inv Cell Count:                  36
  CT Buf/Inv Cell Count:            0
  Combinational Cell Count:       392
  Sequential Cell Count:          138
  Macro Count:                      0
  -----------------------------------
```

```
Area
-----------------------------------
Combinational Area:      142.879200
Noncombinational Area:   115.839598
Buf/Inv Area:             7.725600
Total Buffer Area:            1.33
Total Inverter Area:          6.39
Macro/Black Box Area:     0.000000
Net Area:               254.741660
-----------------------------------
Cell Area:              258.718798
Design Area:            513.460458


Design Rules
-----------------------------------
Total Number of Nets:          547
Nets With Violations:            0
Max Trans Violations:            0
Max Cap Violations:              0
-----------------------------------


Hostname: synopsysserver

Compile CPU Statistics
---------------------------------------
Resource Sharing:                0.13
Logic Optimization:              0.56
Mapping Optimization:            4.45
---------------------------------------
Overall Compile Time:           25.49
Overall Compile Wall Clock Time:    26.08

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.10  TNS: 7.69  Number of Violating Paths: 97

--------------------------------------------------------------------


1
dc_shell> exit

Thank you...
```

**Date:25/4/2022**

## Logic Synthesis of Simple Processor Architecture Realized in Design Complier

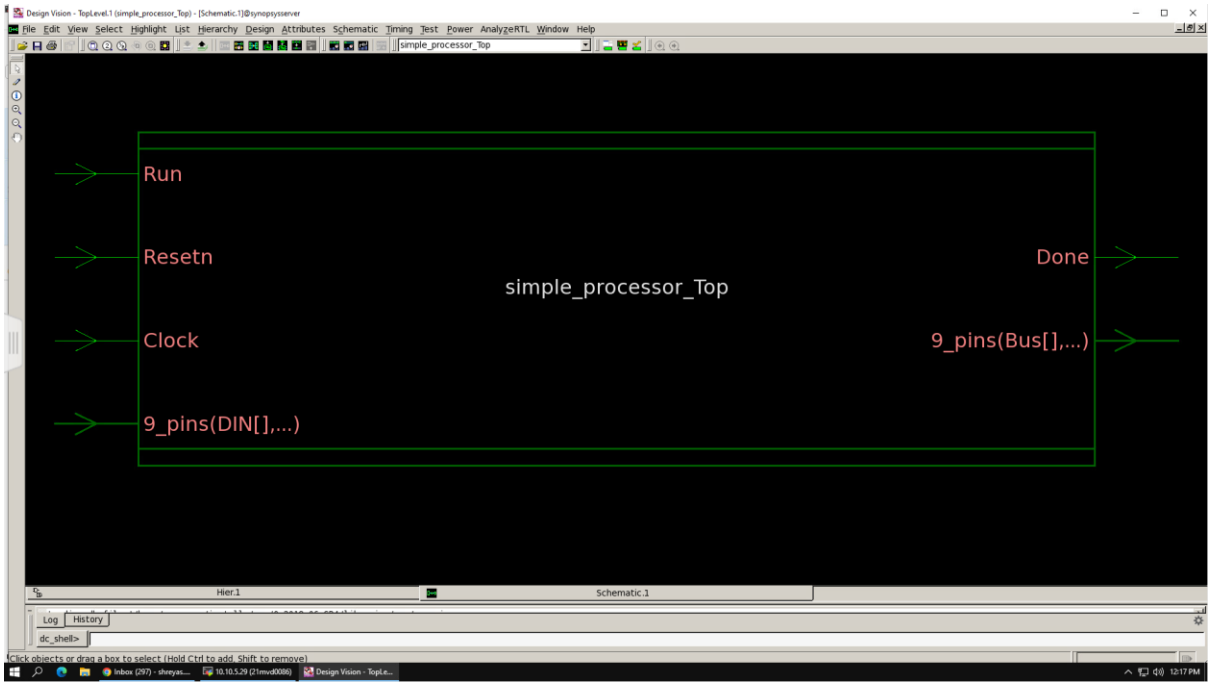


**Figure 1.1** The Block diagram of Top level of Simple processor realized in Design Complier.

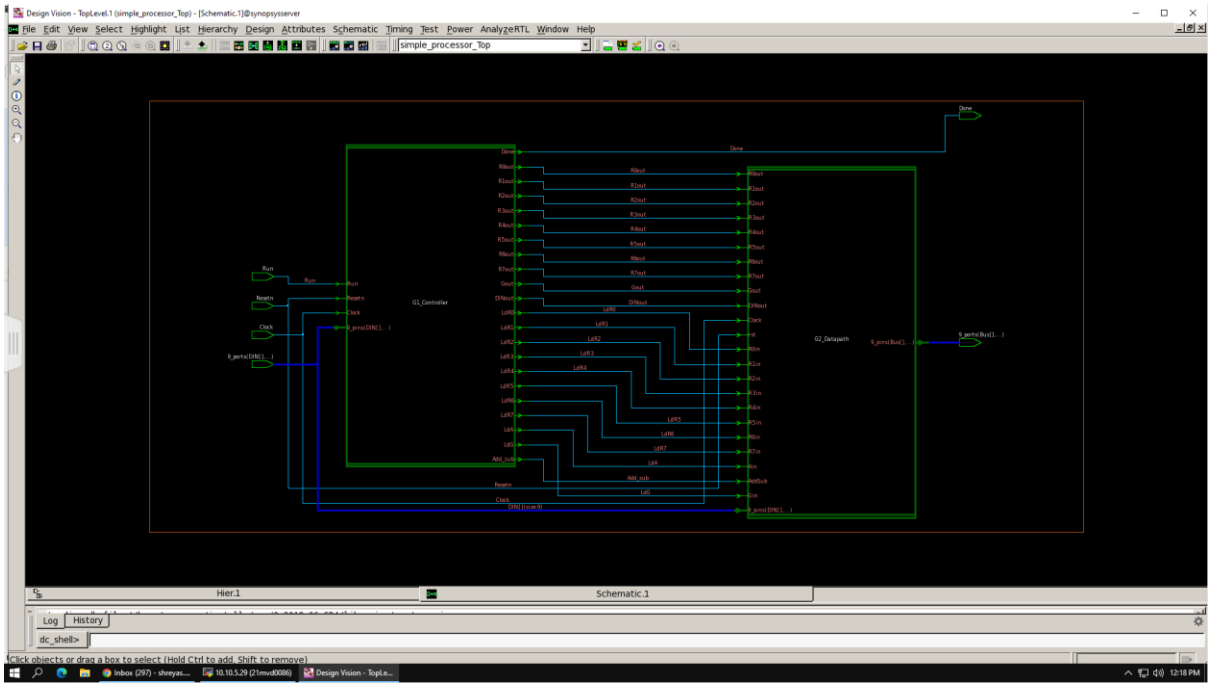

**Figure 1.2** The Block diagram of Simple processor consisting of Controller path and Datapath block realized in Design Complier.

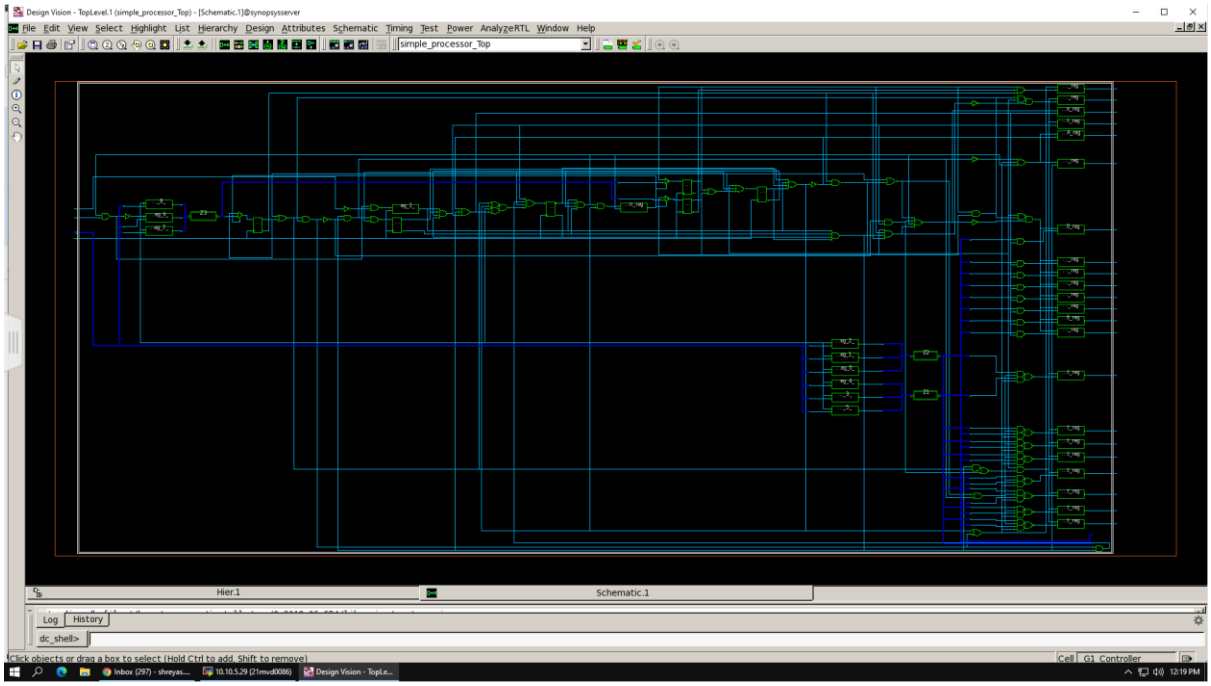


**Figure 1.3** The Block diagram of Controller path realized in Design Complier.

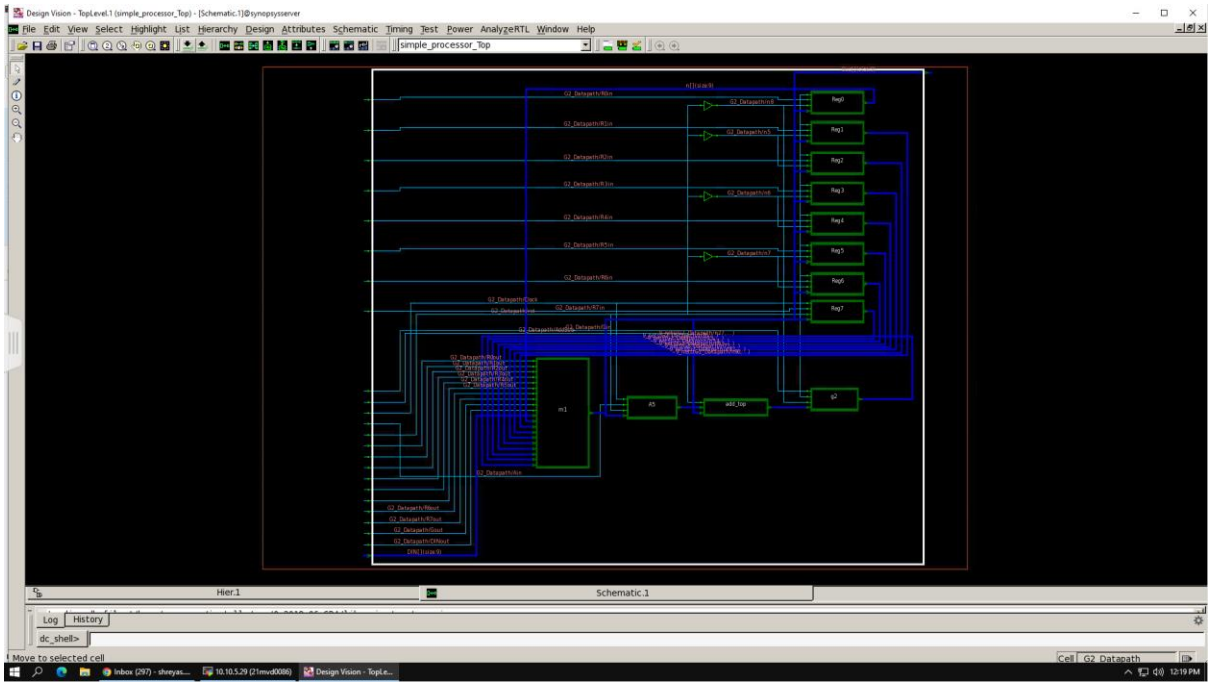


**Figure 1.4** The Block diagram of Datapath realized in Design Complier.

**Date:25/4/2022**

**Logic Synthesis Area, Power and Slack Table for RVT with three corners (TT, SS and FF):**

**Temp = $125^0$C fixed**

| **Constraints** | **tt0p8v125c** | **ss0p72v125c** | **ff0p88v125c** |
|---|---|---|---|
| **Cell Area** | 259.34 | 258.71 | 258.71 |
| **Total Area** | 514.91 | 513.46 | 513.46 |
| **Dynamic Power** | 13.34 uW | 8.65 uW | 24.34 uW |
| **Cell Leakage** | 3.277 uW | 1.29 uW | 9.05 uW |
| **Total Power** | 16.61 uW | 9.95 uW | 33.4 uW |
| **Slack** | 9.03 | 8.97 | 9.05 |

The Process Corners FF is best case because High Vdd and Temp = $125^0$C and RVT library is fixed. The Power consumption is more in case of ff0p88v125c compared to rest.

The speed for process corners.

SS: NMOS slow, PMOS slow
FF: NMOS fast, PMOS fast
TT: NMOS typical, PMOS typical

**Inference:**

1. The Simple Processor 9 bit was designed using Verilog code. The Logic synthesis was done using Synopsys Design Complier tool.
2. The Logic Synthesis is done for 14nm FinFET and target library is for only rvt library with TT, FF and SS.
3. The Table represents the variation in power consumption for tt0p8v125c, ss0p72v125c and ff0p88v125c.

**Date:25/4/2022**

# Section 2 Physical Synthesis

**Aim:** Synopsys Design Complier used for Physical Synthesis of Simple Processor.

**Script used for physical synthesis of Architecture Design of Simple Processor:**

## 1. Tickle Script for saed14rvt_tt0p8v125c

```
set_svf "Simple_Processor_Phy_Synth.svf"

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"


set SEARCH_PATH      " \
      ${DESIGN_REF_PATH}/stdcell_hvt/milkyway/saed14nm_hvt_1p9m \
      ${DESIGN_REF_PATH}/stdcell_rvt/milkyway/saed14nm_rvt_1p9m \
      ${DESIGN_REF_PATH}/stdcell_lvt/milkyway/saed14nm_lvt_1p9m "


# Milkway database ---

# Layout physical format

# Two views are available

# 1.Abstarct view(FRAM) --- Place and route, size, routing, no. of metal layers just view not exact one.

# 2.Layout view(CELL VIEW) --- Exact and complex version one.


set LINK_LIBRARY_FILES   "* \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8vm40c.db \
```

```
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p72v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p72v125c.db "

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db"

#saed14rvt_tt0p8v125c.db -- is my target library and subset of Link Library

##############################################################################
###########
# User-defined variables for physical library setup in dc_setup.tcl
##############################################################################
###########
```

```
set MW_DESIGN_LIB       MY_DESIGN_LIB_PROCESSOR         ;

# User-defined Milkyway design library name


# Milkyway reference libraries

set MW_REFERENCE_LIB_DIRS "${SEARCH_PATH} "


set     TECH_FILE     "${DESIGN_REF_PATH}/tech/milkyway/saed14nm_1p9m_mw.tf"      ;#
Milkyway technology file


set                                                                    TLUPLUS_MAX_FILE
"${DESIGN_REF_PATH}/tech/star_rc/max/saed14nm_1p9m_Cmax.tluplus" ;#Max TLUPlus file


set                                                                    TLUPLUS_MIN_FILE
"${DESIGN_REF_PATH}/tech/star_rc/min/saed14nm_1p9m_Cmin.tluplus" ;#Min TLUPlus file


set    MAP_FILE          "${DESIGN_REF_PATH}/tech/star_rc/saed14nm_tf_itf_tluplus.map"    ;#
Mapping file for TLUplus



#############################################################################

# Logical Library Settings

#############################################################################

set_app_var search_path "$SEARCH_PATH"

set_app_var target_library "$TARGET_LIBRARY_FILES"

set_app_var link_library " $LINK_LIBRARY_FILES "

#############################################################################

# Physical Library Settings

#############################################################################


set_app_var mw_reference_library $MW_REFERENCE_LIB_DIRS

set_app_var mw_design_library $MW_DESIGN_LIB


# create new Milkyway design library


#create_mw_lib   -technology $TECH_FILE \

#                    -mw_reference_library $mw_reference_library \
```

```
#                   $mw_design_library

# Only create new Milkyway design library if it doesn't already exist
   if {![file isdirectory $mw_design_library ]} {
     create_mw_lib   -technology $TECH_FILE \
                  -mw_reference_library $mw_reference_library \
                  -hier_separator {/} \
                  -bus_naming_style {[%d]} \
                  $mw_design_library
   } else {
# If Milkyway design library already exists, continue by opening the existing library
   }

open_mw_lib $mw_design_library
check_library
set_tlu_plus_files -max_tluplus $TLUPLUS_MAX_FILE -min_tluplus $TLUPLUS_MIN_FILE \
-tech2itf_map $MAP_FILE

check_tlu_plus_files

read_verilog ./controller_12_april.v
read_verilog ./Datapath_path_work_version_2.v
read_verilog ./Decoders.v
read_verilog ./Simple_Processor_Top_Module.v

current_design simple_processor_Top
link
check_design

source ./MYDESIGN_phys_cons.tcl
extract_physical_constraints ./floorplan/floorplan.def

source ./constraints.sdc
check_timing
```

```
#set_wire_load_model -name "8000"
#set_wire_load_mode segmented

# input Run, Resetn, Clock;
# input [8:0] DIN;
set_input_transition 0.05 [get_ports Run]
set_input_transition 0.05 [get_ports Resetn]
set_input_transition 0.05 [get_ports DIN]

set_power_prediction true
set_load 2 [all_outputs]

#compile_ultra
compile_ultra -no_autoungroup

report_area
report_power
report_timing
report_timing -delay_type min

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./phy_simple_processor_netlist.v
```

## 2. SDC Script for saed14rvt_tt0p8v125c

```
#set sdc_version 2.1
reset_design

set PERIOD  10.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
#group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name CLOCK\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1

group_path  -name COMBO\
        -from [all_inputs]\
        -to [all_outputs]\
        -weight 1

## IN/OUT
```

```
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_tt0p8v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
        -lib_cell $BUFFER \
        -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 3. QOR Script for saed14rvt_tt0p8v125c

```
dc_shell-topo>
dc_shell-topo> report_qor

****************************************
Report : qor
Design : simple_processor_Top
Version: O-2018.06-SP4
Date   : Sun May  1 15:07:49 2022
****************************************


  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:              2.00
  Critical Path Length:         0.24
  Critical Path Slack:          8.60
  Critical Path Clk Period:     10.00
  Total Negative Slack:         0.00
  No. of Violating Paths:       0.00
  Worst Hold Violation:         0.00
```

Total Hold Violation: 0.00
No. of Hold Violations: 0.00
---

Timing Path Group 'clock'
---
Levels of Logic: 11.00
Critical Path Length: 0.64
Critical Path Slack: 9.20
Critical Path Clk Period: 10.00
Total Negative Slack: 0.00
No. of Violating Paths: 0.00
Worst Hold Violation: -0.08
Total Hold Violation: -3.18
No. of Hold Violations: 79.00
---

Cell Count
---
Hierarchical Cell Count: 78
Hierarchical Port Count: 881
Leaf Cell Count: 559
Buf/Inv Cell Count: 67
Buf Cell Count: 30
Inv Cell Count: 37
CT Buf/Inv Cell Count: 0
Combinational Cell Count: 421
Sequential Cell Count: 138
Macro Count: 0
---

Area
---
Combinational Area: 157.131600
Noncombinational Area: 116.949598
Buf/Inv Area: 19.047600
Total Buffer Area: 9.28
Total Inverter Area: 9.77
Macro/Black Box Area: 0.000000
Net Area: 0.000000
Net XLength : 41022.88
Net YLength : 32641.87
---
Cell Area: 274.081198
Design Area: 274.081198
Net Length : 73664.75

Design Rules
---
Total Number of Nets: 571
Nets With Violations: 1
Max Trans Violations: 0
Max Cap Violations: 0

```
Max Fanout Violations:          1
---------------------------------


Hostname: synopsysserver

Compile CPU Statistics
-----------------------------------------
Resource Sharing:                0.20
Logic Optimization:              1.30
Mapping Optimization:            2.37
-----------------------------------------
Overall Compile Time:          229.77
Overall Compile Wall Clock Time:  240.30

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.08  TNS: 3.18  Number of Violating Paths: 79

--------------------------------------------------------------------


1
dc_shell-topo> exit

Thank you...
```

## 4. Tickle Script for saed14rvt_ss0p72v125c

```
set_svf "Simple_Processor_Phy_Synth.svf"
## Point to the new 14nm SAED libs
set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

set SEARCH_PATH      " \
      ${DESIGN_REF_PATH}/stdcell_hvt/milkyway/saed14nm_hvt_1p9m \
      ${DESIGN_REF_PATH}/stdcell_rvt/milkyway/saed14nm_rvt_1p9m \
      ${DESIGN_REF_PATH}/stdcell_lvt/milkyway/saed14nm_lvt_1p9m "

# Milkway database ---
# Layout physical format
# Two views are available
# 1.Abstarct view(FRAM) --- Place and route, size, routing, no. of metal layers just view not exact one.
# 2.Layout view(CELL VIEW) --- Exact and complex version one.

set LINK_LIBRARY_FILES   "* \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p72v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p72v125c.db "
```

```
set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db"

#saed14rvt_tt0p8v125c.db -- is my target library and subset of Link Library

##########################################################################
###############
# User-defined variables for physical library setup in dc_setup.tcl
##########################################################################
###############

set MW_DESIGN_LIB       MY_DESIGN_LIB_PROCESSOR         ;
# User-defined Milkyway design library name

# Milkyway reference libraries
set MW_REFERENCE_LIB_DIRS "${SEARCH_PATH} "

set    TECH_FILE    "${DESIGN_REF_PATH}/tech/milkyway/saed14nm_1p9m_mw.tf"    ;#
Milkyway technology file

set                                                          TLUPLUS_MAX_FILE
"${DESIGN_REF_PATH}/tech/star_rc/max/saed14nm_1p9m_Cmax.tluplus"              ;#Max
TLUPlus file

set                                                           TLUPLUS_MIN_FILE
"${DESIGN_REF_PATH}/tech/star_rc/min/saed14nm_1p9m_Cmin.tluplus" ;#Min TLUPlus
file

set  MAP_FILE      "${DESIGN_REF_PATH}/tech/star_rc/saed14nm_tf_itf_tluplus.map"  ;#
Mapping file for TLUplus


##########################################################################
# Logical Library Settings
##########################################################################
set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "
##########################################################################
# Physical Library Settings
##########################################################################

set_app_var mw_reference_library $MW_REFERENCE_LIB_DIRS
set_app_var mw_design_library $MW_DESIGN_LIB

# create new Milkyway design library

#create_mw_lib   -technology $TECH_FILE \
#                  -mw_reference_library $mw_reference_library \
#                  $mw_design_library

# Only create new Milkyway design library if it doesn't already exist
   if {![file isdirectory $mw_design_library ]} {
     create_mw_lib   -technology $TECH_FILE \
                 -mw_reference_library $mw_reference_library \
                 -hier_separator {/} \
```

```
                -bus_naming_style {[%d]} \
                $mw_design_library
   } else {
# If Milkyway design library already exists, continue by opening the existing library
   }

open_mw_lib $mw_design_library
check_library
set_tlu_plus_files -max_tluplus $TLUPLUS_MAX_FILE -min_tluplus $TLUPLUS_MIN_FILE \
-tech2itf_map $MAP_FILE

check_tlu_plus_files

read_verilog ./controller_12_april.v
read_verilog ./Datapath_path_work_version_2.v
read_verilog ./Decoders.v
read_verilog ./Simple_Processor_Top_Module.v

current_design simple_processor_Top
link
check_design

source ./MYDESIGN_phys_cons.tcl
extract_physical_constraints ./floorplan/floorplan.def

source ./constraints.sdc
check_timing

#set_wire_load_model -name "8000"
#set_wire_load_mode segmented

# input Run, Resetn, Clock;
# input [8:0] DIN;
set_input_transition 0.05 [get_ports Run]
set_input_transition 0.05 [get_ports Resetn]
set_input_transition 0.05 [get_ports DIN]


set_load 2 [all_outputs]

#compile_ultra
compile_ultra -no_autoungroup

report_area
report_power
report_timing
report_timing -delay_type min

change_names -rule verilog -hier
write -hierarchy -format verilog -output ./phy_simple_processor_netlist.v
```

## 5. SDC Script for saed14rvt_ss0p72v125c

```
#set sdc_version 2.1
reset_design

set PERIOD  10.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]

set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
#group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name CLOCK\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1

group_path  -name COMBO\
        -from [all_inputs]\
        -to [all_outputs]\
        -weight 1

## IN/OUT
```

```
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ss0p72v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
        -lib_cell $BUFFER \
        -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]


## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 6. QOR Script for saed14rvt_ss0p72v125c

```
dc_shell-topo>
dc_shell-topo> report_qor

****************************************
Report : qor
Design : simple_processor_Top
Version: O-2018.06-SP4
Date   : Sun May  1 15:17:35 2022
****************************************


  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:              3.00
  Critical Path Length:         0.36
  Critical Path Slack:          8.48
  Critical Path Clk Period:    10.00
  Total Negative Slack:         0.00
  No. of Violating Paths:       0.00
  Worst Hold Violation:         0.00
  Total Hold Violation:         0.00
  No. of Hold Violations:       0.00
  -----------------------------------

  Timing Path Group 'clock'
  -----------------------------------
  Levels of Logic:             12.00
  Critical Path Length:         0.98
  Critical Path Slack:          8.86
  Critical Path Clk Period:    10.00
  Total Negative Slack:         0.00
  No. of Violating Paths:       0.00
  Worst Hold Violation:        -0.06
  Total Hold Violation:        -1.21
  No. of Hold Violations:      43.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:        78
  Hierarchical Port Count:       886
  Leaf Cell Count:               571
  Buf/Inv Cell Count:             79
  Buf Cell Count:                 42
  Inv Cell Count:                 37
  CT Buf/Inv Cell Count:           0
  Combinational Cell Count:      433
  Sequential Cell Count:         138
  Macro Count:                     0
  -----------------------------------
```

```
Area
-----------------------------------
Combinational Area:      162.859200
Noncombinational Area:   116.549998
Buf/Inv Area:            23.754000
Total Buffer Area:           13.28
Total Inverter Area:         10.48
Macro/Black Box Area:     0.000000
Net Area:                0.000000
Net XLength        :      32465.07
Net YLength        :      38271.63
-----------------------------------
Cell Area:               279.409198
Design Area:             279.409198
Net Length         :      70736.70


Design Rules
-----------------------------------
Total Number of Nets:          583
Nets With Violations:            1
Max Trans Violations:            0
Max Cap Violations:              0
Max Fanout Violations:           1
-----------------------------------


Hostname: synopsysserver

Compile CPU Statistics
-----------------------------------------
Resource Sharing:                0.18
Logic Optimization:              1.26
Mapping Optimization:            2.44
-----------------------------------------
Overall Compile Time:          228.01
Overall Compile Wall Clock Time:   237.31

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.06  TNS: 1.21  Number of Violating Paths: 43

--------------------------------------------------------------------


1
dc_shell-topo> exit

Thank you...
```

## 7. Tickle Script for saed14rvt_ff0p88v125c

```
set_svf "Simple_Processor_Phy_Synth.svf"

## Point to the new 14nm SAED libs

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"


set SEARCH_PATH      " \
      ${DESIGN_REF_PATH}/stdcell_hvt/milkyway/saed14nm_hvt_1p9m \
      ${DESIGN_REF_PATH}/stdcell_rvt/milkyway/saed14nm_rvt_1p9m \
      ${DESIGN_REF_PATH}/stdcell_lvt/milkyway/saed14nm_lvt_1p9m "


# Milkway database ---

# Layout physical format

# Two views are available

# 1.Abstarct view(FRAM) --- Place and route, size, routing, no. of metal layers just view not exact one.

# 2.Layout view(CELL VIEW) --- Exact and complex version one.


set LINK_LIBRARY_FILES   "* \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72v125c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p72v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p88v125c.db \
```

```
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p72vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p7vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p88vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p6vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8vm40c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p7v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ff0p88v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p6v125c.db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_ss0p72v125c.db "

set TARGET_LIBRARY_FILES    " \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_ff0p88v125c.db"

#saed14rvt_tt0p8v125c.db -- is my target library and subset of Link Library

##########################################################################
#################
# User-defined variables for physical library setup in dc_setup.tcl
##########################################################################
#################

set MW_DESIGN_LIB       MY_DESIGN_LIB_PROCESSOR       ;
# User-defined Milkyway design library name

# Milkyway reference libraries
```

```
set MW_REFERENCE_LIB_DIRS "${SEARCH_PATH} "

set TECH_FILE "${DESIGN_REF_PATH}/tech/milkyway/saed14nm_1p9m_mw.tf" ;# Milkyway technology file

set TLUPLUS_MAX_FILE "${DESIGN_REF_PATH}/tech/star_rc/max/saed14nm_1p9m_Cmax.tluplus" ;#Max TLUPlus file

set TLUPLUS_MIN_FILE "${DESIGN_REF_PATH}/tech/star_rc/min/saed14nm_1p9m_Cmin.tluplus" ;#Min TLUPlus file

set MAP_FILE "${DESIGN_REF_PATH}/tech/star_rc/saed14nm_tf_itf_tluplus.map" ;# Mapping file for TLUplus

##########################################################################
# Logical Library Settings
##########################################################################
set_app_var search_path "$SEARCH_PATH"
set_app_var target_library "$TARGET_LIBRARY_FILES"
set_app_var link_library " $LINK_LIBRARY_FILES "
##########################################################################
# Physical Library Settings
##########################################################################

set_app_var mw_reference_library $MW_REFERENCE_LIB_DIRS
set_app_var mw_design_library $MW_DESIGN_LIB

# create new Milkyway design library

#create_mw_lib -technology $TECH_FILE \
#       -mw_reference_library $mw_reference_library \
#       $mw_design_library

# Only create new Milkyway design library if it doesn't already exist
   if {![file isdirectory $mw_design_library ]} {
```

```
        create_mw_lib   -technology $TECH_FILE \
                        -mw_reference_library $mw_reference_library \
                        -hier_separator {/} \
                        -bus_naming_style {[%d]} \
                        $mw_design_library
    } else {
# If Milkyway design library already exists, continue by opening the existing library
    }

open_mw_lib $mw_design_library
check_library
set_tlu_plus_files -max_tluplus $TLUPLUS_MAX_FILE -min_tluplus $TLUPLUS_MIN_FILE \
-tech2itf_map $MAP_FILE

check_tlu_plus_files

read_verilog ./controller_12_april.v
read_verilog ./Datapath_path_work_version_2.v
read_verilog ./Decoders.v
read_verilog ./Simple_Processor_Top_Module.v

current_design simple_processor_Top
link
check_design

source ./MYDESIGN_phys_cons.tcl
extract_physical_constraints ./floorplan/floorplan.def

source ./constraints.sdc
check_timing

#set_wire_load_model -name "8000"
#set_wire_load_mode segmented
```

```
# input Run, Resetn, Clock;

# input [8:0] DIN;

set_input_transition 0.05 [get_ports Run]

set_input_transition 0.05 [get_ports Resetn]

set_input_transition 0.05 [get_ports DIN]



set_load 2 [all_outputs]


#compile_ultra

compile_ultra -no_autoungroup


report_area

report_power

report_timing

report_timing -delay_type min


change_names -rule verilog -hier

write -hierarchy -format verilog -output ./phy_simple_processor_netlist.v
```

## 8. SDC Script for saed14rvt_ff0p88v125c

```
#set sdc_version 2.1
reset_design

set PERIOD  10.0
set INPUT_DELAY  1.0
set OUTPUT_DELAY  1.0
set CLOCK_LATENCY 1.0
set SOURCE_LATENCY 1.0
set UNCERTAINTY 0.15
set MAX_TRANSITION 0.5
set MIN_CLOCK_LATENCY 0.5
set MIN_SOURCE_LATENCY 0.5
set MIN_IO_DELAY 0.5



## CLOCK BASICS
create_clock -name "clock" -period $PERIOD [get_ports Clock]

set_clock_latency $CLOCK_LATENCY [get_clocks clock]
#set_clock_latency -min $MIN_CLOCK_LATENCY [get_clocks clock]
```

```
set_clock_latency -source $SOURCE_LATENCY [get_clocks clock]
#set_clock_latency -source -min $MIN_SOURCE_LATENCY [get_clocks clock]

set_clock_uncertainty -setup $UNCERTAINTY [get_clocks clock]
set_clock_uncertainty -hold $UNCERTAINTY [get_clocks clock]

set_clock_transition 0.12 [get_clocks clock]


## GROUPING
#group_path  -name CLOCK\
        -to clock\
        -weight 1

group_path  -name CLOCK\
        -weight 1

group_path  -name INPUTS\
        -through [all_inputs]\
        -weight 1

group_path  -name OUTPUTS\
        -to [all_outputs]\
        -weight 1

group_path  -name COMBO\
        -from [all_inputs]\
        -to [all_outputs]\
        -weight 1

## IN/OUT
set INPUTPORTS [remove_from_collection [all_inputs] [get_ports Clock]]
set OUTPUTPORTS [all_outputs]

set_input_delay -clock "clock" -max $INPUT_DELAY $INPUTPORTS
set_output_delay -clock "clock" -max $OUTPUT_DELAY $OUTPUTPORTS
set_input_delay -clock "clock" -min $MIN_IO_DELAY $INPUTPORTS
set_output_delay -clock "clock" -min $MIN_IO_DELAY $OUTPUTPORTS

#set REFLIB [get_object_name [index_collection [get_libs *wc] 0]]
set REFLIB saed14rvt_ff0p88v125c
set BUFFER "SAEDRVT14_BUF_10"
set BUF_IN_PIN "A"
set BUF_OUT_PIN "X"

set_load [expr 10 * [load_of $REFLIB/$BUFFER/$BUF_IN_PIN]] [all_outputs]

set_driving_cell -library $REFLIB -lib_cell $BUFFER -pin $BUF_OUT_PIN $INPUTPORTS

#set_driving_cell -library $REFLIB \
        -lib_cell $BUFFER \
        -pin $BUF_OUT_PIN [all_inputs]

#remove_driving_cell [get_ports Clock]
```

```
## DRC
set_max_transition $MAX_TRANSITION [current_design]

set_max_fanout 20 [current_design]

set_max_capacitance 100 [current_design]
```

## 9. QOR Script for saed14rvt_ss0p72v125c

```
dc_shell-topo>
dc_shell-topo> report_qor

****************************************
Report : qor
Design : simple_processor_Top
Version: O-2018.06-SP4
Date   : Sun May  1 15:25:58 2022
****************************************


  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:               2.00
  Critical Path Length:          0.19
  Critical Path Slack:           8.65
  Critical Path Clk Period:     10.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:          0.00
  Total Hold Violation:          0.00
  No. of Hold Violations:        0.00
  -----------------------------------

  Timing Path Group 'clock'
  -----------------------------------
  Levels of Logic:              11.00
  Critical Path Length:          0.60
  Critical Path Slack:           9.24
  Critical Path Clk Period:     10.00
  Total Negative Slack:          0.00
  No. of Violating Paths:        0.00
  Worst Hold Violation:         -0.10
  Total Hold Violation:         -5.01
  No. of Hold Violations:       89.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:         78
  Hierarchical Port Count:        908
  Leaf Cell Count:                561
  Buf/Inv Cell Count:              71
  Buf Cell Count:                  33
```

```
Inv Cell Count:                38
CT Buf/Inv Cell Count:          0
Combinational Cell Count:      423
Sequential Cell Count:         138
Macro Count:                    0
---------------------------------


Area
---------------------------------
Combinational Area:     155.311200
Noncombinational Area:  116.505598
Buf/Inv Area:           18.026400
Total Buffer Area:           9.77
Total Inverter Area:         8.26
Macro/Black Box Area:     0.000000
Net Area:               0.000000
Net XLength       :      35159.82
Net YLength       :      37697.35
---------------------------------
Cell Area:             271.816798
Design Area:           271.816798
Net Length        :      72857.17

Design Rules
---------------------------------
Total Number of Nets:          573
Nets With Violations:           0
Max Trans Violations:           0
Max Cap Violations:             0
---------------------------------
Hostname: synopsysserver

Compile CPU Statistics
-----------------------------------------
Resource Sharing:                0.20
Logic Optimization:              2.81
Mapping Optimization:            5.84
-----------------------------------------
Overall Compile Time:          206.19
Overall Compile Wall Clock Time:  216.22

--------------------------------------------------------------------

Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


Design (Hold)  WNS: 0.10  TNS: 5.01  Number of Violating Paths: 89

--------------------------------------------------------------------


1
dc_shell-topo> exit

Thank you...
```

**Date:25/4/2022**

**Physical Synthesis of Simple Processor Architecture Realized in Design Complier**

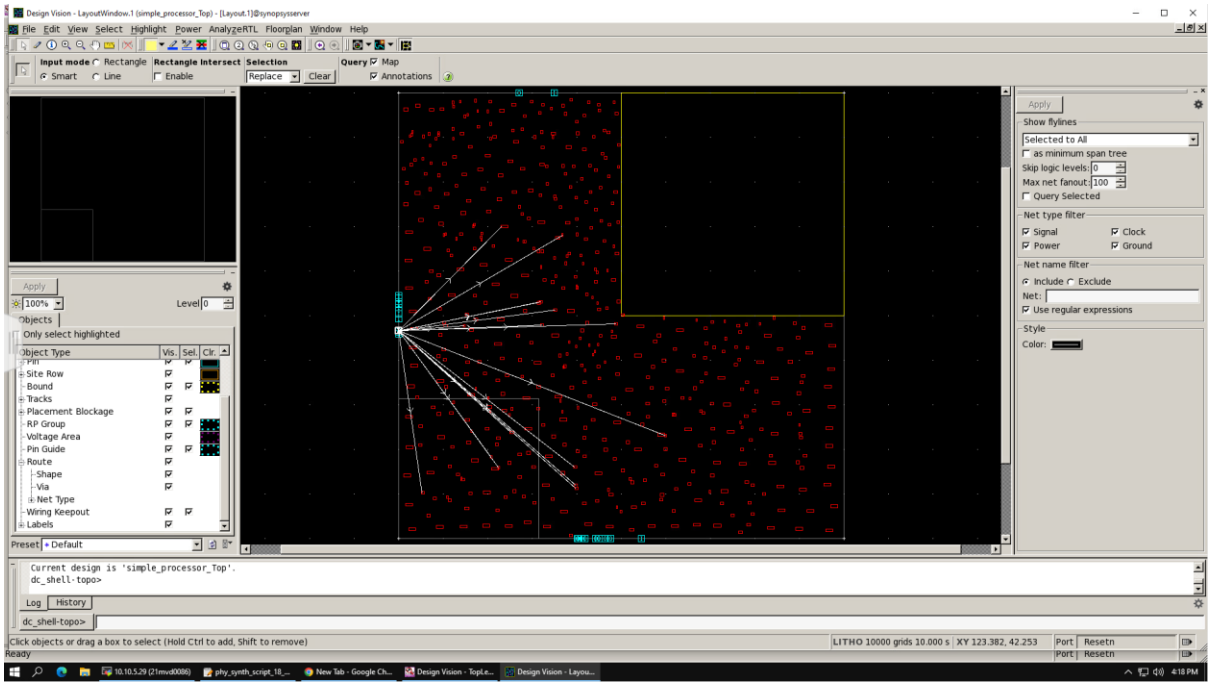


**Figure 2.1** The Physical Synthesis of Simple Processor in Design Complier Topo tool.

In the Figure 2.1 we observe the red colour rectangular are the standard cell and The yellow big box is the blockage block. The light blue colour is Input, output pins of the Simple processor.

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**Physical Synthesis Area, Power and Slack Table for RVT with three corners (TT, SS and FF):**

**Temp = $125^0$C fixed**

| Constraints | tt0p8v125c | ss0p72v125c | ff0p88v125c |
|---|---|---|---|
| **Cell Area** | 274.08 | 279.4 | 271.81 |
| **Dynamic Power** | 55.76 uW | 41.2 uW | 72.59 uW |
| **Cell Leakage** | 4.67 uW | 1.88 uW | 12.52 uW |
| **Total Power** | 18.4 uW | 11.57 uW | 32.57 uW |
| **Slack** | 8.6 | 8.48 | 8.65 |

The Process Corners FF is best case because High Vdd and Temp = $125^0$C and RVT library is fixed. The Power consumption is more in case of ff0p88v125c compared to rest.

The speed for process corners.

SS: NMOS slow, PMOS slow
FF: NMOS fast, PMOS fast
TT: NMOS typical, PMOS typical

**Inference:**

1. The Simple Processor 9 bit was designed using Verilog code. The Physical synthesis was done using Synopsys Design Complier Topo tool.
2. The Physical Synthesis is done for 14nm FinFET and target library is for only rvt library with TT, FF and SS.
3. The Table represents the variation in power consumption for tt0p8v125c, ss0p72v125c and ff0p88v125c.

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