Date:1/6/2022

Fall Semester 2021-2022

ECE5014 – ASIC Design

M.Tech VLSI Design

School of Electronics Engineering

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Lab Task 05

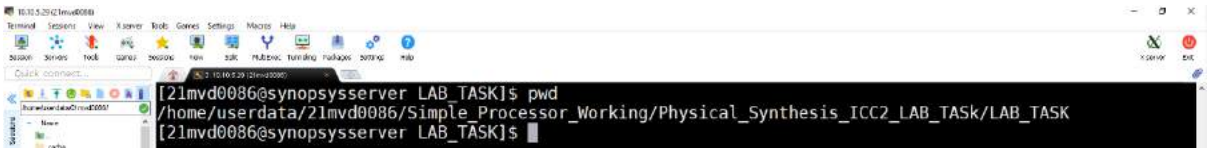
Physical Design – Floor planning, Power planning, Placement, Clock Tree Synthesis (CTS) and Routing.

Section 1 Design Import Stage

Questions :

1. Import the design & all inputs required to do physical design into ICC2.

   Path used in the Design :
   /home/userdata/21mvd0086/Simple_Processor_Working/Physical_Synthesis_ICC2_LAB_TASk/LAB_TASK/



(a) The Scripts used for Import the design and create library file for ICC2 shell is as follows:

1. Simple_Processor_mvt_netlist.v
2. Simple_Processor_mcmm.tcl
3. Simple_Processor_data_preparation.tcl
4. Simple_Processor_common_setup.tcl
5. Simple_Processor.sdc

The icc2_shell is invoked and a log file is created.

Log File name: Simple_Processor_Data_Preparation.log

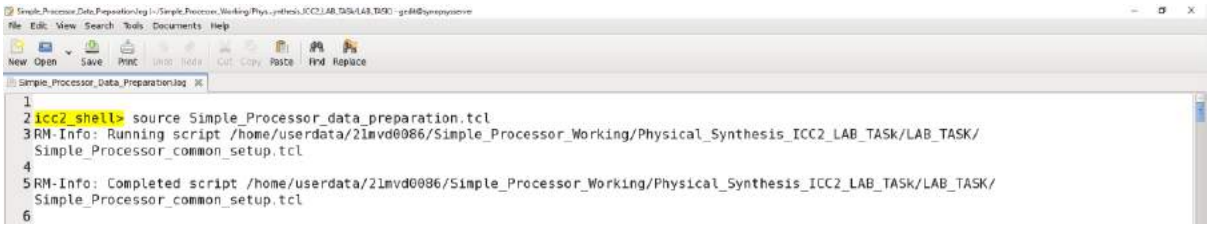


Figure 1.1 Simple_Processor_Data_Preparation.log file

(b) Now use the command "report_design –physical" in ICC2 and redirect(>) the report generated to Reports/ReportDesign.rpt. Keep the report in assignment.

```
icc2_shell> report_design -physical > ./Reports/reportDesign.rpt
icc2_shell> check_design > ./Reports/checkDesign.rpt
```

```
Warning: The option '-physical' has been deprecated and is scheduled to be removed in a future release. Please use report_design -help to see
 the latest supported options of command report_design. (NDMUI-332)
****************************************
Report : design
        -physical
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Mon May 30 16:33:02 2022
****************************************

Physical Information:
  Total moveable cell area: 259.607
  Total fixed cell area: 0.000
  Total physical cell area: 259.607
  Core area: --
                                Count                    Area
  TOTAL LEAF CELLS                532                 259.607
```

Figure 1.2 The Report of report_design -physical of Simple Processor.

(c) Now use the command "check_design" and redirect the report generated to reports/checkDesign.rpt. Keep the report in assignment. Close the block and the lib and exit ICC2.
Check Design

```
****************************************
 Report : check_design
 Options: { design_extraction }
 Design : simple_processor_Top
 Version: P-2019.03-SP4
 Date   : Mon May 30 16:40:51 2022
****************************************

Running atomic-check 'design_extraction'

  *** EMS Message summary ***
  ----------------------------------------------------------------------------------------------------
  Rule         Type   Count      Message
  ----------------------------------------------------------------------------------------------------
  NEX-048      Error  1          Port shape or size is abnormal for port '%portName'.
  ----------------------------------------------------------------------------------------------------
  Total 1 EMS messages : 1 errors, 0 warnings, 0 info.
  ----------------------------------------------------------------------------------------------------

  *** Non-EMS message summary ***
  ----------------------------------------------------------------------------------------------------
  Rule         Type   Count      Message
  ----------------------------------------------------------------------------------------------------
  NEX-001             2          Technology layer '%s' setting '%s' is not valid
  NEX-007             8          Parasitic Tech Library layer '%s' parameter '%s' = %2.3f does no...
  ----------------------------------------------------------------------------------------------------
  Total 10 non-EMS messages : 0 errors, 10 warnings, 0 info.
  ----------------------------------------------------------------------------------------------------

Warning: EMS database "check_design.ems" already exists, over-writing it. (EMS-040)

Information: EMS database is saved to file 'check_design.ems'.
Information: Non-EMS messages are saved into file 'check_design2022May30164051.log'.
```

Figure 1.3 The Report of check_design of Simple Processor.

The Script used for Design Import are here :

1. **Simple_Processor_mcmm.tcl**

```
set Constraints_file "./Simple_Processor.sdc"

remove_corners -all
remove_modes -all
remove_scenarios -all

create_corner slow
create_corner fast

read_parasitic_tech \
        -tlup
/home/synopsys/SAED14nm_EDK/tech/star_rc/min/saed14nm_1p9m_Cmi
n.tluplus \
        -layermap
/home/synopsys/SAED14nm_EDK/tech/star_rc/saed14nm_tf_itf_tluplus.ma
p \
        -name tlup_min

read_parasitic_tech \
        -tlup
/home/synopsys/SAED14nm_EDK/tech/star_rc/max/saed14nm_1p9m_Cma
x.tluplus \
        -layermap
/home/synopsys/SAED14nm_EDK/tech/star_rc/saed14nm_tf_itf_tluplus.ma
p \
        -name tlup_max

set_parasitics_parameters \
        -early_spec tlup_max \
        -late_spec tlup_max \
        -early_temperature 125 \
        -late_temperature 125 \
        -corners {slow}

set_parasitics_parameters \
        -early_spec tlup_min \
        -late_spec tlup_min \
        -early_temperature -40 \
        -late_temperature -40 \
        -corners {fast}

create_mode func
current_mode func
```

```
create_scenario -mode func -corner fast -name func_fast
create_scenario -mode func -corner slow -name func_slow

current_scenario func_slow
read_sdc $Constraints_file

current_scenario func_fast
read_sdc $Constraints_file

set_scenario_status func_slow -none -setup true -hold false -leakage_power true -dynamic_power true -max_transition true -max_capacitance true -min_capacitance false -active true
set_scenario_status func_fast -none -setup false -hold true -leakage_power true -dynamic_power false -max_transition true -max_capacitance false -min_capacitance true -active true
```

2. Simple_Processsor_data_preparation.tcl

```
####### Setting Up Target & Link Libraries ##############
source ./Simple_Processor_common_setup.tcl

####### Creating library of the block ########

set link_library  $LINK_LIBRARY_FILES_CLG
set target_library $TARGET_LIBRARY_FILES_CLG

create_lib -ref_libs $NDM_REFERENCE_LIB_DIRS_CLG -technology $TECH_FILE ./lib

#read netlist
read_verilog ./Simple_Processor_mvt_netlist.v

#set current design -top level module name
current_design simple_processor_Top

#linking library + netlist
link

save_lib -as post_import_design


#defining attributes for metal layers -- HVH (preferable) or VHV
define_user_attribute -type string -name routing_direction -classes routing_rule
```

```
#for horizontal ---- odd number of layers
set_attribute -objects [get_layers {M1 M3 M5 M7 M9}] -name routing_direction -value horizontal

#for vertical ---- even number of layers
set_attribute -objects [get_layers {M2 M4 M6 M8 MRDL}] -name routing_direction -value vertical


#reading TLU+ file ---max file -----> Worst parastics delay Parastic of Resistor and Capacitor.
read_parasitic_tech -tlup /home/synopsys/SAED14nm_EDK/tech/star_rc/max/saed14nm_1p9m_Cmax.tluplus -layermap /home/synopsys/SAED14nm_EDK/tech/star_rc/saed14nm_tf_itf_tluplus.map -name worst_para

#min file
read_parasitic_tech -tlup /home/synopsys/SAED14nm_EDK/tech/star_rc/min/saed14nm_1p9m_Cmin.tluplus -layermap /home/synopsys/SAED14nm_EDK/tech/star_rc/saed14nm_tf_itf_tluplus.map -name best_para

#reading the .sdc file
#read_sdc inputs/dtmf_recvr_core.sdc

source -e -v ./Simple_Processor_mcmm.tcl

save_block -as import_done

save_lib
```

3. Simple_Processor_common_setup.tcl

```
puts "RM-Info: Running script [info script]\n"

################################################################################
# Variables common to all RM scripts
# Script: common_setup.tcl
# Version: F-2011.09-SP4 (April 2, 2012)
# Copyright (C) 2007-2012 Synopsys, Inc. All rights reserved.
################################################################################

set DESIGN_NAME                 "simple_processor_Top"  ;#  The name of the top-level design

## Point to the new 14nm SAED libs
set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"
set DESIGN_REF_PATH1 "/home/synopsys/SAED14nm_EDK"

set DESIGN_REF_TECH_PATH        "${DESIGN_REF_PATH}/tech"

#set DESIGN_REF_DATA_PATH        "" ;#  Absolute path prefix variable for library/design data.
                        #  Use this variable to prefix the common absolute path to
                        #  the common variables defined below.
                        #  Absolute paths are mandatory for hierarchical RM flow.
################################################################################
# Hierarchical Flow Design Variables
################################################################################

set HIERARCHICAL_DESIGNS        "" ;# List of hierarchical block design names "DesignA DesignB" ...
set HIERARCHICAL_CELLS          "" ;# List of hierarchical block cell instance names "u_DesignA u_DesignB" ...

################################################################################
# Library Setup Variables
################################################################################
```

```
# For the following variables, use a blank space to separate multiple entries
# Example: set TARGET_LIBRARY_FILES "lib1.db lib2.db lib3.db"

set ADDITIONAL_SEARCH_PATH      " \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "


#clock_gating
set LINK_LIBRARY_FILES_CLG   "* \
${DESIGN_REF_PATH1}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db \
${DESIGN_REF_PATH1}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.db \
${DESIGN_REF_PATH1}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.db "


#clock_gating
set TARGET_LIBRARY_FILES_CLG    " \
${DESIGN_REF_PATH1}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.db \
${DESIGN_REF_PATH1}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.db \
${DESIGN_REF_PATH1}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.db"



set ADDITIONAL_LINK_LIB_FILES     " \
${DESIGN_REF_PATH}/SAED14nm_EDK_SRAM_v_05072020/lib/sra
m/logic_synth/single/saed14sram_ff0p88v125c.db \
saed32io_wb_ff1p16v125c_2p75v.db"



set NDM_REFERENCE_LIB_DIRS_CLG  " \
${DESIGN_REF_PATH}/stdcell_rvt/ndm/saed14rvt_frame_only.ndm \
${DESIGN_REF_PATH}/stdcell_hvt/ndm/saed14hvt_frame_only.ndm \
${DESIGN_REF_PATH}/stdcell_lvt/ndm/saed14lvt_frame_only.ndm \
${DESIGN_REF_PATH}/stdcell_slvt/ndm/saed14slvt_frame_only.ndm"

set MW_REFERENCE_CONTROL_FILE    ""                                  ;#
Reference Control file to define the MW ref libs

set                                                          TECH_FILE
"${DESIGN_REF_PATH}/tech/milkyway/saed14nm_1p9m_mw.tf"       ;#
Milkyway technology file
set                                                           MAP_FILE
"${DESIGN_REF_PATH}/tech/star_rc/saed14nm_tf_itf_tluplus.map"    ;#
Mapping file for TLUplus
```

```
set                                                    TLUPLUS_MAX_FILE
"${DESIGN_REF_PATH}/tech/star_rc/max/saed14nm_1p9m_Cmax.tluplu
s"  ;#  Max TLUplus file
set                                                    TLUPLUS_MIN_FILE
"${DESIGN_REF_PATH}/tech/star_rc/min/saed14nm_1p9m_Cmin.tluplus
"  ;#  Min TLUplus file
set                                                    GDS_MAP_FILE
"${DESIGN_REF_PATH}/tech/milkyway/saed14nm_1p9m_gdsout_mw.m
ap"

set STD_CELL_GDS       " \
${DESIGN_REF_PATH}/stdcell_rvt/gds/saed14rvt.gds \
${DESIGN_REF_PATH}/stdcell_lvt/gds/saed14lvt.gds \
${DESIGN_REF_PATH}/stdcell_hvt/gds/saed14hvt.gds \
${DESIGN_REF_PATH}/stdcell_slvt/gds/saed14slvt.gds "

set NDM_POWER_NET             "VDD" ;#
set NDM_POWER_PORT             "VDD" ;#
set NDM_GROUND_NET             "VSS" ;#
set NDM_GROUND_PORT             "VSS" ;#

set MIN_ROUTING_LAYER          "M2"   ;# Min routing layer
set MAX_ROUTING_LAYER           "M7"   ;# Max routing layer

# M8 and M9 Power routing 9 layer chip design
##RH variable for ICC SAED library and design input data
#set                                                    ICC_INPUT_DATA
"/global/scratch/mculver/PD_fest_2012/initial_design/dhm"

#set LIBRARY_DONT_USE_FILE       "../../DATA_SAED/use_tie.tcl"   ;#
Tcl file with library modifications for dont_use

##################################################################
##############################
# Multi-Voltage Common Variables
#
# Define the following MV common variables for the RM scripts for multi-
voltage flows.
# Use as few or as many of the following definitions as needed by your design.
##################################################################
##############################

set PD1                    ""          ;# Name of power domain/voltage area  1
set PD1_CELLS                    ""            ;# Instances to include in power
domain/voltage area 1
```

```
set VA1_COORDINATES          {}         ;# Coordinates for voltage area
1
set NDM_POWER_NET1           "VDD1"     ;# Power net for voltage area
1
set NDM_POWER_PORT1            "VDD"      ;# Power port for voltage
area 1

set PD2                      ""         ;# Name of power domain/voltage area  2
set PD2_CELLS                ""           ;# Instances to include in power
domain/voltage area 2
set VA2_COORDINATES          {}         ;# Coordinates for voltage area
2
set NDM_POWER_NET2           "VDD2"     ;# Power net for voltage area
2
set NDM_POWER_PORT2            "VDD"      ;# Power port for voltage
area 2

set PD3                      ""         ;# Name of power domain/voltage area  3
set PD3_CELLS                ""           ;# Instances to include in power
domain/voltage area 3
set VA3_COORDINATES          {}         ;# Coordinates for voltage area
3
set NDM_POWER_NET3           "VDD3"     ;# Power net for voltage area
3
set NDM_POWER_PORT3            "VDD"      ;# Power port for voltage
area 3

set PD4                      ""         ;# Name of power domain/voltage area  4
set PD4_CELLS                ""           ;# Instances to include in power
domain/voltage area 4
set VA4_COORDINATES          {}         ;# Coordinates for voltage area
4
set NDM_POWER_NET4           "VDD4"     ;# Power net for voltage area
4
set NDM_POWER_PORT4            "VDD"      ;# Power port for voltage
area 4

puts "RM-Info: Completed script [info script]\n"
```

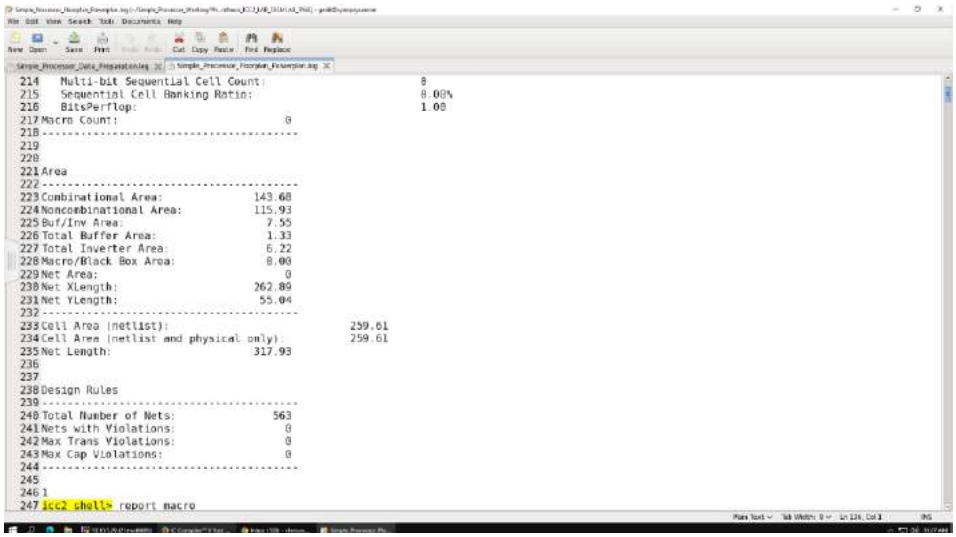
Date:1/6/2022

Section 2 Floorplan and Powerplan

1. Report the following using suitable commands.

Log File Name: Simple_Processor_Floorplan_Powerplan.log

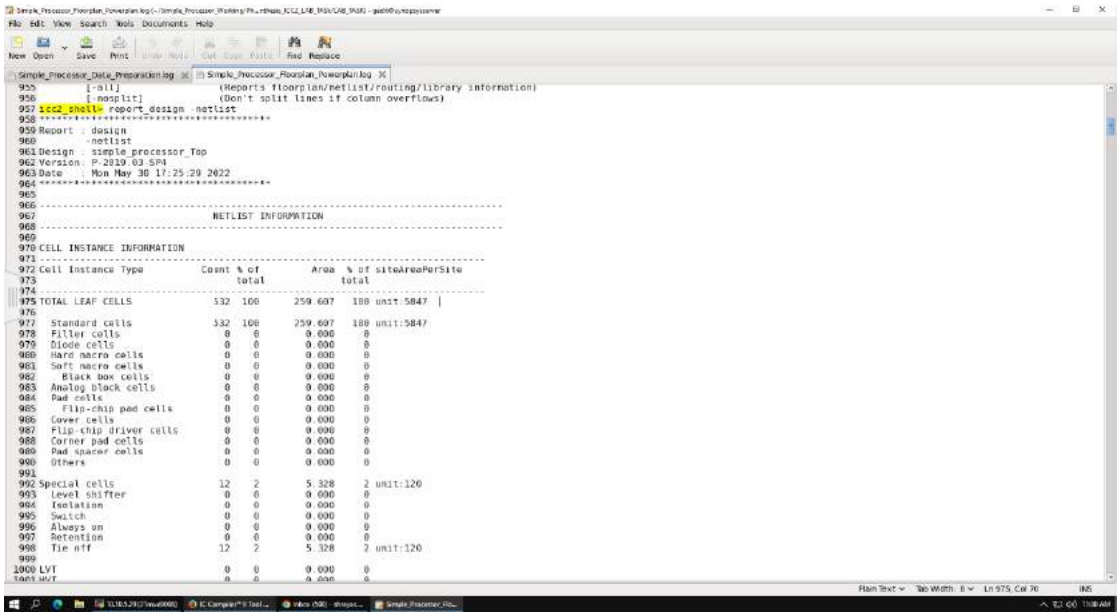
(a) Total Cell area ------- Command : report_qor



```
214   Multi-bit Sequential Cell Count:                    8
215   Sequential Cell Banking Ratio:                  8.00%
216   BitsPerFlop:                                    1.00
217 Macro Count:                          0
218 ---------------------------------------
219
220
221 Area
222 ---------------------------------------
223 Combinational Area:                143.68
224 Noncombinational Area:            115.93
225 Buf/Inv Area:                       7.55
226 Total Buffer Area:                  1.33
227 Total Inverter Area:                6.22
228 Macro/Black Box Area:               8.00
229 Net Area:                              0
230 Net XLength:                      262.89
231 Net YLength:                       55.04
232 ---------------------------------------
233 Cell Area (netlist):                        259.61
234 Cell Area (netlist and physical only):      259.61
235 Net Length:                       317.93
236
237
238 Design Rules
239 ---------------------------------------
240 Total Number of Nets:             563
241 Nets with Violations:               0
242 Max Trans Violations:               0
243 Max Cap Violations:                 0
244 ---------------------------------------
245
246 1
247 icc2_shell> report_macro
```

Figure 2.1: The report_qor gives information about total cell area.

(b) Number of Standard Cells in the design Command : report_design -netlist



```
955         [-all]                  (Reports floorplan/netlist/routing/library information)
956         [-nosplit]              (Don't split lines if column overflows)
957 icc2_shell> report_design -netlist
958 ****************************************
959 Report : design
960         -netlist
961 Design : simple_processor_Top
962 Version: P-2019.03-SP4
963 Date   : Mon May 30 17:25:29 2022
964 ****************************************
965
966 --------------------------------------------------------------------------------
967                              NETLIST INFORMATION
968 --------------------------------------------------------------------------------
969
970 CELL INSTANCE INFORMATION
971 ------------------------------------------------------------------------------
972 Cell Instance Type          Count % of        Area  % of siteAreaPerSite
973                                   total             total
974 ------------------------------------------------------------------------------
975 TOTAL LEAF CELLS              132  100      259.607   100 unit:5847  |
976
977   Standard cells              132  100      259.607   100 unit:5847
978   Filler cells                  0    0        0.000     0
979   Diode cells                   0    0        0.000     0
980   Hard macro cells              0    0        0.000     0
981   Soft macro cells              0    0        0.000     0
982     Black box cells             0    0        0.000     0
983   Analog block cells            0    0        0.000     0
984   Pad cells                     0    0        0.000     0
985     Flip-chip pad cells         0    0        0.000     0
986   Cover cells                   0    0        0.000     0
987   Flip-chip driver cells        0    0        0.000     0
988   Corner pad cells              0    0        0.000     0
989   Pad spacer cells              0    0        0.000     0
990   Others                        0    0        0.000     0
991
992 Special cells                  12    2        5.328     2 unit:120
993   Level shifter                 0    0        0.000     0
994   Isolation                     0    0        0.000     0
995   Switch                        0    0        0.000     0
996   Always on                     0    0        0.000     0
997   Retention                     0    0        0.000     0
998   Tie off                      12    2        5.328     2 unit:120
999
1000 LVT                          0    0        0.000     0
```

Figure 2.2: The report_design -netlist gives information about the Number of Standard cells and other cells included in the design.

(c) Number of Macros --- Command: report_design -netlist

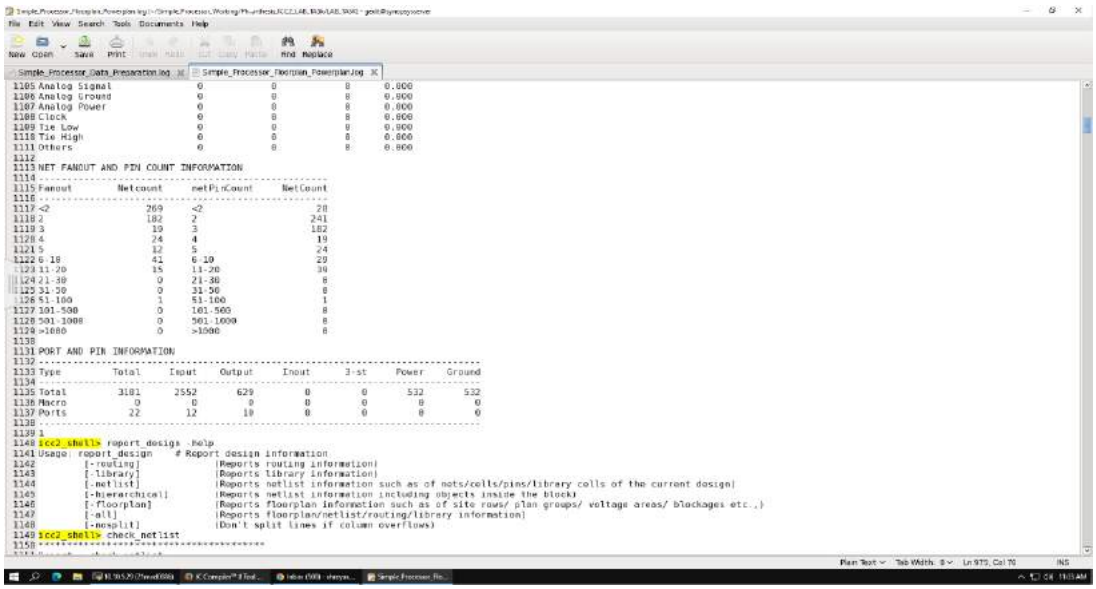


Figure 2.3 : The report_design -netlist command gives the Number of Macros present in the design.

(d) Number of IO Ports ----- Command: report_design -netlist

The Figure 2.3 also shows the Port details.

(e) Pre-Layout timing

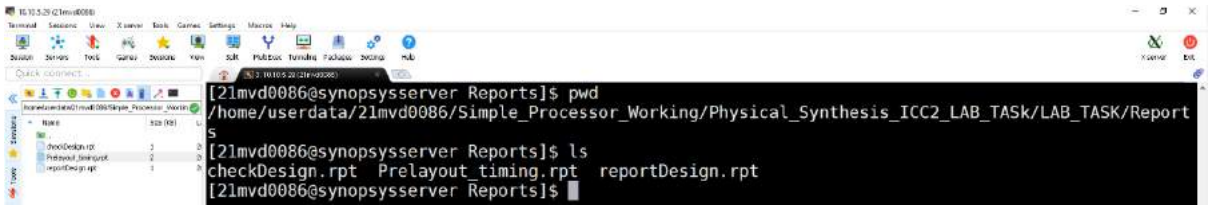
Command :

report_timing -delay_type min > ./Reports/Prelayout_timing.rpt

report_timing -delay_type max >> ./Reports/Prelayout_timing.rpt

report_timing -nworst 1 >> ./Reports/Prelayout_timing.rpt

The File Name is Prelayout_timing.rpt



Log File Name : Simple_Processor_Floorplan_Powerplan.log

2. Create a Floorplan given specifications as follows:

(a) Utilization of the core area of the design is 40%.

(b) Die-edge to core-edge space is equal to 1um.

(c) Let each side of the block be of same length.

Floorplan Steps :

Date:1/6/2022

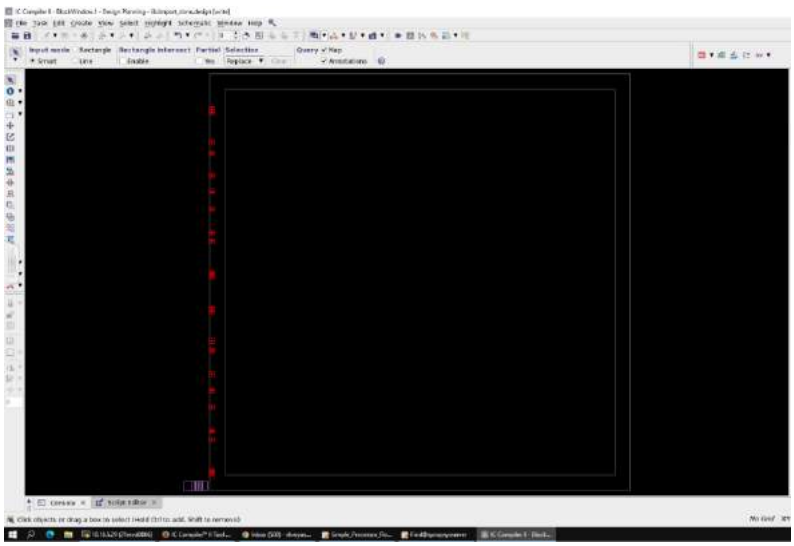


Figure 2.4: The Input and Output pins are placed on the die of chip.

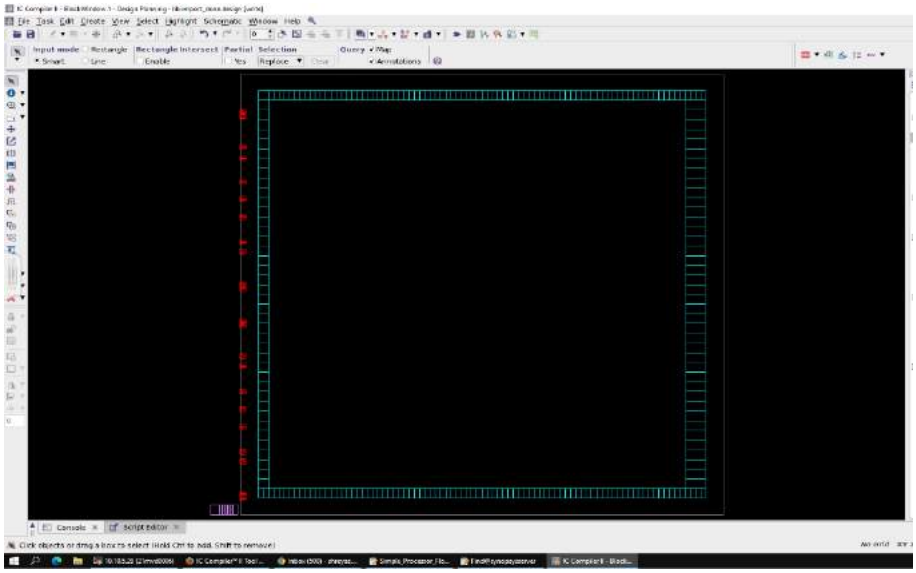


Figure 2.5: The End Cap cells are placed.

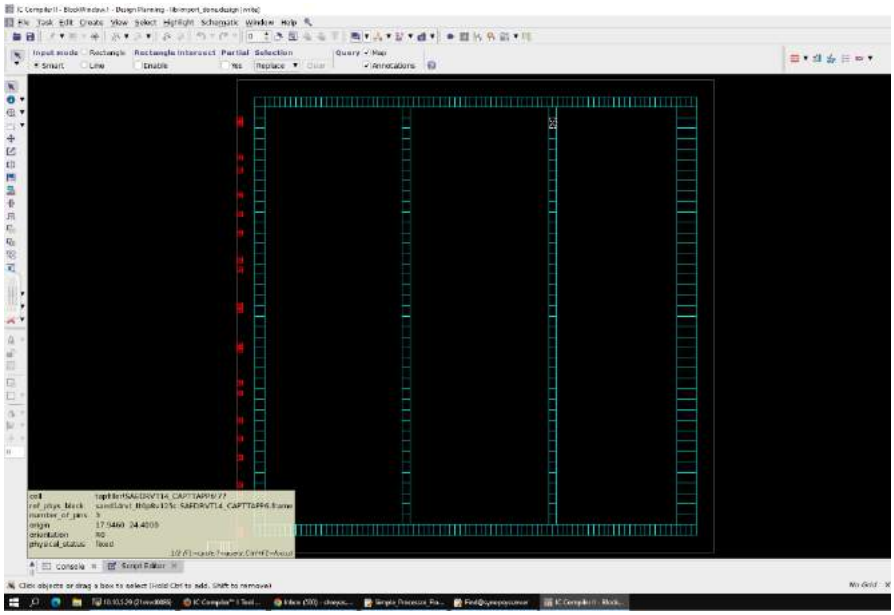


Figure 2.6: The Tap Filler cell placed

Date:1/6/2022

Powerplan:

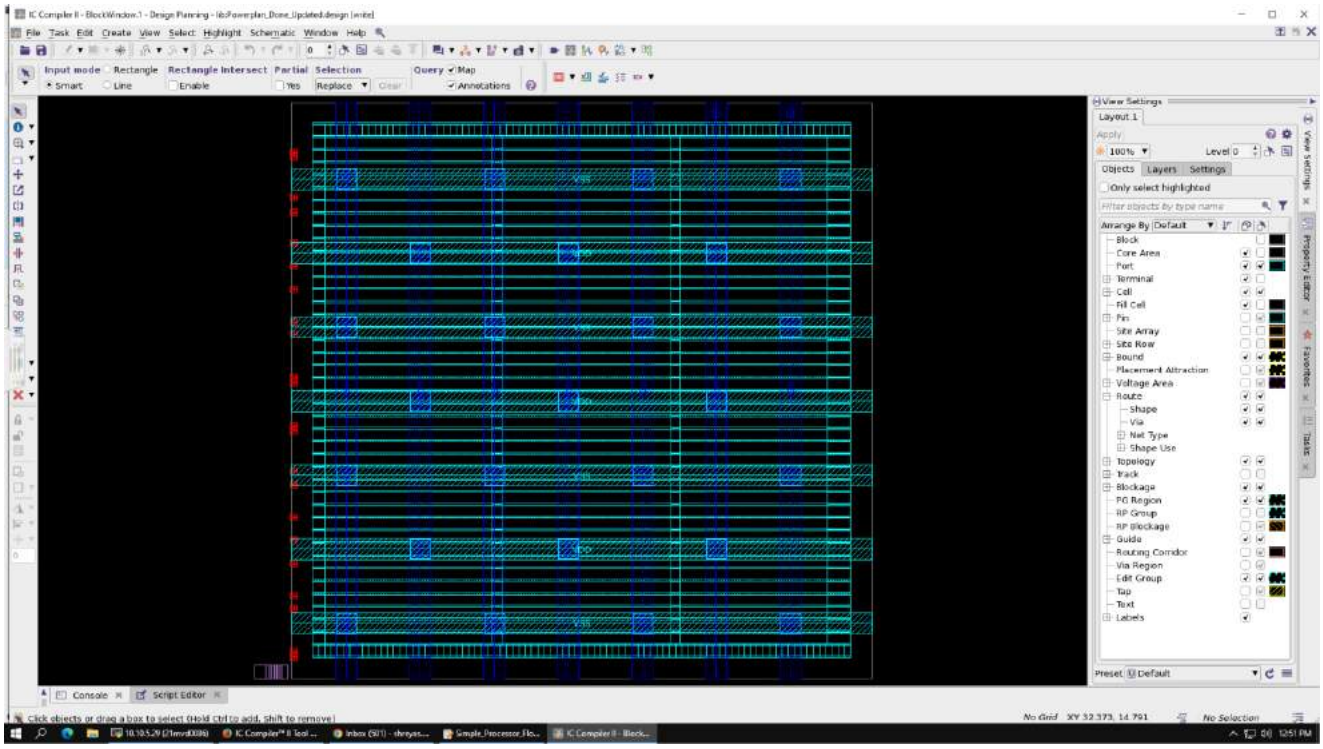


Figure 2.7 : The VDD and VSS power rail are routed in Horizontal and Vertical.

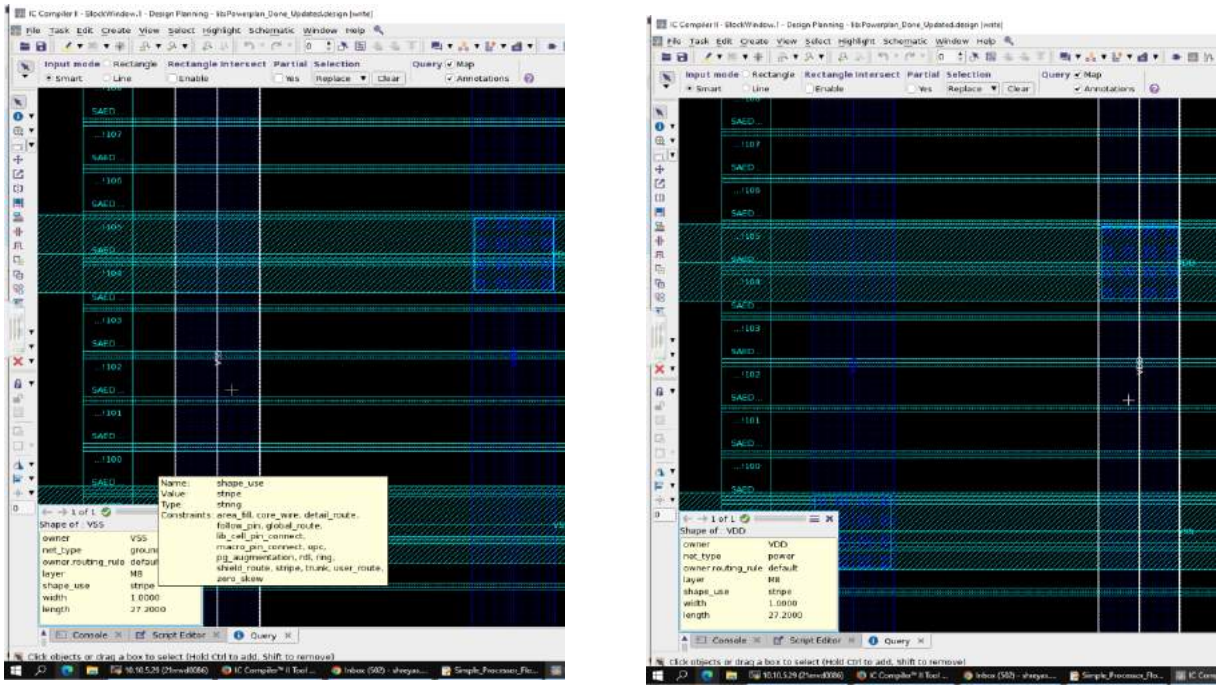


Figure 2.8 : The VDD and VSS power rail are routed in Horizontal and Vertical. The Figure descripts the VDD and VSS width and net details.

The Scripts used are :

1. **Simple_Processor_Floorplan_only.tcl**

```
# SANITY CHECK
#
check_netlist
check_timing
report_design_mismatch -verbose

############## create  shape of Block and proceed with next steps ##########################

initialize_floorplan -core_utilization 0.4 -side_ratio {10 10} -core_offset {1}

# PLACE PINS
#set_block_pin_constraints -self -allowed_layers {M3 M4}
#place_pins -self

#setting pin locations and direction  2=out,,4=in, 1=inout(if available)


set_block_pin_constraints -self -allowed_layers {M4 M5} -sides 1
place_pins -ports [get_ports -filter direction==out]
set_block_pin_constraints -self -allowed_layers {M4 M5} -sides 1
place_pins -ports [get_ports -filter direction==in]

set_app_option -name time.disable_recovery_removal_checks -value false
set_app_option -name time.disable_case_analysis -value false

# fix the ports
set_attribute [get_ports *] physical_status fixed
get_attribute [get_ports *] is_fixed

#ADD END CAP cells
set_boundary_cell_rules                                  -top_boundary_cells
saed14rvt_tt0p8v125c/SAEDRVT14_CAPT2          -bottom_boundary_cells
saed14rvt_tt0p8v125c/SAEDRVT14_CAPB2             -right_boundary_cell
saed14rvt_tt0p8v125c/SAEDRVT14_CAPBIN13          -left_boundary_cell
saed14rvt_tt0p8v125c/SAEDRVT14_CAPBTAP6 -prefix endcap
compile_targeted_boundary_cells -target_objects [get_voltage_areas]

#Add  TAP CELLS
create_tap_cells                                                  -lib_cell
saed14rvt_tt0p8v125c/SAEDRVT14_CAPTTAPP6      -distance      17      -
skip_fixed_cells
```

```
check_legality -cells [get_cells bound*]
check_legality -cells [get_cells tap*]

save_block -as Floorplan_done
close_blocks -f
close_lib
stop_gui
```

2. Simple_Processor_Powerplan_only.tcl

```
## create the PG nets
create_net -power VDD
create_net -ground VSS

## Making Logical Connections
connect_pg_net -net VDD [get_pins -hierarchical "*/VDD"]
connect_pg_net -net VSS [get_pins -hierarchical "*/VSS"]

## Setting up the attribute for TIE cells
set_attribute [get_lib_cells */*TIE*] dont_touch false
set_lib_cell_purpose -include optimization [get_lib_cells */*TIE*]

### creating PG Rails
create_pg_mesh_pattern P_top_two -layers { { {horizontal_layer: M9} {width: 1} {spacing: interleaving} {pitch: 7} {offset: 1.6} {trim : true} } { {vertical_layer: M8}  {width: 1} {spacing: interleaving} {pitch: 7} {offset: 1.6}  {trim : true} } }

set_pg_strategy S_default_vddvss -core -pattern { {name: P_top_two} {nets:{VSS VDD}} } -extension { {{stop:design_boundary_and_generate_pin}} }
compile_pg -strategies {S_default_vddvss}

#### Creating Standard cell rails
create_pg_std_cell_conn_pattern std_rail_conn1 -rail_width 0.094 -layers M1
set_pg_strategy  std_rail_1 -pattern {{name : std_rail_conn1} {nets: "VDD VSS"}} -core
compile_pg -strategies std_rail_1

#### Creation of Vias b/w rails and PG straps
#create_pg_vias -nets {VDD VSS} -from_layers M1 -to_layers M9 -drc no_check

# Check physical Connectivity of PG nets
check_pg_connectivity
```

```
#Check for DRC errors in the design,
check_pg_drc

### saving block
save_block -as Powerplan_Done_Updated
close_block -f
close_lib
stop_gui
```

Date:1/6/2022

Section 3 Placement

(a) Insert End-cap cells, tap-cells, IO port buffers. Place tapcells such that on every row, nwell/pwell will be tied to pwr/gnd respectively at no farther than 17um.

These are inserted during Floor planning.

```
#ADD END CAP cells
set_boundary_cell_rules -top_boundary_cells saed14rvt_tt0p8v125c/SAEDRVT14_CAPT2 -bottom_boundary_cells saed14rvt_tt0p8v125c/SAEDRVT14_CAPB2 -right_boundary_cell saed14rvt_tt0p8v125c/
SAEDRVT14_CAPBIN13 -left_boundary_cell saed14rvt_tt0p8v125c/SAEDRVT14_CAPBTAP6 -prefix endcap
compile_targeted_boundary_cells -target_objects [get_voltage_areas]

#Add  TAP CELLS
create_tap_cells -lib_cell saed14rvt_tt0p8v125c/SAEDRVT14_CAPTTAPP6 -distance 17 -skip_fixed_cells
```

(b) Place the design using congestion driven placement with high effort as the option.

(c) Command : create_placement -congestion -effort high

(d) Once placement is done, check QOR of the design using congestion and timing reports. Note down the over congestion (vertical and horizontal) numbers in the answer sheet. Also, note down the total wire length in the design as estimated by the tool during global route from the log file

The following figure represents the reports. The files are saved in Reports Folder.

```
****************************************
Report : qor
        -summary
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 21:43:37 2022
****************************************

Timing
--------------------------------------------------------------------------------
Context                                WNS             TNS             NVE
--------------------------------------------------------------------------------
func_slow           (Setup)           8.77            0.00               0
Design              (Setup)           8.77            0.00               0

func_fast           (Hold)           -0.10           -9.71              97
Design              (Hold)           -0.10           -9.71              97
--------------------------------------------------------------------------------

Miscellaneous
--------------------------------------------------------------------------------
Cell Area (netlist):                              253.48
Cell Area (netlist and physical only):            346.19
Nets with DRC Violations:       0
1
```

```
****************************************
Report : report_placement
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 21:43:37 2022
****************************************

  Wire length report (all)
  ================
  wire length in design Powerplan_Done_Updated: 2394.802 microns.
  wire length in design Powerplan_Done_Updated (see through blk pins): 2394.802 microns.

  Physical hierarchy violations report
  ====================================
  Violations in design Powerplan_Done_Updated:
     0 cells have placement violation.

  Voltage area violations report
  ==============================
  Voltage area placement violations in design Powerplan_Done_Updated:
     0 cells placed outside the voltage area which they belong to.

Information: Default error view Powerplan_Done_Updated_dpplace.err is created in GUI error browser. (DPP-054)
1
```

```
Placement_design_library.rpt (~/Simple_Processer_Working/Physical...hesis_ICC2_LAB_TASK/LAB_TASK/Reports) - gedit@synopsysserver
File  Edit  View  Search  Tools  Documents  Help
New  Open  Save  Print  Undo  Redo  Cut  Copy  Paste  Find  Replace
Simple_Processor_Floorplan_only.tcl  CTS_LAB_TASK.tcl  Placement_timing.rpt  Placemer
```

```
****************************************
Report : design
        -library
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 21:43:37 2022
****************************************
--------------------------------------------------------------------------------
                            LIBRARY INFORMATION
--------------------------------------------------------------------------------

Search path : .

Units :
    time                : 1.00ns
    resistance          : 1.00MOhm
    capacitance         : 1.00fF
    voltage             : 1.00V
    current             : 1.00uA
    power               : 1.00pW

Tech file : /home/synopsys/SAED14nm_EDK/tech/milkyway/saed14nm_lp9m_mw.tf

Number of active scenarios      = 2
Number of inactive scenarios    = 0

Total number of standard cells  = 2643

Total number of dont_use lib cells      = 54
Total number of dont_touch lib cells    = 54

Total number of buffers         = 177
Total number of inverters       = 153
Total number of flip-flops      = 513
Total number of latches         = 135
Total number of ICGs            = 90
```

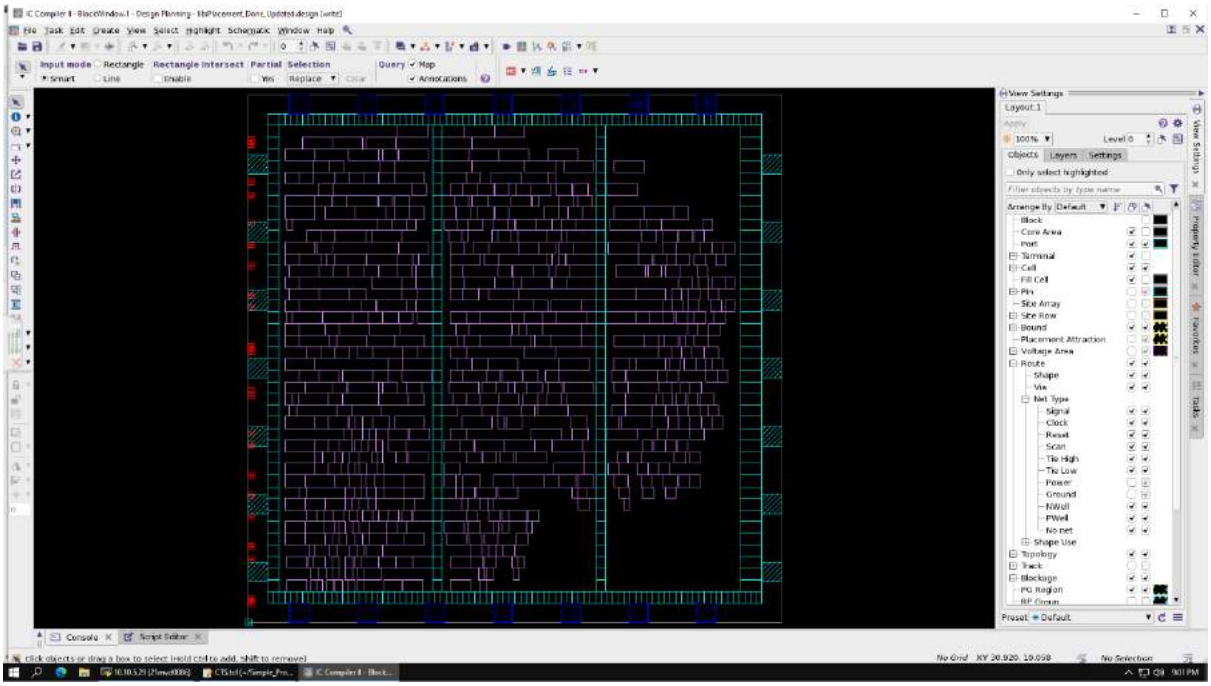


Figure 3.1 The Figure shows after legalize_placement. The standard cell placement.

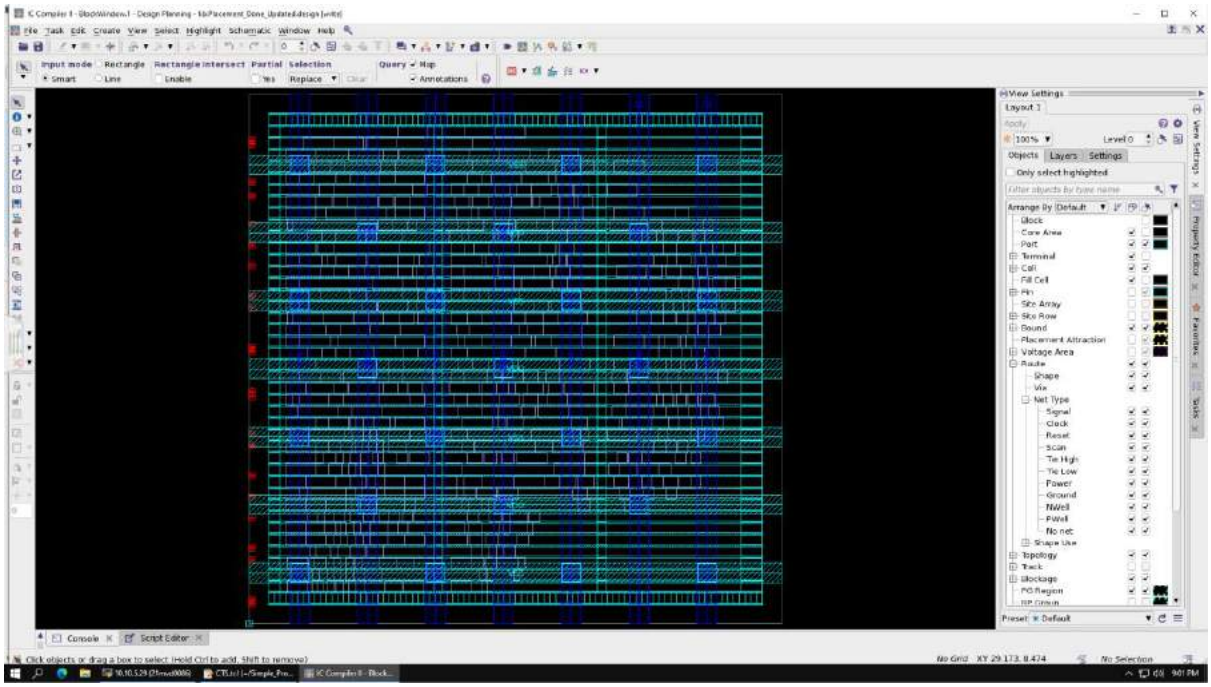


Figure 3.2 The Figure shows after legalize_placement. The standard cell placement with Power planning.

The Script used is **Simple_Processor_Placement.tcl**

```
#add_buffer [get_nets -of [get_ports *]] [get_lib_cells */SAEDRVT14_BUF_20]
#magnet_plalcement [get_ports *]
#set_attribute [get_cells eco_cel*] physical_status fixed

#After Powerplan done do check_design below command
check_design -checks pre_placement_stage

# No Scan Def design in our file
set_app_options -name place.coarse.continue_on_missing_scandef -value true

##placement density setting
#Specify a maximum density that controls how densely the tool can place cells in uncongested areas during wire-length-driven placement
set_app_options -name place.coarse.max_density -value 0.6

#Specify a maximum utilization that controls how densely the tool can place cells in less congested areas that surround highly congested areas, so
#that the cells in the congested areas can be spread out to reduce the congestion
set_app_options -name place.coarse.congestion_driven_max_util -value 0.6

#to analyze all cells have proper or legal location
analyze_lib_cell_placement -lib_cells *
#for placement of cells

create_placement -congestion -effort high
#route_global -floorplan true -effort_level high

#set RC delay for timings which were set during "DATA PREPARATION"
set_parasitic_parameters -early_spec best_para
```

```
set_parasitic_parameters -late_spec worst_para


check_legality -verbose
legalize_placement
check_legality -verbose
report_qor -summary
set_attribute [get_lib_cells */*LVT*] threshold_voltage_group LVT
set_threshold_voltage_group_type -type low_vt LVT
#set_multi_vth_constraint -low_vt_percentage 5 -cost cell_count
analyze_design_violations
#for OPTIMIZATION
place_opt -to final_opto
#TIMING REPORT
report_qor -summary > ./Reports/Placement_qor.rpt
report_timing > ./Reports/Placement_timing.rpt
report_placement > ./Reports/Placement_placement_report.rpt
report_design -routing > ./Reports/Placement_design_routing.rpt
report_design -library > ./Reports/Placement_design_library.rpt
report_design -all > ./Reports/Placement_design_all.rpt
save_block -as Placement_Done_Updated
close_blocks -f
close_lib lib
stop_gui
```

Date:1/6/2022

Section 4 : Clock Tree Analysis (CTS)

(a) **Case 1 :** Use only clock INVERTER cells with all drive strengths and route the clock tree with double width and double-spacing routing rules

Capture the following metrics from each run

- Inst Count
- Buf/Inv Count
- Congestion number post Clock routing
- Insertion Delay
- Skew
- Clock-Cell Count
- No. of Levels in the clock tree

Clock Inverter

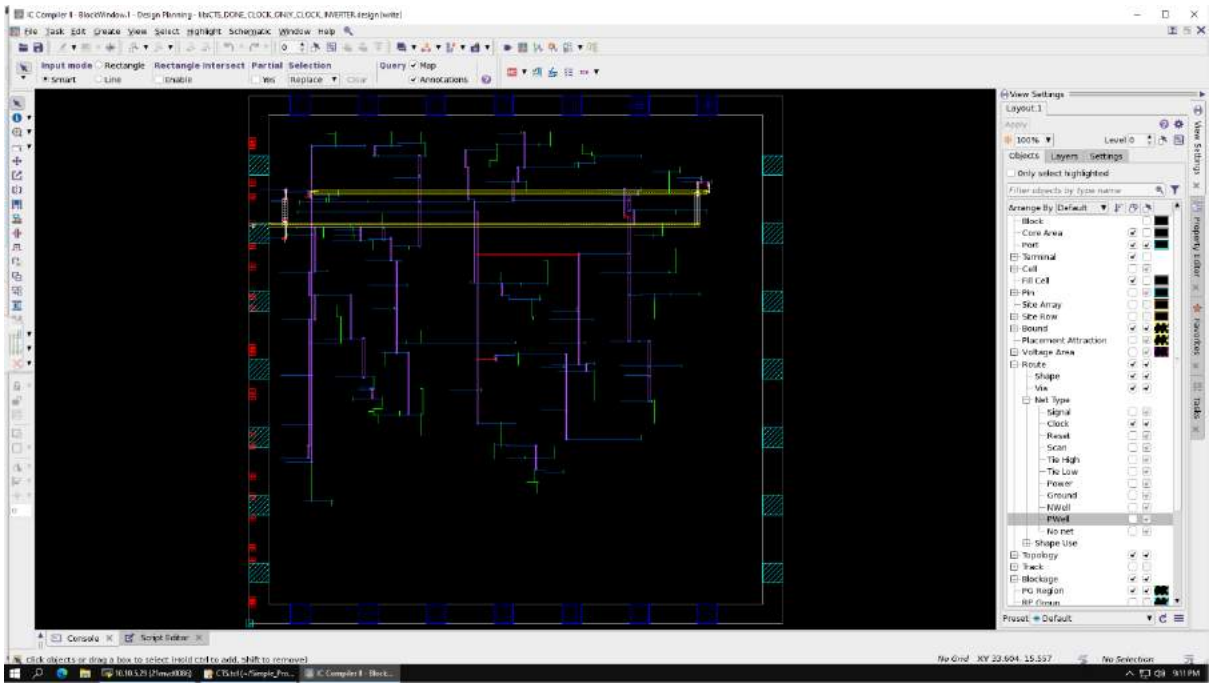


Figure 4.1 The Clock tree synthesis using inserting clock inverter.

The Following figures gives various report for mentioned question. The reports are saved in Reports folder. **Date:1/6/2022**

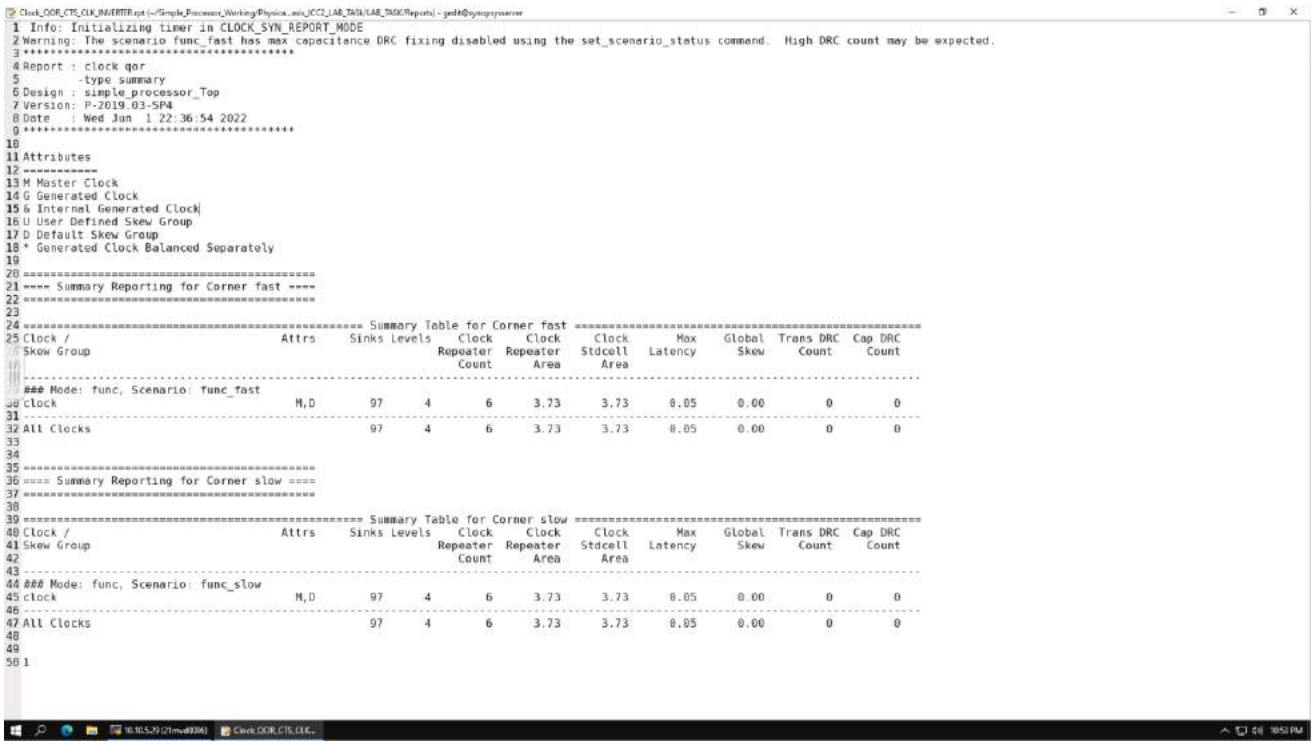
```
Report : timing
        -path_type full
        -delay_type min
        -max_paths 1
        -report_by design
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:37:32 2022

  Startpoint: G2_Datapath/Reg2/dout_reg_2_ (rising edge-triggered flip-flop clocked by clock)
  Endpoint: G2_Datapath/Reg2/dout_reg_2_ (rising edge-triggered flip-flop clocked by clock)
  Mode: func
  Corner: fast
  Scenario: func_fast
  Path Group: CLOCK
  Path Type: min

  Point                                                   Incr       Path
  ---------------------------------------------------------------------------
  clock clock (rise edge)                                 0.00       0.00
  clock network delay (propagated)                        1.05       1.05

  G2_Datapath/Reg2/dout_reg_2_/CK (SAEDHVT14_FDP_V2LP_1)
                                                          0.00       1.05 r
  G2_Datapath/Reg2/dout_reg_2_/Q (SAEDHVT14_FDP_V2LP_1)
                                                          0.03       1.08 r
  G2_Datapath/Reg2/copt_h_inst_10031/X (SAEDHVT14_DEL_R2V3_1)
                                                          0.03       1.11 r
  G2_Datapath/Reg2/copt_h_inst_10033/X (SAEDHVT14_DEL_R2V2_1)
                                                          0.03       1.14 r
  G2_Datapath/Reg2/copt_h_inst_10032/X (SAEDHVT14_DEL_R2V3_1)
                                                          0.03       1.17 r
  G2_Datapath/Reg2/U10/X (SAEDHVT14_A032_4)               0.03       1.20 r
  G2_Datapath/Reg2/dout_reg_2_/D (SAEDHVT14_FDP_V2LP_1)
                                                          0.00       1.20 r
  data arrival time                                                  1.20

  clock clock (rise edge)                                 0.00       0.00
  clock network delay (propagated)                        1.05       1.05
  G2_Datapath/Reg2/dout_reg_2_/CK (SAEDHVT14_FDP_V2LP_1)
                                                          0.00       1.05 r
  clock uncertainty                                       0.15       1.20
  library hold time                                      -0.00       1.20
  data required time                                                 1.20
  ---------------------------------------------------------------------------
  data required time                                                 1.20
  data arrival time                                                 -1.20
  ---------------------------------------------------------------------------
  slack (MET)                                                        0.00
```

```
Startpoint: Run (input port clocked by clock)
Endpoint: G1_Controller/PS_reg_0_ (rising edge-triggered flip-flop clocked by clock)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: INPUTS
Path Type: max

Point                                                   Incr       Path
---------------------------------------------------------------------------
clock clock (rise edge)                                 0.00       0.00
clock network delay (ideal)                             1.05       1.05
input external delay                                    1.00       2.05

Run (in)                                                0.00       2.06 r
G1_Controller/U50/X (SAEDRVT14_ND2_MM_16)               0.00       2.06 f
G1_Controller/copt_h_inst_10049/X (SAEDHVT14_DEL_R2V3_1)
                                                        0.03       2.09 f
G1_Controller/U14/X (SAEDRVT14_INV_S_0P5)               0.03       2.13 r
G1_Controller/U54/X (SAEDHVT14_NR2_MM_0P5)              0.02       2.14 f
G1_Controller/U56/X (SAEDHVT14_OR4_1)                   0.02       2.17 f
G1_Controller/copt_h_inst_10077/X (SAEDHVT14_DEL_R2V3_1)
                                                        0.04       2.20 f
G1_Controller/copt_h_inst_10076/X (SAEDHVT14_DEL_R2V3_2)
                                                        0.03       2.23 f
G1_Controller/PS_reg_0_/D (SAEDHVT14_FDP_V2LP_0P5)
                                                        0.00       2.23 f
data arrival time                                                  2.23

clock clock (rise edge)                                10.00      10.00
clock network delay (propagated)                        1.05      11.05
G1_Controller/PS_reg_0_/CK (SAEDHVT14_FDP_V2LP_0P5)
                                                        0.00      11.05 r
clock uncertainty                                      -0.15      10.90
library setup time                                     -0.01      10.89
data required time                                                10.89
---------------------------------------------------------------------------
data required time                                                10.89
data arrival time                                                 -2.23
---------------------------------------------------------------------------
slack (MET)                                                        8.66
```

```
Report : qor
        -summary
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:37:10 2022

Timing
-------------------------------------------------------------------------------
Context                                 WNS             TNS             NVE
-------------------------------------------------------------------------------
func_slow          (Setup)             8.66            0.00               0
Design             (Setup)             8.66            0.00               0

func_fast          (Hold)              0.00            0.00               0
Design             (Hold)              0.00            0.00               0
-------------------------------------------------------------------------------

Miscellaneous
-------------------------------------------------------------------------------
Cell Area (netlist):                              421.13
Cell Area (netlist and physical only):            513.84
Nets with DRC Violations:       0
```

```
Cell Count
---------------------------------------
Hierarchical Cell Count:            78
Hierarchical Port Count:           991
Leaf Cell Count:                   874
Buf/Inv Cell Count:                394
Buf Cell Count:                    354
Inv Cell Count:                     40
CT Buf/Inv Cell Count:               0
Combinational Cell Count:          736
Sequential Cell Count:             138
   Integrated Clock-Gating Cell Count:                       0
   Sequential Macro Cell Count:                              0
   Single-bit Sequential Cell Count:                       138
   Multi-bit Sequential Cell Count:                          0
   Sequential Cell Banking Ratio:                       0.00%
   BitsPerFlop:                                          1.00
Macro Count:                        0
---------------------------------------


Area
---------------------------------------
Combinational Area:           305.21
Noncombinational Area:        115.93
Buf/Inv Area:                 143.77
Total Buffer Area:            132.62
Total Inverter Area:           11.14
Macro/Black Box Area:           0.00
Net Area:                          0
Net XLength:                  234.44
Net YLength:                  137.93
---------------------------------------
Cell Area (netlist):                              421.13
Cell Area (netlist and physical only):            513.84
Net Length:                   372.36


Design Rules
---------------------------------------
Total Number of Nets:             893
Nets with Violations:               0
Max Trans Violations:               0
Max Cap Violations:                 0
---------------------------------------
```

```
*****************************************
 Report : target skew and latency
 Design : simple_processor_Top
 Date   : Wed Jun  1 22:36:38 2022
*****************************************

##Target Skew

Clock                          Corner                          Target
-----------------------------------------------------------------------
clock (mode func)              fast                            2
clock (mode func)              slow                            2

##Target Latency

Clock                          Corner                          Target
-----------------------------------------------------------------------
clock (mode func)              fast                            0.05

##Max Level Count

Clock                                  Count
-----------------------------------------------------------------------
No max level constraints found.

##Root NDR Fanout Limit

Clock                                  Fanout limit
-----------------------------------------------------------------------
No Root NDR fanout limit constraints applied.
```



```
Info: Initializing timer in CLOCK_SYN_REPORT_MODE
Warning: The scenario func_fast has max capacitance DRC fixing disabled using the set_scenario_status command.  High DRC count may be expected.
****************************************
Report : clock qor
         -type summary
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:36:54 2022
****************************************

Attributes
----------
M Master Clock
G Generated Clock
& Internal Generated Clock
U User Defined Skew Group
D Default Skew Group
* Generated Clock Balanced Separately

============================================
==== Summary Reporting for Corner fast ====
============================================

================================================ Summary Table for Corner fast ================================================
Clock /                                  Attrs     Sinks Levels    Clock      Clock      Clock        Max     Global  Trans DRC  Cap DRC
Skew Group                                                       Repeater  Repeater   Stdcell    Latency      Skew      Count     Count
                                                                   Count       Area      Area
------------------------------------------------------------------------------------------------------------------------------------
### Mode: func, Scenario: func_fast
clock                                    M,D       97     4         6      3.73       3.73       0.05      0.00          0         0
------------------------------------------------------------------------------------------------------------------------------------
All Clocks                                         97     4         6      3.73       3.73       0.05      0.00          0         0


============================================
==== Summary Reporting for Corner slow ====
============================================

================================================ Summary Table for Corner slow ================================================
Clock /                                  Attrs     Sinks Levels    Clock      Clock      Clock        Max     Global  Trans DRC  Cap DRC
Skew Group                                                       Repeater  Repeater   Stdcell    Latency      Skew      Count     Count
                                                                   Count       Area      Area
------------------------------------------------------------------------------------------------------------------------------------
### Mode: func, Scenario: func_slow
clock                                    M,D       97     4         6      3.73       3.73       0.05      0.00          0         0
------------------------------------------------------------------------------------------------------------------------------------
All Clocks                                         97     4         6      3.73       3.73       0.05      0.00          0         0


1
```

Figure 4.2 : The figure gives report on clock_qor.

Case 2 : Clock Only Buffer

Use only clock Buffer cells with all drive strengths and route the clock tree with double width and double-spacing routing rules

Capture the following metrics from each run

- Inst Count
- Buf/Inv Count
- Congestion number post Clock routing
- Insertion Delay
- Skew
- Clock-Cell Count
- No. of Levels in the clock tree

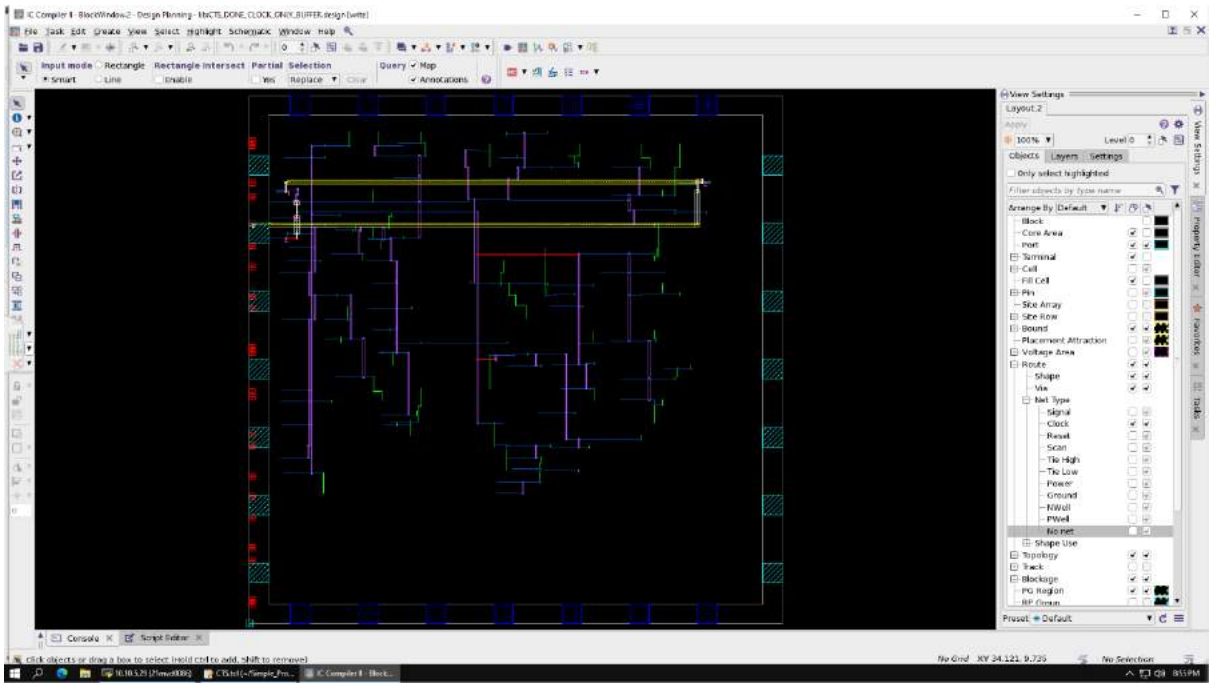
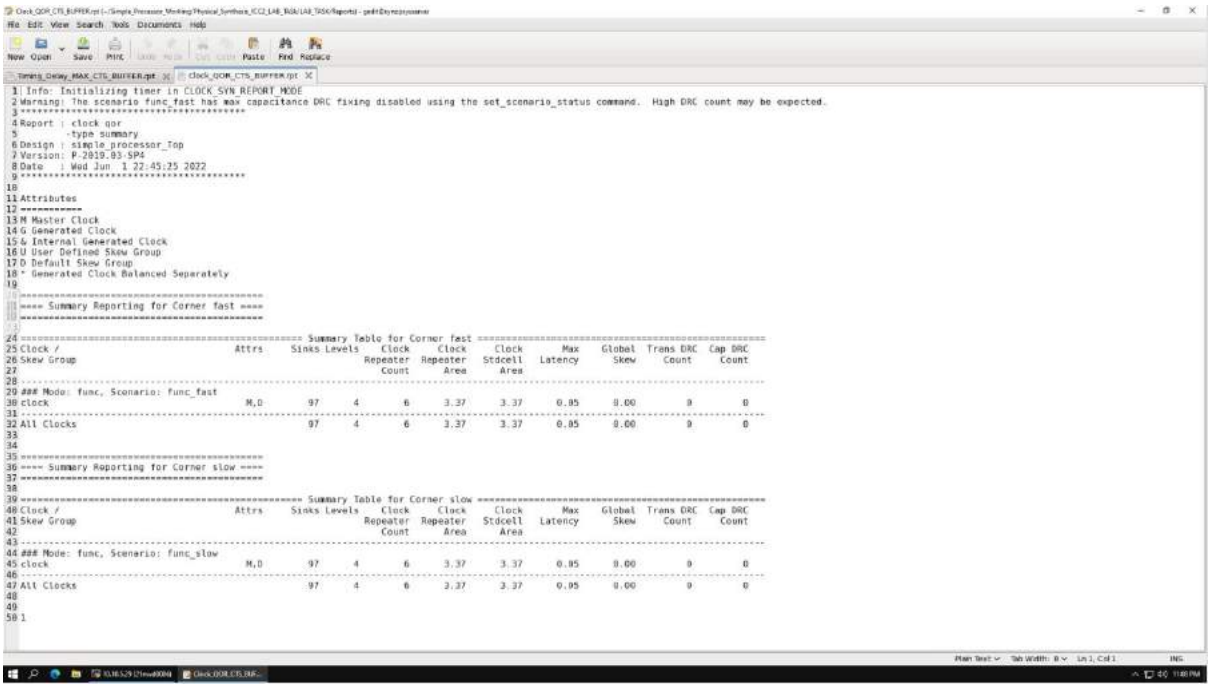
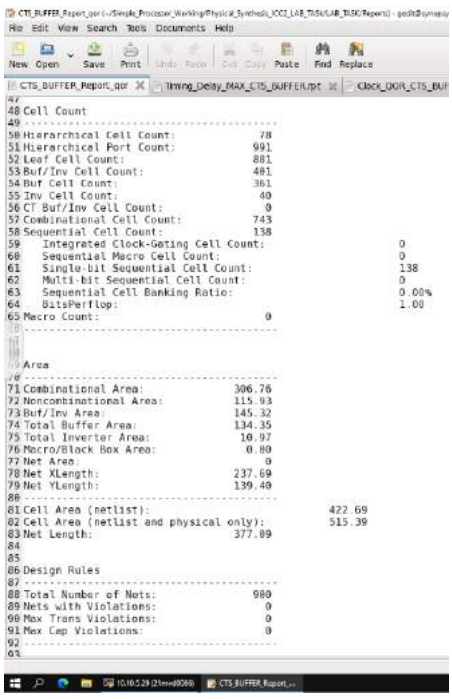


Figure 4.3 : The figure shows CTS using Buffers.



```
Info: Initializing timer in CLOCK_SYN_REPORT_MODE
Warning: The scenario func_fast has max capacitance DRC fixing disabled using the set_scenario_status command.  High DRC count may be expected.
****************************************
Report : clock qor
        -type summary
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:45:25 2022
****************************************

Attributes
----------
M Master Clock
G Generated Clock
& Internal Generated Clock
U User Defined Skew Group
D Default Skew Group
* Generated Clock Balanced Separately

****************************************
==== Summary Reporting for Corner fast ====
****************************************

                                  ============================== Summary Table for Corner fast ==============================
Clock /                                Attrs    Sinks Levels    Clock    Clock    Clock      Max   Global  Trans DRC  Cap DRC
Skew Group                                                     Repeater  Repeater  Stdcell  Latency   Skew    Count     Count
                                                                 Count     Area      Area
-------------------------------------------------------------------------------------------------------------------------------
### Mode: func, Scenario: func_fast
clock                                  M,D      97      4        6      3.37      3.37     0.05     0.00       0         0
-------------------------------------------------------------------------------------------------------------------------------
All Clocks                                      97      4        6      3.37      3.37     0.05     0.00       0         0


****************************************
==== Summary Reporting for Corner slow ====
****************************************

                                  ============================== Summary Table for Corner slow ==============================
Clock /                                Attrs    Sinks Levels    Clock    Clock    Clock      Max   Global  Trans DRC  Cap DRC
Skew Group                                                     Repeater  Repeater  Stdcell  Latency   Skew    Count     Count
                                                                 Count     Area      Area
-------------------------------------------------------------------------------------------------------------------------------
### Mode: func, Scenario: func_slow
clock                                  M,D      97      4        6      3.37      3.37     0.05     0.00       0         0
-------------------------------------------------------------------------------------------------------------------------------
All Clocks                                      97      4        6      3.37      3.37     0.05     0.00       0         0


1
```

Figure 4.4 : The figure gives clock_qor for CTS using Buffers.



```
Cell Count
----------------------------------------
Hierarchical Cell Count:             78
Hierarchical Port Count:            991
Leaf Cell Count:                    881
Buf/Inv Cell Count:                 481
Buf Cell Count:                     361
Inv Cell Count:                      40
CT Buf/Inv Cell Count:                0
Combinational Cell Count:           743
Sequential Cell Count:              138
   Integrated Clock-Gating Cell Count:                0
   Sequential Macro Cell Count:                       0
   Single-bit Sequential Cell Count:                138
   Multi-bit Sequential Cell Count:                   0
   Sequential Cell Banking Ratio:                  0.00%
   BitsPerFlop:                                    1.00
Macro Count:                         0
----------------------------------------


Area
----------------------------------------
Combinational Area:             306.76
Noncombinational Area:          115.93
Buf/Inv Area:                   145.32
Total Buffer Area:              134.35
Total Inverter Area:             10.97
Macro/Block Box Area:             0.00
Net Area:                            0
Net XLength:                    237.69
Net YLength:                    139.40
----------------------------------------
Cell Area (netlist):                     422.69
Cell Area (netlist and physical only):   515.39
Net Length:                     377.09


Design Rules
----------------------------------------
Total Number of Nets:           980
Nets with Violations:             0
Max Trans Violations:             0
Max Cap Violations:               0
----------------------------------------
```

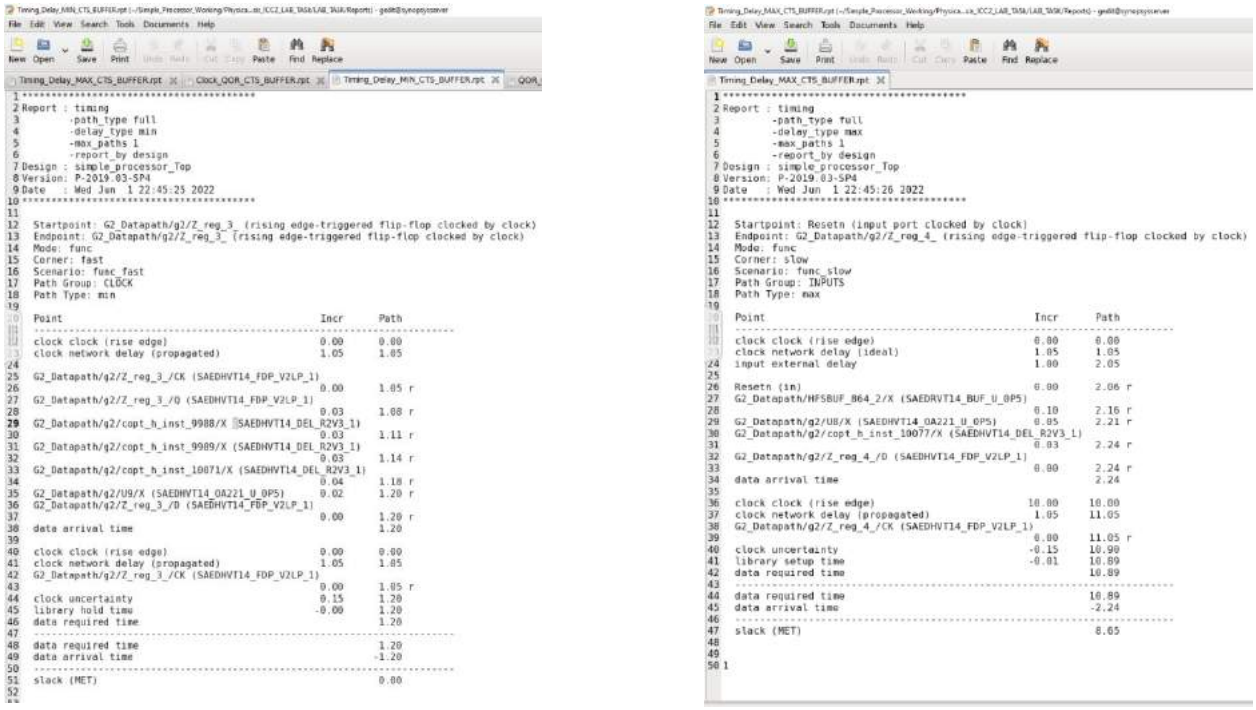
(a)

```
Timing_Delay_MAX_CTS_BUFFER.rpt | Clock_QOR_CTS_BUFFER.rpt | Constraints_CTS_BUFFER.rpt | Timing_Delay_MIN_CTS_BUFFER.rpt

****************************************
Report : constraint
        -all_violators
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:45:25 2022
****************************************

   late_timing
   -----------

Error: None of the specified scenarios are active for setup analysis. (UIC-057)
Endpoint                          Path Delay     Path Required       CRP    Slack Group    Scenario
--------------------------------------------------------------------------------------------------
No paths.

   early_timing
   -----------

Endpoint                          Path Delay     Path Required       CRP    Slack Group    Scenario
--------------------------------------------------------------------------------------------------
No paths.

   Mode: func Corner: fast
   Scenario: func_fast
   max_transition

                                  Required        Actual
   Net                           Transition     Transition        Slack  Violation
   -------------------------------------------------------------------------------
   Bus[0]                           0.50           0.15           0.35  (MET)

   -------------------------------------------------------------------------------
   Number of max_transition violation(s): 0


   Mode: func Corner: fast
   Scenario: func_fast
   -------------------------------------------------------------------------------
   Number of min_capacitance violation(s): 0

   Total number of violation(s): 0
```

(b)

Figure 4.5 : (a) The figure gives cell count, area after CTS done using Buffers.

(b) The figure gives constraint violations



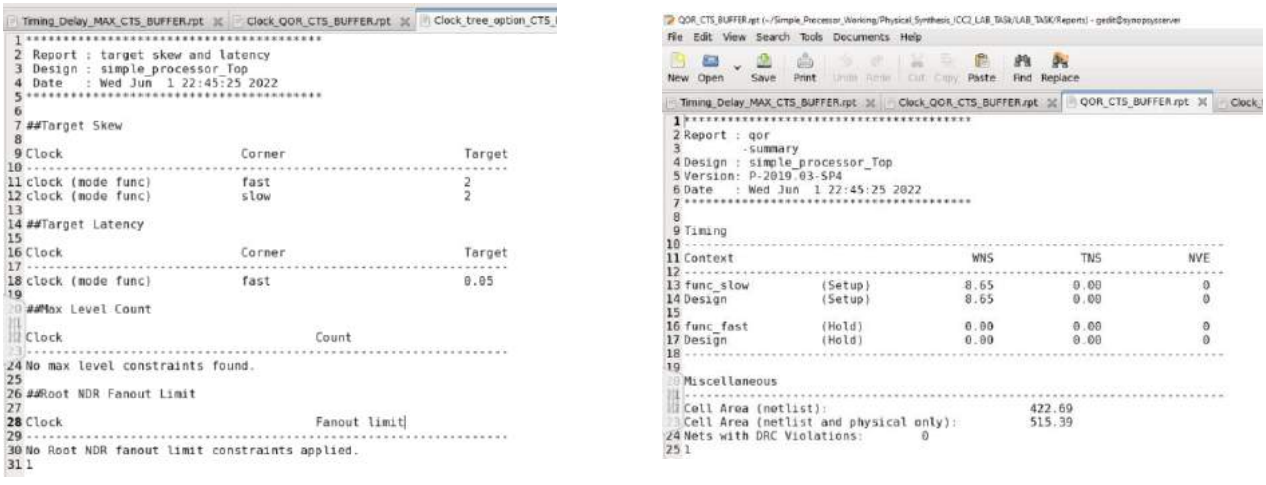
```
Report : timing
        -path_type full
        -delay_type min
        -max_paths 1
        -report_by design
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:45:25 2022

Startpoint: G2_Datapath/g2/Z_reg_3_ (rising edge-triggered flip-flop clocked by clock)
Endpoint: G2_Datapath/g2/Z_reg_3_ (rising edge-triggered flip-flop clocked by clock)
Mode: func
Corner: fast
Scenario: func_fast
Path Group: CLOCK
Path Type: min

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock clock (rise edge)                                 0.00       0.00
clock network delay (propagated)                        1.05       1.05

G2_Datapath/g2/Z_reg_3_/CK (SAEDHVT14_FDP_V2LP_1)
                                                        0.00       1.05 r
G2_Datapath/g2/Z_reg_3_/Q (SAEDHVT14_FDP_V2LP_1)
                                                        0.03       1.08 r
G2_Datapath/g2/copt_h_inst_9988/X (SAEDHVT14_DEL_R2V3_1)
                                                        0.03       1.11 r
G2_Datapath/g2/copt_h_inst_9989/X (SAEDHVT14_DEL_R2V3_1)
                                                        0.03       1.14 r
G2_Datapath/g2/copt_h_inst_10071/X (SAEDHVT14_DEL_R2V3_1)
                                                        0.04       1.18 r
G2_Datapath/g2/U9/X (SAEDHVT14_OA221_U_0P5)             0.02       1.20 r
G2_Datapath/g2/Z_reg_3_/D (SAEDHVT14_FDP_V2LP_1)
                                                        0.00       1.20 r
data arrival time                                                  1.20

clock clock (rise edge)                                 0.00       0.00
clock network delay (propagated)                        1.05       1.05
G2_Datapath/g2/Z_reg_3_/CK (SAEDHVT14_FDP_V2LP_1)
                                                        0.00       1.05 r
clock uncertainty                                       0.15       1.20
library hold time                                      -0.00       1.20
data required time                                                 1.20
-----------------------------------------------------------------------
data required time                                                 1.20
data arrival time                                                 -1.20
-----------------------------------------------------------------------
slack (MET)                                                        0.00
```

```
Report : timing
        -path_type full
        -delay_type max
        -max_paths 1
        -report_by design
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:45:26 2022

Startpoint: Resetn (input port clocked by clock)
Endpoint: G2_Datapath/g2/Z_reg_4_ (rising edge-triggered flip-flop clocked by clock)
Mode: func
Corner: slow
Scenario: func_slow
Path Group: INPUTS
Path Type: max

Point                                                   Incr       Path
-----------------------------------------------------------------------
clock clock (rise edge)                                 0.00       0.00
clock network delay (ideal)                             1.05       1.05
input external delay                                    1.00       2.05

Resetn (in)                                             0.00       2.06 r
G2_Datapath/HFSBUF_864_2/X (SAEDRVT14_BUF_U_0P5)
                                                        0.10       2.16 r
G2_Datapath/g2/U8/X (SAEDHVT14_OA221_U_0P5)             0.05       2.21 r
G2_Datapath/g2/copt_h_inst_10077/X (SAEDHVT14_DEL_R2V3_1)
                                                        0.03       2.24 r
G2_Datapath/g2/Z_reg_4_/D (SAEDHVT14_FDP_V2LP_1)
                                                        0.00       2.24 r
data arrival time                                                  2.24

clock clock (rise edge)                                10.00      10.00
clock network delay (propagated)                        1.05      11.05
G2_Datapath/g2/Z_reg_4_/CK (SAEDHVT14_FDP_V2LP_1)
                                                        0.00      11.05 r
clock uncertainty                                      -0.15      10.90
library setup time                                     -0.01      10.89
data required time                                                10.89
-----------------------------------------------------------------------
data required time                                                10.89
data arrival time                                                 -2.24
-----------------------------------------------------------------------
slack (MET)                                                        8.65
```

(a) (b)

Figure 4.6 : (a) The Figure represents report_timing -delay_type -max.

(b) The Figure represents report_timing -delay_type -min.



```
Report : target skew and latency
Design : simple_processor_Top
Date   : Wed Jun  1 22:45:25 2022

##Target Skew

Clock                           Corner                          Target
-----------------------------------------------------------------------
clock (mode func)               fast                            2
clock (mode func)               slow                            2

##Target Latency

Clock                           Corner                          Target
-----------------------------------------------------------------------
clock (mode func)               fast                            0.05

##Max Level Count

Clock                                   Count
-----------------------------------------------------------------------
No max level constraints found.

##Root NDR Fanout Limit

Clock                                   Fanout limit
-----------------------------------------------------------------------
No Root NDR fanout limit constraints applied.
1
```

```
Report : qor
        -summary
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Wed Jun  1 22:45:25 2022

Timing
-----------------------------------------------------------------------------
Context                         WNS             TNS             NVE
-----------------------------------------------------------------------------
func_slow           (Setup)     8.65            0.00            0
Design              (Setup)     8.65            0.00            0

func_fast           (Hold)      0.00            0.00            0
Design              (Hold)      0.00            0.00            0
-----------------------------------------------------------------------------

Miscellaneous
-----------------------------------------------------------------------------
Cell Area (netlist):                          422.69
Cell Area (netlist and physical only):        515.39
Nets with DRC Violations:       0
1
```

(a) (b)

Figure 4.7 : (a) The figure gives report on Skew and Latency.

(b) The figure gives report on report_qor.

The script used for **CTS_LAB_TASK.tcl**

```
#Before performing CTS, execute the following command and analyze the report

check_design -checks pre_clock_tree_stage

# set NDR

#create_routing_rule  clk_rule -widths  {M6 0.224 M7 0.224 } -spacings  {M6 0.224 M7 0.224 }

create_routing_rule  clk_rule -widths  {M6 0.224 M7 0.224 } -spacings  {M6 0.336 M7 0.336 }

#check_clock_tree

# specify clock tree cell list

set_lib_cell_purpose -exclude cts [get_lib_cells]

# INVERTER

#set_lib_cell_purpose -include cts [get_lib_cells
"saed14rvt_tt0p8v125c/SAEDRVT14_INV_S_4
saed14rvt_tt0p8v125c/SAEDRVT14_INV_S_4
saed14rvt_tt0p8v125c/SAEDRVT14_INV_S_6
saed14rvt_tt0p8v125c/SAEDRVT14_INV_S_8"]

# Clock INVERTER

#set_lib_cell_purpose -include cts [get_lib_cells
"saed14rvt_tt0p8v125c/SAEDRVT14_CKINVGTPLT_V7_1
saed14rvt_tt0p8v125c/SAEDRVT14_CKINVGTPLT_V7_2
saed14rvt_tt0p8v125c/SAEDRVT14_CKINVGTPLT_V7_3
saed14rvt_tt0p8v125c/SAEDRVT14_CKINVGTPLT_V7_4
saed14rvt_tt0p8v125c/SAEDRVT14_CKINVGTPLT_V7_5
saed14rvt_tt0p8v125c/SAEDRVT14_CKINVGTPLT_V7_6
saed14rvt_tt0p8v125c/SAEDRVT14_CKINVGTPLT_V7_8"]

#BUFFER

set_lib_cell_purpose -include cts [get_lib_cells
"saed14rvt_tt0p8v125c/SAEDRVT14_BUF_S_4
saed14rvt_tt0p8v125c/SAEDRVT14_BUF_S_4
saed14rvt_tt0p8v125c/SAEDRVT14_BUF_S_6
saed14rvt_tt0p8v125c/SAEDRVT14_BUF_S_8"]


#Specify Max fanout

set_app_options -name  cts.common.max_fanout -value 30
```

```
set_clock_tree_options -clocks [all_clocks] -target_latency 0.05 -target_skew 0.030

#set_clock_tree_options -clocks [get_clocks -filter "is_virtual==false"] -target_latency 0.25 -target_skew 0.03


set_clock_routing_rules -clocks [all_clocks ] -net_type {internal} -rules clk_rule -min_routing_layer M6 -max_routing_layer M7

set_clock_routing_rules -clocks [all_clocks ] -net_type {root} -rules clk_rule -min_routing_layer M6 -max_routing_layer M7


clock_opt


connect_pg_net -net VDD [get_pins -hier * -filter "name == VDD"]

connect_pg_net -net VSS [get_pins -hier * -filter "name == VSS"]


save_block -as CTS_DONE_CLOCK_ONLY_BUFFER


report_constraints -all_violators > ./Reports/Constraints_CTS_BUFFER.rpt

report_clock_tree_options > ./Reports/Clock_tree_option_CTS_BUFFER.rpt

report_clock_qor > ./Reports/Clock_QOR_CTS_BUFFER.rpt

report_qor -summary > ./Reports/QOR_CTS_BUFFER.rpt

report_timing -delay_type min > ./Reports/Timing_Delay_MIN_CTS_BUFFER.rpt

report_timing -delay_type max > ./Reports/Timing_Delay_MAX_CTS_BUFFER.rpt
```

Date:1/6/2022

Section 5 : Routing

(a) How does congestion number help you to estimate routing issues?

If the number of routing tracks available for routing in one particular area is less than the required routing tracks then the area said to be congested. There will be a limit for number of nets that can be routed through particular area.

Congestion driven placement is performed to reduce the congestion. During congestion driven placement, the cells (Higher cell density) which caused for congestion are spread apart. If the cells along timing critical paths spread apart, the timing constraints along that particular path are not met which cause for timing violations. But these violations can be fixed during incremental optimization.

(b) How will you route only few selected nets in ICC? Write down the options you need to set in ICC to do this.

Step 1: get_nets

Step 2: route_custom -nets netname

Step 3:change_selection [get_nets netname]. To show in design highlighted net.

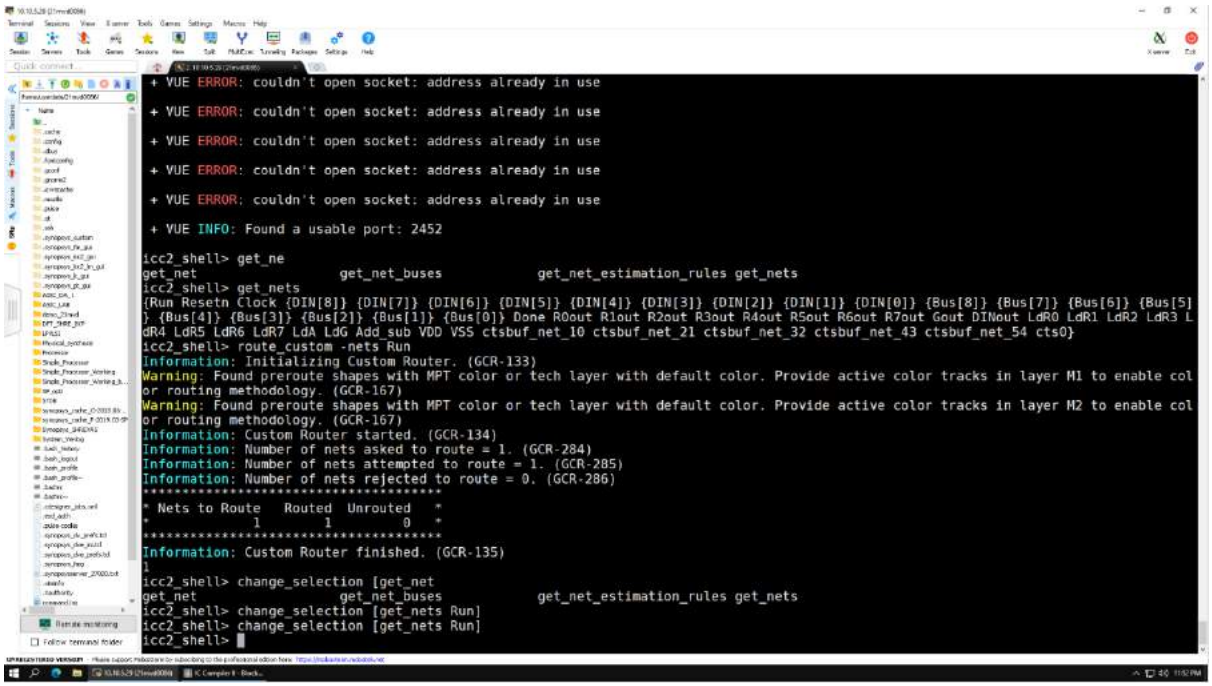


Figure 5.1 The Figure shows manual routing using route_custom -nets NETNAME.

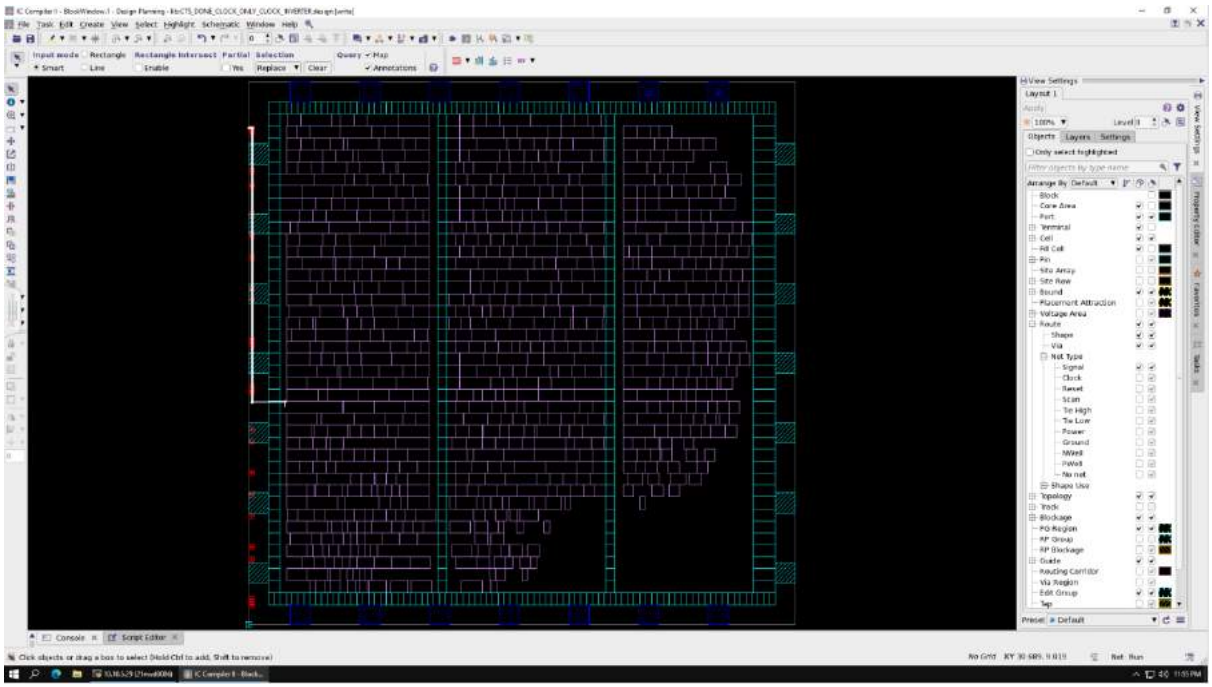


Figure 5.2 The Figure shows highlighted net Run routed.

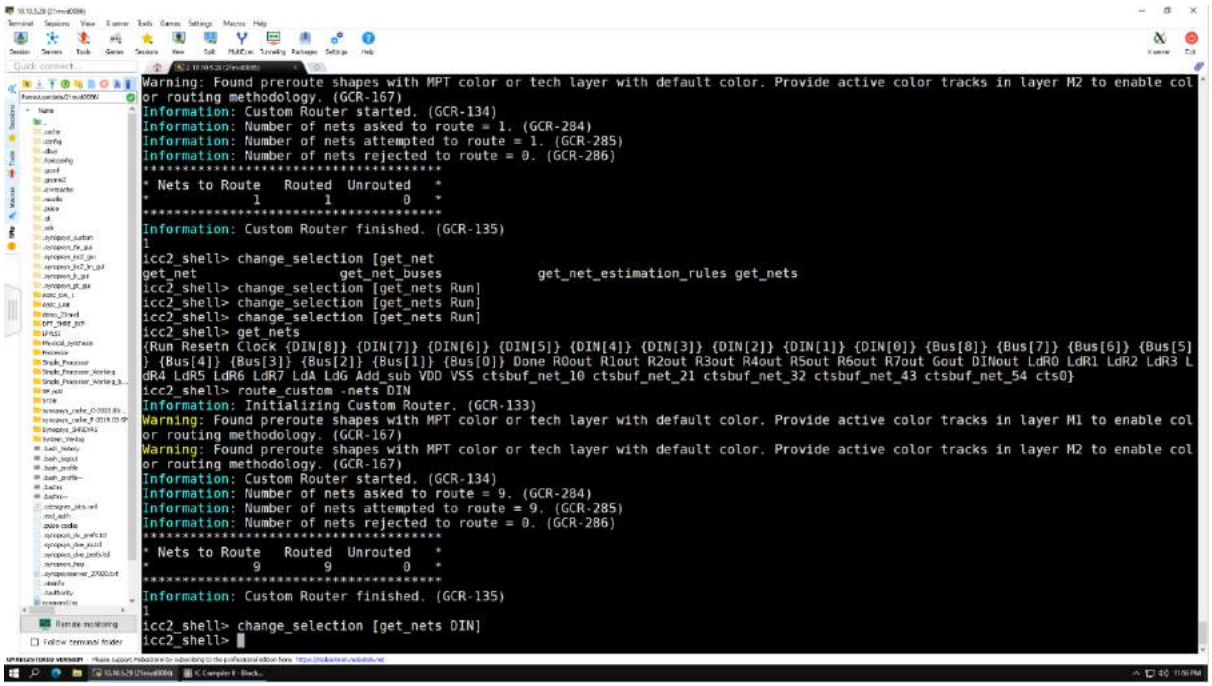


Figure 5.3: The Figure shows route_custom -nets DIN. The DIN is a 9bit bus.

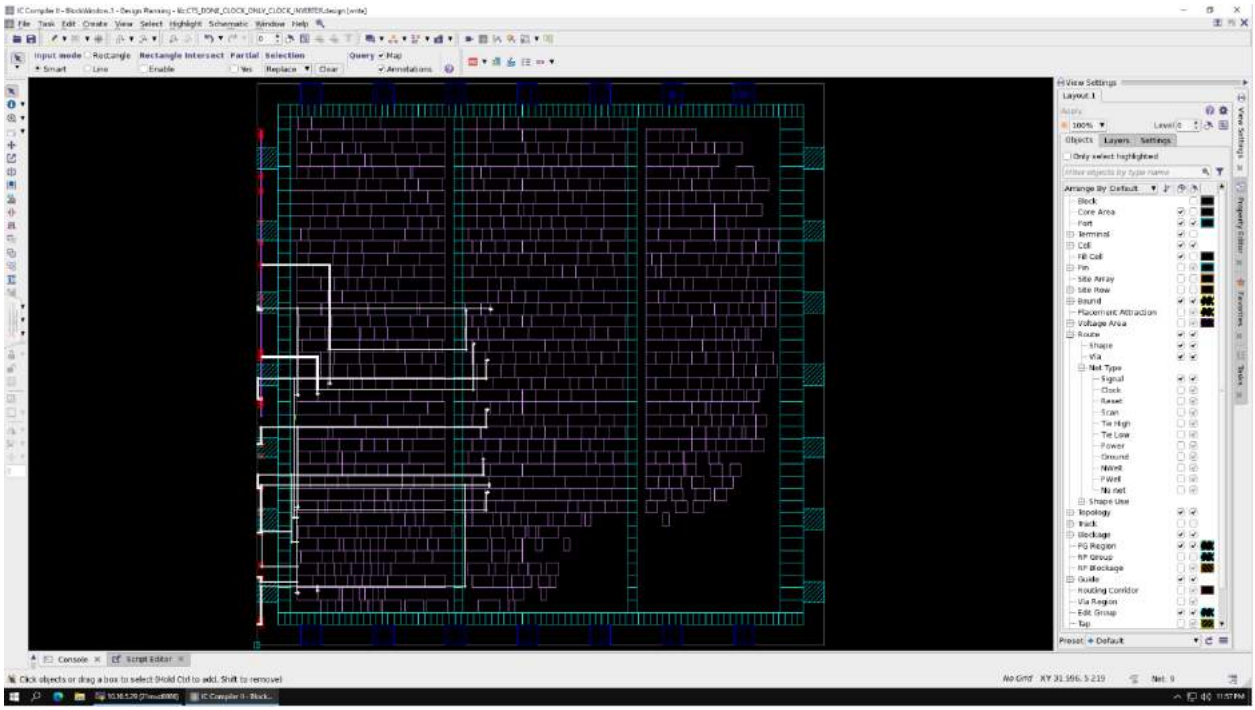


Figure 5.4: The Figure shows highlighted DIN nets.

The script used for routing before eco cells placement and routing:

File name : **Simple_Processor_initial_route.tcl**

```
check_design -checks pre_route_stage

check_routability

set_app_options -name route.detail.timing_driven -value true

set_app_options -name route.track.timing_driven -value true

set_app_options -name route.track.crosstalk_driven -value true

set_app_options -name route.global.timing_driven -value true

set_ignored_layers -max_routing_layer M7 -min_routing_layer M2

set_app_options -name route.common.global_min_layer_mode -value allow_pin_connection

set_app_options -name route.common.global_max_layer_mode -value soft

set_app_options -name time.si_enable_analysis -value true

set_app_options -name time.enable_si_timing_windows -value true

check_design -checks pre_route_stage
```

check_routability

set_app_options -name route.detail.timing_driven -value true

set_app_options -name route.track.timing_driven -value true

set_app_options -name route.track.crosstalk_driven -value true

set_app_options -name route.global.timing_driven -value true

set_ignored_layers -max_routing_layer M7 -min_routing_layer M2

set_app_options -name route.common.global_min_layer_mode -value allow_pin_connection

set_app_options -name route.common.global_max_layer_mode -value soft

set_app_options -name time.si_enable_analysis -value true

set_app_options -name time.enable_si_timing_windows -value true

set_app_options -name time.enable_ccs_rcv_cap -value true

route_auto

save_block -as Initial_Route_Done

route_opt

save_block -as Final_Route_Done

After Routing :

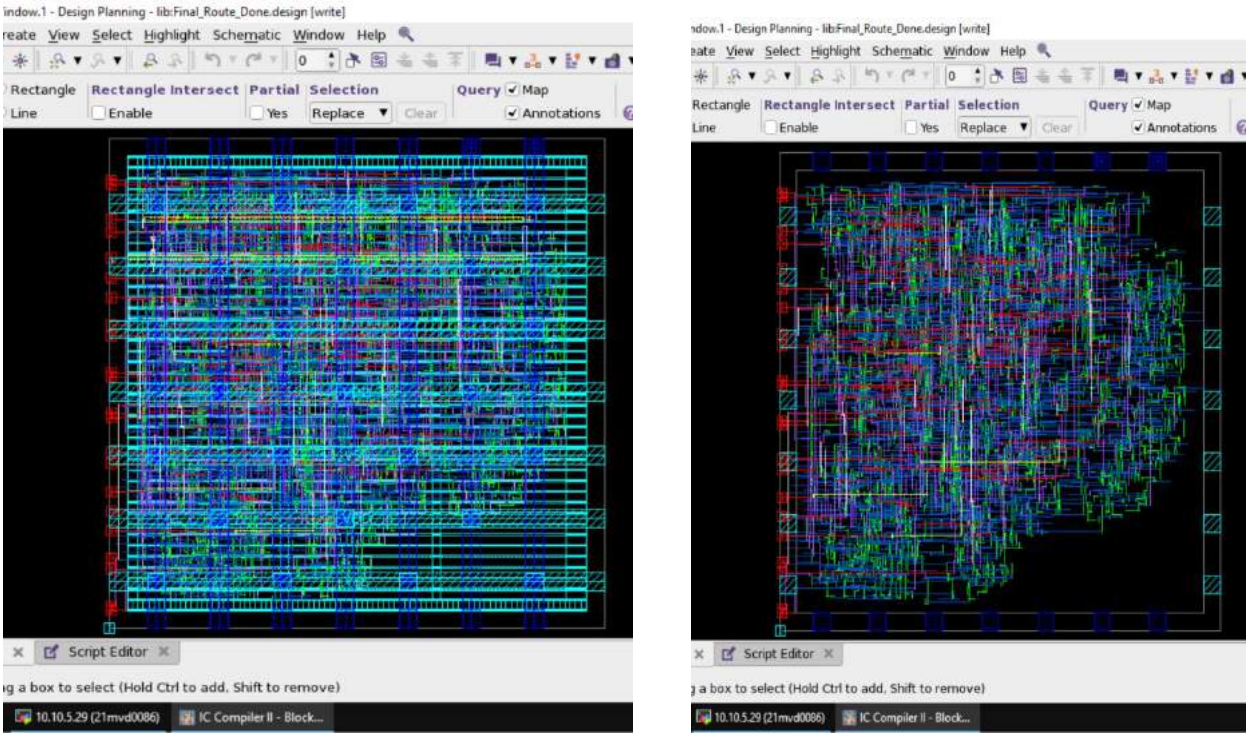


Figure 5.5 : The Figure shows the Simple Processor after Routing.

The Path and Folder present is show in below figure :

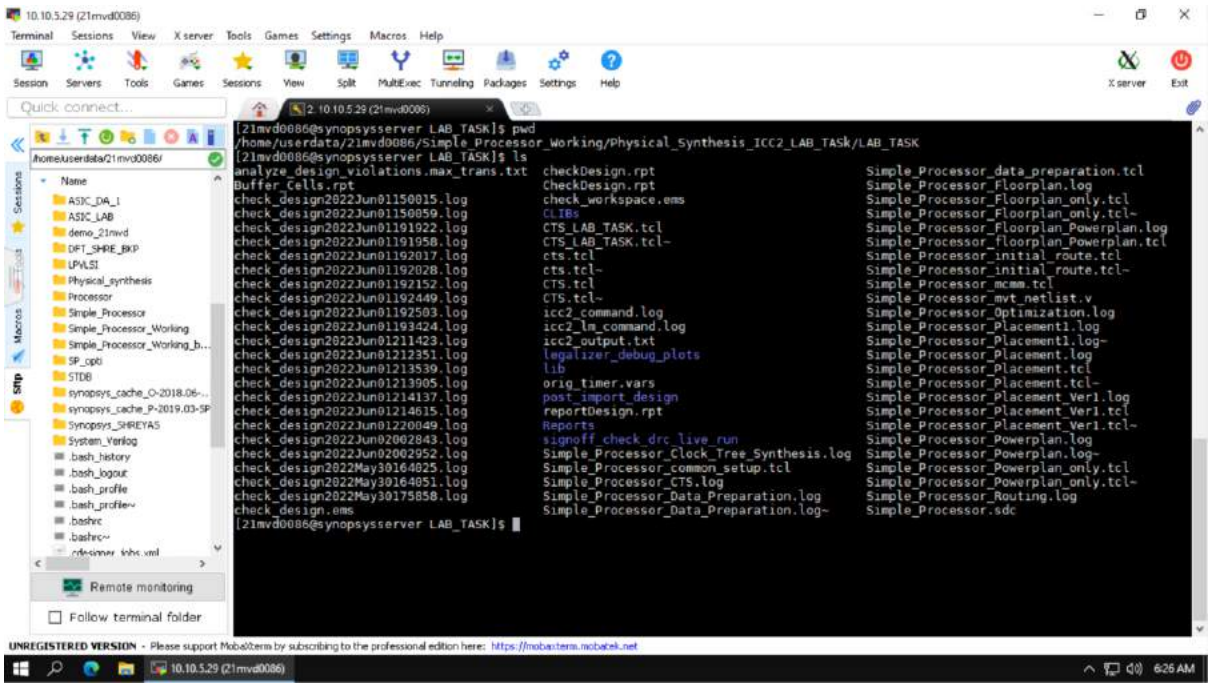


Figure 5.6 : The Figure shows the Design path and reports present in Report Folder.