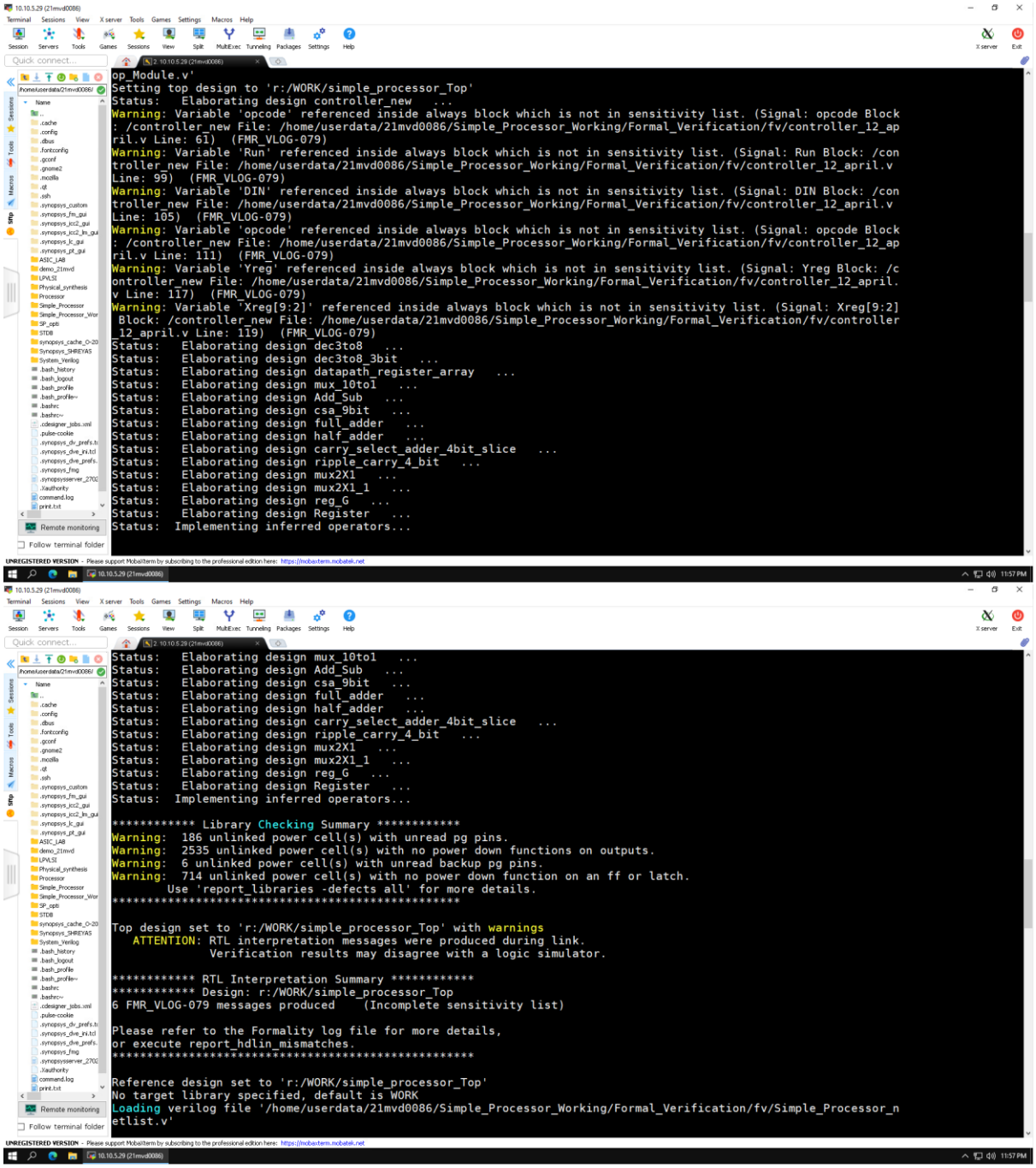
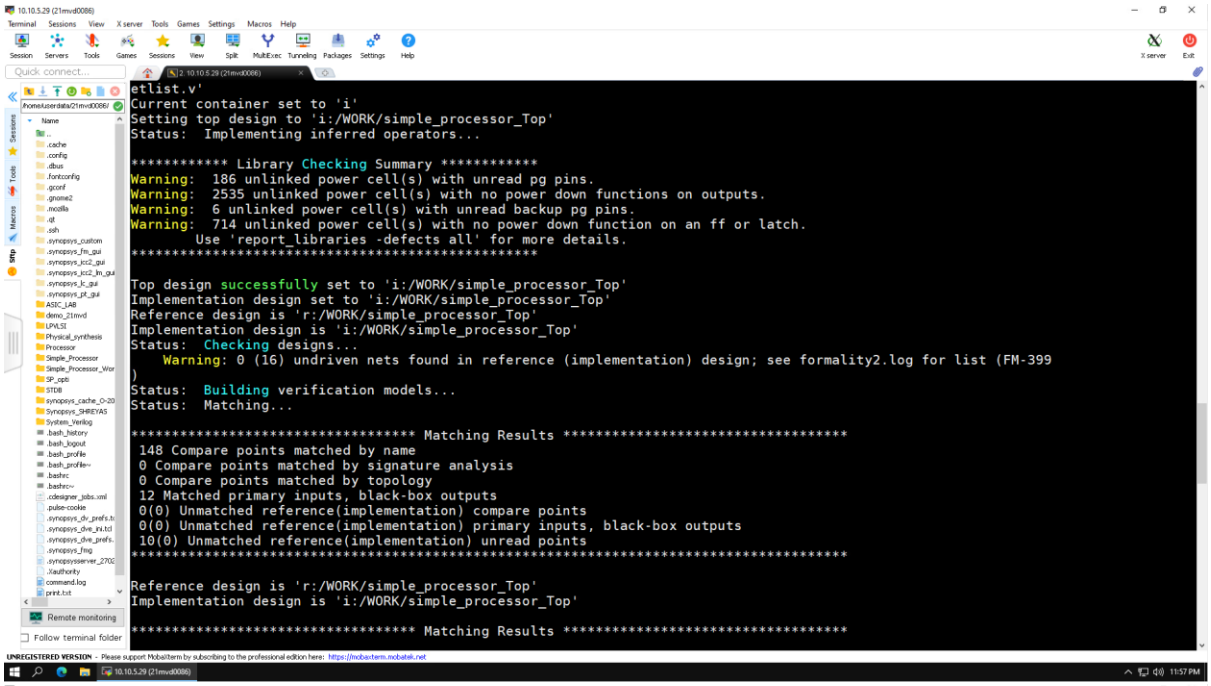
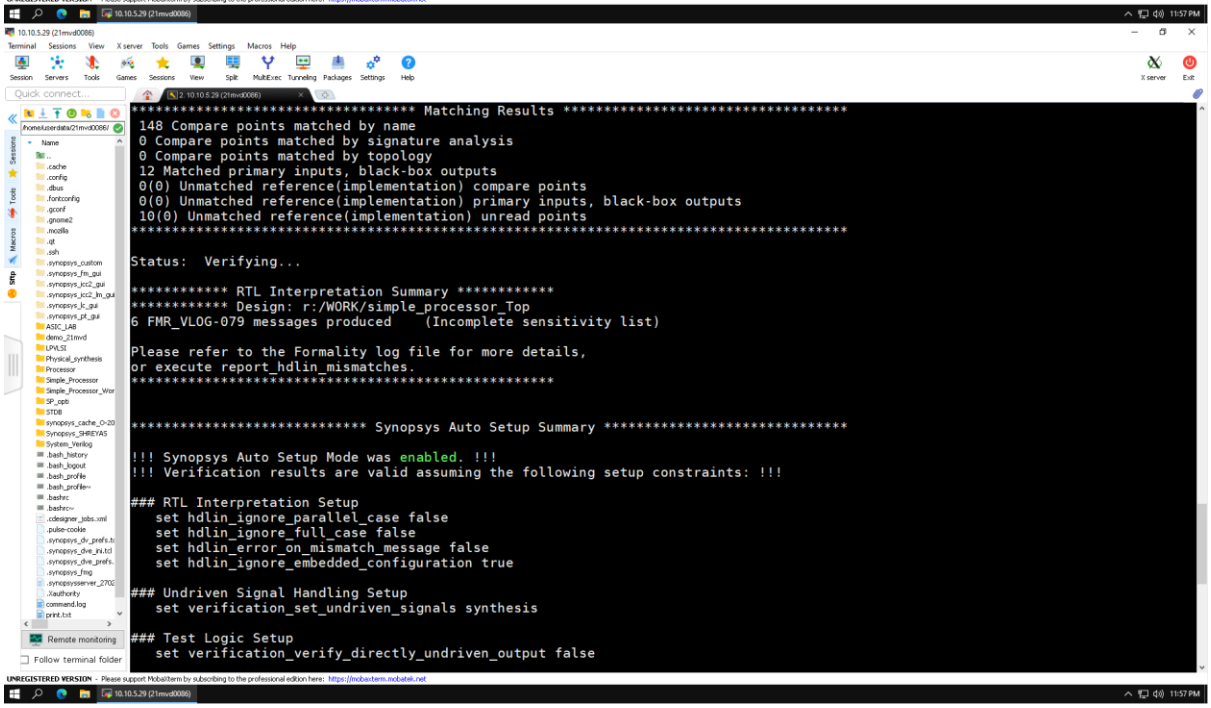
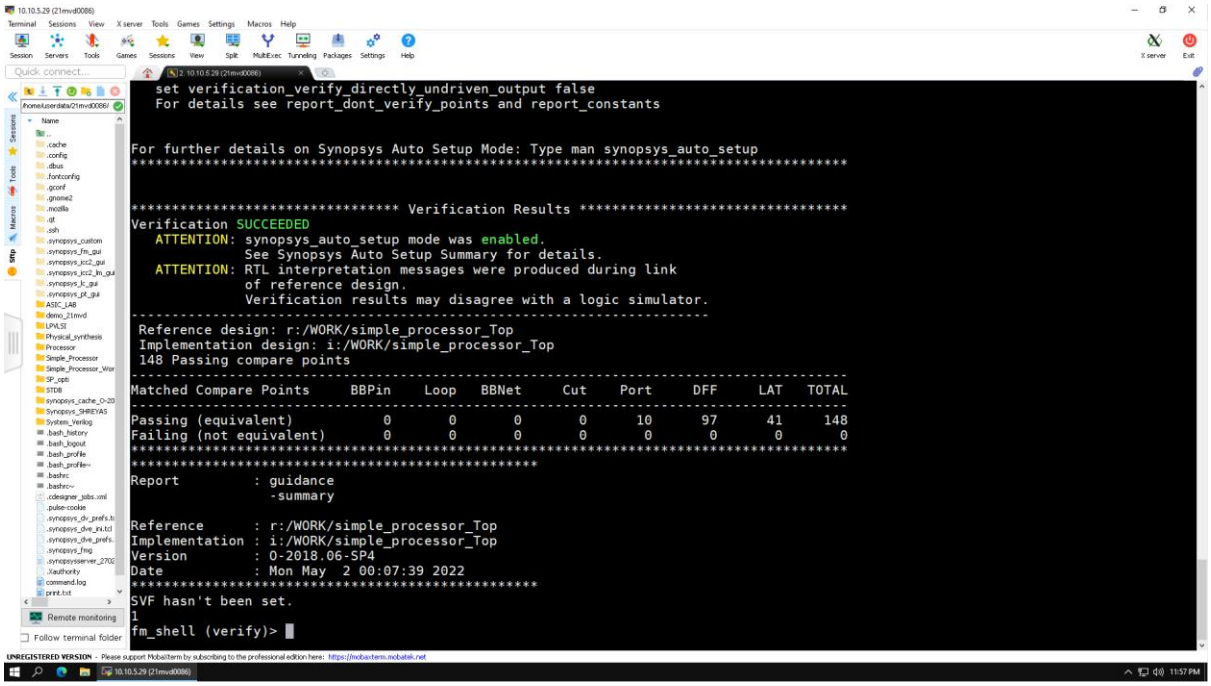
Formal Verification Screenshots




etlist.v'
Current container set to 'i'
Setting top design to 'i:/WORK/simple_processor_Top'
Status: Implementing inferred operators...
*********** Library Checking Summary ***********
Warning: 186 unlinked power cell(s) with unread pg pins.
Warning: 2535 unlinked power cell(s) with no power down functions on outputs.
Warning: 6 unlinked power cell(s) with unread backup pg pins.
Warning: 714 unlinked power cell(s) with no power down function on an ff or latch.
Use 'report_libraries -defects all' for more details.
Top design successfully set to 'i:/WORK/simple_processor_Top'
Implementation design set to 'i:/WORK/simple_processor_Top'
Reference design is 'r:/WORK/simple_processor_Top'
Implementation design is 'i:/WORK/simple_processor_Top'
Status: Checking designs...
Warning: 0 (16) undriven nets found in reference (implementation) design; see formality2.log for list (FM-399
)
Status: Building verification models...
Status: Matching...
********** Matching Results **********
148 Compare points matched by name
0 Compare points matched by signature analysis
0 Compare points matched by topology
12 Matched primary inputs, black-box outputs
0(0) Unmatched reference(implementation) compare points
0(0) Unmatched reference(implementation) primary inputs, black-box outputs
10(0) Unmatched reference(implementation) unread points
Reference design is 'r:/WORK/simple_processor_Top'
Implementation design is 'i:/WORK/simple_processor_Top'
********** Matching Results **********


********** Matching Results **********
148 Compare points matched by name
0 Compare points matched by signature analysis
0 Compare points matched by topology
12 Matched primary inputs, black-box outputs
0(0) Unmatched reference(implementation) compare points
0(0) Unmatched reference(implementation) primary inputs, black-box outputs
10(0) Unmatched reference(implementation) unread points
Status: Verifying...
************ RTL Interpretation Summary ************
************ Design: r:/WORK/simple_processor_Top
6 FMR_VLOG-079 messages produced (Incomplete sensitivity list)
Please refer to the Formality log file for more details,
or execute report_hdlin_mismatches.
********** Synopsys Auto Setup Summary **********
!!! Synopsys Auto Setup Mode was enabled. !!!
!!! Verification results are valid assuming the following setup constraints: !!!
RTL Interpretation Setup
set hdlin_ignore_parallel_case false
set hdlin_ignore_full_case false
set hdlin_error_on_mismatch_message false
set hdlin_ignore_embedded_configuration true
Undriven Signal Handling Setup
set verification_set_undriven_signals synthesis
Test Logic Setup
set verification_verify_directly_undriven_output false


set verification_verify_directly_undriven_output false
For details see report_dont_verify_points and report_constants
For further details on Synopsys Auto Setup Mode: Type man synopsys_auto_setup
Verification Results
Verification SUCCEEDED
ATTENTION: synopsys_auto_setup mode was enabled.
See Synopsys Auto Setup Summary for details.
ATTENTION: RTL interpretation messages were produced during link
of reference design.
Verification results may disagree with a logic simulator.
Reference design: r:/WORK/simple_processor_Top
Implementation design: i:/WORK/simple_processor_Top
148 Passing compare points
Matched Compare Points BBPin Loop BBNet Cut Port DFF LAT TOTAL
Passing (equivalent) 0 0 0 0 10 97 41 148
Failing (not equivalent) 0 0 0 0 0 0 0 0
Report : guidance
-summary
Reference : r:/WORK/simple_processor_Top
Implementation : i:/WORK/simple_processor_Top
Version : O-2018.06-SP4
Date : Mon May 2 00:07:39 2022
SVF hasn't been set.
1
fm_shell (verify)>