**Date:6/4/2022**


**Fall Semester 2021-2022**

# ECE6024 – VLSI Verification Methodologies

**M.Tech VLSI Design**

**School of Electronics Engineering**

**Vellore Institute of Technology**

**Name: Shreyas S Bagi**

**Register Number: 21MVD0086**

**Slot: D2**

**Date:6/4/2022**

# Digital Assignment 01

## SoC Design Using OpenPOWER Cores

## Day 1

### (a) Session 1: Open POWER Cores and Accelerators by Dr. Peter Hofstee, IBM

Dr. Peter Hofstee started the session by giving brief introduction on Power ISA: Compliancy Subsets by explaining the Scalar Fixed-Point subset, Floating point subset, Linux subset, AIX subset. These all are composed in PowerISA v3.0C. The POWER ISA is open source.

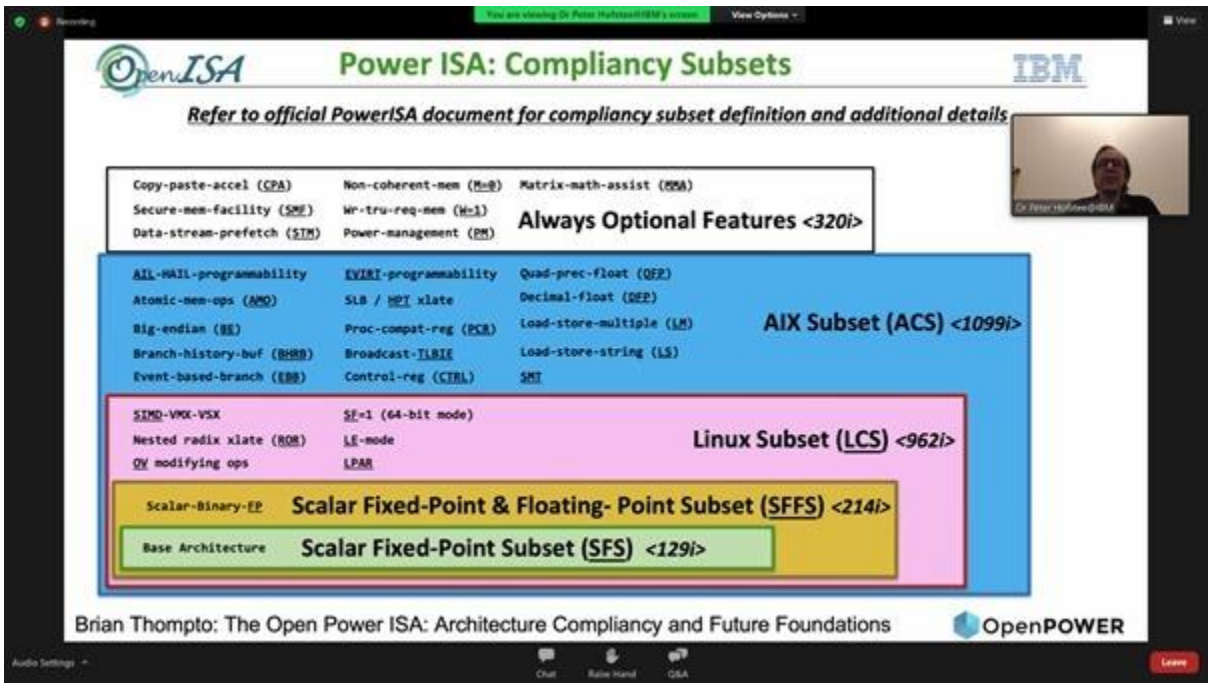


**Figure 1.1** The Open Power ISA: Compliancy Subsets.

He gave brief description on POWER10 Processor chip. The features of Power10 Processor chip are as follows:

Clock Speed: 3.5GHz to 4GHz.

L1 Cache: 48+32 KB per core.

L2 Cache: 2 MB per core.

L3 Cache: 120MB per chip.

Technology Node: 7nm.

Instruction Set: Power ISA.

Cores: 15 SMT8 cores and 30SMT4 cores

- The chip will be packaged as an SCM (one chip per socket) and a DCM (two chips per socket), depending on the server.
- The chip is built for massive data handling and, to enable compute to keep up, the L2 cache has been increased to 2MB per core and the L3 cache is now 128MB per chip.
- The processor is enabled to support PCIe Gen5 devices once they become available.
- The GHz will likely be about the same as the POWER9 processor but the larger pipes, bandwidth, and interconnect speeds should make the per-core performance 25 to 30% faster.

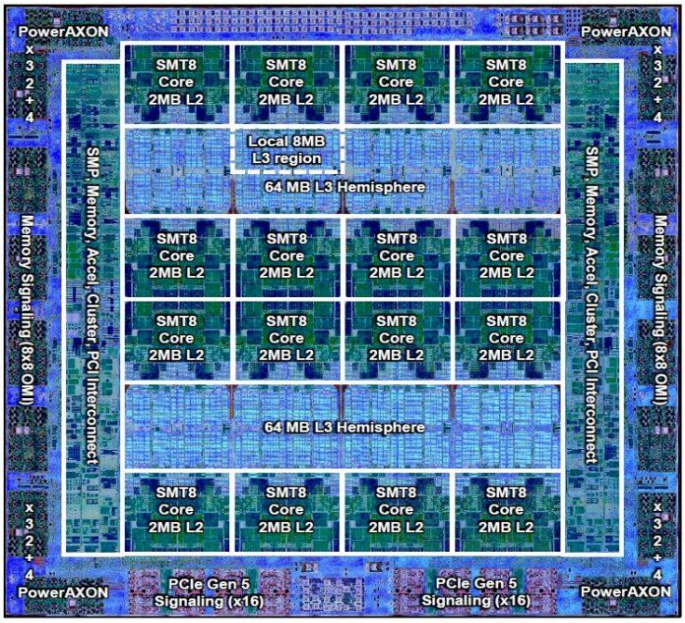


**Figure 1.2** The Die Photo of Power10 Processor Chip.

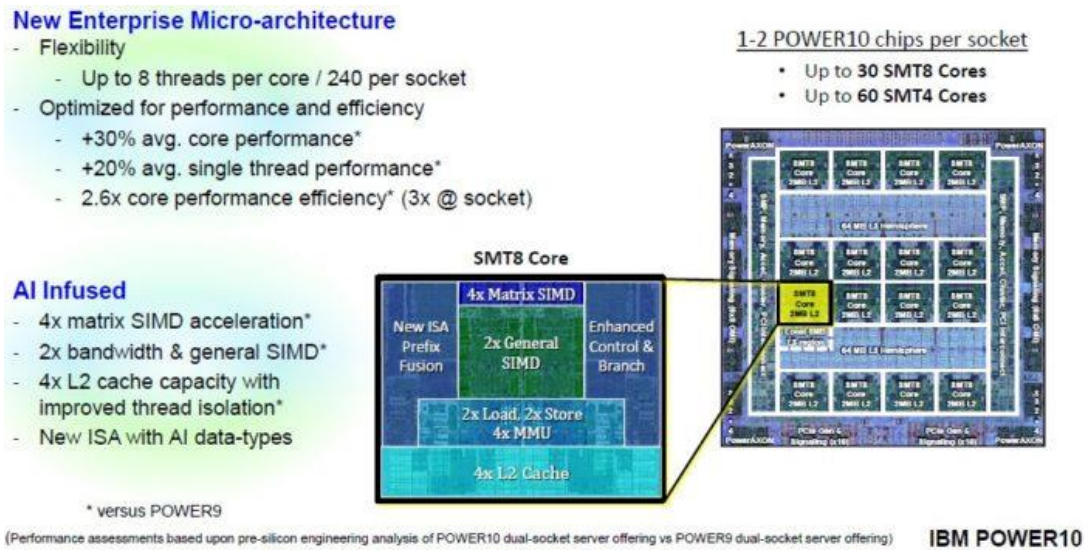


**Figure 1.3** The IBM POWER10.

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**Microwatt**

The Microwatt is a soft-core processor written by Anton Blanchard at IBM. Microwatt is a tiny 64-bit bi-endian scalar integer processor core, implementing a subset of the Power ISA 3.0 instruction set. It has 32× 64-bit general purpose registers and 32x 64-bit floating-point registers. It uses Wishbone for the memory interface.

**A2I Processor Family**

- A 4-way simultaneous multithreaded core which implements the 64-bit Power ISA
- Embedded platform specification with support for the embedded hypervisor features.
- The high throughput and many simultaneous threads. A2I was written in VHDL.
- The core has 4×32 64-bit general purpose registers (GPR) with full support for both little- and big-endian byte ordering.
- 16 KB+16 KB instruction and data cache and is capable of four-way multithreading.
- Blue Gene/Q: The Blue Gene/Q processor is an 18 core chip using the A2I core running at 1.6 GHz with special features for fast thread context switching, quad SIMD floating point unit, 5D torus chip-to-chip network and 2 GB/s external I/O.

**A2O Processor Family**

- Two threads per core, out-of-order, single-threaded performance-optimized.
- The A2O is a slightly more modern version, written in Verilog, using the Power ISA v.2.07 Book III-E. It is optimized for single core performance and designed to reach 3 GHz at 45 nm process technology.
- The A2O differs from its sibling in that it is only two-way multithreaded, 32+32 kB data and instruction L1 caches, and is capable of out-of-order execution.
- Modular Design with optional units for application-specific implementations
- MMU: 512 X 4 TLB, 4TB physical addressability
- AXU: tightly-coupled accelerator interface, 16B L/S
- Microcode engine.
- Full support for both big- and little-endian byte ordering.

**Inference:**

1. The Open source PowerISA is discussed and advantages of it is mentioned.
2. The detailed explanation of Microwatt and implementation of it in A2I and A2O processor was discussed.

## (b) Session 2: Power ISA by Vinod IBM

The PowerISA Architecture history is as shown in figure:

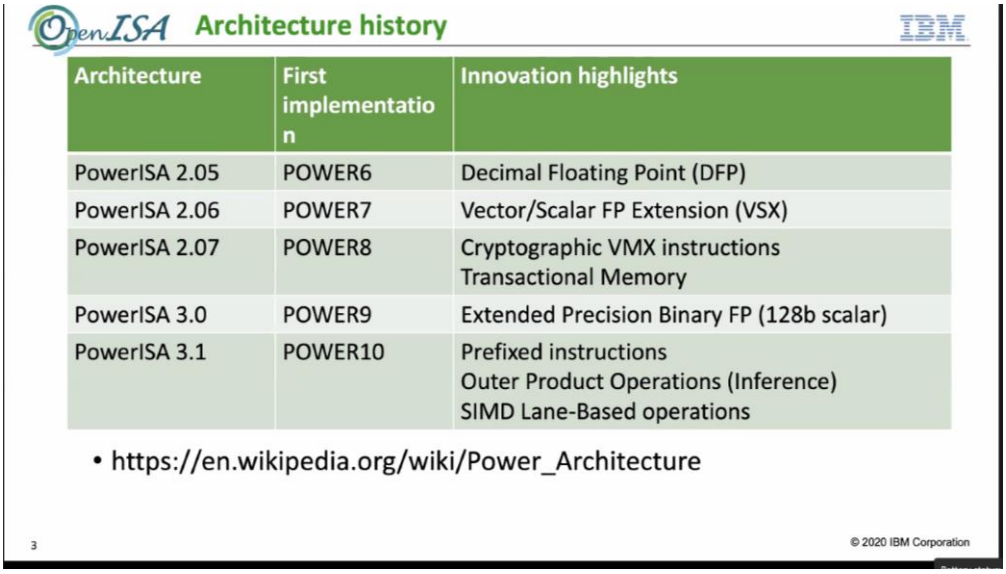


**Figure 1.4** The IBM Power ISA architecture history.

The Power ISA has 32 General Purpose Registers of each 64-bit in length.

The Fixed-point Exception Register (XER) is a 64-bit.

The 32 number of Floating-point Registers of each 64-bit in length.

There are 32 Vector Registers (VRs) each containing 128-bits.

The Vector-Scalar Registers (VSX) each containing 128-bits.

The Special Purpose Registers (SPR's):

- Condition Register (CR)
- Count Register (CTR)
- Target Address Register (TAR)
- Link Register (LR)
- Fixed Point Exception Register (XER)
- Floating Point status and Control Register (FPSCR)
- Vector Status and Control Register (VSCR)

OpenPOWER ISA Key Architectural Elements

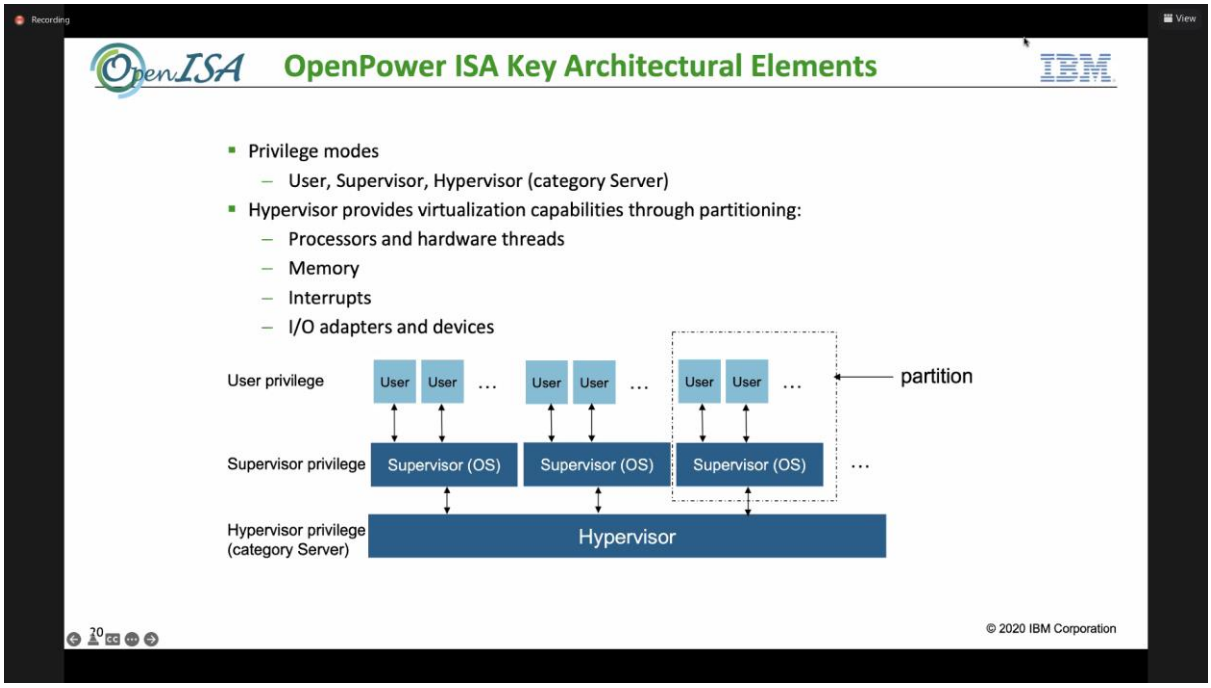


**Figure 1.5** The OpenPower ISA Key Architectural Elements.

The new features included in the PowerISA 3.1 is as shown in this figure.

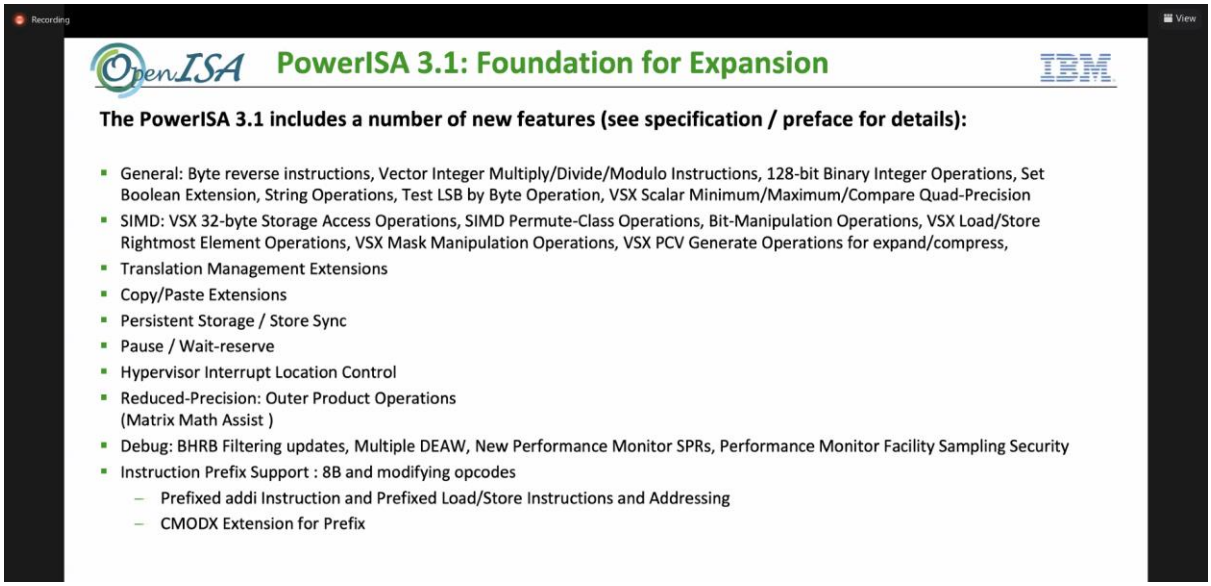


**Figure 1.6** The PowerISA 3.1 new features included.

A soft-core processor also offers the flexibility of configuring the core itself for the application. Using a SoPC solution also offers flexibility outside the FPGA while designing the circuit board.

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# (c) Session 3: System on a Chip and Components IP Cores by Man ikandan

**Soc (System on Chip):**

- A chip/IC that holds many components of a computer. CPU (via a microprocessor or microcontroller), memory, input/output (I/O) ports and secondary storage-on a single substrate, such as silicon.
- Having all these components on one substrate means SoCs use less power and take up less space than their multi-chip counterparts.
- System on Chip (SoC) is an integrated circuit and tightly couple's microprocessor, processors and peripherals interface and memory etc.

**Basic System-on-chip model**

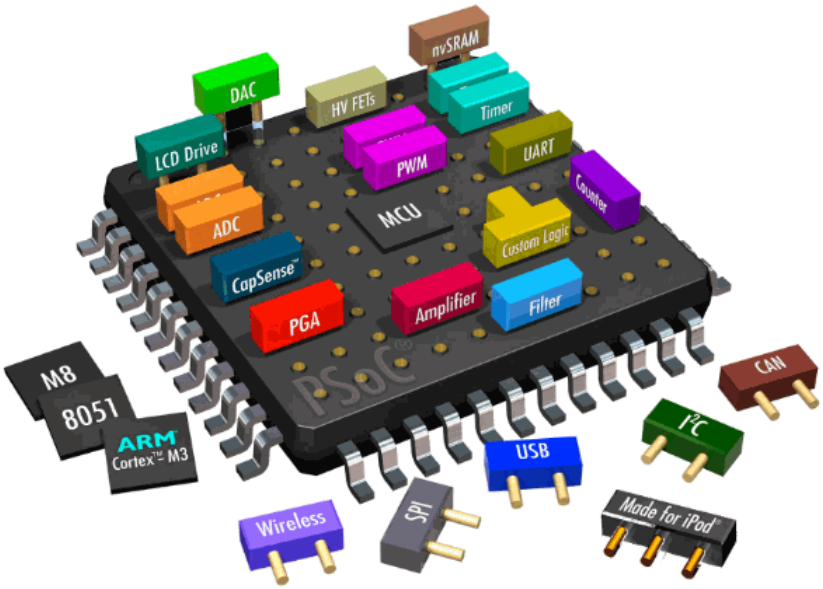


**Figure 1.7** The basic System-on-chip model.

There many SoC vendors based on application, specifications the type and configuration of SoC changes. In Presentation they gave example of high-end processor like NVIDIA Tegra X1.

The SoC includes following elements:

1. CPUs
2. GPUs
3. Buses
4. Memory controllers
5. Arbiters
6. Simple peripherals (PWM, SPI, I2C, UART, Ethernet, JTAG)

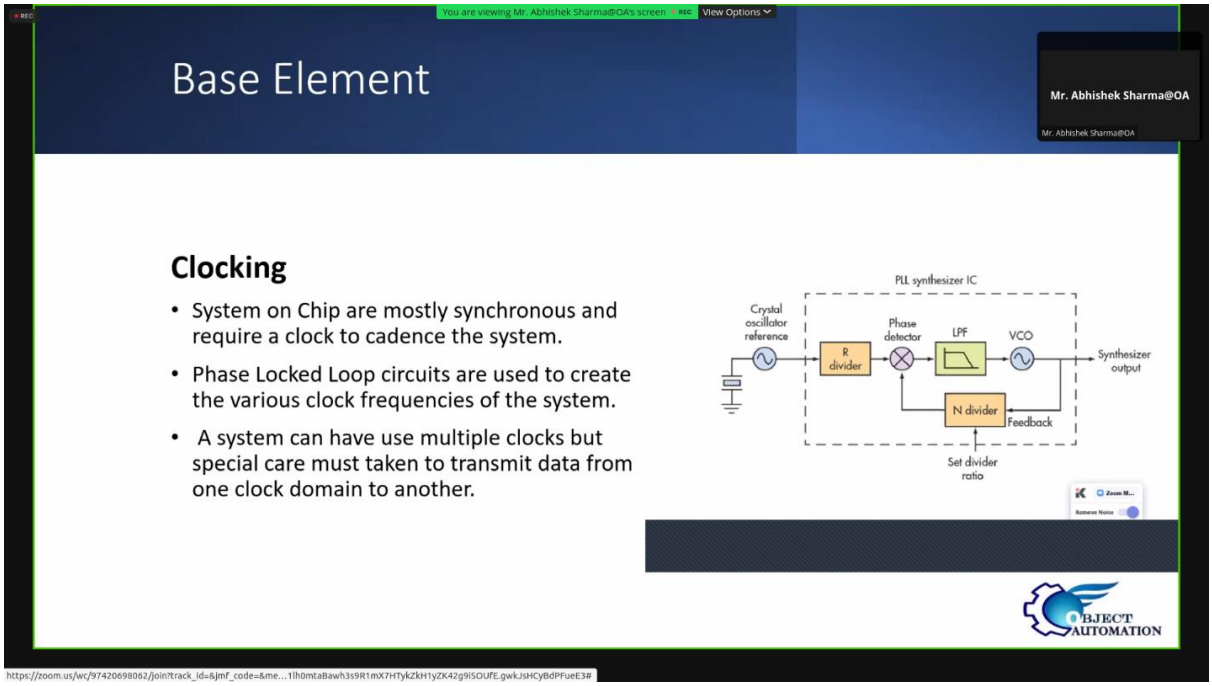


**Figure 1.8** The Base Element Clocking.

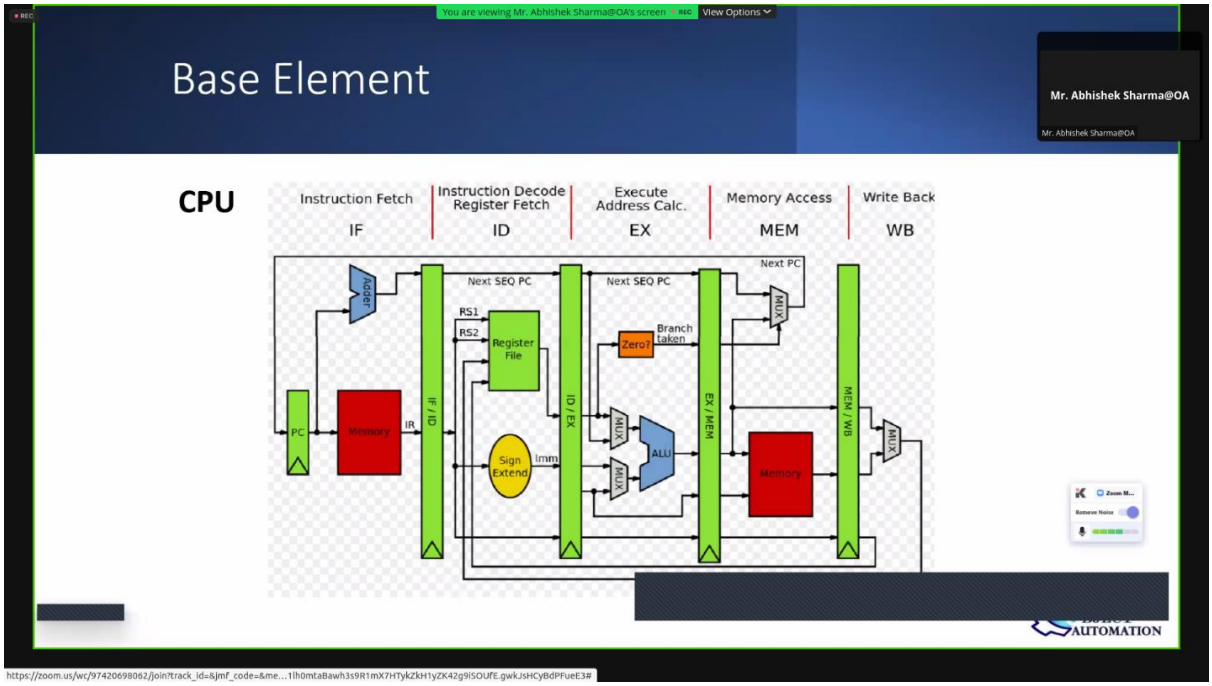


**Figure 1.9** The Base Element CPU.

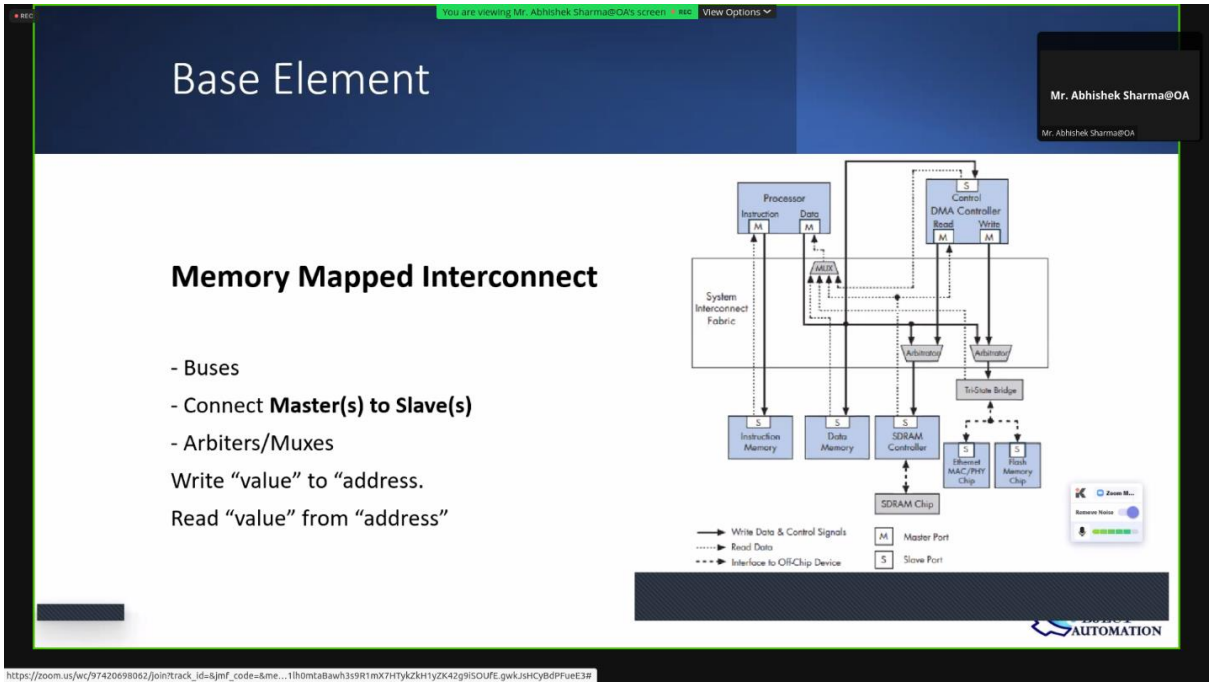


**Figure 1.10** The Base Element Memory mapped Interconnect.

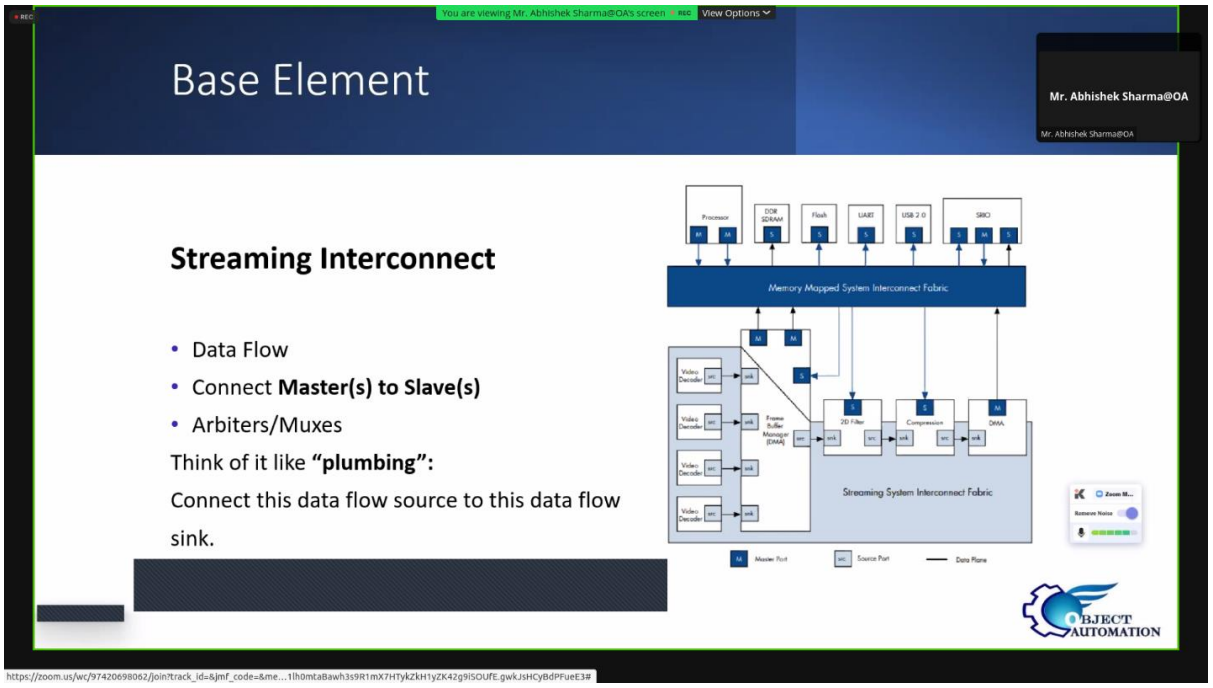


**Figure 1.11** The Base Element Memory Streaming Interconnect.

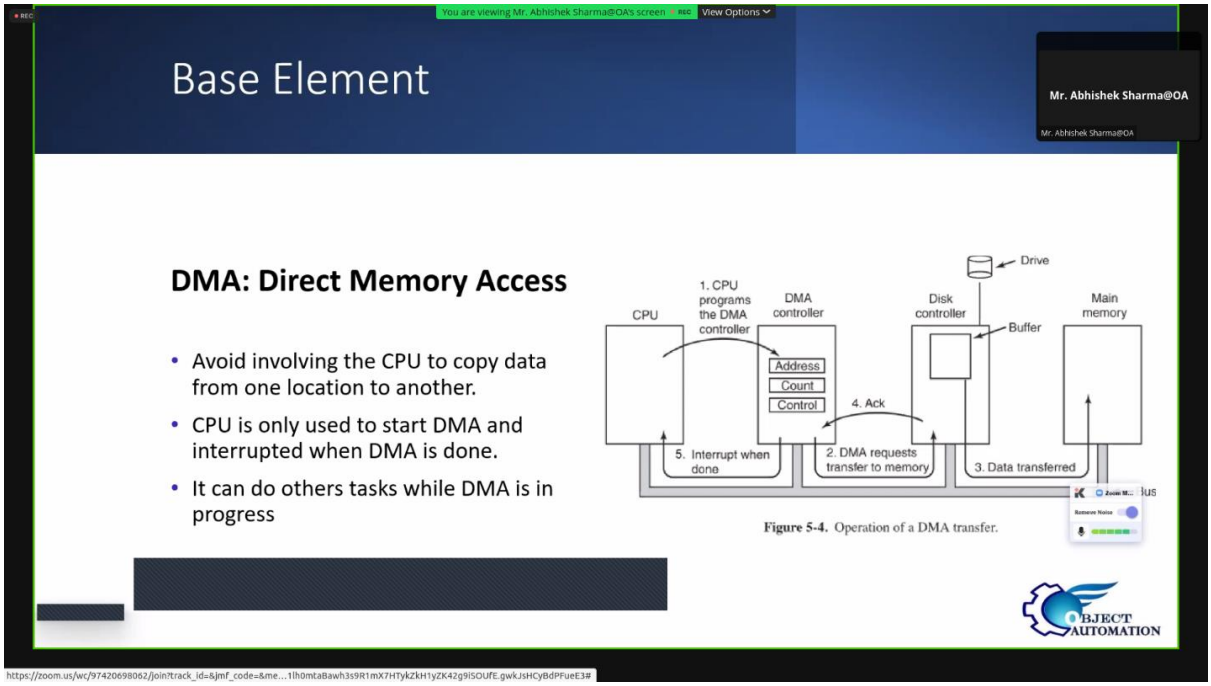


**Figure 1.12** The Base Element Direct Memory Access.

The Serial Interface like I2C and SPI were explained.

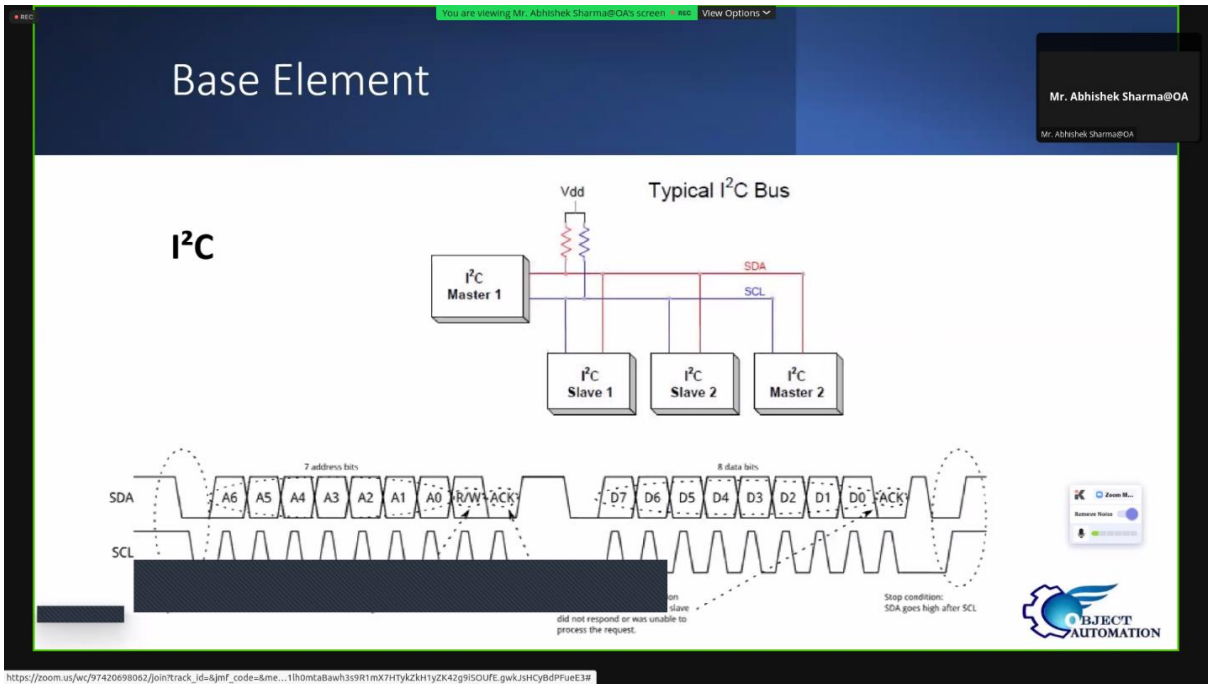


**Figure 1.13** The I2C interface.

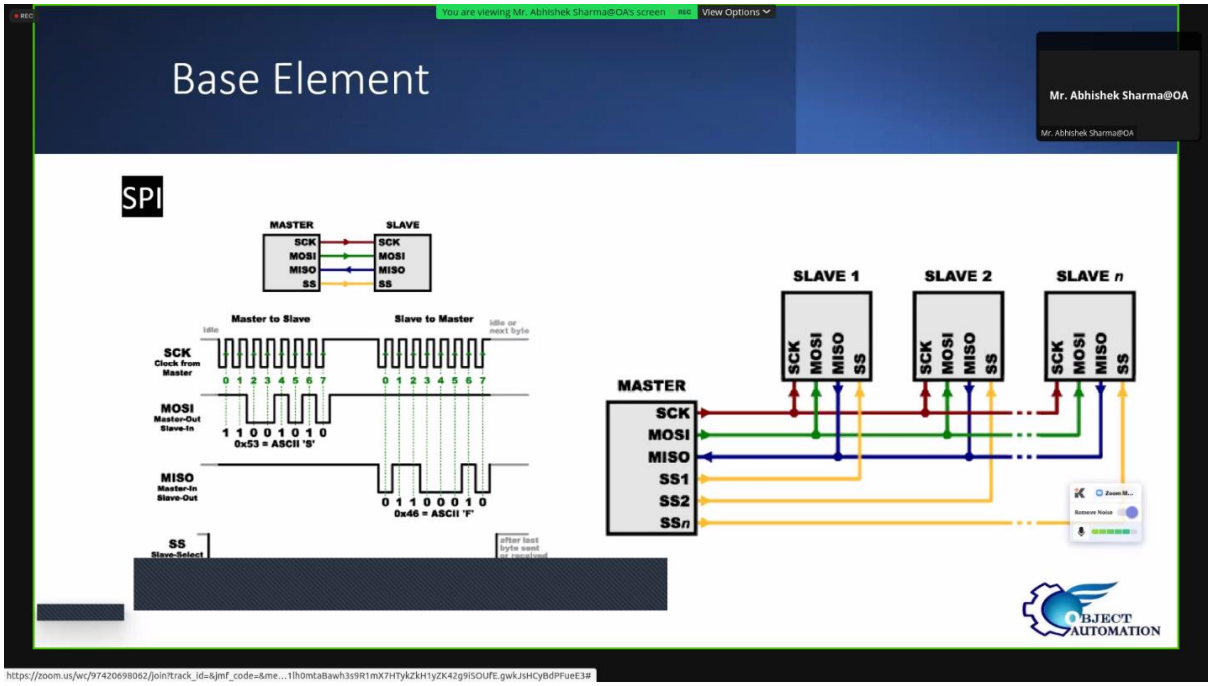


**Figure 1.14** The SPI interface.

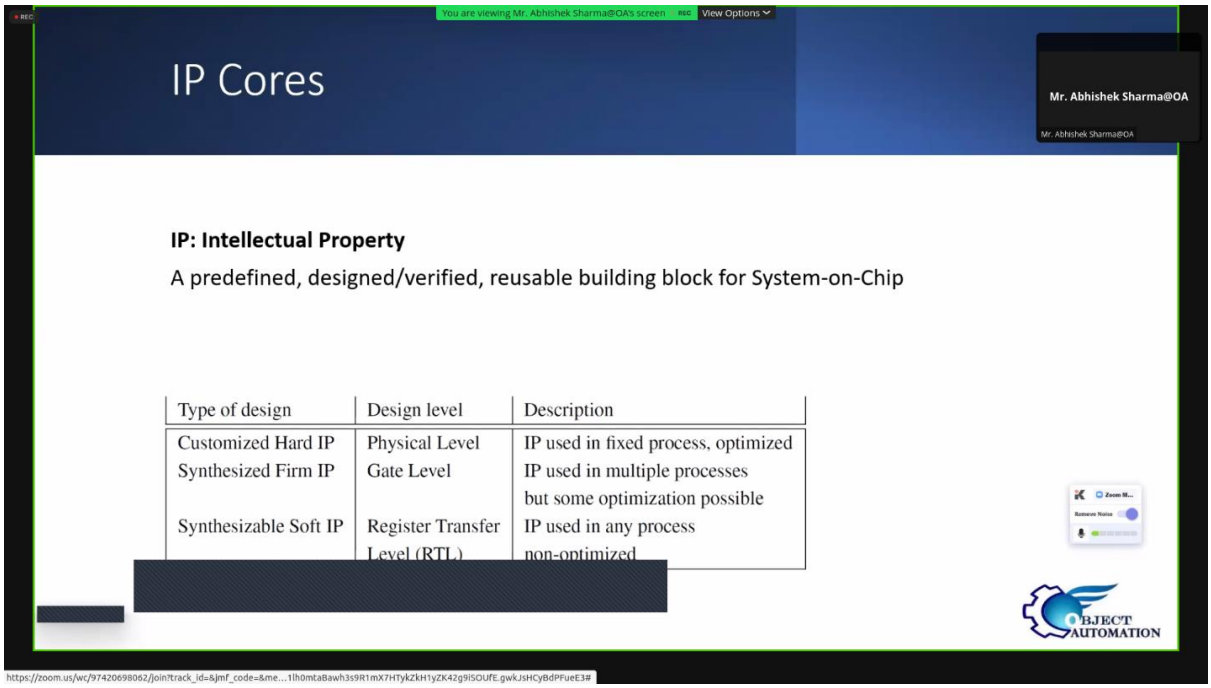


**Figure 1.15** The IP Cores.

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# (d) System Verilog

The System Verilog concepts like Data types, OOPs advantages of System Verilog over Verilog was discussed. Some of the snapshots has been shown below.

System Verilog:

- A Hardware Description and Verification language (HDVL).
- It is extensive set of enhancements to IEEE 1364 Verilog-2001 standards.
- It has features inherited from Verilog HDL, VHDL, C, C++.
- Adds extended features to Verilog.

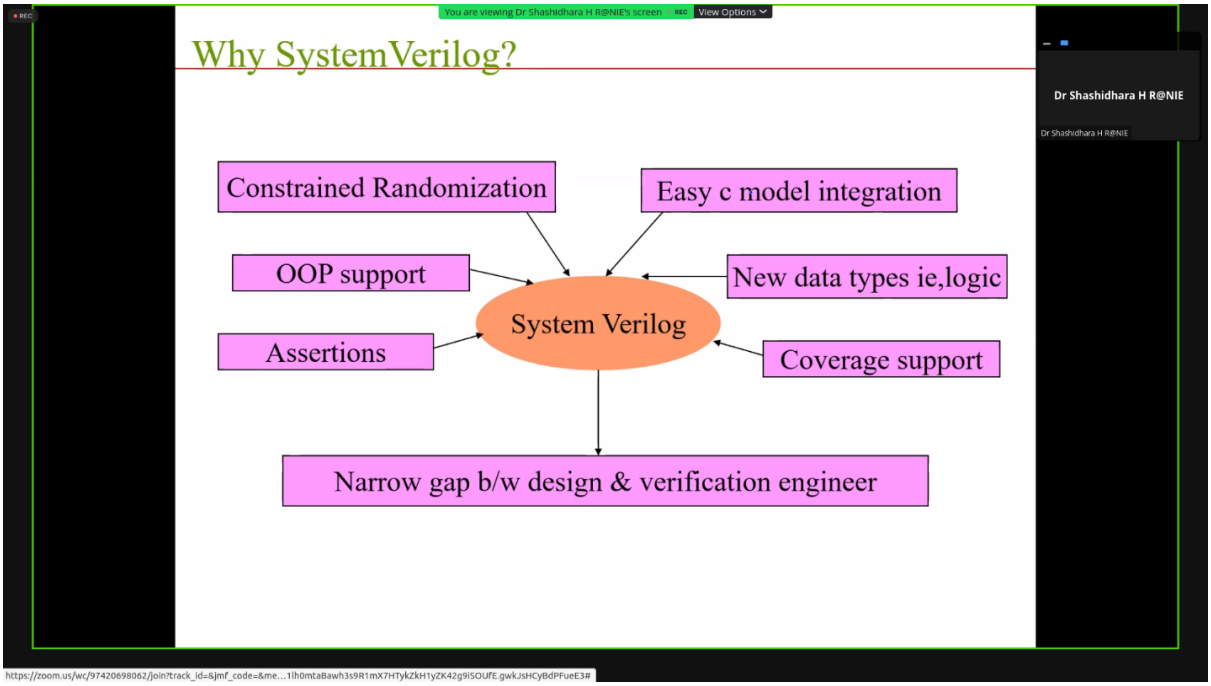


**Figure 1.16** The reason for System Verilog.

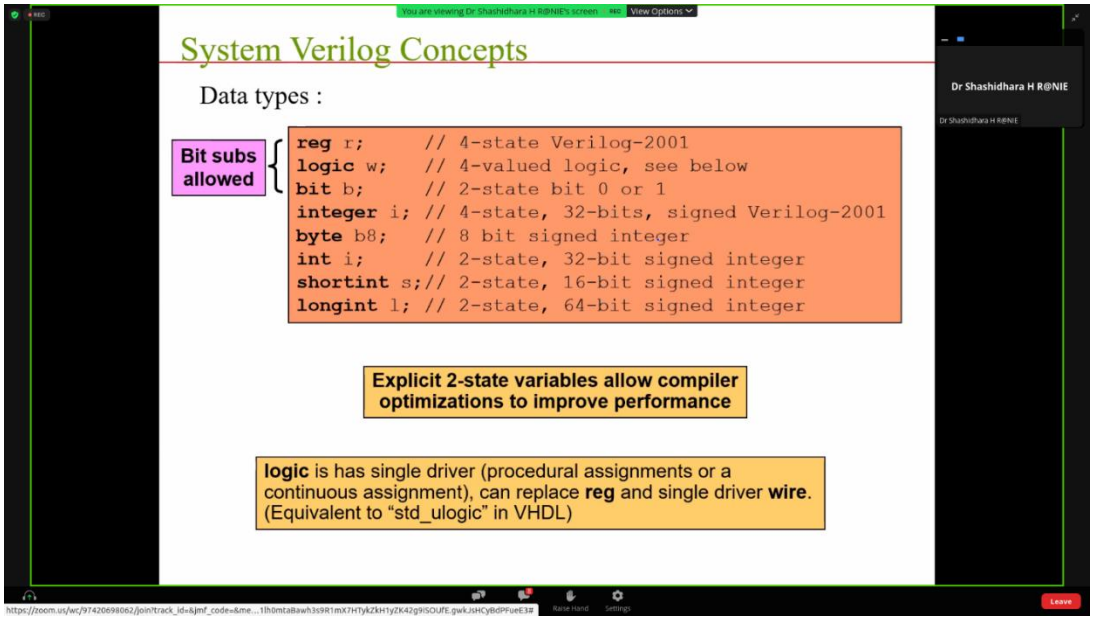


**Figure 1.17** The System Verilog Data types.

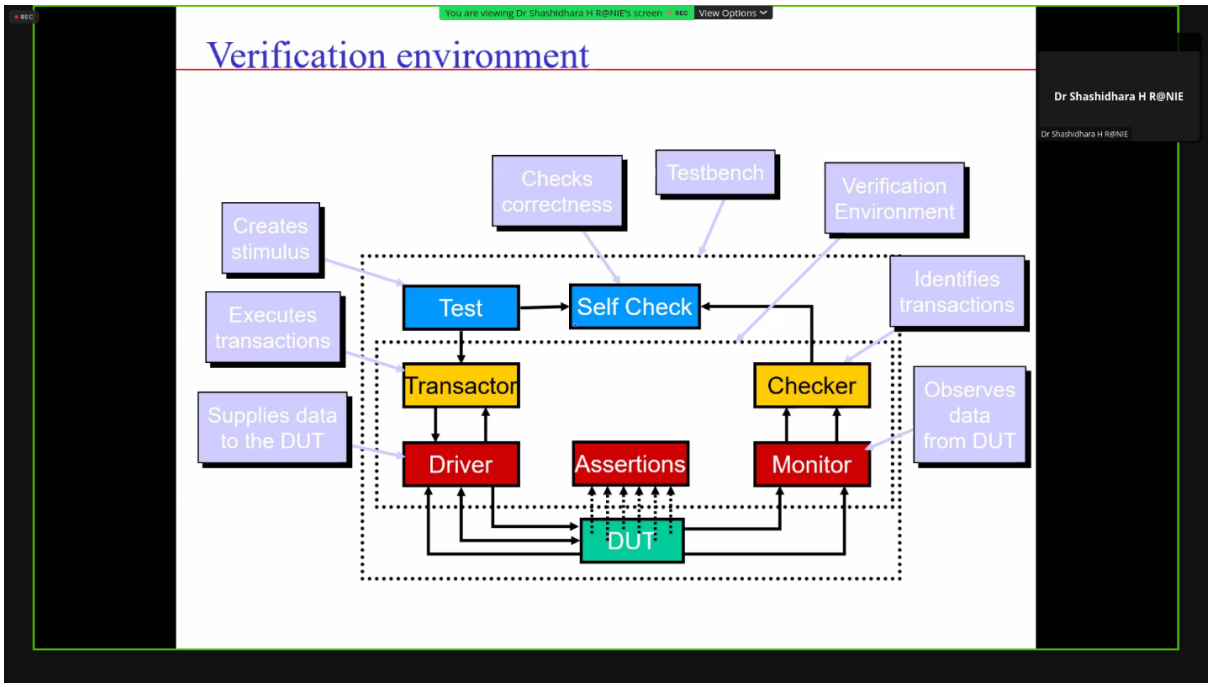


**Figure 1.18** The System Verilog Verification environment.

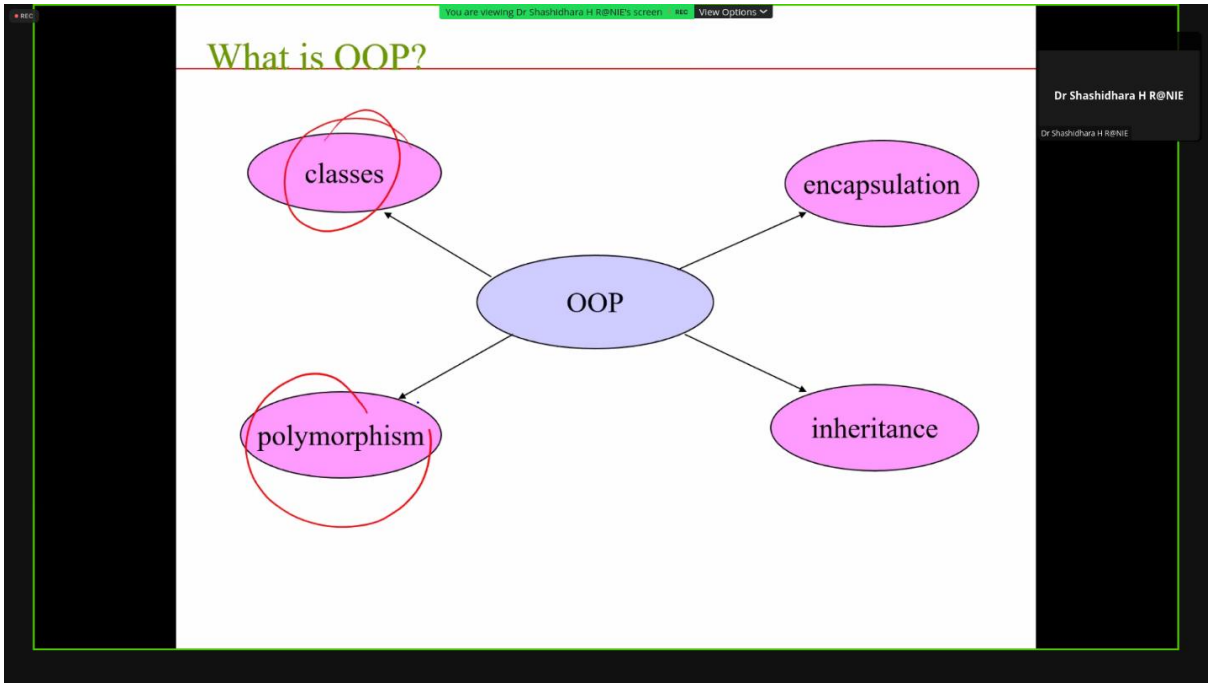


**Figure 1.19** The System Verilog OOP.

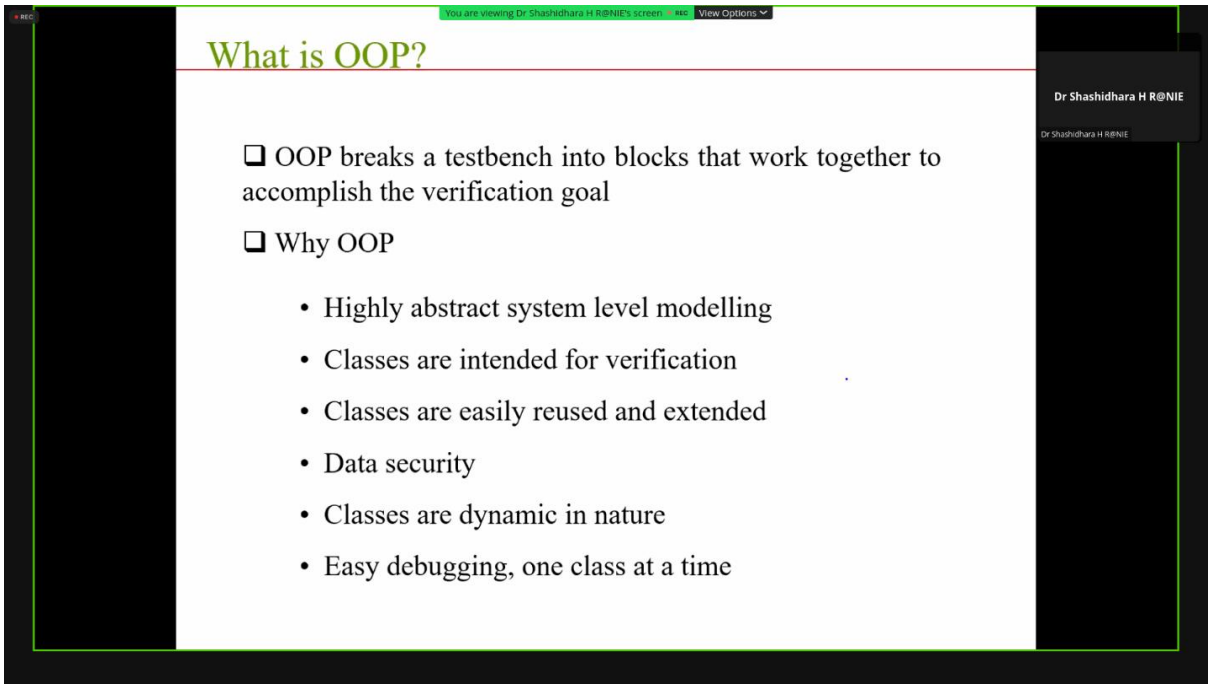


**Figure 1.20** The System Verilog OOP.

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## **(e)** SoC Design using OpenPower Cores Chiplet Integration.

The implementing the Chiplet model as a means to develop next-generation 3D-like chip designs. Chiplets can have different functions and process nodes. Customers can mix-and-match the chiplets, and then assemble them in an existing advanced package or a new architecture. The goal is to speed up time to market and reduce the cost.


**Figure 1.20** The Chiplet Integration.

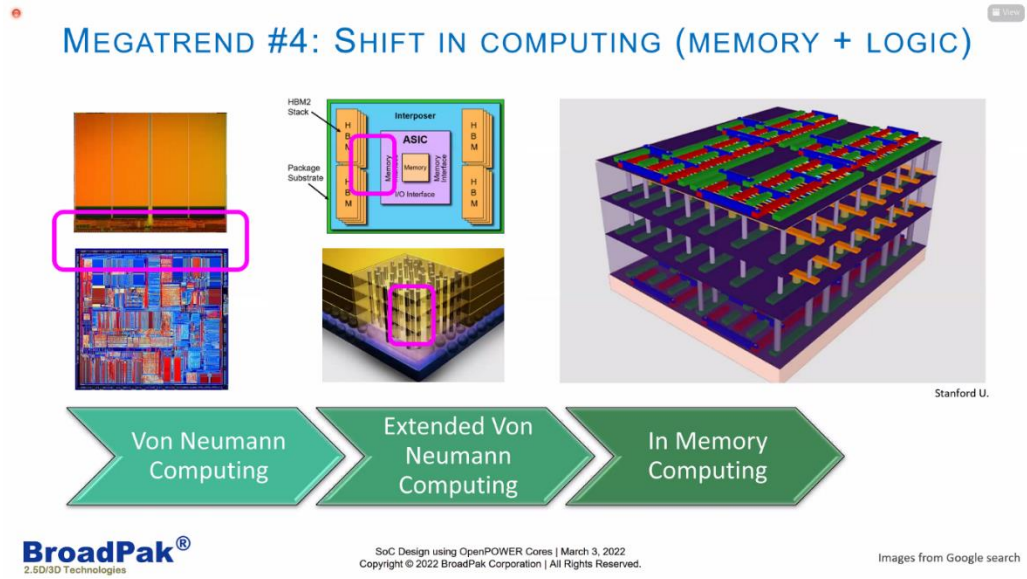


**Figure 1.21** The Memory Computing.


**Figure 1.21** The DARPA Chips Program.

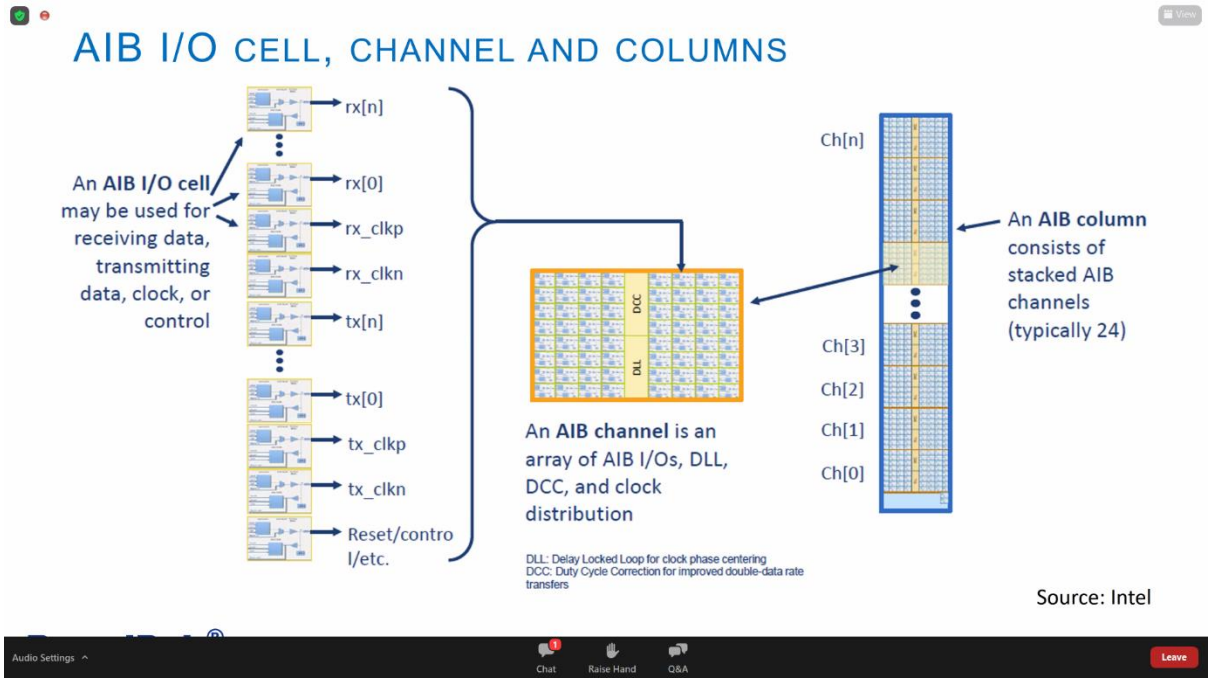


**Figure 1.22** The AIB I/O Cell, Channel and Columns.

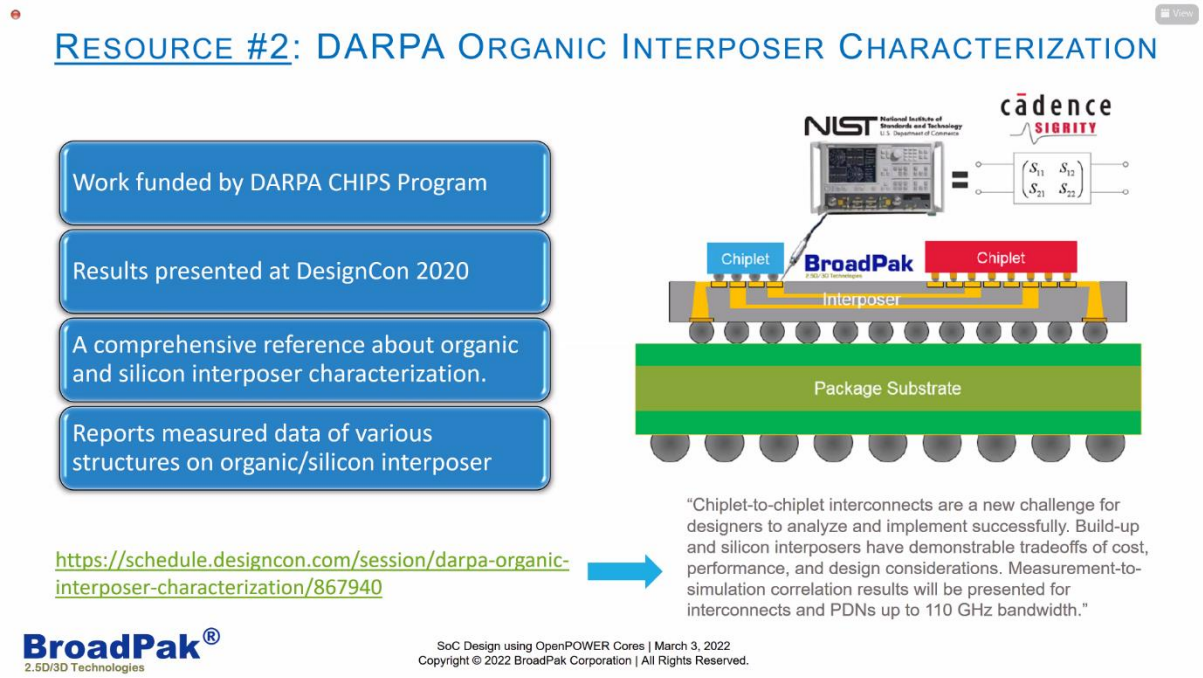


**Figure 1.23** The Organic Interposer Characterization.

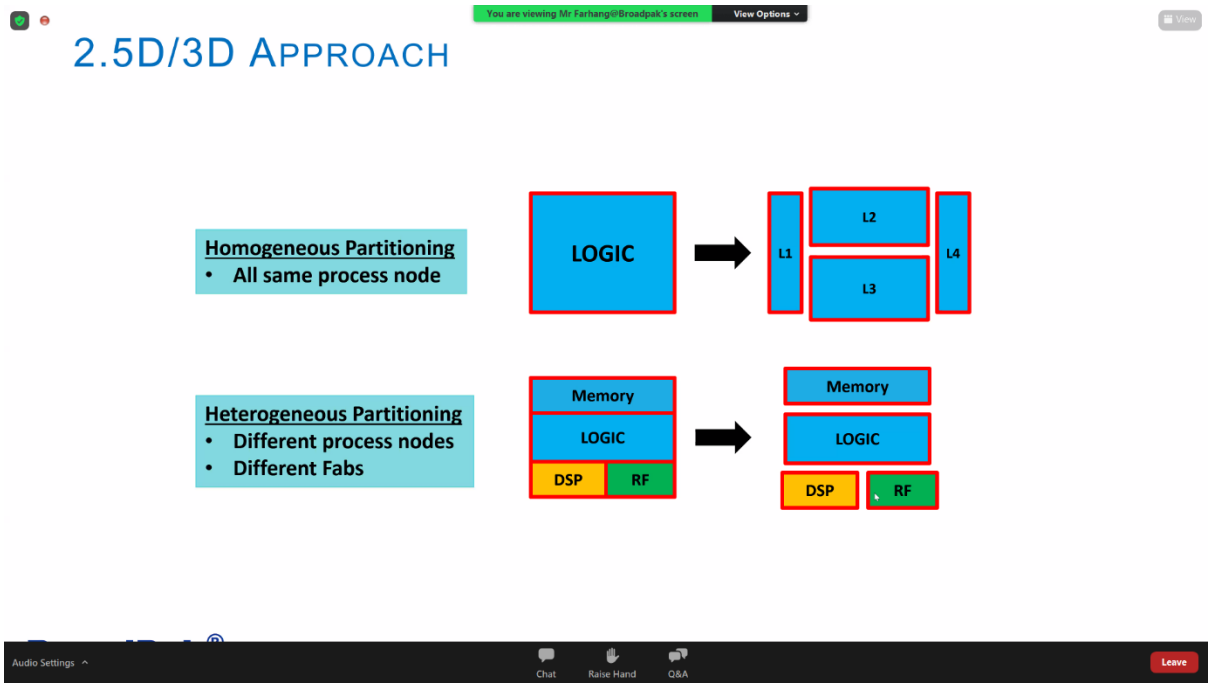


**Figure 1.24** The 2.5D/3D Approach.

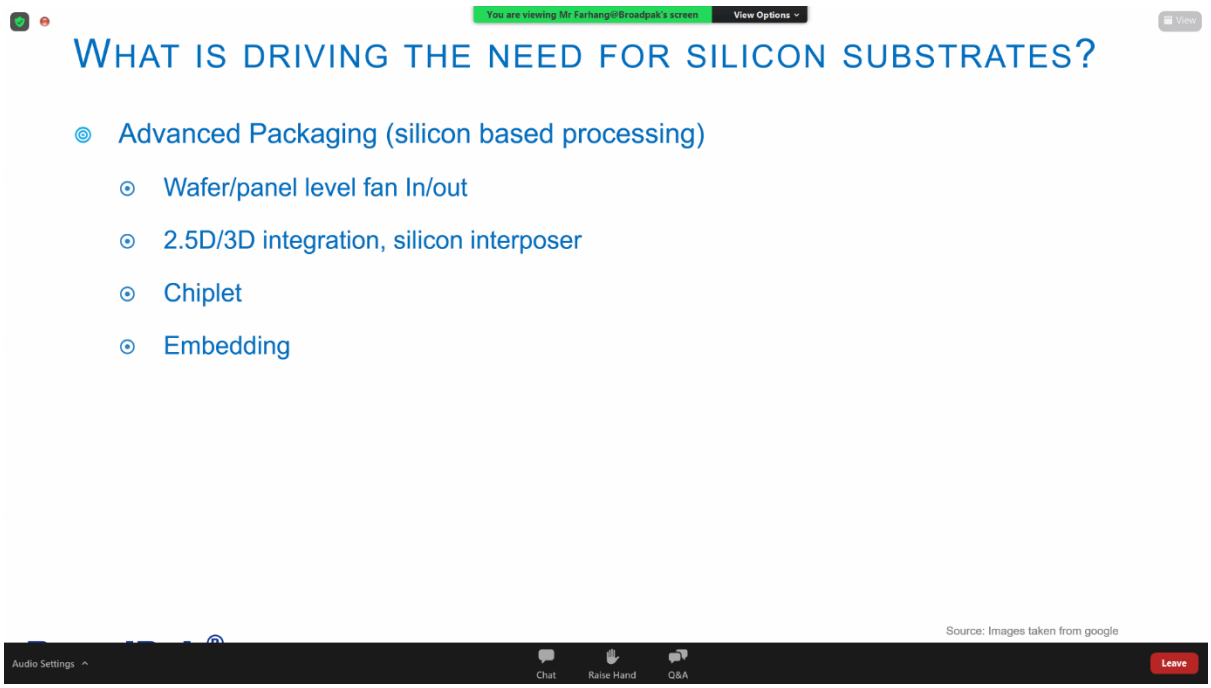


**Figure 1.25** The Silicon Substrate.

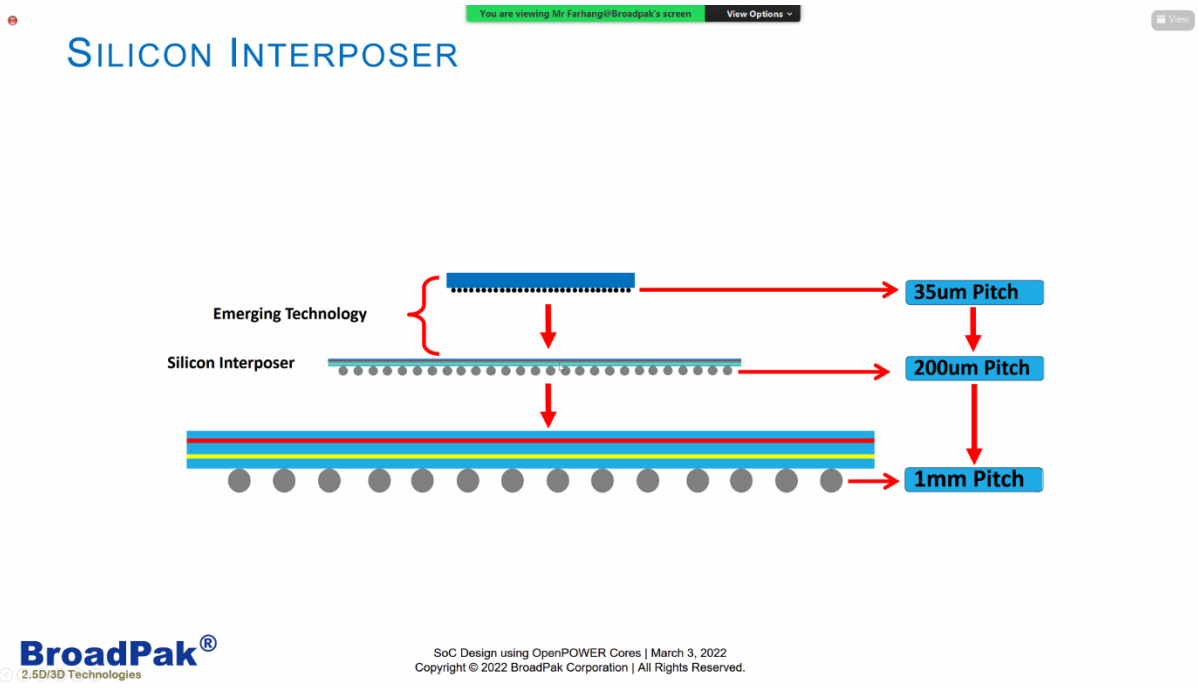


**Figure 1.26** The Silicon Interposer.

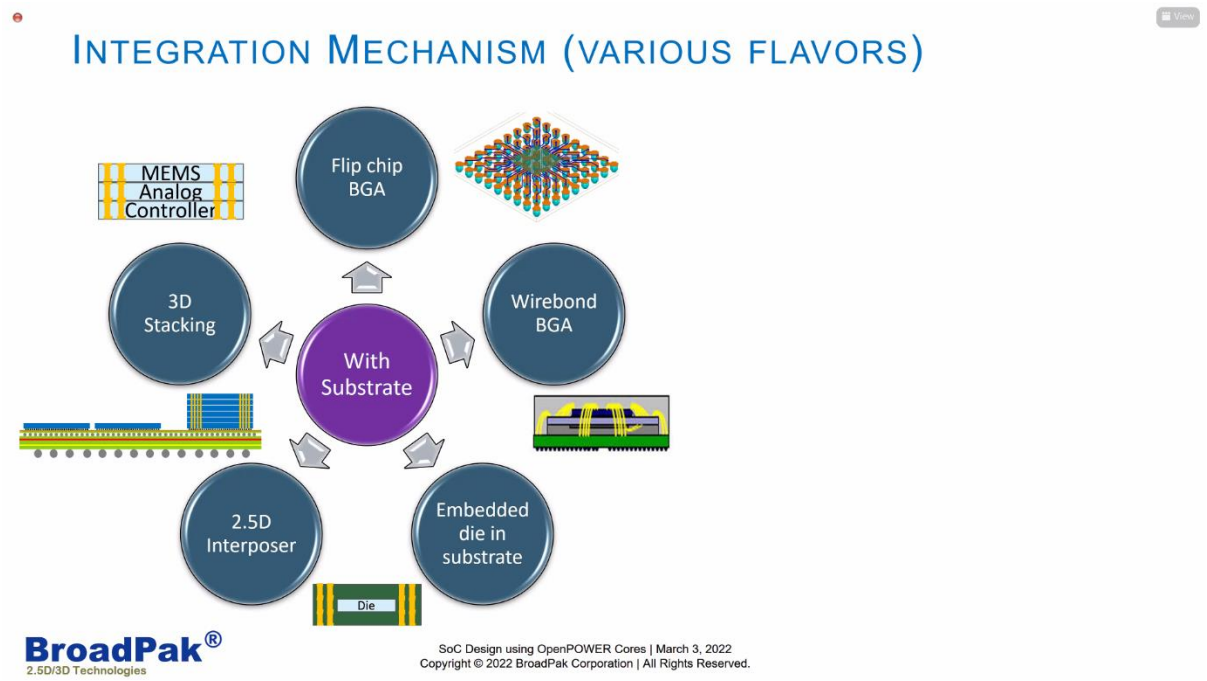


**Figure 1.27** The Integration Mechanism.

# Programming, Coriolis 2 Flow for GDS II by Abhishek Sharma

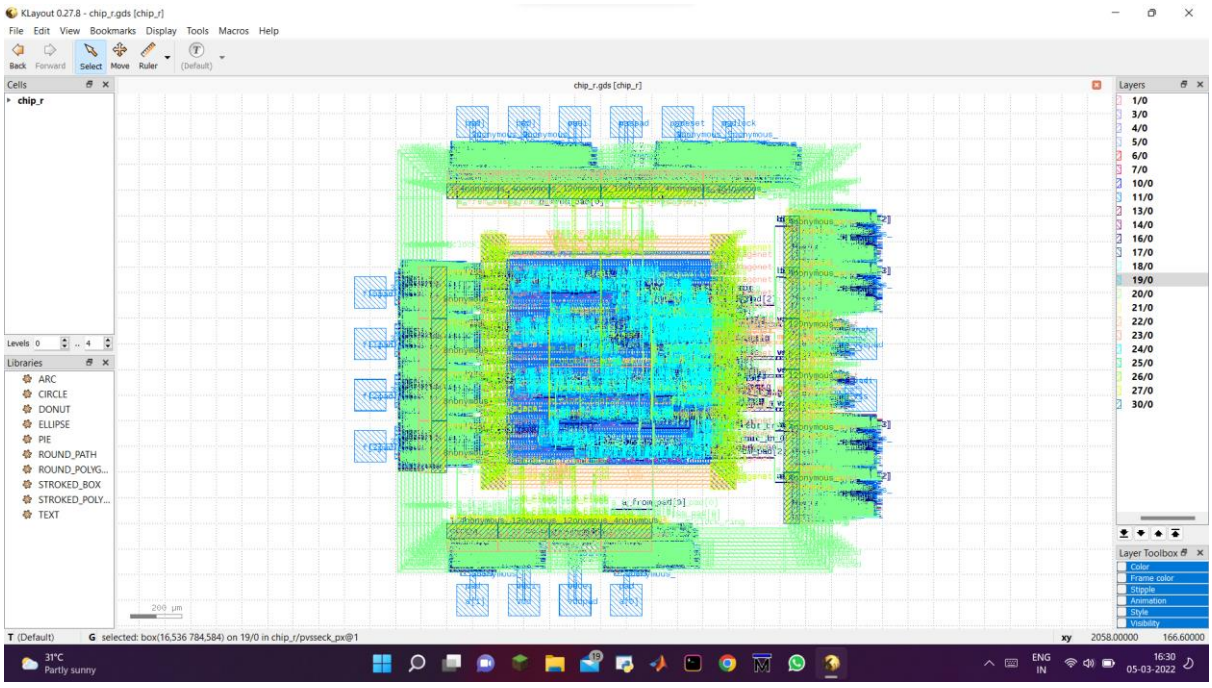


**Figure 1.28** The Coriolis 2 Flow for GDS II Flow.