

ECE6024 – VLSI Verification Methodologies

Project: Design and Verification of Simple Processor

by

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OVERVIEW

This project presents a verification technique of Simple Processor using System Verilog. The Simple Processor is a digital system that used to store 9-bit data and also performs arithmetic operations (addition, subtraction) on 9-bit data. This digital system contains registers(R0–R7), multiplexer, adder and also a controller. The following tasks have been performed as part of verification plan - checking reset functionality, checking MVI (move Immediate operation), checking MV (move operation), checking ADD (addition) operations, checking SUB (subtraction) operation using assertions.

DUT

The DUT consists of Controller block and Datapath block. The Control Path implements FSM and provide control signals to the Datapath in proper sequence. The Data Path consists of functional units where all computations are carried out.

TEST PLAN

- Provide the reset signal and check whether the registers are loaded with 9'b0.
- Store the initial data into the registers.
- Randomize the data "DIN" and store the values to the respective registers, check the values in the registers using immediate assertions.
- Perform Move immediate, Move, Addition and Subtraction operation.
- Provide the "DIN [8:6]" for non-instructional value and check the status of the system.

CONCLUSION

- The main objective of the DUT has been verified with randomized instructions.
- The coverage has been achieved to be **96.93%**.
- The code coverage has been achieved to be **100%**.
- The cover group coverage is **87.5%**.

Top Module

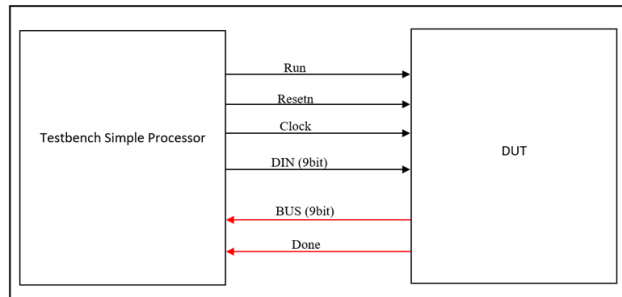


Figure 1 Top Module

RESULTS

```
Transcript
405INSTRUCTION EXECUTED
405---DATA LOADED TO DIN---
----- START RANDOMIZATION ----- START RANDOMIZATION ----- S'
Generating Sequence 0
Time=420 [GEN] : Send Data to Driver
# Time=420 -- DIN=000_000_110 --
# MOVE OPERATION GENERATED
Time=420 [DRV] : Rcvd Data from Generator
# Time=420 -- DIN=000_000_110 --
# [DRV] :----- INTERFACE TRIGGER -----
Time=425 [MON] : data send to Scoreboard
# Time=425 [DUT---MON] BUS LOADED WITH DIN :000000110
# *****
Generating Sequence 1
Time=430 [GEN] : Send Data to Driver
# Time=430 -- DIN=000_101_001 --
# MOVE OPERATION GENERATED
Time=430 [DRV] : Rcvd Data from Generator
# Time=430 -- DIN=000_101_001 --
# [DRV] :----- INTERFACE TRIGGER -----
Time=440 [DUT---MON] BUS LOADED WITH MOVE DATA :111011011
Time=445 [MON] : data send to Scoreboard
# Time=445 [DUT---MON] BUS LOADED WITH DIN :111011011
# ***** [SCOREBOARD] -----MOVE OPERATION DONE
Time=445 -- DIN=000_101_001 --
Time=445 [SCOREBOARD] BUS CONTENTS = 111011011
Time=445 [SCOREBOARD]-----MOVE OPERATION DATA DONE
Time=445 [SCOREBOARD] MOVE OPERATION DONE PASS---MOVE OPERATION DONE PASS---
# *****
```

Figure 2 Bug Free

```
Transcript
# *****
Generating Sequence 3
# Time=480 [GEN] : Send Data to Driver
# Time=480 -- DIN=000_000_110 --
# MOVE OPERATION GENERATED
# Time=480 [DRV] : Rcvd Data from Generator
# Time=480 -- DIN=000_000_110 --
# [DRV] :----- INTERFACE TRIGGER -----
Time=485 [MON] : data send to Scoreboard
# Time=485 [DUT---MON] BUS LOADED WITH DIN :000000110
# *****
Generating Sequence 4
# Time=490 [GEN] : Send Data to Driver
# Time=490 -- DIN=000_101_001 --
# MOVE OPERATION GENERATED
# Time=490 [DRV] : Rcvd Data from Generator
# Time=490 -- DIN=000_101_001 --
# [DRV] :----- INTERFACE TRIGGER -----
Time=500 [DUT---MON] BUS LOADED WITH MOVE DATA :111011011
Time=505 [MON] : data send to Scoreboard
# Time=505 [DUT---MON] BUS LOADED WITH DIN :111011011
Time=505 [SCOREBOARD]-----MOVE OPERATION NOT DONE
# Time=505 -- DIN=000_101_001 --
Time=505 [SCOREBOARD] BUS CONTENTS = 111011011
Time=505 [SCOREBOARD]-----MOVE OPERATION DATA NOT DONE
Time=505 [SCOREBOARD] MOVE OPERATION NOT DONE FAIL ---MOVE OPERATION NOT DONE FAIL---
# *****
```

Figure 3 Bug detected in DUT

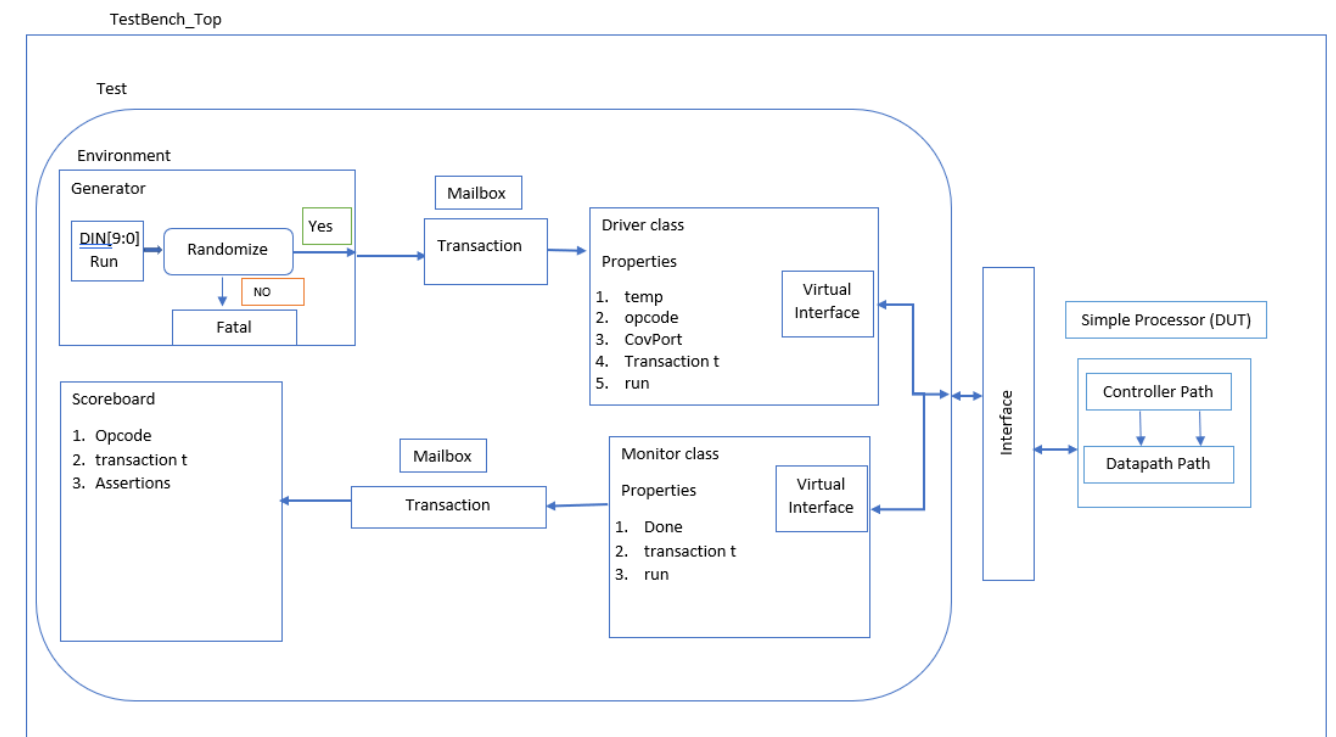


Figure 2 Testbench Setup

Design Units Coverage Summary (96.93%)

Coverage Type	Bins	Has	Misses	Coverage
Search	Search	Search	Search	Search
Branches	104	95	9	91.34%
Conditions	32	29	3	90.62%
Expressions	12	12	0	100%
FSM States	4	4	0	100%
FSM Transitions	6	6	0	100%
Statements	296	292	4	98.64%
Toggles	1238	1212	26	97.89%

Figure 4 Code Coverage

Covergroups

Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	Get_inst_coverage	Comment
test_Version1_sv_unit:driver		87.50%							
TYPE CovPort		87.50%	100	87.50%					auto(1)

Figure 5 Covergroup for DIN