Date:3/6/2022

Fall Semester 2021-2022

ECE5014 – ASIC Design

M.Tech VLSI Design

School of Electronics Engineering

Vellore Institute of Technology

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Slot: L3+L4

Date:3/6/2022

Lab Task 05

Physical Design – Extraction, Timing ECO Flow.

Section 1 Extraction of Parasitic

Questions :

1. Extraction of parasitic extraction in .spef in best and worst corners.

   Path used in the Design :
   /home/userdata/21mvd0086/Simple_Processor_Working/Physical_Synthesis_ICC2_LAB_TASk/LAB_TASK/starrc

1. The Scripts used for extraction of parasitic of Simple Processor Routed design

   (a) run.csh

   (b) cworst_spef.cmd

   (c) cbest_spef.cmd

   Script for run.csh :

   alias StarXtract /tools/synopsys/installers/starrc/starrc/P-2019.03/bin/StarXtract

   StarXtract -clean cworst_spef.cmd

   StarXtract -clean cbest_spef.cmd

   Script for cworst_spef.cmd :

   TCAD_GRD_FILE: saed14nm_1p9m_Cmin.nxtgrd

   MAPPING_FILE: saed14nm_tf_itf_tluplus.map

   NETLIST_FORMAT: SPEF

   BLOCK: Final_Route_Done

   NDM_DATABASE: ../lib

   NETLIST_FILE: Route_Simple_Processor_3_June.cbest.spef

Script for cbest_spef.cmd :

TCAD_GRD_FILE: saed14nm_1p9m_Cmax.nxtgrd

MAPPING_FILE: saed14nm_tf_itf_tluplus.map

NETLIST_FORMAT: SPEF

BLOCK: Final_Route_Done

NDM_DATABASE: ../lib

NETLIST_FILE: Route_Simple_Processor_3_June.cworst.spef

Section 2 Timing ECO Flow

(a) report _analysis_coverage in both corners with parasitics (.spef)

Worst case Scenario :

```
****************************************
Report : analysis_coverage
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Fri Jun  3 12:22:25 2022
****************************************
```

Type of Check	Total	Met	Violated	Untested
setup	138	97 (70%)	0 (0%)	41 (30%)
hold	138	95 (69%)	2 (1%)	41 (30%)
min_pulse_width	705	582 (83%)	0 (0%)	123 (17%)
out_setup	10	0 (0%)	0 (0%)	10 (100%)
out_hold	10	0 (0%)	0 (0%)	10 (100%)
All Checks	1001	774 (77%)	2 (0%)	225 (22%)

1

Best case Scenario :

```
****************************************
Report : analysis_coverage
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Fri Jun  3 12:27:45 2022
****************************************
```

Type of Check	Total	Met	Violated	Untested
setup	138	97 (70%)	0 (0%)	41 (30%)
hold	138	87 (63%)	10 (7%)	41 (30%)
min_pulse_width	705	582 (83%)	0 (0%)	123 (17%)
out_setup	10	0 (0%)	0 (0%)	10 (100%)
out_hold	10	0 (0%)	0 (0%)	10 (100%)
All Checks	1001	766 (77%)	10 (1%)	225 (22%)

1

(b) generate eco script used in pt_shell

The pt.tcl script

```
set std_cell_delay_corner "tt0p8v125c"
#set macro_cell_delay_corner "ff1p16v125c"

#provide path for routed netlist
#this should be dumped from the icc2 session and used as input here.
set input_verilog "../Simple_Processor_Routed_3rd_June.v"

#provide path for sdc
set input_sdc "../Simple_Processor_Routed_3rd_June.sdc"

#provide path for spef
set input_spef "../starrc/Route_Simple_Processor_3_June.cworst.spef"

set my_design "simple_processor_Top"

set DESIGN_REF_PATH "/home/synopsys/SAED14nm_EDK"

set search_path      " \
      ${DESIGN_REF_PATH}/stdcell_rvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_hvt/db_nldm \
      ${DESIGN_REF_PATH}/stdcell_lvt/db_nldm "


set link_path   "* \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.
db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.d
b \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.d
b"

set target_library " \
${DESIGN_REF_PATH}/stdcell_hvt/db_nldm/saed14hvt_tt0p8v125c.
db \
${DESIGN_REF_PATH}/stdcell_lvt/db_nldm/saed14lvt_tt0p8v125c.d
b \
${DESIGN_REF_PATH}/stdcell_rvt/db_nldm/saed14rvt_tt0p8v125c.d
b"


catch {sh mkdir db report_post_layout}
```

```
read_verilog "${input_verilog}"
#read_verilog "./${input_verilog}"
#set link_create_black_boxes false
current_design $my_design
link_design $my_design
read_sdc "${input_sdc}"
#read_sdc "./${input_sdc}"
read_parasitics "${input_spef}" -keep_capacitive_coupling -format
SPEF
#read_parasitics "./${input_spef}" -keep_capacitive_coupling -format
SPEF
update_timing -full
save_session ./db/${my_design}.session
```

The generate_eco.tcl

```
fix_eco_drc -type max_transition -verbose -methods size_cell
fix_eco_drc -type max_capacitance -verbose -methods size_cell
fix_eco_drc -type max_transition -verbose -buffer_list
{SAEDLVT14_BUF_4 SAEDLVT14_BUF_2 SAEDLVT14_BUF_6
SAEDLVT14_BUF_8}
fix_eco_drc -type max_capacitance -verbose -buffer_list
{SAEDLVT14_BUF_4 SAEDLVT14_BUF_2 SAEDLVT14_BUF_6
SAEDLVT14_BUF_8}
fix_eco_timing -type setup -slack_lesser_than 0 -buffer_list
{SAEDLVT14_BUF_4 SAEDLVT14_BUF_2 SAEDLVT14_BUF_6
SAEDLVT14_BUF_8}
fix_eco_timing -type hold -slack_lesser_than 0 -buffer_list
{SAEDHVT14_BUF_4 SAEDHVT14_BUF_2 SAEDHVT14_BUF_6
SAEDHVT14_BUF_8}

write_changes -format icctcl -output timing_eco_1.tcl
```

(c) report _analysis_coverage in both corners with parasitics (.spef) after fixing violations

Worst case Scenario :

```
****************************************
Report : analysis_coverage
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Fri Jun  3 12:22:25 2022
****************************************
```

Type of Check	Total	Met	Violated	Untested
setup	138	97 (70%)	0 (0%)	41 (30%)
hold	138	97 (70%)	0 (0%)	41 (30%)
min_pulse_width	705	582 (83%)	0 (0%)	123 (17%)
out_setup	10	0 (0%)	0 (0%)	10 (100%)
out_hold	10	0 (0%)	0 (0%)	10 (100%)
All Checks	1001	776 (77%)	0 (0%)	225 (23%)

1

Best case Scenario :

```
****************************************
Report : analysis_coverage
Design : simple_processor_Top
Version: P-2019.03-SP4
Date   : Fri Jun  3 12:27:45 2022
****************************************
```

Type of Check	Total	Met	Violated	Untested
setup	138	97 (70%)	0 (0%)	41 (30%)
hold	138	97 (63%)	0 (0%)	41 (30%)
min_pulse_width	705	582 (83%)	0 (0%)	123 (17%)
out_setup	10	0 (0%)	0 (0%)	10 (100%)
out_hold	10	0 (0%)	0 (0%)	10 (100%)
All Checks	1001	776 (77%)	0 (0%)	225 (23%)

1

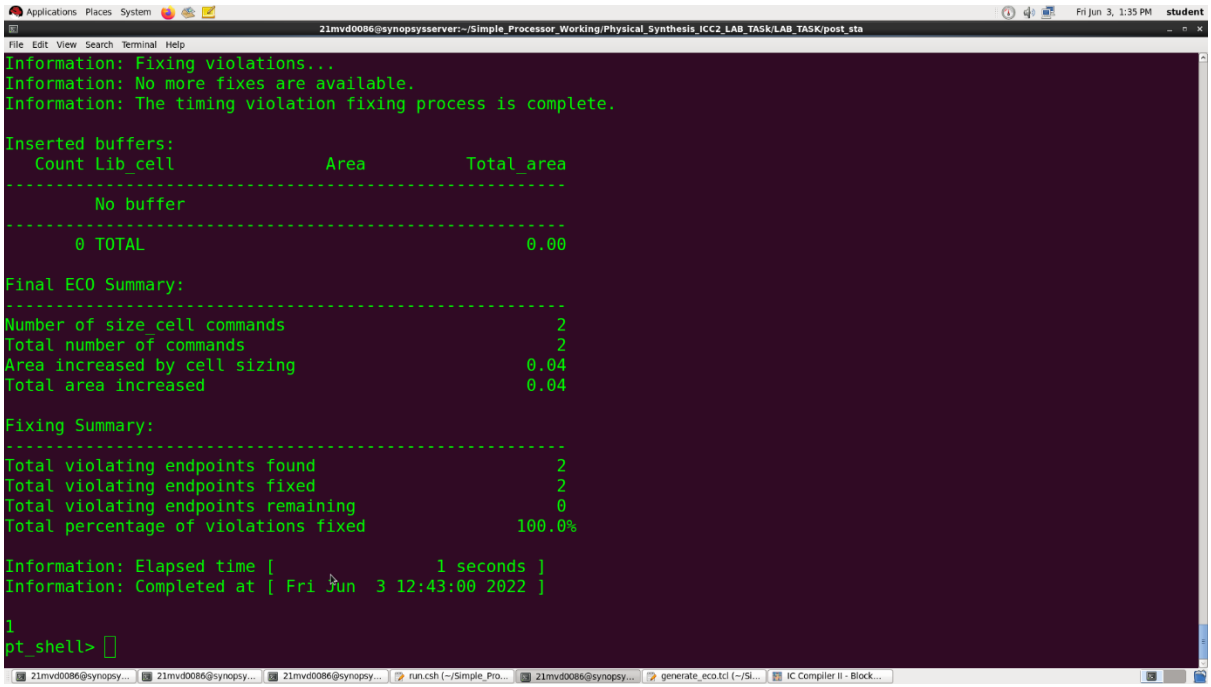

Figure 2.1 : The Figure shows the timing violations.

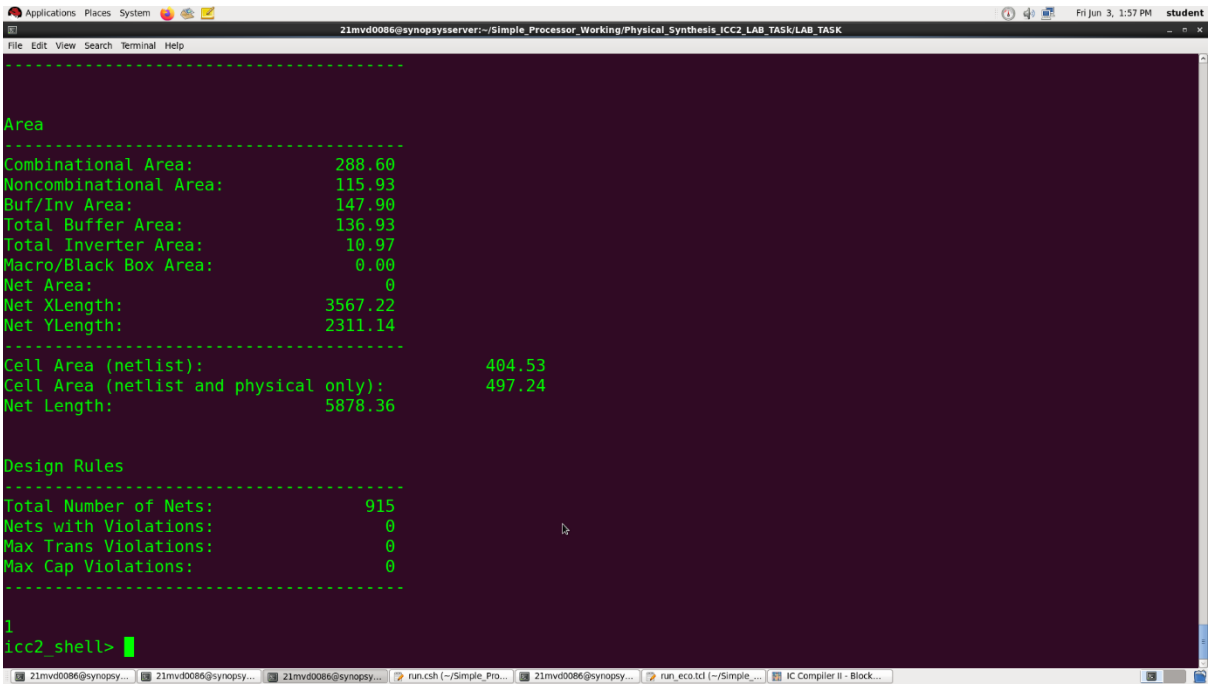

Figure 2.2 : The Figure shows the No DRC Violations

(d) timing_eco script to fix violations

Timing ECO Script

The filename :

```
##############################################################################

# Change list, formatted for IC Compiler
#
#
#
##############################################################################
####
current_instance
current_instance {G2_Datapath}
size_cell {HFSBUF_864_2} {SAEDLVT14_BUF_ECO_1}
current_instance
current_instance {G2_Datapath/m1}
insert_buffer [get_pins {Bus_reg_3_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET1} -new_cell_names {U_PTECO_DRC_BUF1}
insert_buffer [get_pins {Bus_reg_0_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET2} -new_cell_names {U_PTECO_DRC_BUF2}
insert_buffer [get_pins {Bus_reg_4_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET3} -new_cell_names {U_PTECO_DRC_BUF3}
insert_buffer [get_pins {Bus_reg_5_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET4} -new_cell_names {U_PTECO_DRC_BUF4}
insert_buffer [get_pins {Bus_reg_6_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET5} -new_cell_names {U_PTECO_DRC_BUF5}
insert_buffer [get_pins {Bus_reg_7_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET6} -new_cell_names {U_PTECO_DRC_BUF6}
insert_buffer [get_pins {Bus_reg_2_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET7} -new_cell_names {U_PTECO_DRC_BUF7}
insert_buffer [get_pins {Bus_reg_1_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET8} -new_cell_names {U_PTECO_DRC_BUF8}
insert_buffer [get_pins {Bus_reg_8_/Q}] SAEDLVT14_BUF_2 -new_net_names
{net_PTECO_DRC_NET9} -new_cell_names {U_PTECO_DRC_BUF9}
current_instance
current_instance {G2_Datapath/Reg0}
size_cell {copt_h_inst_9918} {SAEDHVT14_BUF_S_0P5}
current_instance
current_instance {G2_Datapath/Reg7}
size_cell {copt_h_inst_9761} {SAEDRVT14_BUF_S_1P5}
insert_buffer [get_pins {U12/X}] SAEDHVT14_BUF_2 -new_net_names {net10} -
new_cell_names {U13}
current_instance
```

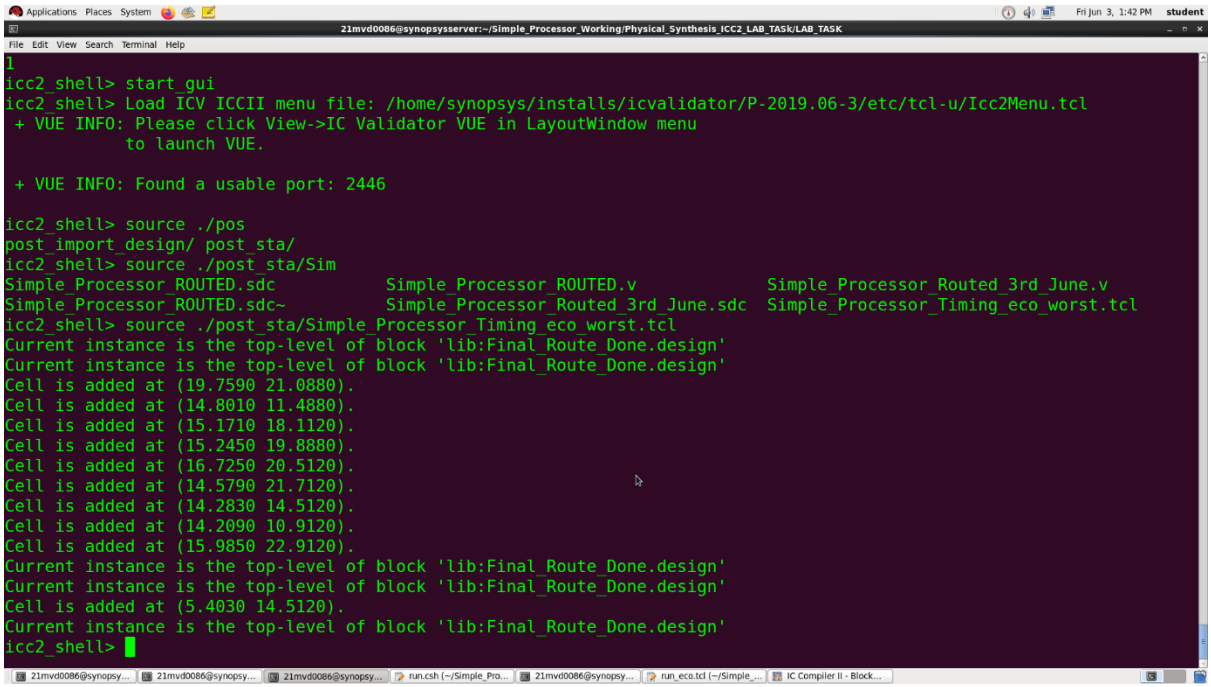

Figure 2.3: shows addition of Cells to remove the Buffers.

(e) report_qor after place and route in ICC2 using timing_eco.

```
****************************************
Report : qor
Design : simple_processor_Top/G2_Datapath
Version: P-2019.03-SP4
Date   : Fri Jun  3 12:58:23 2022
****************************************
Information: Timer using 'PrimeTime Delay Calculation, SI, Timing
Window Analysis'. (TIM-050)


Scenario          'func_fast'
Timing Path Group  'CLOCK'
-----------------------------------
Worst Hold Violation:          -0.00
Total Hold Violation:          -0.01
No. of Hold Violations:            5
-----------------------------------

Scenario          'func_fast'
Timing Path Group  'INPUTS'
-----------------------------------
Worst Hold Violation:           0.00
Total Hold Violation:           0.00
```

```
No. of Hold Violations:             0
----------------------------------------

Scenario          'func_slow'
Timing Path Group  'CLOCK'
----------------------------------------
Levels of Logic:                   15
Critical Path Length:              0.32
Critical Path Slack:               9.51
Critical Path Clk Period:          10.00
Total Negative Slack:              0.00
No. of Violating Paths:             0
----------------------------------------

Scenario          'func_slow'
Timing Path Group  'INPUTS'
----------------------------------------
Levels of Logic:                    2
Critical Path Length:              1.16
Critical Path Slack:               8.68
Critical Path Clk Period:          10.00
Total Negative Slack:              0.00
No. of Violating Paths:             0
----------------------------------------


Cell Count
----------------------------------------
Hierarchical Cell Count:           78
Hierarchical Port Count:          991
Leaf Cell Count:                  896
Buf/Inv Cell Count:               416
Buf Cell Count:                   376
Inv Cell Count:                   40
CT Buf/Inv Cell Count:             0
Combinational Cell Count:         758
Sequential Cell Count:            138
  Integrated Clock-Gating Cell Count:          0
  Sequential Macro Cell Count:                 0
  Single-bit Sequential Cell Count:            99
  Multi-bit Sequential Cell Count:             0
  Sequential Cell Banking Ratio:               0.00%
  BitsPerflop:                          1.00
Macro Count:                       0
----------------------------------------
```

Area

Combinational Area: 288.60
Noncombinational Area: 115.93
Buf/Inv Area: 147.90
Total Buffer Area: 136.93
Total Inverter Area: 10.97
Macro/Black Box Area: 0.00
Net Area: 0
Net XLength: 3567.22
Net YLength: 2311.14

Cell Area (netlist): 404.53
Cell Area (netlist and physical only): 497.24
Net Length: 5878.36

Design Rules

Total Number of Nets: 915
Nets with Violations: 0
Max Trans Violations: 0
Max Cap Violations: 0

1

(f) if any logical DRC and timing violations, try to fix manually and give the report.

From above report we observe there is no DRC and Timing Violations.

```
****************************************
Report : constraint
       -all_violators
Design : simple_processor_Top/G2_Datapath
Version: P-2019.03-SP4
Date   : Fri Jun  3 13:08:30 2022
****************************************

  late_timing
  -----------

Error: None of the specified scenarios are active for setup analysis. (UIC-057)
Information: Timer using 'PrimeTime Delay Calculation, SI, Timing Window Analysis'. (TIM-050)
Endpoint                  Path Delay     Path Required      CRP    Slack Group    Scenario
--------------------------------------------------------------------------------------------
```

```
No paths.

  early_timing
  ----------

Information: Timer using 'PrimeTime Delay Calculation, SI, Timing Window Analysis'. (TIM-
050)
Endpoint                    Path Delay    Path Required      CRP    Slack Group    Scenario
-------------------------------------------------------------------------------------------------
G2_Datapath/A5/dout_reg_1_/D (SAEDHVT14_FDP_V2LP_1)
                          1.19 r        1.20          0.00    -0.00   CLOCK    func_fast
G2_Datapath/Reg1/dout_reg_3_/D (SAEDHVT14_FDP_V2LP_0P5)
                          1.20 f        1.20          0.00    -0.00   CLOCK    func_fast
G2_Datapath/Reg4/dout_reg_3_/D (SAEDHVT14_FDP_V2LP_1)
                          1.20 f        1.20          0.00    -0.00   CLOCK    func_fast
G2_Datapath/Reg0/dout_reg_4_/D (SAEDHVT14_FDP_V2LP_1)
                          1.20 f        1.20          0.00    -0.00   CLOCK    func_fast
G2_Datapath/Reg6/dout_reg_5_/D (SAEDHVT14_FDP_V2LP_1)
                          1.20 f        1.20          0.00    -0.00   CLOCK    func_fast

  Mode: func Corner: fast
  Scenario: func_fast
  max_transition
                    Required       Actual
  Net                Transition     Transition       Slack  Violation
 ------------------------------------------------------------------------
  G2_Datapath/HFSNET_0        0.50          0.14          0.36  (MET)

 ------------------------------------------------------------------------
  Number of max_transition violation(s): 0

  Mode: func Corner: fast
  Scenario: func_fast
 ------------------------------------------------------------------------
  Number of min_capacitance violation(s): 0

  Total number of violation(s): 0
1
```

```
icc2_shell> current_scenario func_slow
{func_slow}
icc2_shell> report_constraints -all_violators
****************************************
Report : constraint
      -all_violators
Design : simple_processor_Top/G2_Datapath
Version: P-2019.03-SP4
Date   : Fri Jun  3 13:08:31 2022
****************************************

  late_timing
  ----------
```

```
Information: Timer using 'PrimeTime Delay Calculation, SI, Timing Window Analysis'.
(TIM-050)
Endpoint                  Path Delay    Path Required     CRP    Slack Group    Scenario
-------------------------------------------------------------------------------------------------------------
No paths.

  early_timing
  ----------

Error: None of the specified scenarios are active for hold analysis. (UIC-057)
Information: Timer using 'PrimeTime Delay Calculation, SI, Timing Window Analysis'.
(TIM-050)
Endpoint                  Path Delay    Path Required     CRP    Slack Group    Scenario
-------------------------------------------------------------------------------------------------------------
No paths.

  Mode: func Corner: slow
  Scenario: func_slow
  max_transition
                    Required      Actual
  Net               Transition    Transition      Slack  Violation
 ---------------------------------------------------------------------------
  G2_Datapath/HFSNET_0       0.50          0.14          0.36  (MET)

 ---------------------------------------------------------------------------
  Number of max_transition violation(s): 0

  Mode: func Corner: slow
  Scenario: func_slow
  max_capacitance
                    Required      Actual
  Net               Capacitance   Capacitance     Slack  Violation
    ---------------------------------------------------------------------------
      Number of min_capacitance violation(s): 0

      Total number of violation(s): 0
    1
```

(g) Physical verification script. Report for DRC and LVS errors.

The pt.tcl script used :

```
#Now Let's insert the filler cells

create_stdcell_fillers -lib_cells { */SAEDLVT14_FILL64 */SAEDLVT14_FILL32 */SAEDLVT14_FILL3 */SAEDLVT14_FILL2 */SAEDLVT14_FILL4 }


#Perform Logical Connections

connect_pg_net -net VSS [get_pins */VSS]

connect_pg_net -net VDD [get_pins */VDD]


# Delete the filler cells that have routing DRC violations

remove_stdcell_fillers_with_violation


#Let us verify and report routing design rule checking (DRC) violations, by using "check_routes" command

check_routes


# Set the DRC runset file.

set_app_options -name signoff.check_drc.runset -value ./pv/saed14nm_1p9m_drc_rules.rs

set_app_options -name signoff.check_drc.max_errors_per_rule -value 1000

set_app_options -name signoff.check_drc.run_dir -value "icvDRC_run"

setenv _ICV_RSH_COMMAND ssh

signoff_check_drc

#set_app_options -list {signoff.fix_drc.init_drc_error_db "icvDRC_run"}

#signoff_fix_drc


#Run the command to check the LVS,by using "check_lvs" command

check_lvs
```

#Metal fill

set_app_options -name signoff.create_metal_fill.runset -value "./pv/saed14nm_1p9m_mfill_rules.rs"

signoff_create_metal_fill

create_utilization_configuration -scope block core_utilization -include {all}

report_utilization -config core_utilization

save_block -as Simple_Processor_Final_DRC_LVS_after_Done

Check LVS

icc2_shell> check_lvs

Information: Using 1 threads for LVS

[Check Short] Stage 1 Elapsed = 0:00:00, CPU = 0:00:00

[Check Short] Stage 1-2 Elapsed = 0:00:00, CPU = 0:00:00

[Check Short] Stage 2 Elapsed = 0:00:00, CPU = 0:00:00

Detected more than 20 short violations. Skip checking short violations

[Check Short] Stage 3 Elapsed = 0:00:00, CPU = 0:00:00

[Check Short] End Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] Init Elapsed = 0:00:00, CPU = 0:00:00

Warning: Port VDD have no valid pin shapes. Skip this port. (RT-203)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n5. BBox: (5.1250 4.9050)(5.2150 4.9390). Layer: M1. (RT-586)

Information: Detected open violation for Net VDD. BBox: (0.0000 0.0000)(27.4560 27.2000). (RT-585)

Information: Detected short violation. Net1: G1_Controller/n21. Net2: G1_Controller/n7. BBox: (7.2360 6.1630)(7.2700 6.1790). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n21. Net2: G1_Controller/n7. BBox: (7.2360 6.1630)(7.2700 6.1790). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/N150. Net2: G1_Controller/n9. BBox: (5.9780 6.0890)(5.9950 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/N150. Net2: G1_Controller/n9. BBox: (5.9780 6.0890)(5.9950 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n9. BBox: (5.8450 6.0890)(5.8640 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n9. BBox: (5.8450 6.0890)(5.8640 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n9. BBox: (5.9040 6.0890)(5.9350 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n9. BBox: (5.9040 6.0890)(5.9350 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n10. Net2: G1_Controller/n23. BBox: (5.7850 6.0890)(5.7900 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n10. Net2: G1_Controller/n23. BBox: (5.7850 6.0890)(5.7900 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n9. BBox: (5.8450 6.0890)(5.9350 6.1230). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/HFSNET_0. Net2: G1_Controller/n23. BBox: (5.3120 6.1630)(5.3350 6.1970). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/HFSNET_0. Net2: G1_Controller/n23. BBox: (5.3120 6.1630)(5.3350 6.1970). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G2_Datapath/m1/n3. Net2: R2out. BBox: (14.0440 5.4970)(14.0780 5.5310). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G2_Datapath/m1/n3. Net2: R2out. BBox: (14.0440 5.4970)(14.0780 5.5310). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n9. BBox: (5.2380 4.9050)(5.2720 4.9390). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n9. BBox: (5.2380 4.9050)(5.2720 4.9390). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n5. BBox: (5.1640 4.9050)(5.1980 4.9390). Layer: M1. (RT-586)

Information: Detected short violation. Net1: G1_Controller/n23. Net2: G1_Controller/n5. BBox: (5.1640 4.9050)(5.1980 4.9390). Layer: M1. (RT-586)

Warning: Port VSS have no valid pin shapes. Skip this port. (RT-203)

[Check Net] 10% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 20% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 30% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 40% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 50% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 60% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 70% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 80% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] 90% Elapsed = 0:00:00, CPU = 0:00:00

[Check Net] All nets are submitted.

[Check Net] 100% Elapsed = 0:00:00, CPU = 0:00:00

Information: Detected open violation for Net VSS. BBox: (0.0000 0.0000)(27.4560 27.2000). (RT-585)

==========

Maximum number of violations is set to 20

Abort checking when more than 20 violations are found

All violations might not be found.

==========

Total number of input nets is 915.

Total number of short violations is 20.

Total number of open nets is 2.

Open nets are VDD VSS

Total number of floating route violations is 0.

Elapsed = 0:00:00, CPU = 0:00:00

1

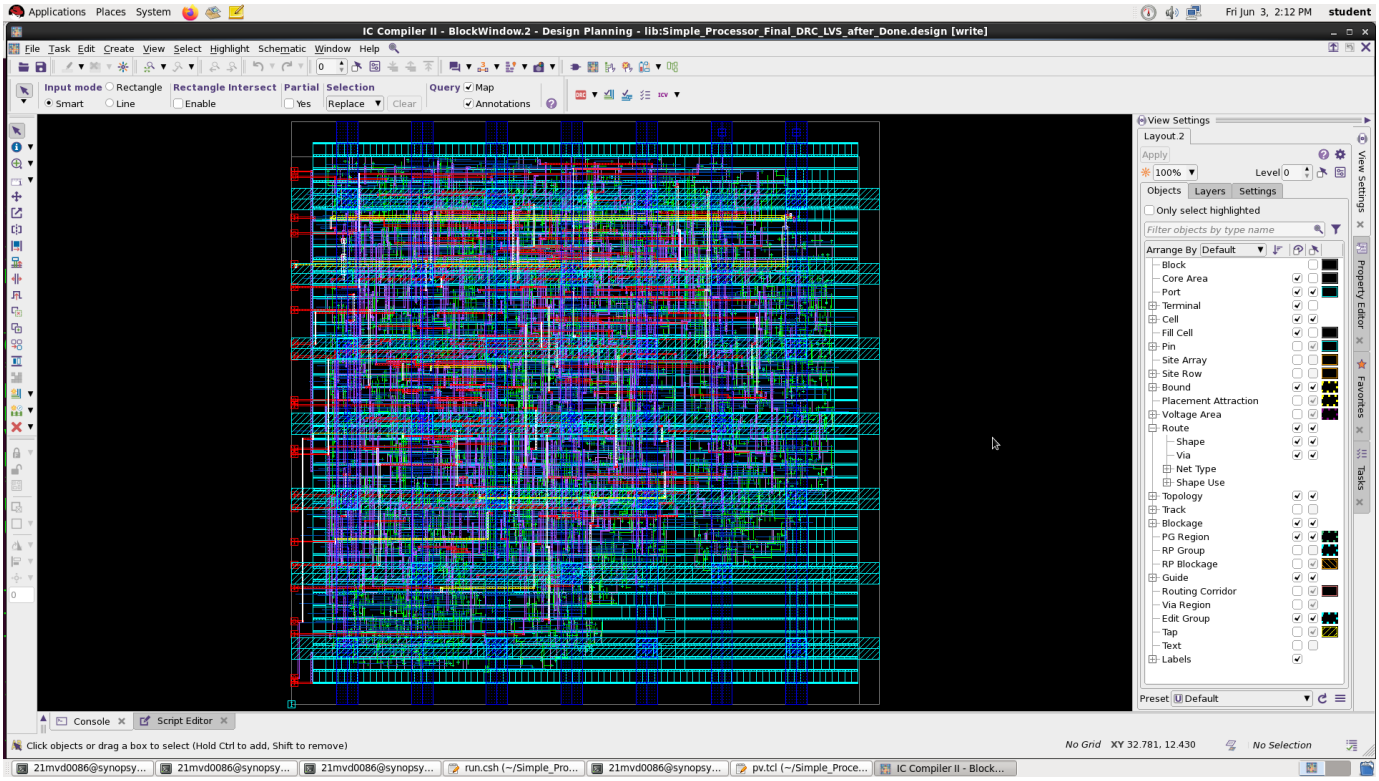

Figure 2.4 The Final Signoff Simple Processor Design.

Path Details :

1. **starrc Folder location :**

   /home/userdata/21mvd0086/Simple_Processor_Working/Physical_Synthesis_ICC2_LAB_TASk/LAB_TASK/starrc

2. **post_sta Folder location :**

   /home/userdata/21mvd0086/Simple_Processor_Working/Physical_Synthesis_ICC2_LAB_TASk/LAB_TASK/post_sta

3. **pv Folder location :**

   /home/userdata/21mvd0086/Simple_Processor_Working/Physical_Synthesis_ICC2_LAB_TASk/LAB_TASK/pv

4. **Report folder :**

   /home/userdata/21mvd0086/Simple_Processor_Working/Physical_Synthesis_ICC2_LAB_TASk/LAB_TASK/Reports