Winter Semester 2021-2022

ECE6024 – VLSI VERIFICATION METHODOLOGIES

M.Tech VLSI Design

School of Electronics Engineering

Vellore Institute of Technology

VERIFICATION OF SIMPLE PROCESSOR

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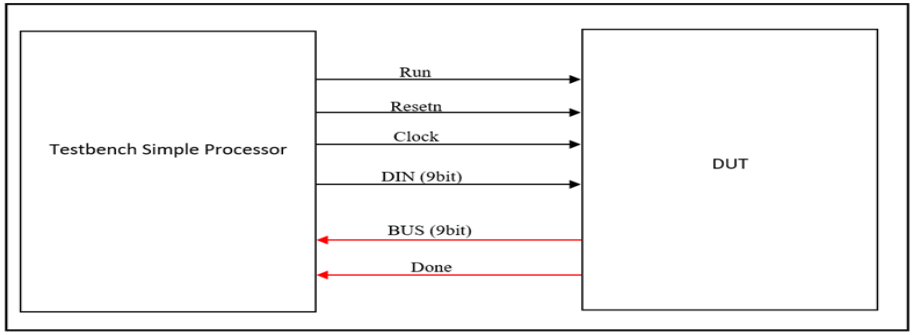
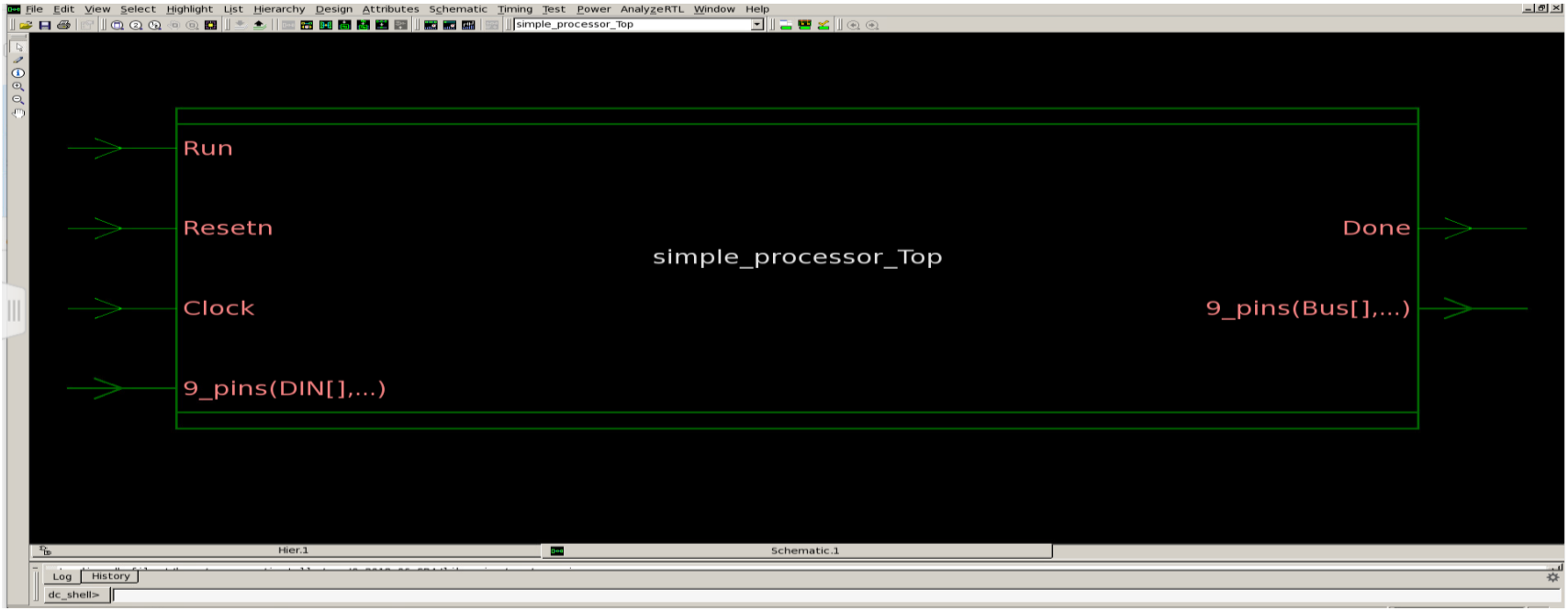
Shreyas S Bagi 21MVD0086

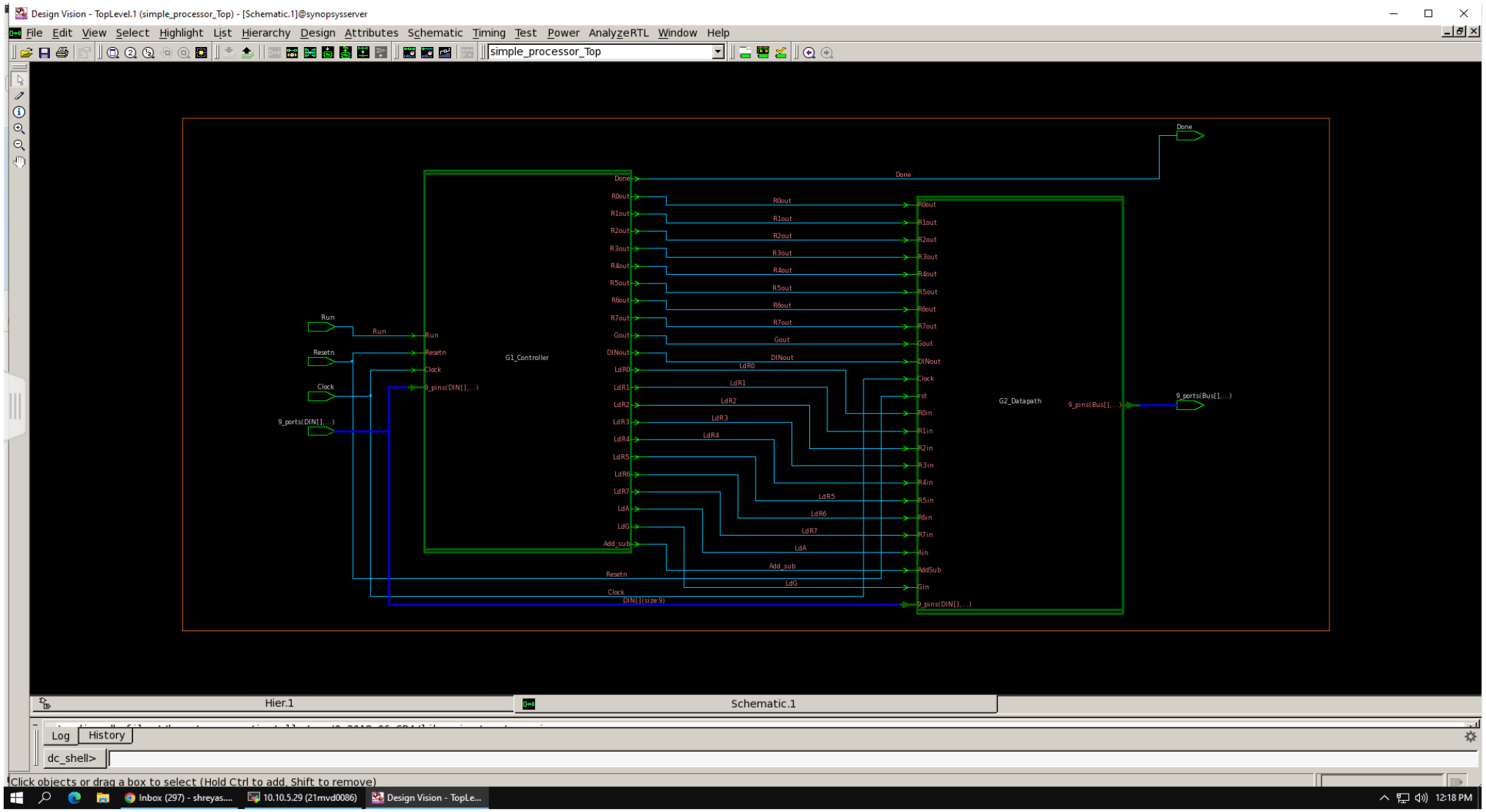
Srinidhi K S 21MVD0105

SIMPLE PROCESSOR ARCHITECTURE

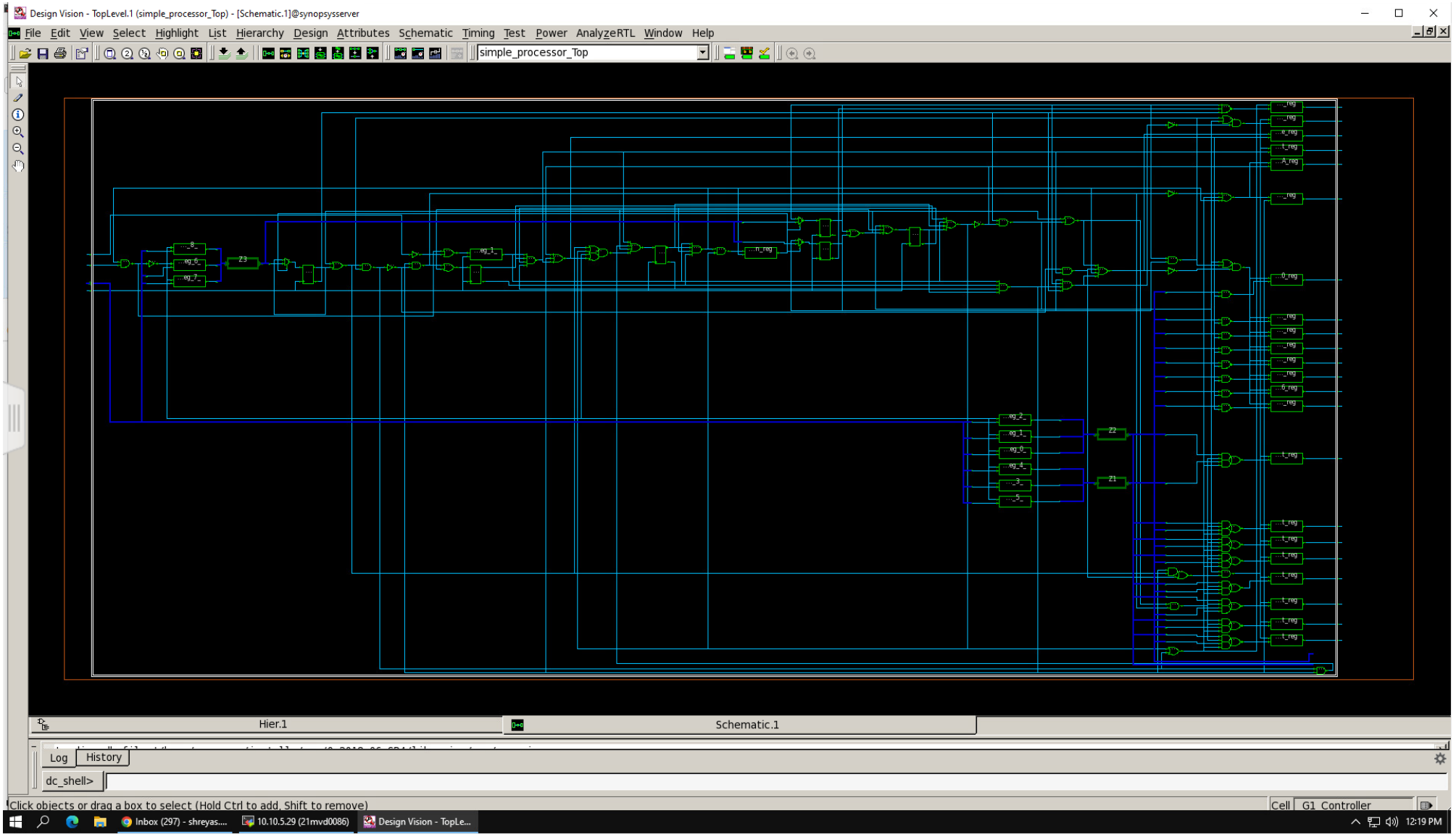
Top Module

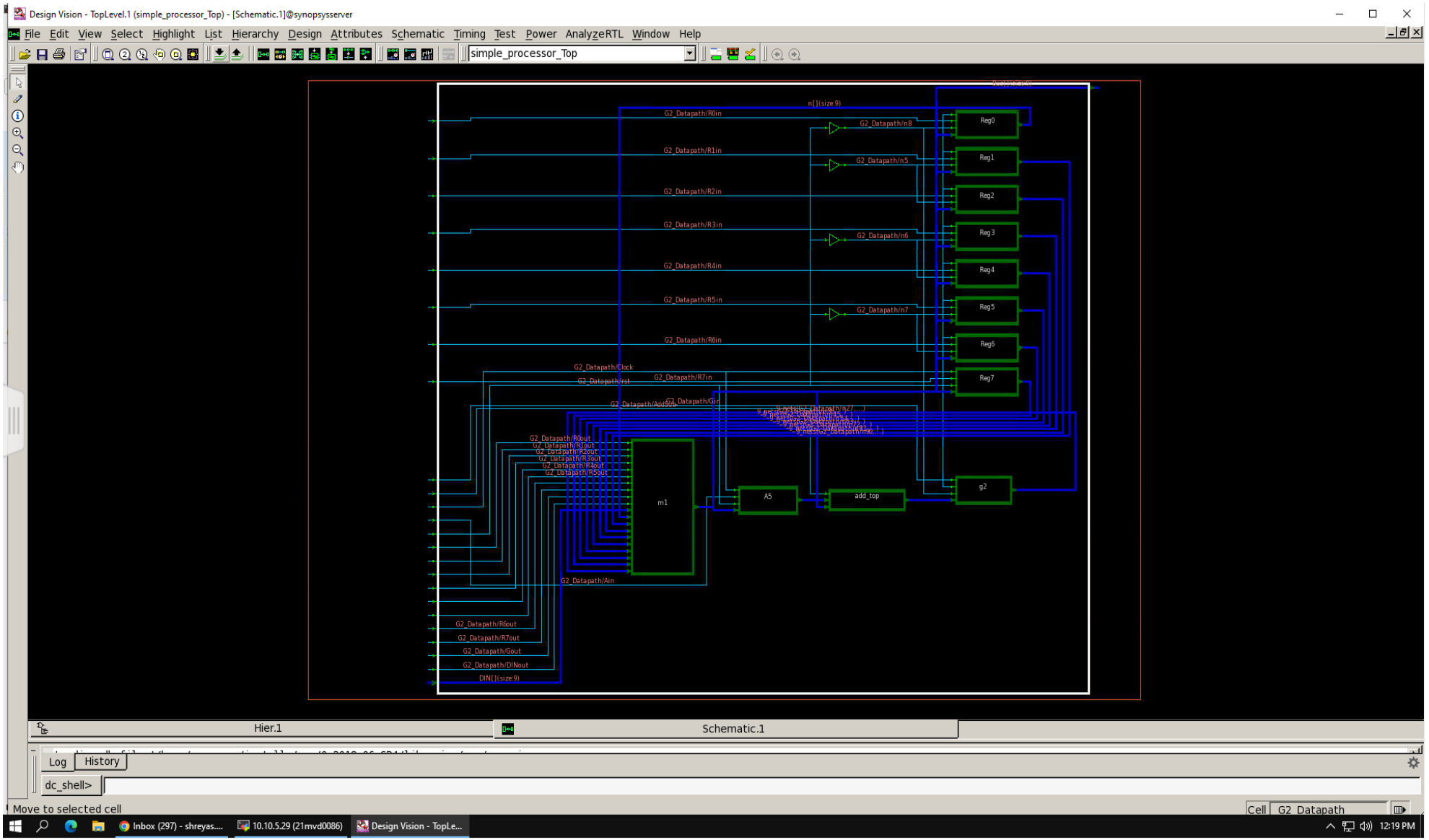




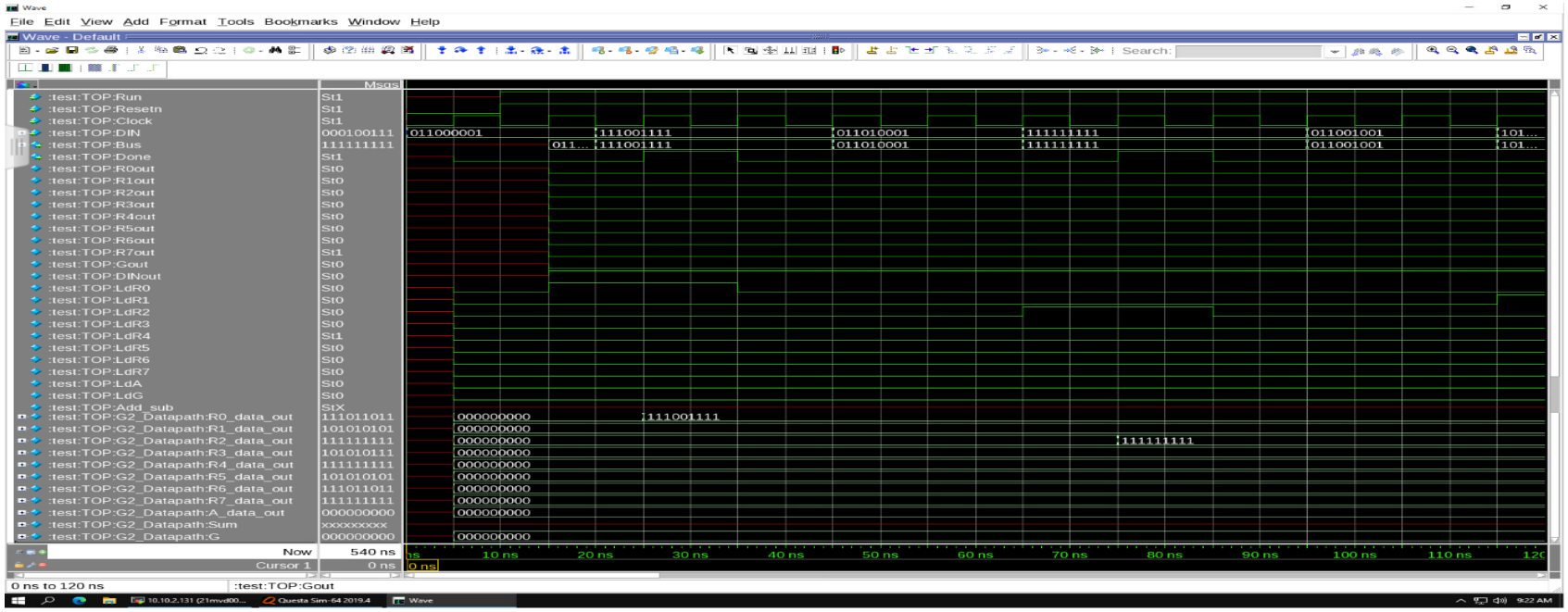


- The figures are the architecture screenshots of the simple processor executed in Synopsys VCS complier.

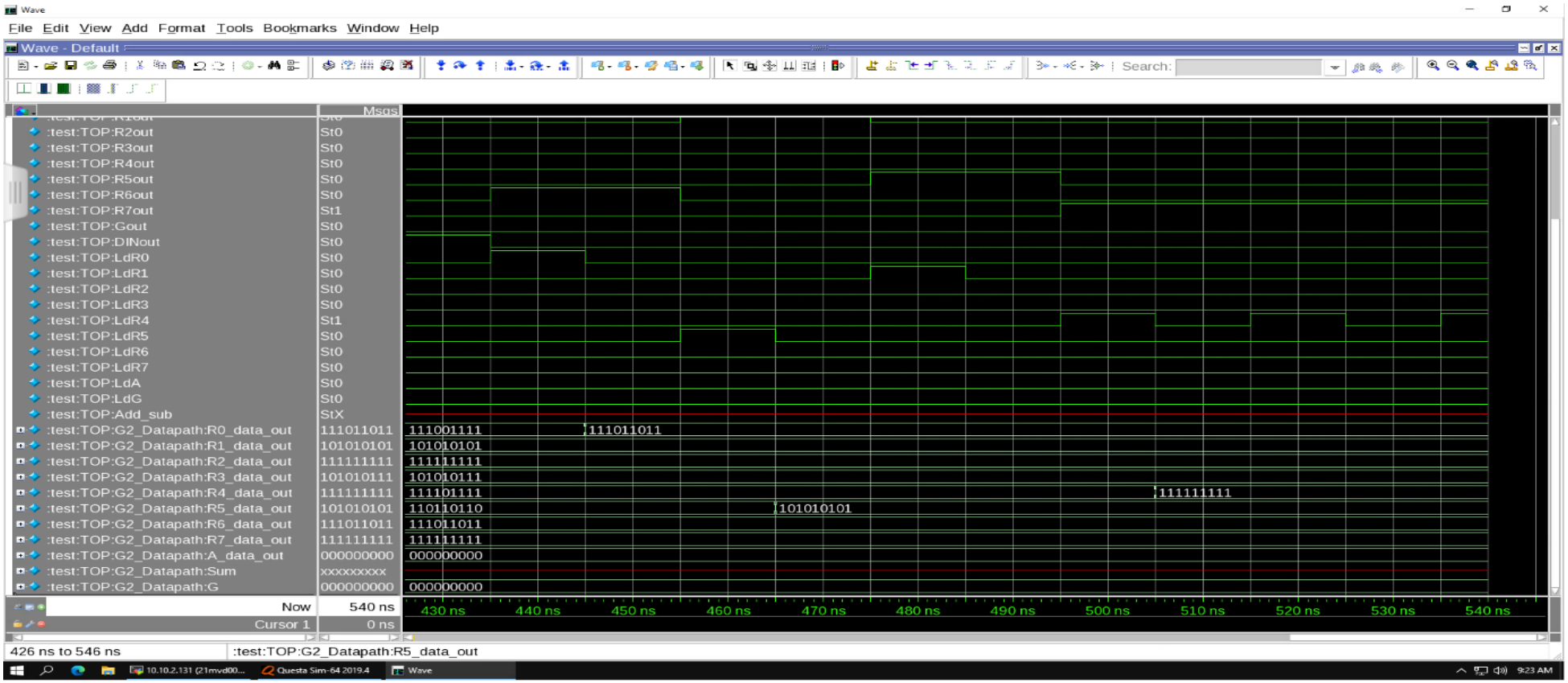

Design Vision - TopLevel.1 (simple_processor_Top) - [Schematic.1]@synopsysserver
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
simple_processor_Top
Z3
Z2
Z1
Hier.1
Schematic.1
Log History
dc_shell>
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
Cell G1_Controller
Inbox (297) - shreyas....
10.10.5.29 (21mvd0086)
Design Vision - TopLe...
12:19 PM


Design Vision - TopLevel.1 (simple_processor_Top) - [Schematic.1]@synopsysserver
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window Help
simple_processor_Top
n[](size:9)
G2_Datapath/R0in
G2_Datapath/R1in
G2_Datapath/R2in
G2_Datapath/R3in
G2_Datapath/R4in
G2_Datapath/R5in
G2_Datapath/R6in
G2_Datapath/R7in
G2_Datapath/Clock
G2_Datapath/rst
G2_Datapath/Gin
G2_Datapath/n8
G2_Datapath/n5
G2_Datapath/n6
G2_Datapath/n7
Reg0
Reg1
Reg2
Reg3
Reg4
Reg5
Reg6
Reg7
m1
A5
add_top
g2
G2_Datapath/Ain
G2_Datapath/R6out
G2_Datapath/R7out
G2_Datapath/Gout
G2_Datapath/DINout
DIN[](size:9)
Hier.1
Schematic.1
Log
History
dc_shell>
Move to selected cell
Cell G2_Datapath
Inbox (297) - shreyas....
10.10.5.29 (21mvd0086)
Design Vision - TopLe...
12:19 PM

1. RESET:



Initially, after 8 clock cycles Move Immediate Operation results are obtained because, Register should be loaded with some Data for further Operations.


Wave
File Edit View Add Format Tools Bookmarks Window Help
Wave - Default
Search:
Msgs
:test:TOP:R2out St0
:test:TOP:R3out St0
:test:TOP:R4out St0
:test:TOP:R5out St0
:test:TOP:R6out St0
:test:TOP:R7out St1
:test:TOP:Gout St0
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:test:TOP:LdR3 St0
:test:TOP:LdR4 St1
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:test:TOP:LdR6 St0
:test:TOP:LdR7 St0
:test:TOP:LdA St0
:test:TOP:LdG St0
:test:TOP:Add_sub StX
:test:TOP:G2_Datapath:R0_data_out 111011011 111001111 111011011
:test:TOP:G2_Datapath:R1_data_out 101010101 101010101
:test:TOP:G2_Datapath:R2_data_out 111111111 111111111
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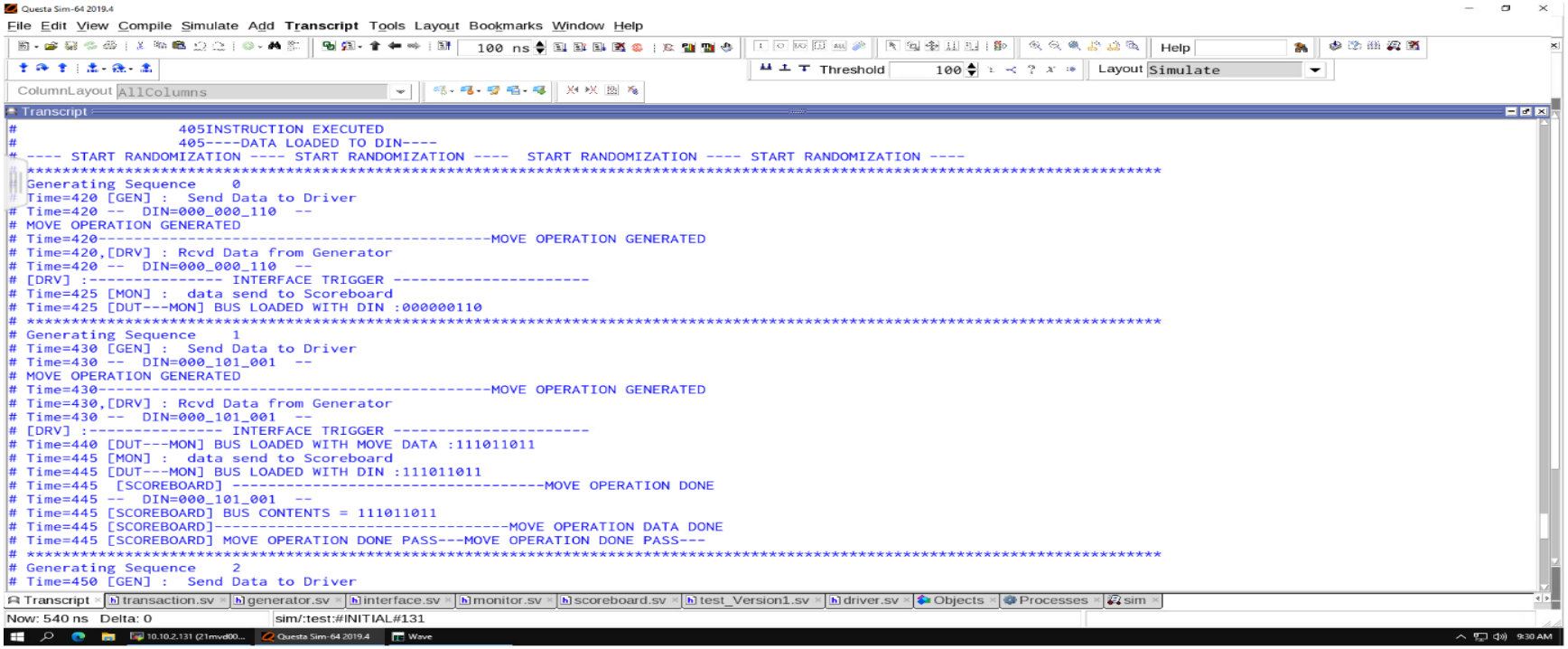
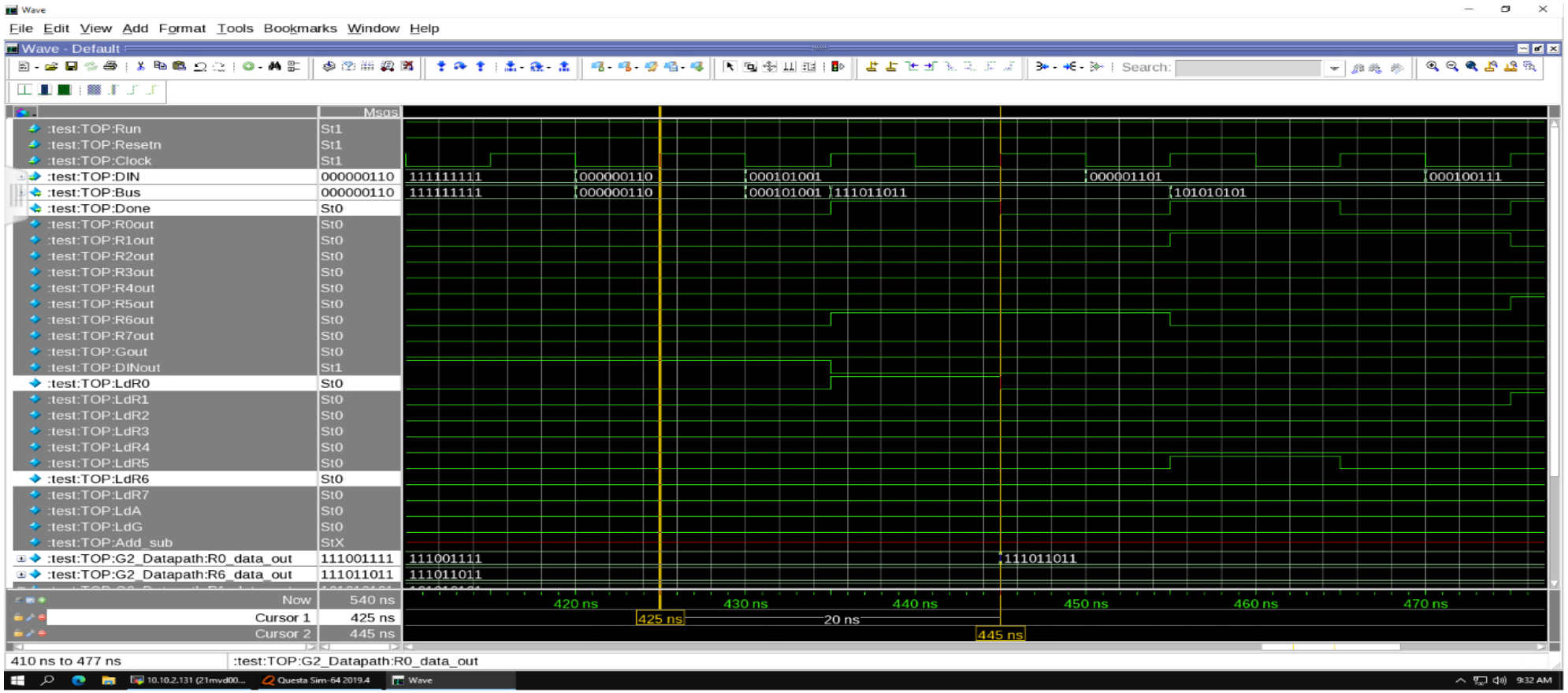
:test:TOP:G2_Datapath:R4_data_out 111111111 111101111 111111111
:test:TOP:G2_Datapath:R5_data_out 101010101 110110110 101010101
:test:TOP:G2_Datapath:R6_data_out 111011011 111011011
:test:TOP:G2_Datapath:R7_data_out 111111111 111111111
:test:TOP:G2_Datapath:A_data_out 000000000 000000000
:test:TOP:G2_Datapath:Sum xxxxxxxxx
:test:TOP:G2_Datapath:G 000000000 000000000
Now 540 ns
Cursor 1 0 ns
430 ns 440 ns 450 ns 460 ns 470 ns 480 ns 490 ns 500 ns 510 ns 520 ns 530 ns 540 ns
426 ns to 546 ns
:test:TOP:G2_Datapath:R5_data_out
Questa Sim-64 2019.4
Wave
9:23 AM

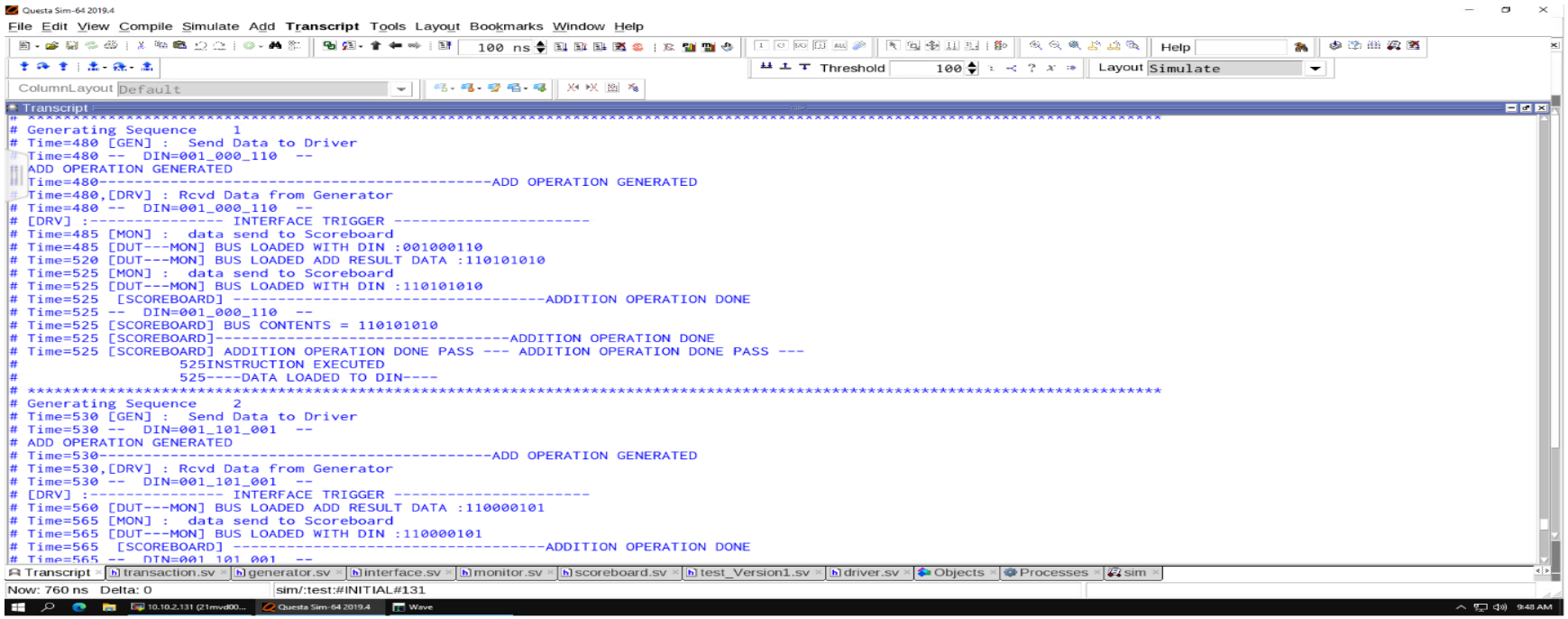
2. MOVE OPERATION:



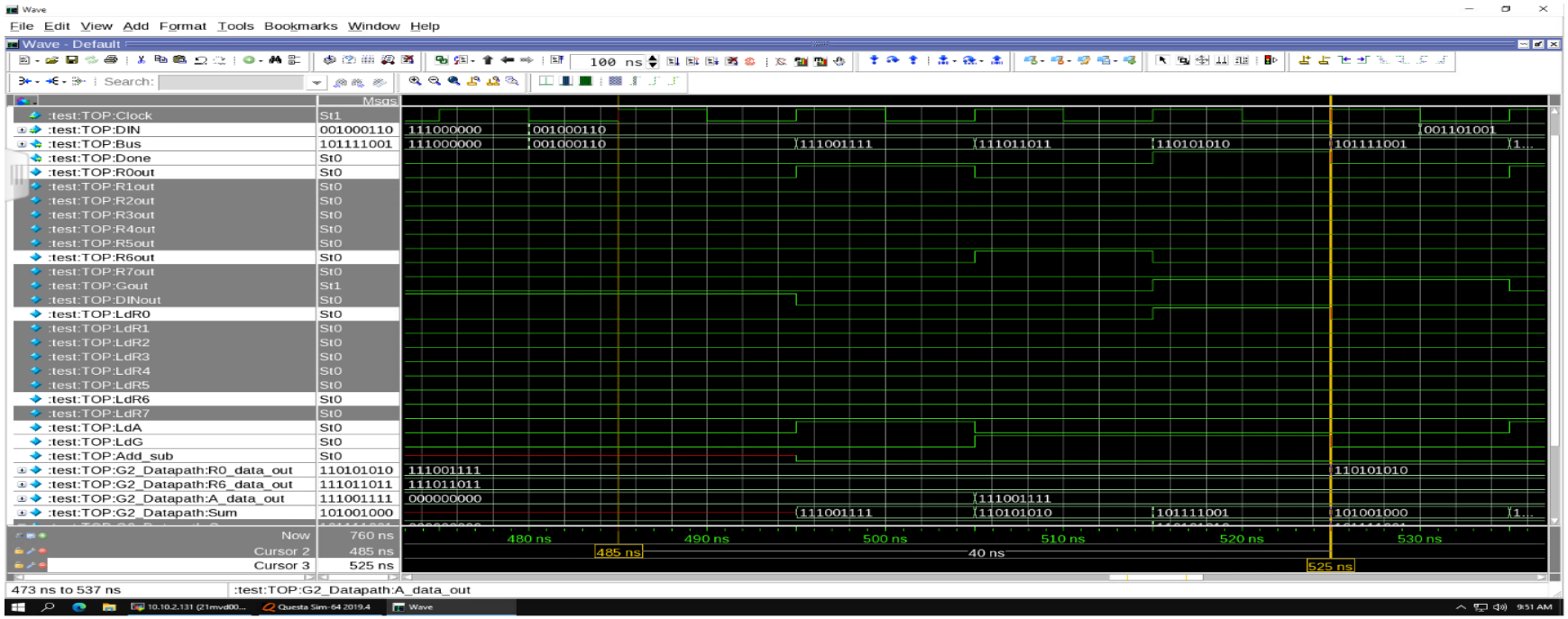


The above figure depicts Move operation. We have done the Move immediate operation for Register R0 and R5 already. At time instant from t=425ns to 445ns we observe that. The Move operation takes two states (two clock pulses) to complete the operation. We observe the data stored in Register R6 (111011011) is copied to Register R0 (111011011).

3. ADD OPERATION:



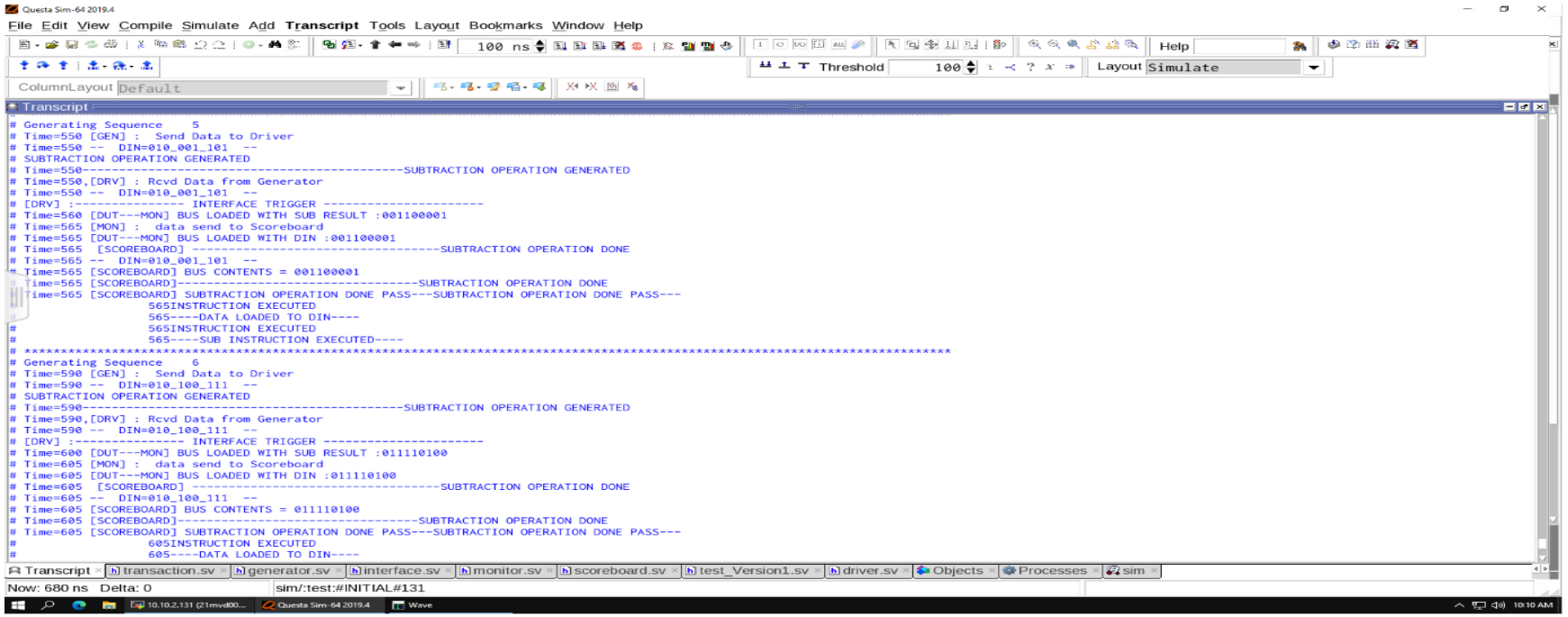
- Add operation is done as **add R0, R6**



In this figure we observe that the data 111001111 loaded to register R0. After 40ns (4 cycles) we observe that R0 is loaded with the data. We are doing Move immediate operation for Register R0. In the figure we observe that the data 111011011 loaded to register R6. We are doing Move immediate operation for Register R6. We observe that the R0 data value is copied to Register A. The control signal LdA is generated high and goes low after that, the addition takes place with bus loaded with R6 data. In next clock pulse we observe that the LdG signal became high and addition result is stored to Register G. Finally, we observe that sum result stored Register G is stored back to register R0.

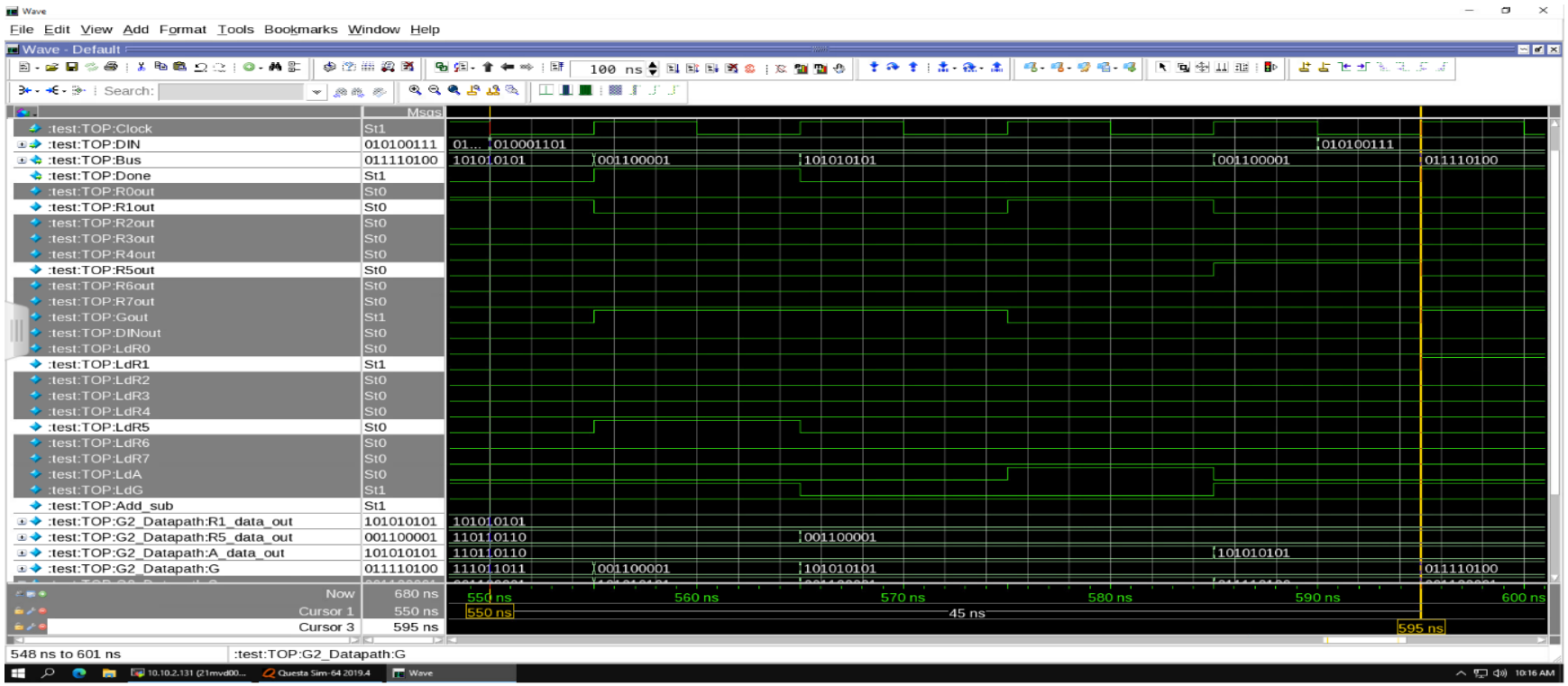
The result can be seen at t=525ns, 10101010 is the addition result (it's taking 9bit value).

4. Subtraction Operation



- Subtration operation is done as **sub R1, R5**

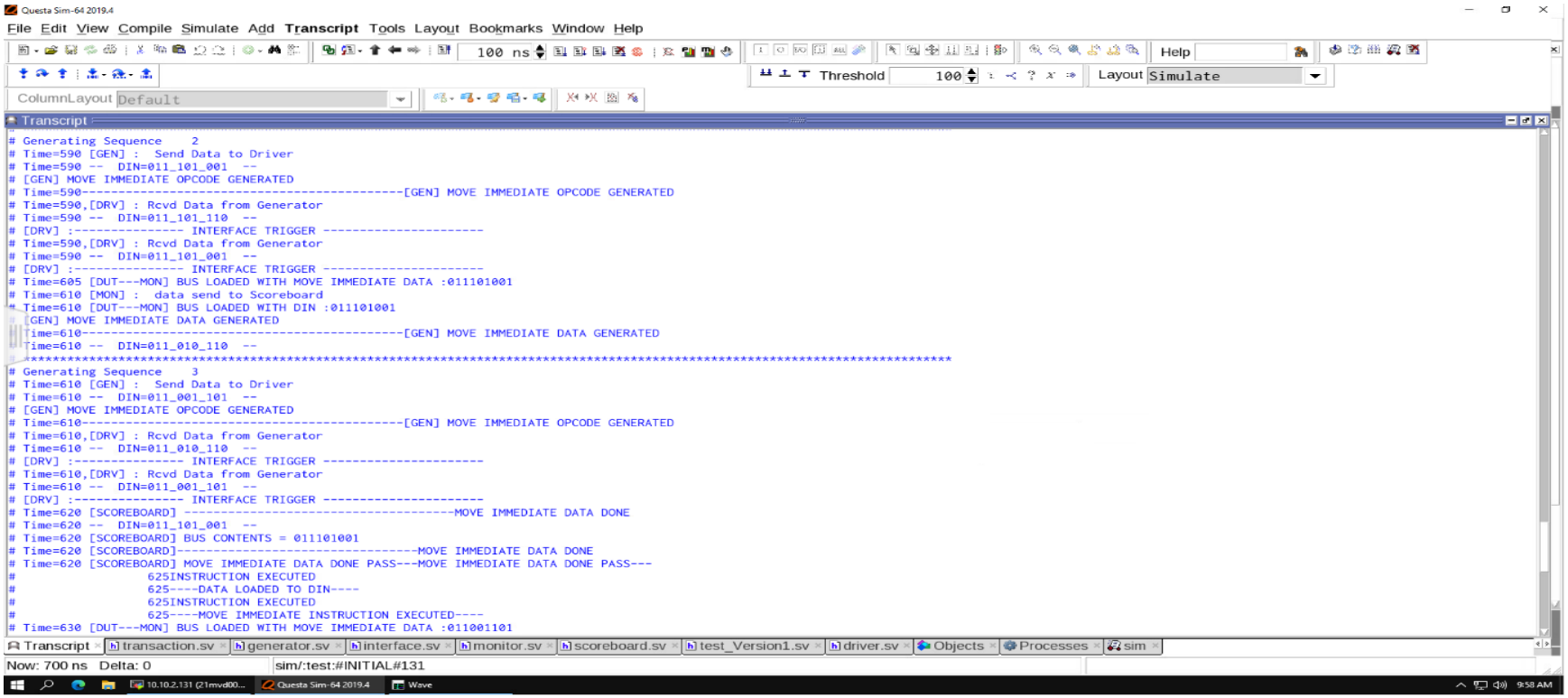
  R1 = R1 -R5

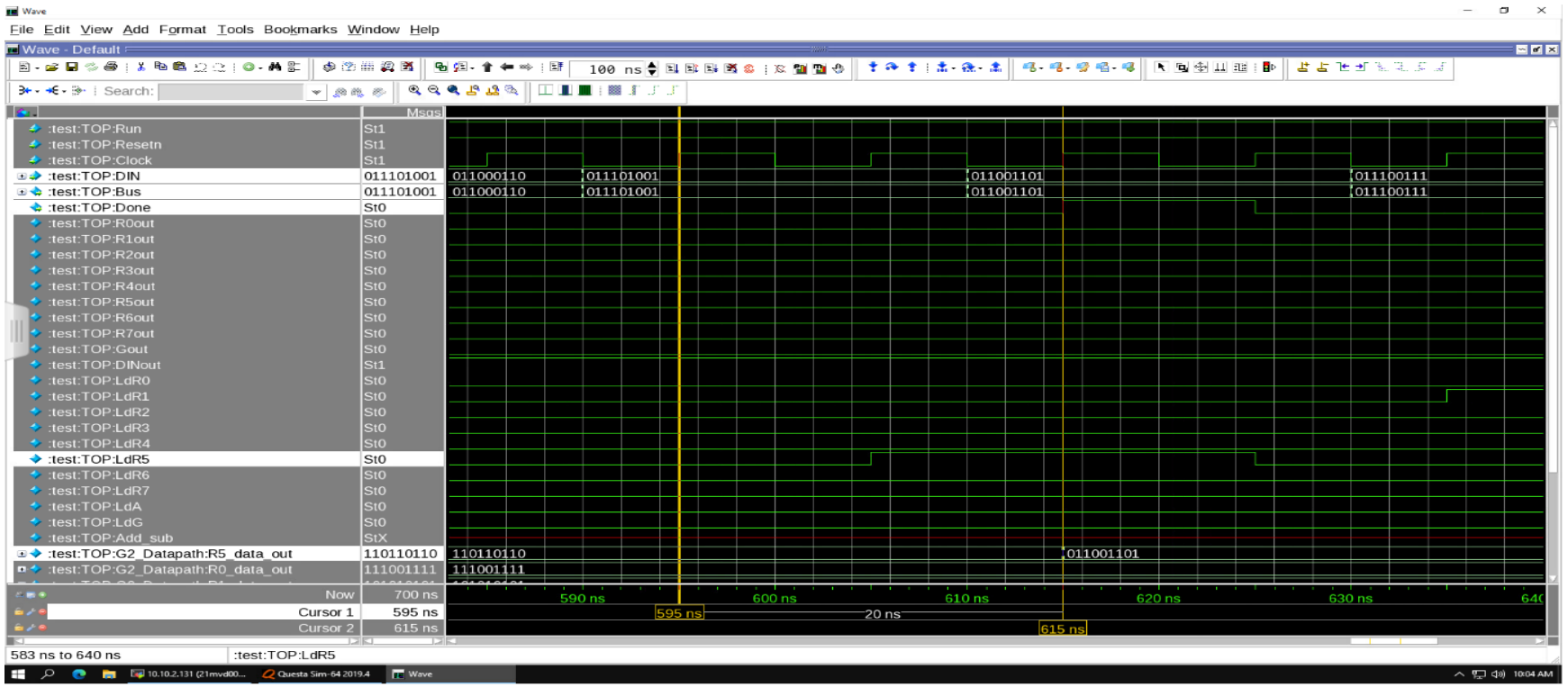


In this figure we observe that the data 101010101 loaded to register R1. After 40ns (4 cycles) we observe that R1 is loaded with the data. We are doing Move immediate operation for Register R1. In the figure we observe that the data 001100001 loaded to register R5. We are doing Move immediate operation for Register R5. We observe that the R1 data value is copied to Register A. The control signal LdA is generated high and goes low after that, the addition takes place with bus loaded with R5 data. In next clock pulse we observe that the LdG signal became high and addition result is stored to Register G. Finally, we observe that sum result stored Register G is stored back to register R1.

The result can be seen at t=595ns, 011110100 is the addition result (it's taking 9bit value).

5. Move Immediate Operation

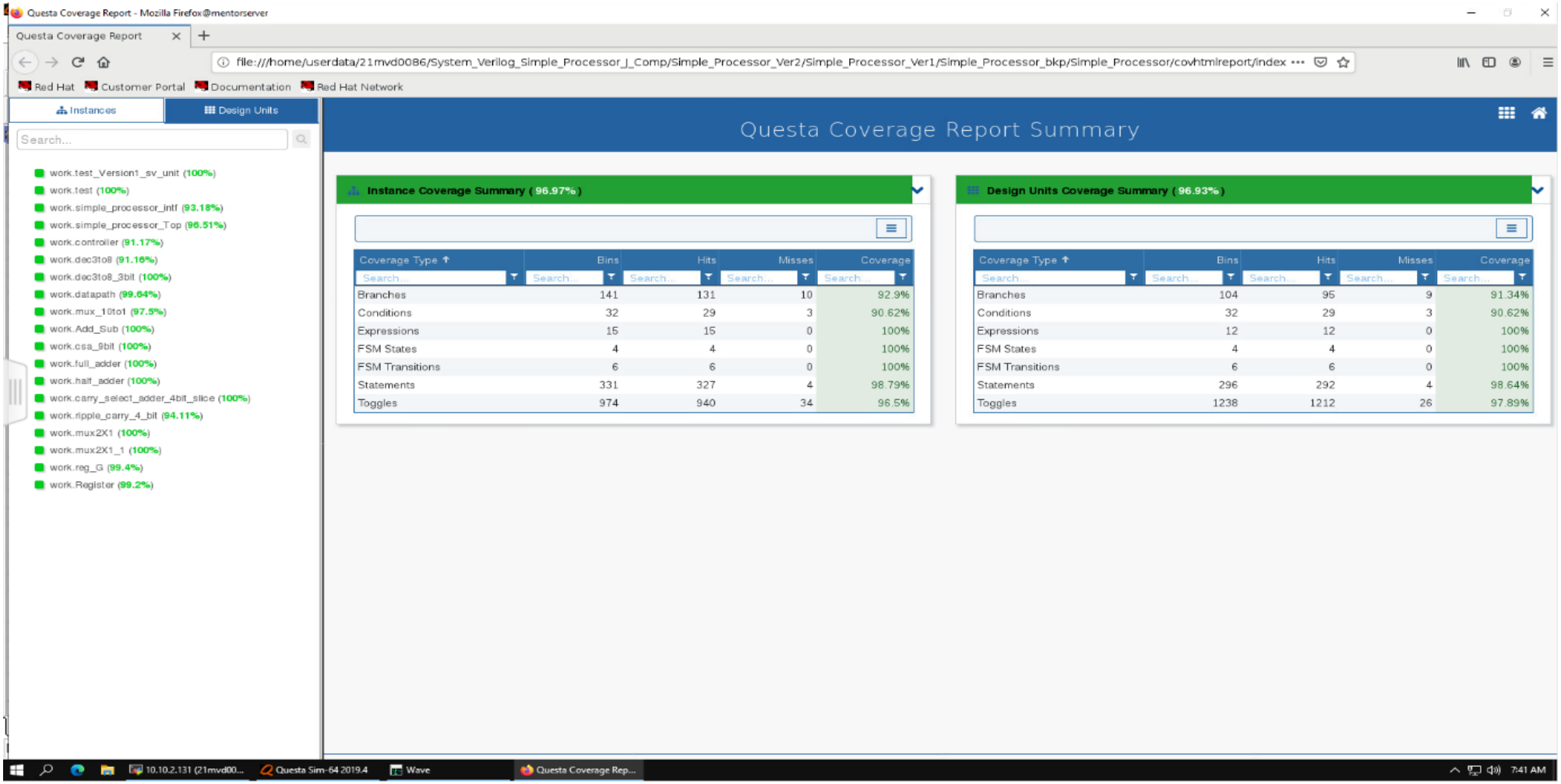




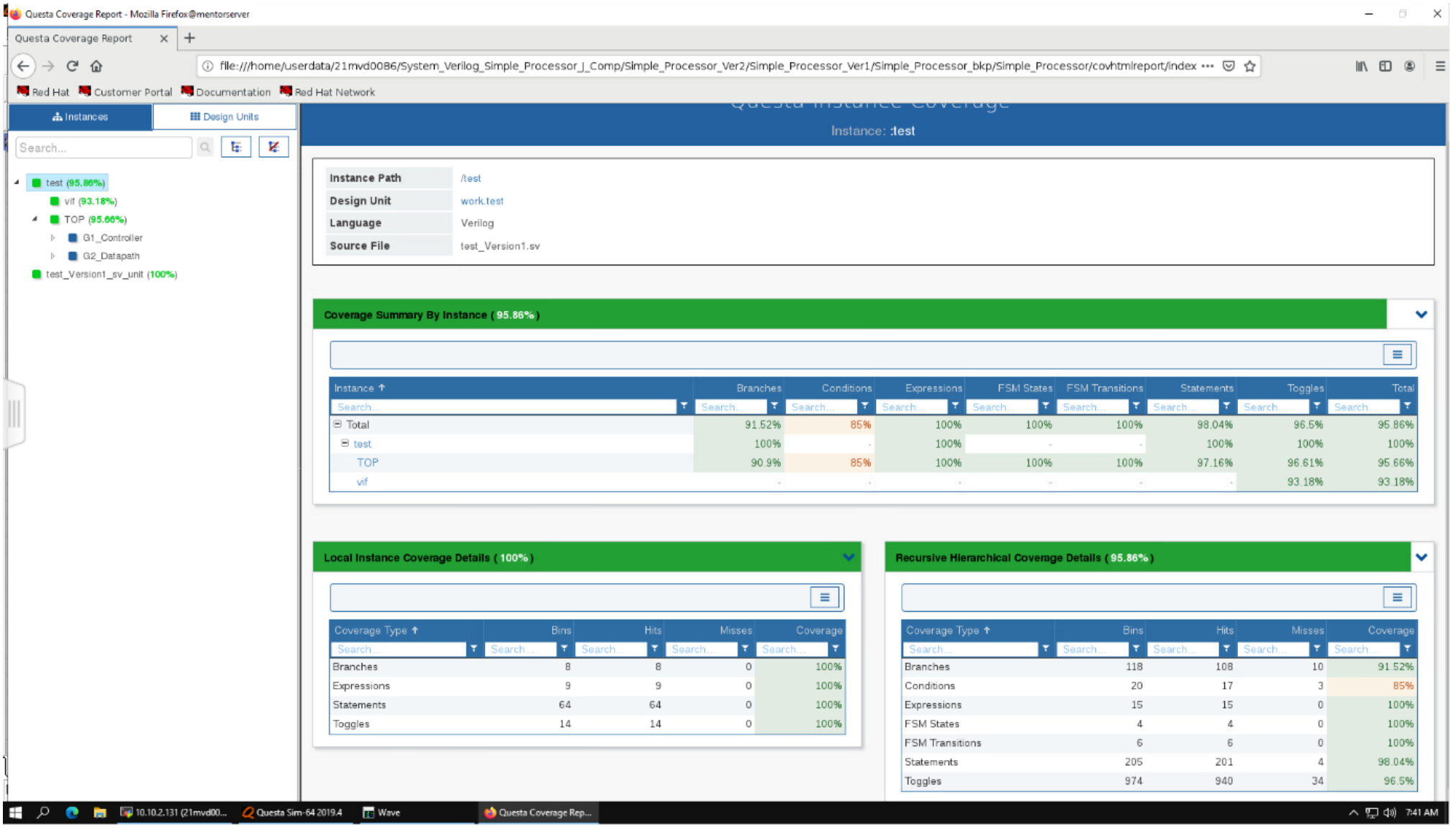
In the above figure we are performing move immediate operation. In this figure we observe that the data 011001101 loaded to register R5. After 20ns (2 cycles) we observe that R5 is loaded with the data. We are doing Move immediate operation for Register R5. In the figure we observe that the data 011001101 loaded to register R5. The control signal LdR5 is generated high and goes low after that, the move immediate takes place with bus loaded with R5 data. In next clock pulse we observe that the data back to register R5.

The result can be seen at t=615ns, 011001101 is the move immediate result.

QUESTA COVERAGE REPORT



- Design units coverage summary = 96.93%


Questa Coverage Report - Mozilla Firefox@mentorserver
Questa Coverage Report
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Red Hat
Customer Portal
Documentation
Red Hat Network
Instances
Design Units
Search...
test (95.86%)
vif (93.18%)
TOP (95.66%)
G1_Controller
G2_Datapath
test_Version1_sv_unit (100%)
Instance: :test
Instance Path /test
Design Unit work.test
Language Verilog
Source File test_Version1.sv
Coverage Summary By Instance (95.86%)
Instance ↑ Branches Conditions Expressions FSM States FSM Transitions Statements Toggles Total
Total 91.52% 85% 100% 100% 100% 98.04% 96.5% 95.86%
test 100% - 100% - - 100% 100% 100%
TOP 90.9% 85% 100% 100% 100% 97.16% 96.61% 95.66%
vif - - - - - - 93.18% 93.18%
Local Instance Coverage Details (100%)
Coverage Type ↑ Bins Hits Misses Coverage
Branches 8 8 0 100%
Expressions 9 9 0 100%
Statements 64 64 0 100%
Toggles 14 14 0 100%
Recursive Hierarchical Coverage Details (95.86%)
Coverage Type ↑ Bins Hits Misses Coverage
Branches 118 108 10 91.52%
Conditions 20 17 3 85%
Expressions 15 15 0 100%
FSM States 4 4 0 100%
FSM Transitions 6 6 0 100%
Statements 205 201 4 98.04%
Toggles 974 940 34 96.5%
10.10.2.131 (21mvd00...
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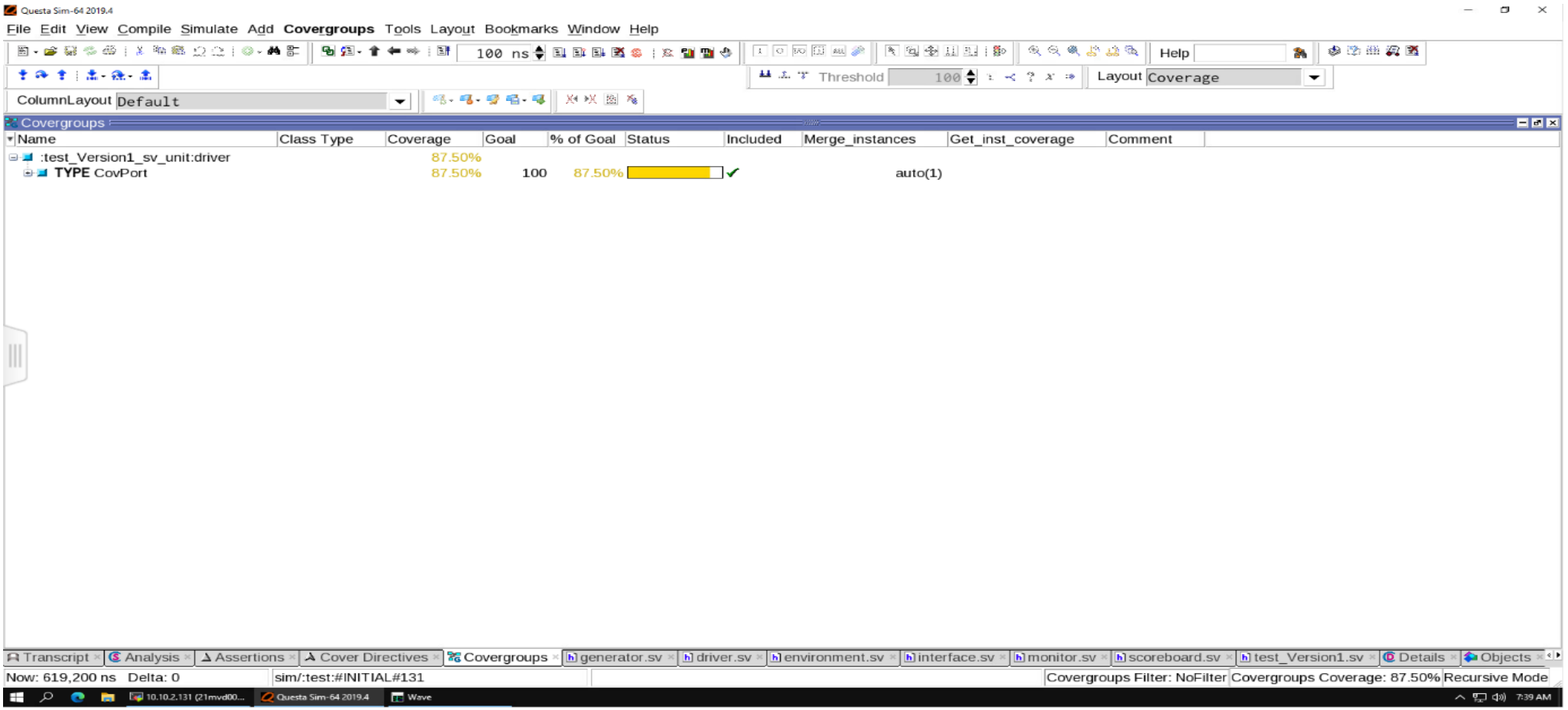
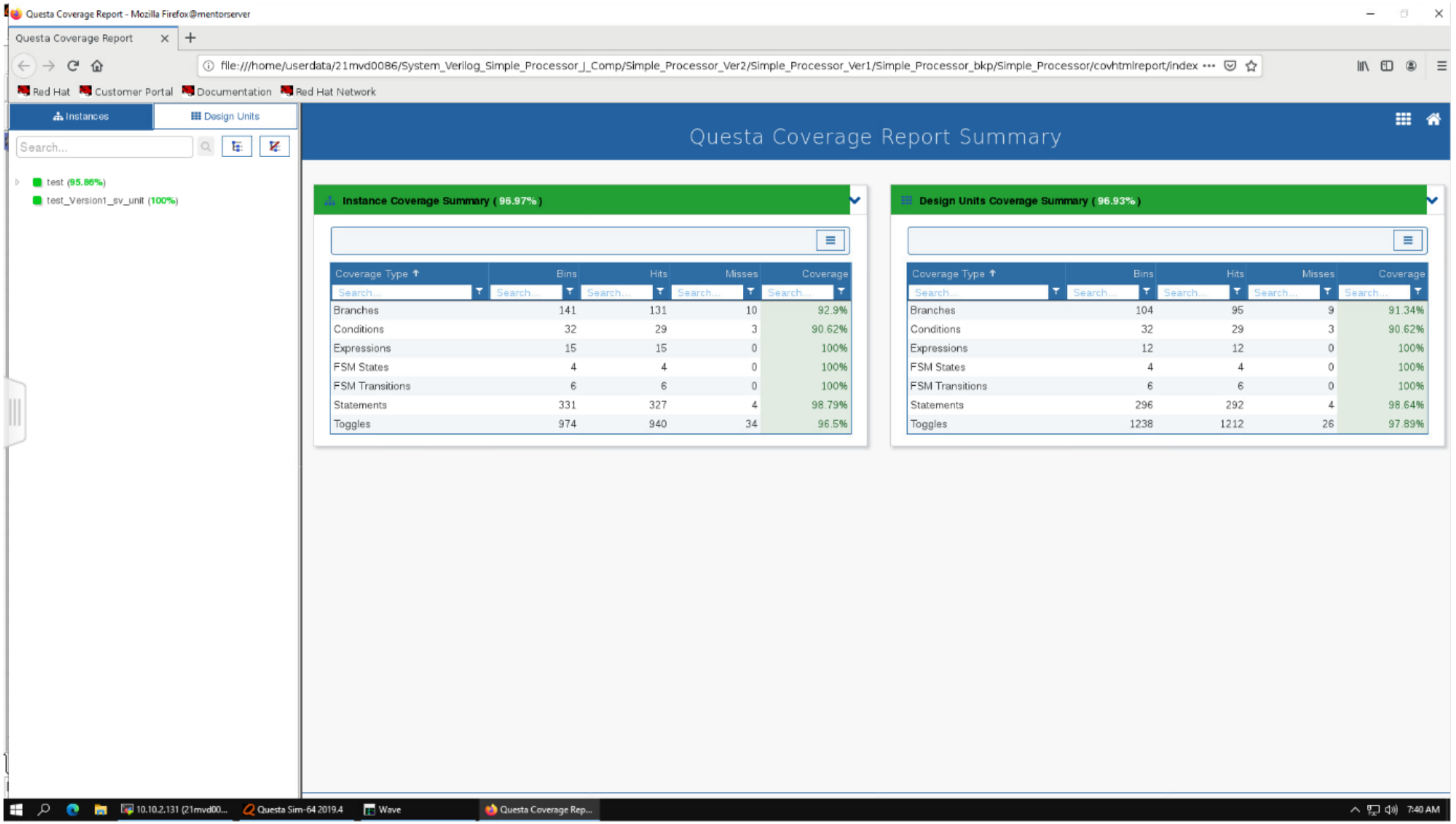
7:41 AM

COVER GROUPS




Questa Coverage Report - Mozilla Firefox@mentorserver
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Red Hat
Customer Portal
Documentation
Red Hat Network
Instances
Design Units
Search...
test (95.86%)
test_Version1_sv_unit (100%)
Questa Coverage Report Summary
Instance Coverage Summary (96.97%)
Coverage Type
Bins
Hits
Misses
Coverage
Branches 141 131 10 92.9%
Conditions 32 29 3 90.62%
Expressions 15 15 0 100%
FSM States 4 4 0 100%
FSM Transitions 6 6 0 100%
Statements 331 327 4 98.79%
Toggles 974 940 34 96.5%
Design Units Coverage Summary (96.93%)
Coverage Type
Bins
Hits
Misses
Coverage
Branches 104 95 9 91.34%
Conditions 32 29 3 90.62%
Expressions 12 12 0 100%
FSM States 4 4 0 100%
FSM Transitions 6 6 0 100%
Statements 296 292 4 98.64%
Toggles 1238 1212 26 97.89%
10.10.2.131 (21mvd00...
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Wave
Questa Coverage Rep...
7:40 AM