



Winter Semester 2021-2022

ECE6024 – VLSI VERIFICATION METHODOLOGIES

M.Tech VLSI Design

School of Electronics Engineering

Vellore Institute of Technology

VERIFICATION OF SIMPLE PROCESSOR

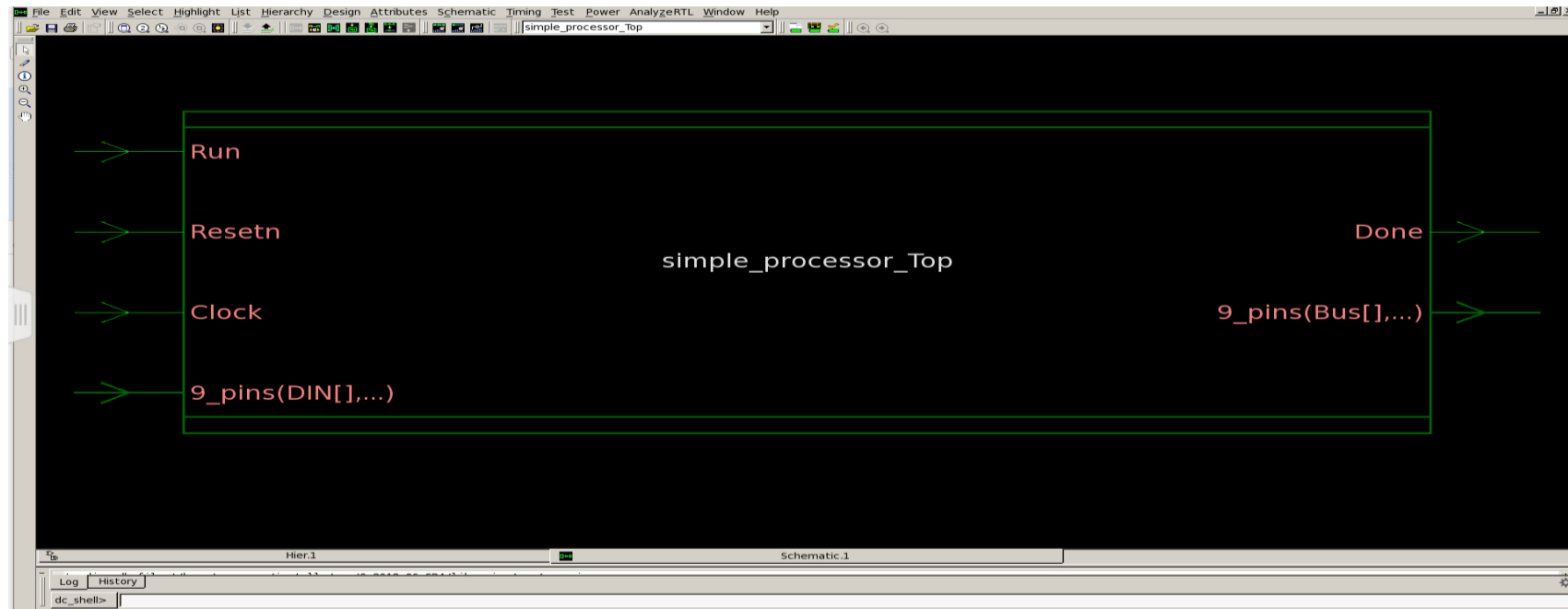
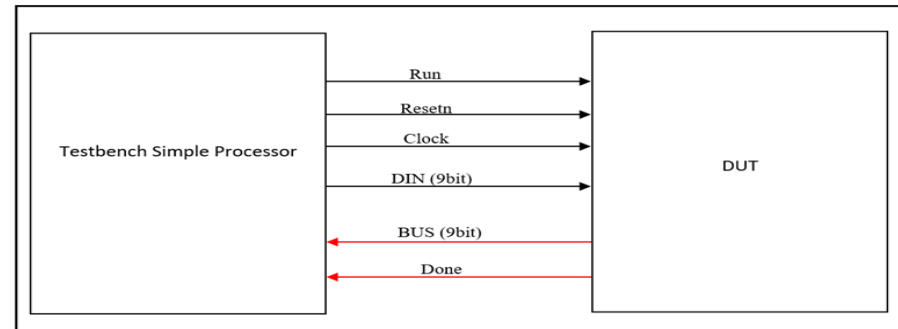
Panchagnula Krishna Vamsidhar 21MVD0085

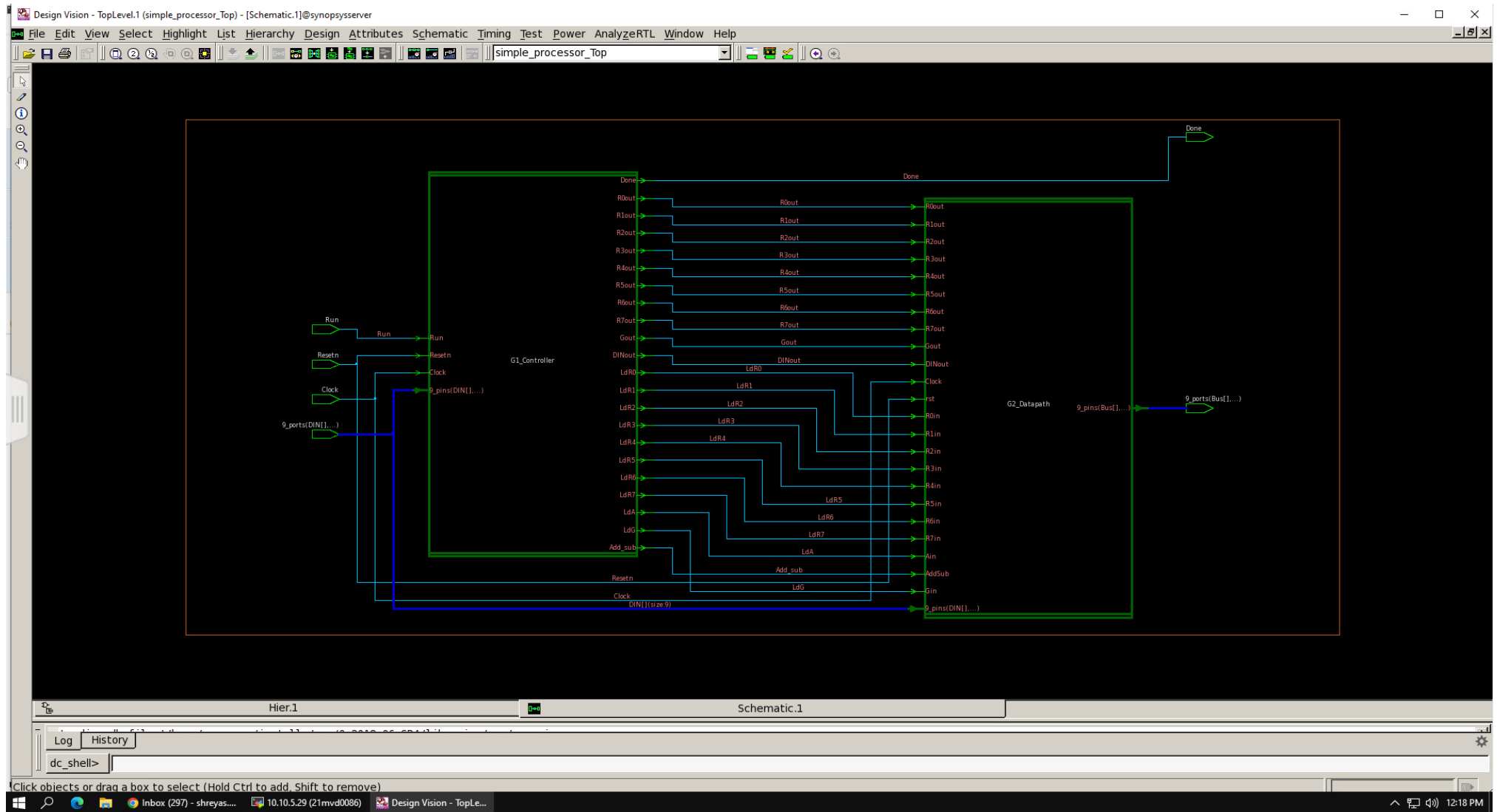
Shreyas S Bagi 21MVD0086

Srinidhi K S 21MVD0105

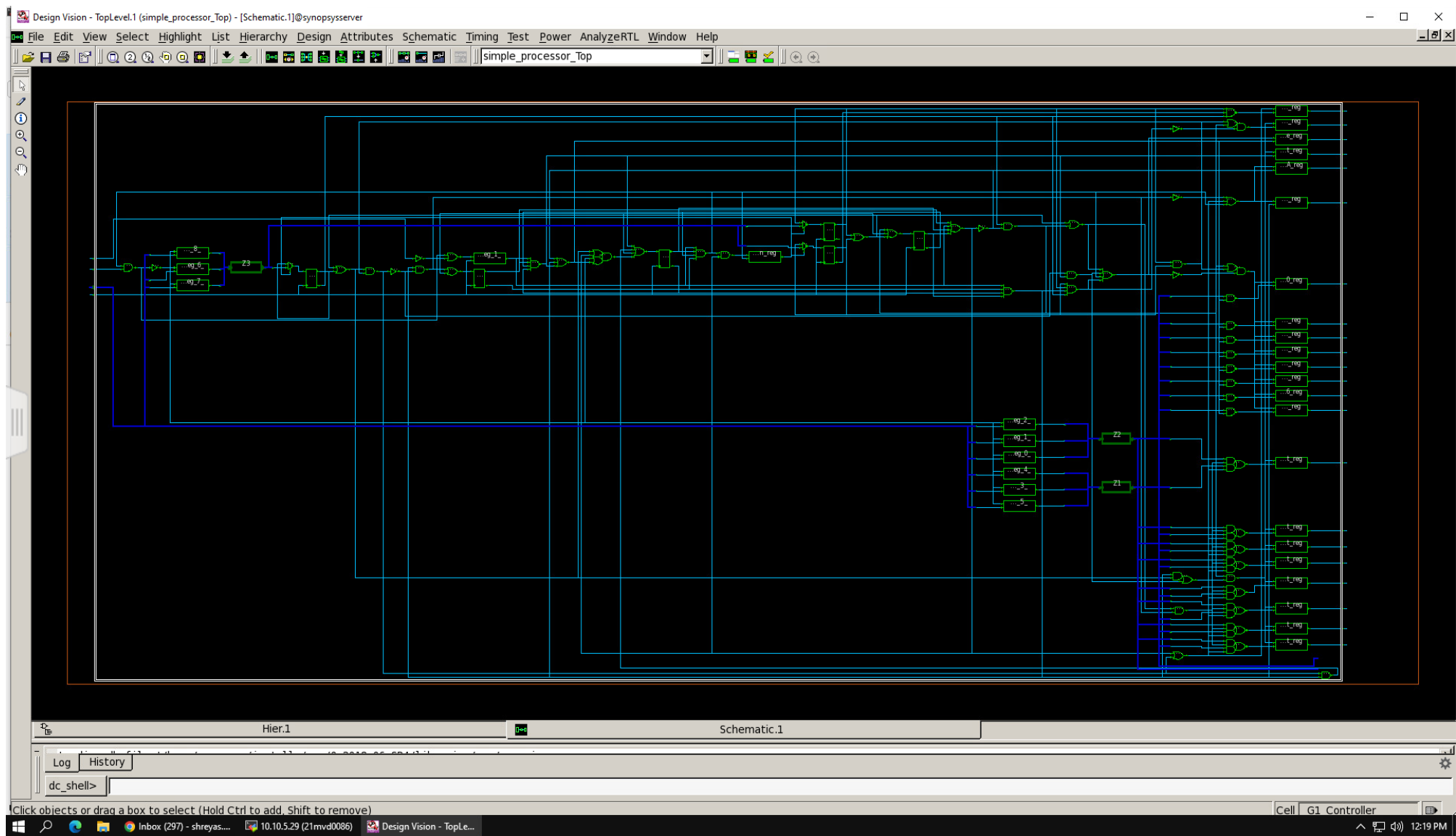
SIMPLE PROCESSOR ARCHITECTURE

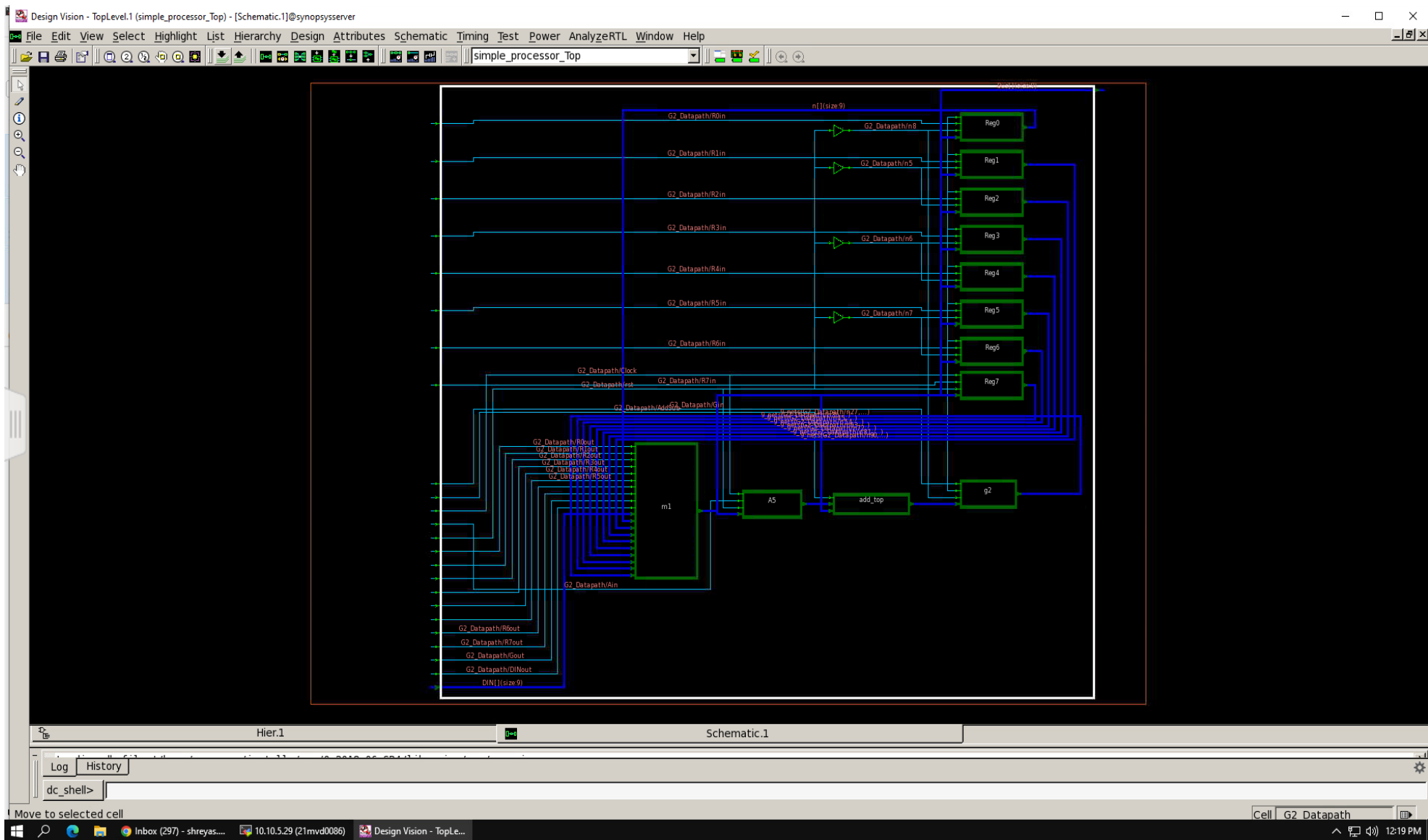
Top Module



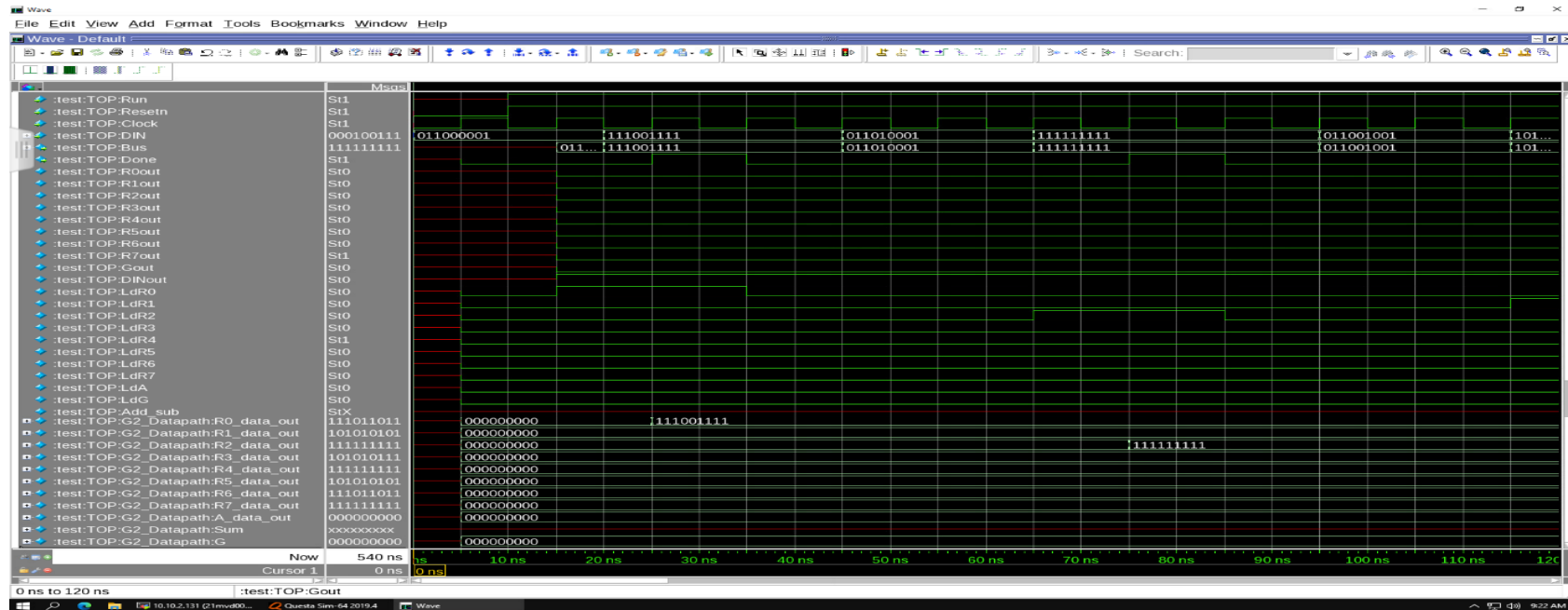


➤ The figures are the architecture screenshots of the simple processor executed in Synopsys VCS compiler.

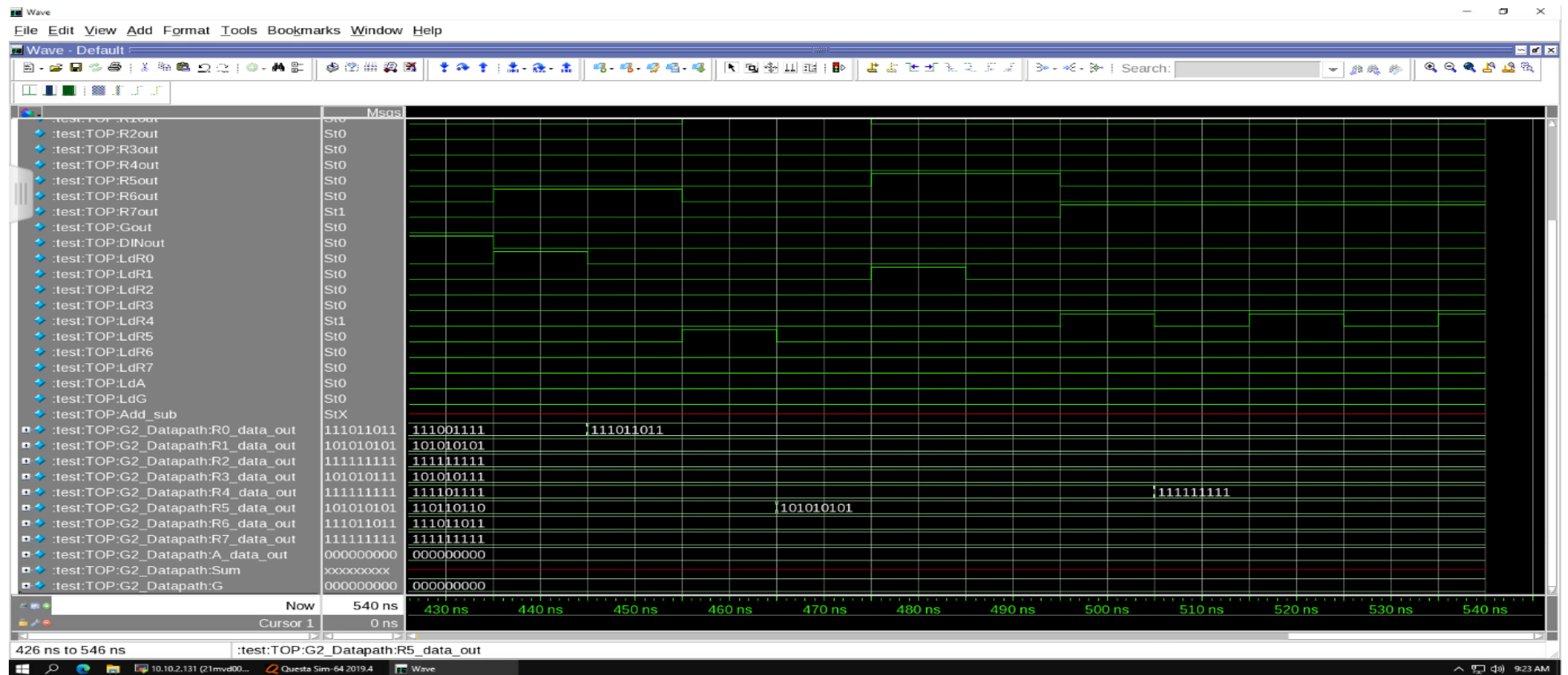




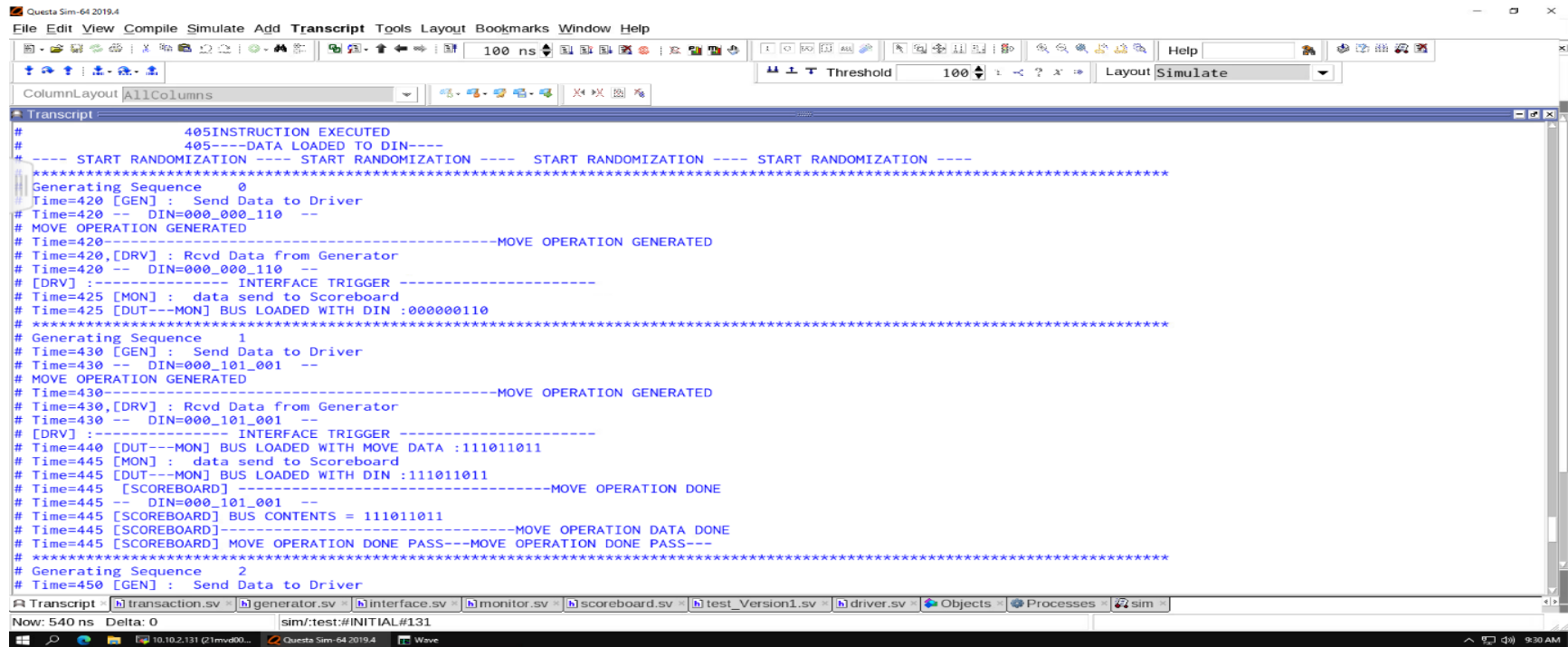
1. RESET:



Initially, after 8 clock cycles Move Immediate Operation results are obtained because, Register should be loaded with some Data for further Operations.



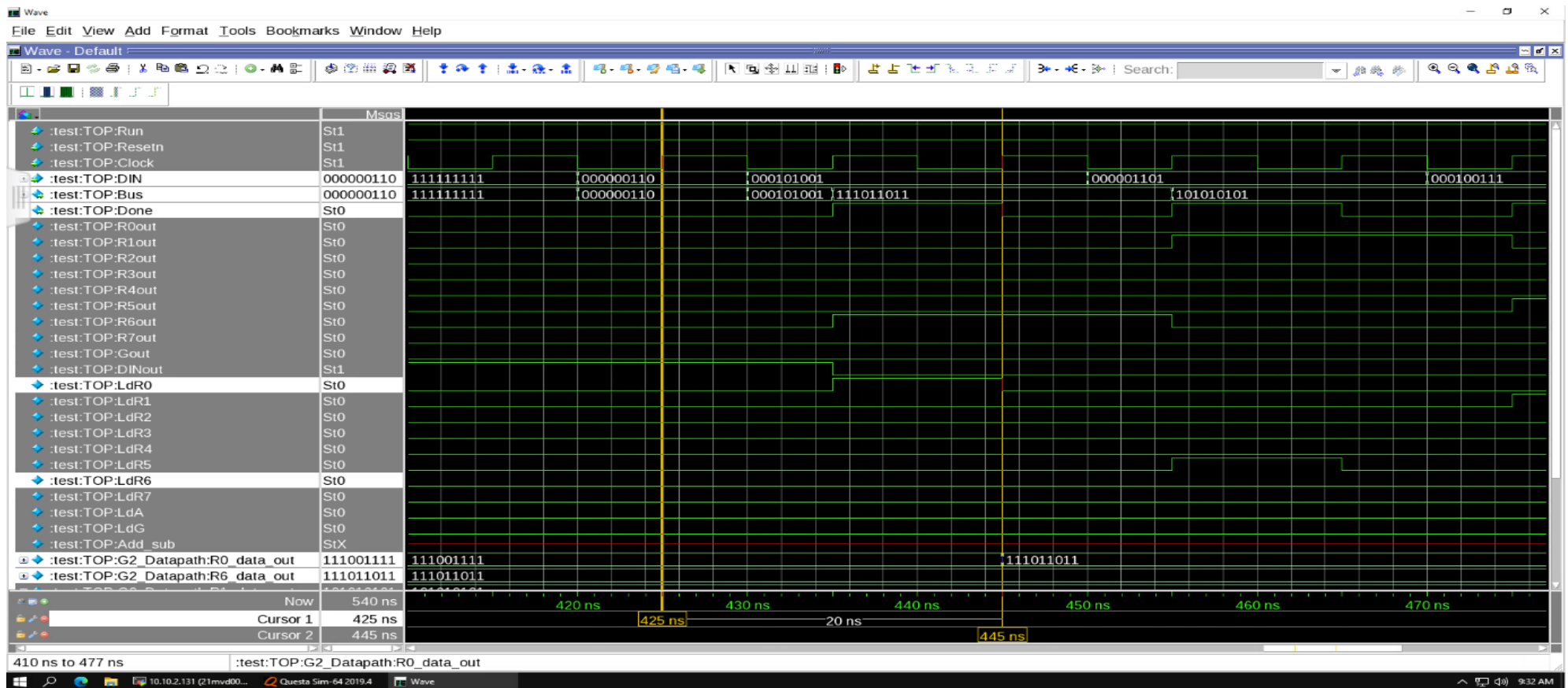
2. MOVE OPERATION:



The screenshot displays the Questa Sim-64 2019.4 software interface. The main window is titled 'Transcript' and shows the following simulation log:

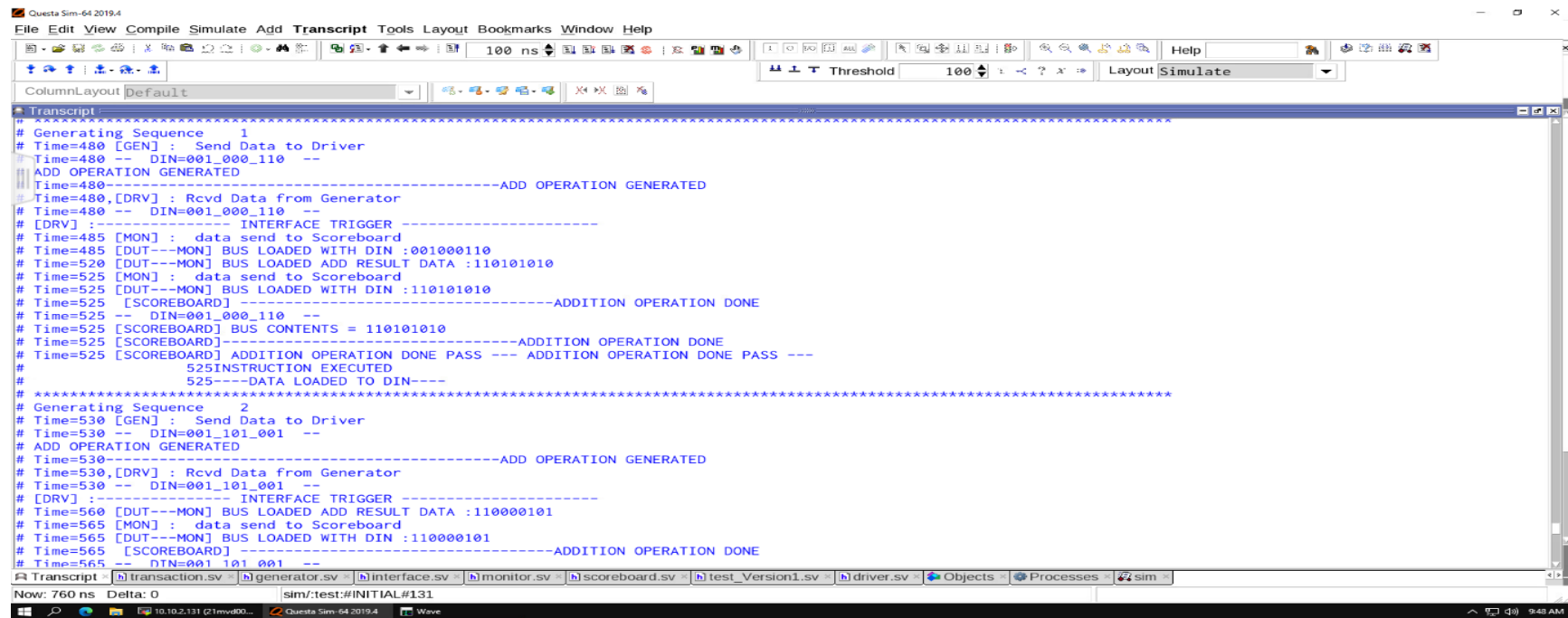
```
# 405INSTRUCTION EXECUTED
# 405----DATA LOADED TO DIN----
# ---- START RANDOMIZATION ---- START RANDOMIZATION ---- START RANDOMIZATION ---- START RANDOMIZATION ----
*****
# Generating Sequence 0
# Time=420 [GEN] : Send Data to Driver
# Time=420 -- DIN=000_000_110 --
# MOVE OPERATION GENERATED
# Time=420-----MOVE OPERATION GENERATED
# Time=420,[DRV] : Rcvd Data from Generator
# Time=420 -- DIN=000_000_110 --
# [DRV] :----- INTERFACE TRIGGER -----
# Time=425 [MON] : data send to Scoreboard
# Time=425 [DUT---MON] BUS LOADED WITH DIN :000000110
# *****
# Generating Sequence 1
# Time=430 [GEN] : Send Data to Driver
# Time=430 -- DIN=000_101_001 --
# MOVE OPERATION GENERATED
# Time=430-----MOVE OPERATION GENERATED
# Time=430,[DRV] : Rcvd Data from Generator
# Time=430 -- DIN=000_101_001 --
# [DRV] :----- INTERFACE TRIGGER -----
# Time=440 [DUT---MON] BUS LOADED WITH MOVE DATA :111011011
# Time=445 [MON] : data send to Scoreboard
# Time=445 [DUT---MON] BUS LOADED WITH DIN :111011011
# Time=445 [SCOREBOARD] -----MOVE OPERATION DONE
# Time=445 -- DIN=000_101_001 --
# Time=445 [SCOREBOARD] BUS CONTENTS = 111011011
# Time=445 [SCOREBOARD]-----MOVE OPERATION DATA DONE
# Time=445 [SCOREBOARD] MOVE OPERATION DONE PASS---MOVE OPERATION DONE PASS---
# *****
# Generating Sequence 2
# Time=450 [GEN] : Send Data to Driver
```

The interface includes a menu bar (File, Edit, View, Compile, Simulate, Add, Transcript, Tools, Layout, Bookmarks, Window, Help), a toolbar, and a status bar at the bottom showing 'Now: 540 ns Delta: 0' and 'sim/:test:#INITIAL#131'.



The above figure depicts Move operation. We have done the Move immediate operation for Register R0 and R5 already. At time instant from $t=425\text{ns}$ to 445ns we observe that. The Move operation takes two states (two clock pulses) to complete the operation. We observe the data stored in Register R6 (111011011) is copied to Register R0 (111011011).

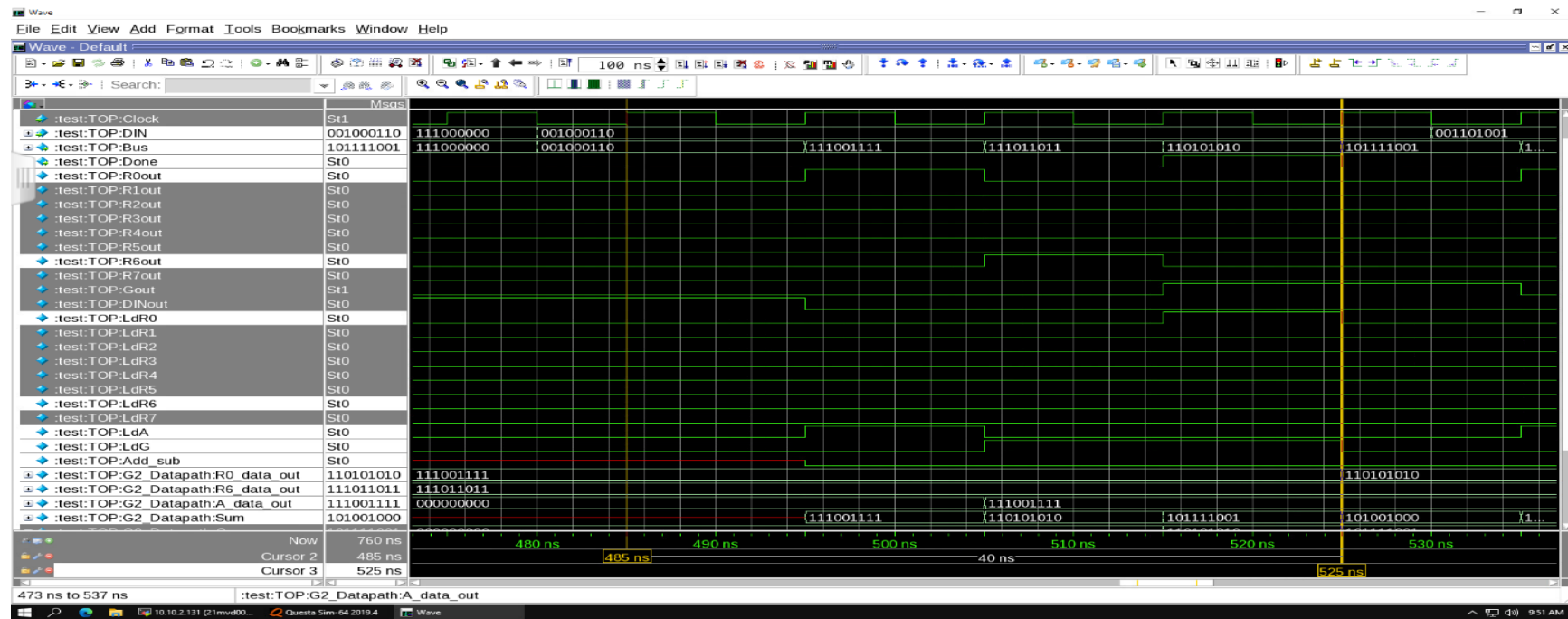
3. ADD OPERATION:



The screenshot displays the Questa Sim-64 2019.4 software interface. The main window shows a transcript of simulation events. The transcript is divided into two sections, one for 'Generating Sequence 1' and another for 'Generating Sequence 2'. Both sections show the execution of an 'ADD' operation, including data generation, interface triggering, and scoreboard updates. The simulation is currently at 760 ns.

```
# Generating Sequence 1
# Time=480 [GEN] : Send Data to Driver
# Time=480 -- DIN=001_000_110 --
# ADD OPERATION GENERATED
# Time=480-----ADD OPERATION GENERATED
# Time=480,[DRV] : Rcvd Data from Generator
# Time=480 -- DIN=001_000_110 --
# [DRV] :-----INTERFACE TRIGGER -----
# Time=485 [MON] : data send to Scoreboard
# Time=485 [DUT---MON] BUS LOADED WITH DIN :001000110
# Time=520 [DUT---MON] BUS LOADED ADD RESULT DATA :110101010
# Time=525 [MON] : data send to Scoreboard
# Time=525 [DUT---MON] BUS LOADED WITH DIN :110101010
# Time=525 [SCOREBOARD] -----ADDITION OPERATION DONE
# Time=525 -- DIN=001_000_110 --
# Time=525 [SCOREBOARD] BUS CONTENTS = 110101010
# Time=525 [SCOREBOARD]-----ADDITION OPERATION DONE
# Time=525 [SCOREBOARD] ADDITION OPERATION DONE PASS --- ADDITION OPERATION DONE PASS ---
# 525INSTRUCTION EXECUTED
# 525----DATA LOADED TO DIN----
# *****
# Generating Sequence 2
# Time=530 [GEN] : Send Data to Driver
# Time=530 -- DIN=001_101_001 --
# ADD OPERATION GENERATED
# Time=530-----ADD OPERATION GENERATED
# Time=530,[DRV] : Rcvd Data from Generator
# Time=530 -- DIN=001_101_001 --
# [DRV] :-----INTERFACE TRIGGER -----
# Time=560 [DUT---MON] BUS LOADED ADD RESULT DATA :110000101
# Time=565 [MON] : data send to Scoreboard
# Time=565 [DUT---MON] BUS LOADED WITH DIN :110000101
# Time=565 [SCOREBOARD] -----ADDITION OPERATION DONE
# Time=565 -- DIN=001_101_001 --
```

- Add operation is done as **add R0, R6**



In this figure we observe that the data 111001111 loaded to register R0. After 40ns (4 cycles) we observe that R0 is loaded with the data. We are doing Move immediate operation for Register R0. In the figure we observe that the data 111011011 loaded to register R6. We are doing Move immediate operation for Register R6. We observe that the R0 data value is copied to Register A. The control signal LdA is generated high and goes low after that, the addition takes place with bus loaded with R6 data. In next clock pulse we observe that the LdG signal became high and addition result is stored to Register G. Finally, we observe that sum result stored Register G is stored back to register R0.

The result can be seen at t=525ns, 10101010 is the addition result (it's taking 9bit value).

4. Subtraction Operation

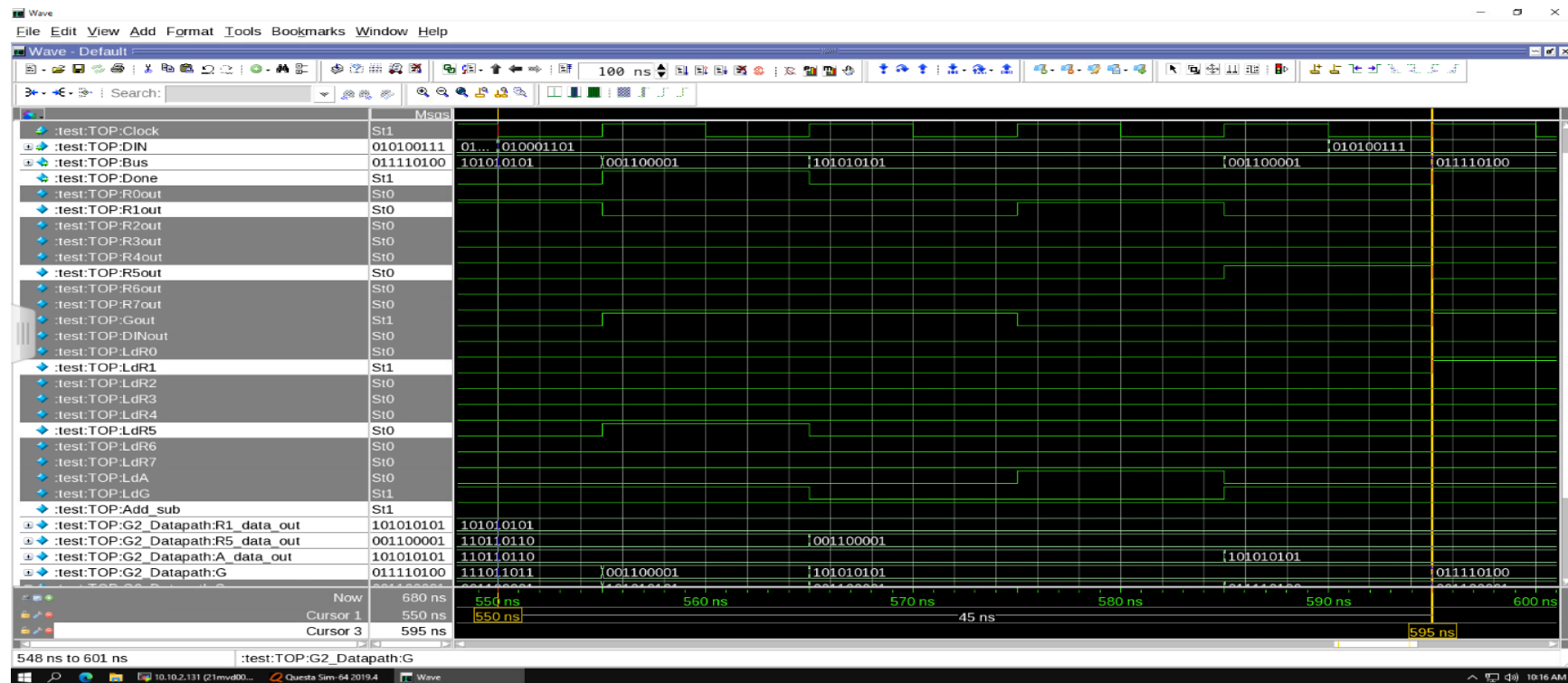
The screenshot shows the Questa Sim-64 2019.4 interface. The main window displays the Transcript window, which contains a log of simulation events. The log shows the following sequence of events:

- Generating Sequence 5
- Time=550 [GEN] : Send Data to Driver
- Time=550 -- DIN=010_001_101 --
- SUBTRACTION OPERATION GENERATED
- Time=550-----SUBTRACTION OPERATION GENERATED
- Time=550,[DRV] : Rcvd Data from Generator
- Time=550 -- DIN=010_001_101 --
- [DRV] :----- INTERFACE TRIGGER -----
- Time=560 [DUT---MON] BUS LOADED WITH SUB RESULT :001100001
- Time=565 [MON] : data send to Scoreboard
- Time=565 [DUT---MON] BUS LOADED WITH DIN :001100001
- Time=565 [SCOREBOARD] -----SUBTRACTION OPERATION DONE
- Time=565 -- DIN=010_001_101 --
- Time=565 [SCOREBOARD] BUS CONTENTS = 001100001
- Time=565 [SCOREBOARD] -----SUBTRACTION OPERATION DONE
- Time=565 [SCOREBOARD] SUBTRACTION OPERATION DONE PASS---SUBTRACTION OPERATION DONE PASS---
- Time=565 [SCOREBOARD] 565INSTRUCTION EXECUTED
- Time=565 [SCOREBOARD] 565----DATA LOADED TO DIN----
- Time=565 [SCOREBOARD] 565INSTRUCTION EXECUTED
- Time=565 [SCOREBOARD] 565----SUB INSTRUCTION EXECUTED----
- *****
- Generating Sequence 6
- Time=590 [GEN] : Send Data to Driver
- Time=590 -- DIN=010_100_111 --
- SUBTRACTION OPERATION GENERATED
- Time=590-----SUBTRACTION OPERATION GENERATED
- Time=590,[DRV] : Rcvd Data from Generator
- Time=590 -- DIN=010_100_111 --
- [DRV] :----- INTERFACE TRIGGER -----
- Time=600 [DUT---MON] BUS LOADED WITH SUB RESULT :011110100
- Time=605 [MON] : data send to Scoreboard
- Time=605 [DUT---MON] BUS LOADED WITH DIN :011110100
- Time=605 [SCOREBOARD] -----SUBTRACTION OPERATION DONE
- Time=605 -- DIN=010_100_111 --
- Time=605 [SCOREBOARD] BUS CONTENTS = 011110100
- Time=605 [SCOREBOARD] -----SUBTRACTION OPERATION DONE
- Time=605 [SCOREBOARD] SUBTRACTION OPERATION DONE PASS---SUBTRACTION OPERATION DONE PASS---
- Time=605 [SCOREBOARD] 605INSTRUCTION EXECUTED
- Time=605 [SCOREBOARD] 605----DATA LOADED TO DIN----

The status bar at the bottom shows 'Now: 680 ns' and 'Delta: 0'. The window title is 'sim:/test:/INITIAL#131'.

- Subtraction operation is done as **sub R1, R5**

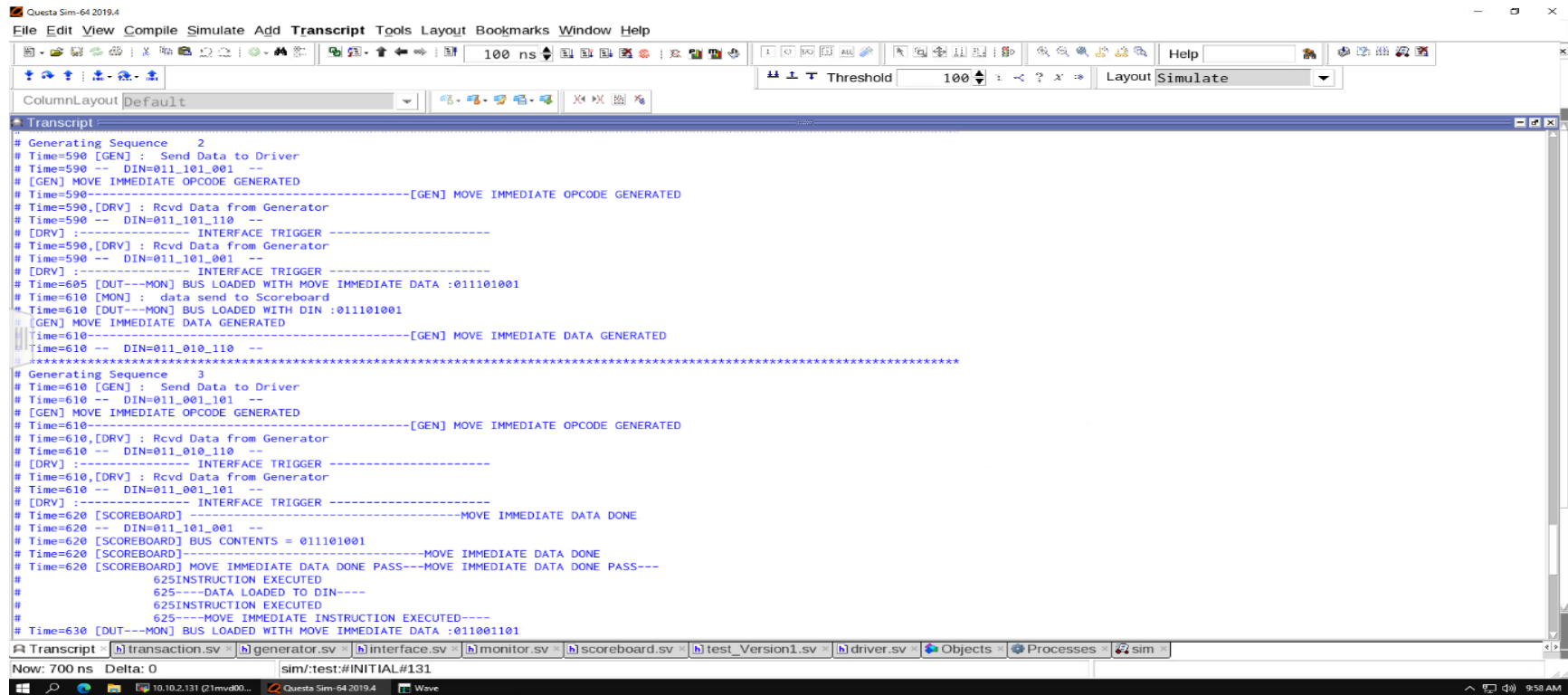
$$R1 = R1 - R5$$



In this figure we observe that the data 101010101 loaded to register R1. After 40ns (4 cycles) we observe that R1 is loaded with the data. We are doing Move immediate operation for Register R1. In the figure we observe that the data 001100001 loaded to register R5. We are doing Move immediate operation for Register R5. We observe that the R1 data value is copied to Register A. The control signal LdA is generated high and goes low after that, the addition takes place with bus loaded with R5 data. In next clock pulse we observe that the LdG signal became high and addition result is stored to Register G. Finally, we observe that sum result stored Register G is stored back to register R1.

The result can be seen at t=595ns, 011110100 is the addition result (it's taking 9bit value).

5. Move Immediate Operation



The screenshot displays the Questa Sim-64 2019.4 software interface. The main window shows a transcript of simulation events. The transcript includes the following text:

```
# Generating Sequence 2
# Time=590 [GEN] : Send Data to Driver
# Time=590 -- DIN=011_101_001 --
# [GEN] MOVE IMMEDIATE OPCODE GENERATED
# Time=590-----[GEN] MOVE IMMEDIATE OPCODE GENERATED
# Time=590,[DRV] : Rcvd Data from Generator
# Time=590 -- DIN=011_101_110 --
# [DRV] :-----INTERFACE TRIGGER-----
# Time=590,[DRV] : Rcvd Data from Generator
# Time=590 -- DIN=011_101_001 --
# [DRV] :-----INTERFACE TRIGGER-----
# Time=605 [DUT---MON] BUS LOADED WITH MOVE IMMEDIATE DATA :011101001
# Time=610 [MON] : data send to Scoreboard
# Time=610 [DUT---MON] BUS LOADED WITH DIN :011101001
# [GEN] MOVE IMMEDIATE DATA GENERATED
# Time=610-----[GEN] MOVE IMMEDIATE DATA GENERATED
# Time=610 -- DIN=011_010_110 --
# *****
# Generating Sequence 3
# Time=610 [GEN] : Send Data to Driver
# Time=610 -- DIN=011_001_101 --
# [GEN] MOVE IMMEDIATE OPCODE GENERATED
# Time=610-----[GEN] MOVE IMMEDIATE OPCODE GENERATED
# Time=610,[DRV] : Rcvd Data from Generator
# Time=610 -- DIN=011_010_110 --
# [DRV] :-----INTERFACE TRIGGER-----
# Time=610,[DRV] : Rcvd Data from Generator
# Time=610 -- DIN=011_001_101 --
# [DRV] :-----INTERFACE TRIGGER-----
# Time=620 [SCOREBOARD]-----MOVE IMMEDIATE DATA DONE
# Time=620 -- DIN=011_101_001 --
# Time=620 [SCOREBOARD] BUS CONTENTS = 011101001
# Time=620 [SCOREBOARD]-----MOVE IMMEDIATE DATA DONE
# Time=620 [SCOREBOARD] MOVE IMMEDIATE DATA DONE PASS---MOVE IMMEDIATE DATA DONE PASS---
#
# 625INSTRUCTION EXECUTED
# 625---DATA LOADED TO DIN---
# 625INSTRUCTION EXECUTED
# 625---MOVE IMMEDIATE INSTRUCTION EXECUTED---
# Time=630 [DUT---MON] BUS LOADED WITH MOVE IMMEDIATE DATA :011001101
```

The bottom status bar shows the current time is 700 ns, Delta is 0, and the simulation is at the initial state (#131). The taskbar at the bottom indicates the system is running on 10.10.2.131 with the date 10/10/2019.

QUESTA COVERAGE REPORT

The screenshot displays the Questa Coverage Report web application in a Mozilla Firefox browser. The browser's address bar shows the file path: `file:///home/Userdata/21mvd0086/System_Verilog_Simple_Processor_J_Comp/Simple_Processor_Ver2/Simple_Processor_Ver1/Simple_Processor_bkp/Simple_Processor/covhtmlreport/index ...`. The application's navigation bar includes links for Red Hat, Customer Portal, Documentation, and Red Hat Network. The main content area is titled "Questa Coverage Report Summary" and features two expandable panels: "Instance Coverage Summary (96.97%)" and "Design Units Coverage Summary (96.93%)". The "Design Units Coverage Summary" panel is currently expanded, showing a table with coverage data for various design units. A left sidebar lists design units with their respective coverage percentages, such as `work.test_Version1_sv_unit (100%)` and `work.test (100%)`. The bottom of the image shows a Windows taskbar with several open applications, including "10.10.2.131 (21mvd00...)", "Questa Sim-64 2019.4", "Wave", and "Questa Coverage Rep...". The system clock in the bottom right corner indicates the time is 7:41 AM.

Design Units Coverage Summary (96.93%)

Coverage Type ↑	Bins	Hits	Misses	Coverage
Search...	Search...	Search...	Search...	Search...
Branches	104	95	9	91.34%
Conditions	32	29	3	90.62%
Expressions	12	12	0	100%
FSM States	4	4	0	100%
FSM Transitions	6	6	0	100%
Statements	296	292	4	98.64%
Toggles	1238	1212	26	97.89%

➤ Design units coverage summary = 96.93%

Questa Coverage Report - Mozilla Firefox@mentorserver

Questa Coverage Report

file:///home/userdata/21mvd0086/System_Verilog_Simple_Processor_J_Comp/Simple_Processor_Ver2/Simple_Processor_Ver1/Simple_Processor_bkp/Simple_Processor/covhtmlreport/index ...

Red Hat Customer Portal Documentation Red Hat Network

InstancesDesign Units

Search...

test (95.86%)

vif (93.18%)

TOP (95.66%)

G1_Controller

G2_Datapath

test_Version1_sv_unit (100%)

Questa Instance Coverage

Instance: :test

Instance Path

/test

Design Unit

work.test

Language

Verilog

Source File

test_Version1.sv

Coverage Summary By Instance (95.86%)

Instance ↑

Search...

Branches

Conditions

Expressions

FSM States

FSM Transitions

Statements

Toggles

Total

Total

91.52%

85%

100%

100%

100%

98.04%

96.5%

95.86%

test

100%

-

100%

-

-

100%

100%

100%

TOP

90.9%

85%

100%

100%

100%

97.16%

96.61%

95.66%

vif

93.18%

93.18%

Local Instance Coverage Details (100%)

Coverage Type ↑

Search...

Bins

Hits

Misses

Coverage

Branches

8

8

0

100%

Expressions

9

9

0

100%

Statements

64

64

0

100%

Toggles

14

14

0

100%

Recursive Hierarchical Coverage Details (95.86%)

Coverage Type ↑

Search...

Bins

Hits

Misses

Coverage

Branches

118

108

10

91.52%

Conditions

20

17

3

85%

Expressions

15

15

0

100%

FSM States

4

4

0

100%

FSM Transitions

6

6

0

100%

Statements

205

201

4

98.04%

Toggles

974

940

34

96.5%

Windows Taskbar

10.10.2.131 (21mvd00...)

Questa Sim-64 2019.4

Wave

Questa Coverage Rep...

7:41 AM

COVER GROUPS

Questa Sim-64 2019.4

File Edit View Compile Simulate Add Covergroups Tools Layout Bookmarks Window Help

100 ns

Threshold 100

Layout Coverage

ColumnLayout Default

Covergroups:

Name	Class Type	Coverage	Goal	% of Goal	Status	Included	Merge_instances	Get_inst_coverage	Comment
test_Version1_sv_unit:driver		87.50%							
TYPE CovPort		87.50%	100	87.50%	<div><div></div></div>		auto(1)		

Transcript Analysis Assertions Cover Directives Covergroups generator.sv driver.sv environment.sv interface.sv monitor.sv scoreboard.sv test_Version1.sv Details Objects

Now: 619,200 ns Delta: 0 sim/:test:#INITIAL#131

Covergroups Filter: NoFilter Covergroups Coverage: 87.50% Recursive Mode

Questa Sim-64 2019.4 Wave 7:39 AM

Questa Coverage Report - Mozilla Firefox@mentorserver

Questa Coverage Report

file:///home/userdata/21mvd0086/System_Verilog_Simple_Processor_J_Comp/Simple_Processor_Ver2/Simple_Processor_Ver1/Simple_Processor_bkp/Simple_Processor/covhtmlreport/index ...

Red Hat Customer Portal Documentation Red Hat Network

InstancesDesign Units

Search...

test (95.86%)

test_Version1_sv_unit (100%)

Questa Coverage Report Summary

Instance Coverage Summary (96.97%)

Coverage Type ↑	Bins	Hits	Misses	Coverage
Search...	Search...	Search...	Search...	Search...
Branches	141	131	10	92.9%
Conditions	32	29	3	90.62%
Expressions	15	15	0	100%
FSM States	4	4	0	100%
FSM Transitions	6	6	0	100%
Statements	331	327	4	98.79%
Toggles	974	940	34	96.5%

Design Units Coverage Summary (96.93%)

Coverage Type ↑	Bins	Hits	Misses	Coverage
Search...	Search...	Search...	Search...	Search...
Branches	104	95	9	91.34%
Conditions	32	29	3	90.62%
Expressions	12	12	0	100%
FSM States	4	4	0	100%
FSM Transitions	6	6	0	100%
Statements	296	292	4	98.64%
Toggles	1238	1212	26	97.89%

10.10.2.131 (21mvd0086)Questa Sim-64 2019.4WaveQuesta Coverage Rep...

7:40 AM