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**ECE6024 – VLSI Verification Methodologies**

**Project: Design and Verification of Simple Processor**

**by**

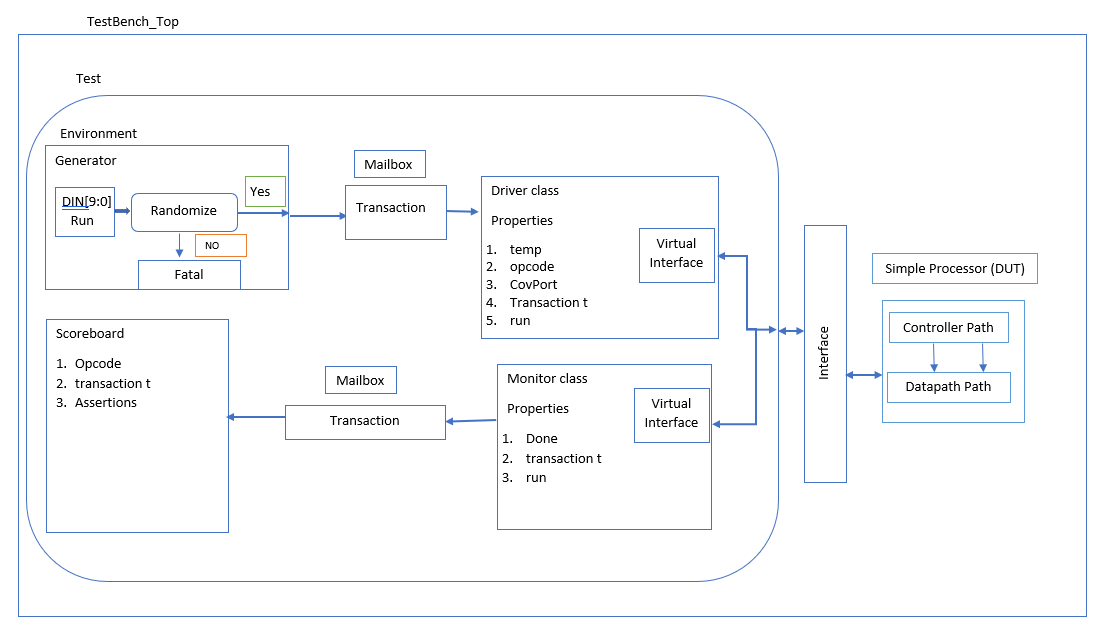
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**OVERVIEW**

This project presents a verification technique of Simple Processor using System Verilog. The Simple Processor is a digital system that used to store 9-bit data and also performs arithmetic operations (addition, subtraction) on 9-bit data. This digital system contains registers(R0–R7), multiplexer, adder and also a controller. The following tasks have been performed as part of verification plan - checking reset functionality, checking MVI (move Immediate operation), checking MV (move operation), checking ADD (addition) operations, checking SUB (subtraction) operation using assertions.

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**DUT**

The DUT consists of Controller block and Datapath block. The Control Path implements FSM and provide control signals to the Datapath in proper sequence. The Data Path consists of functional units where all computations are carried out.

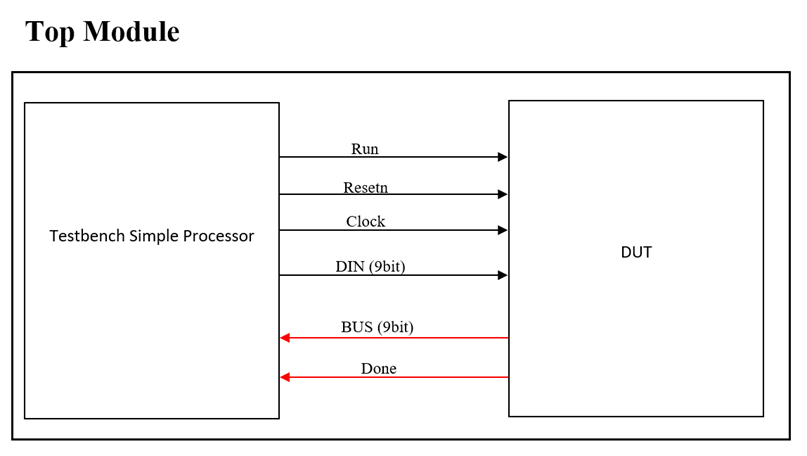
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Figure 1 Top Module

**RESULTS**

**TEST PLAN**

* Provide the reset signal and check whether the registers are loaded with 9’b0.
* Store the initial data into the registers.
* Randomize the data "DIN" and store the values to the respective registers, check the values in the registers using immediate assertions.
* Perform Move immediate, Move, Addition and Subtraction operation.
* Provide the "DIN [8:6]" for non-instructional value and check the status of the system.

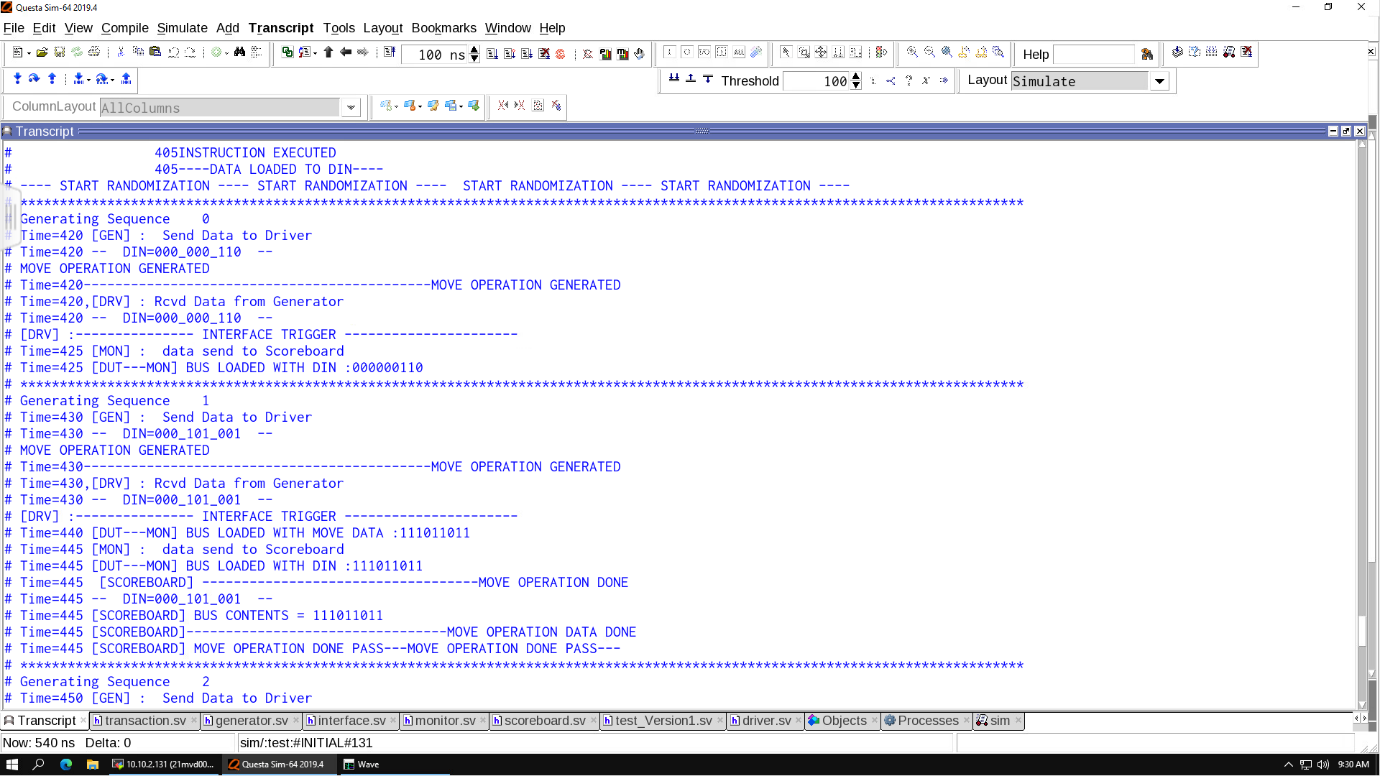
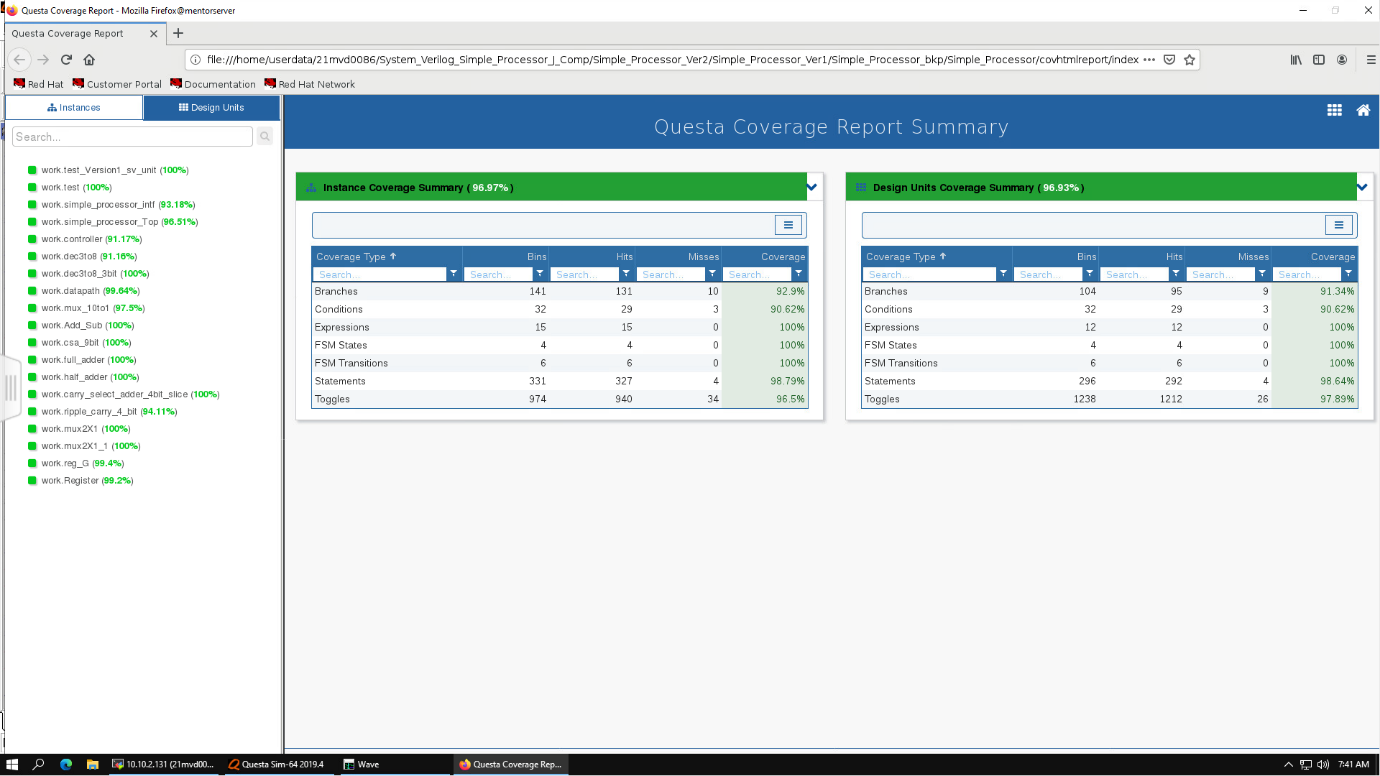


Figure 2 Testbench Setup



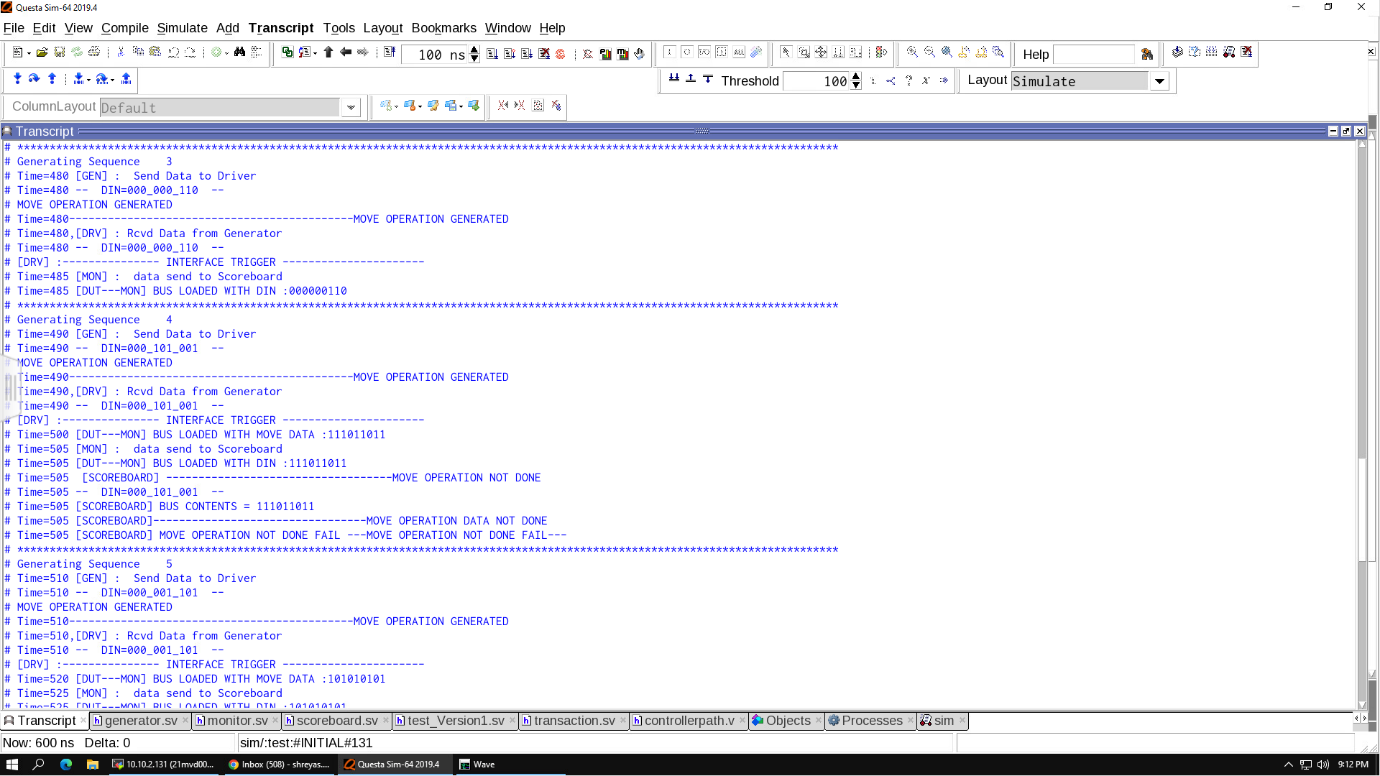
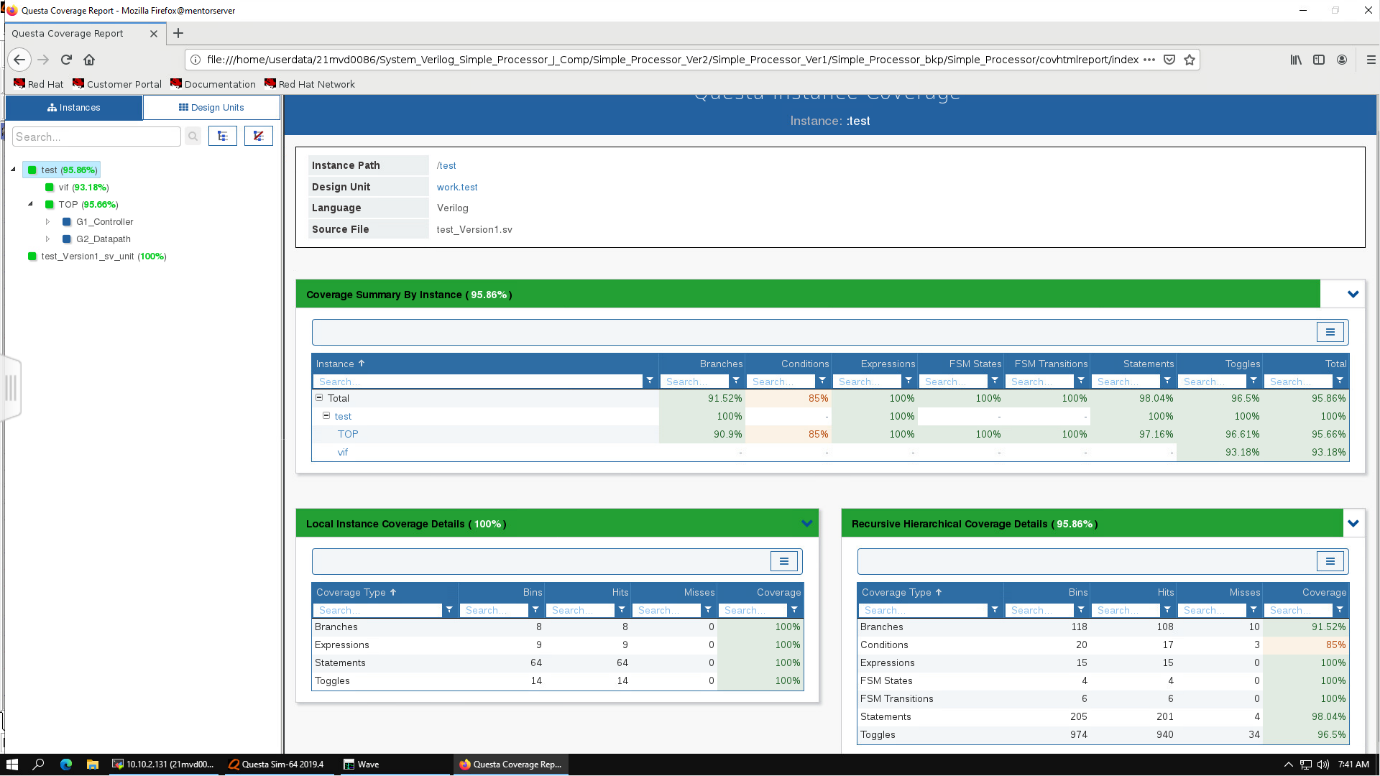
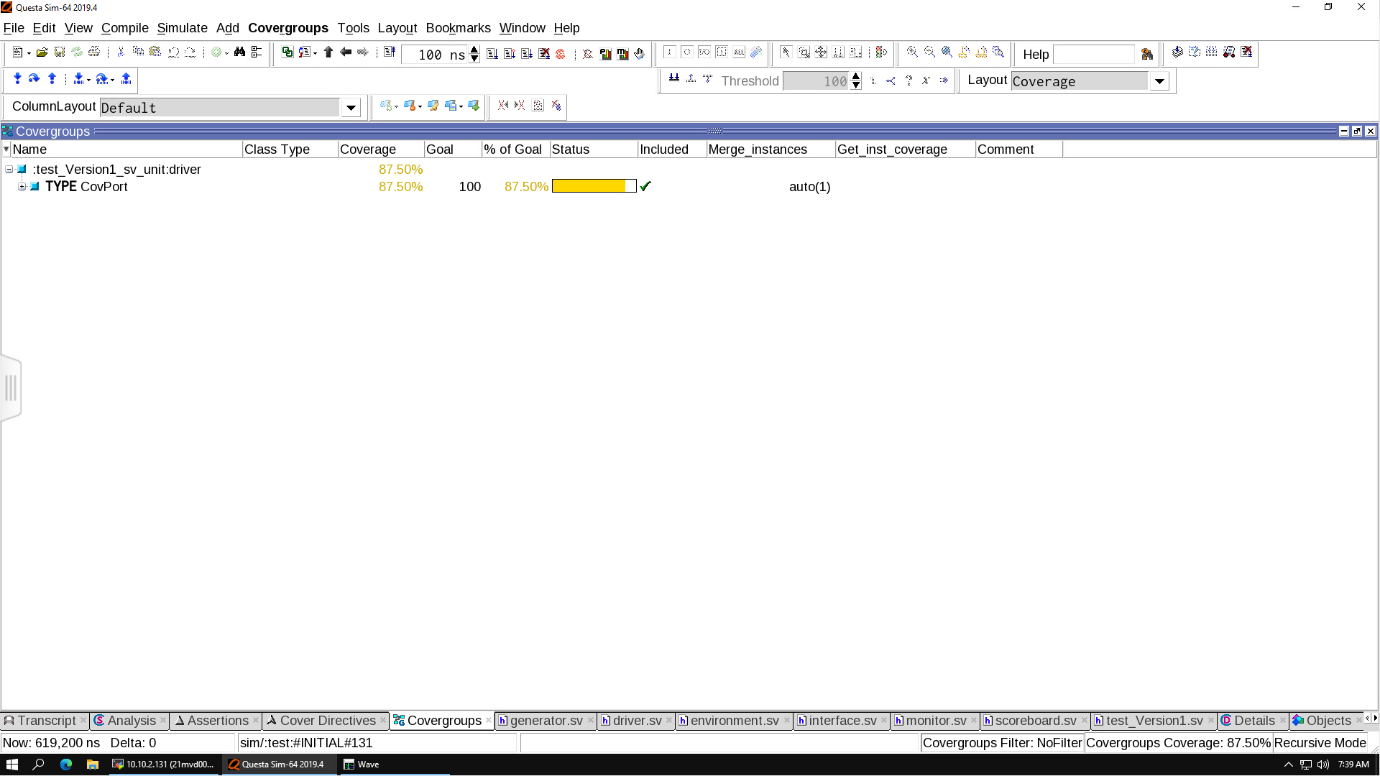


Figure 5 Covergroup for DIN

Figure 4 Code Coverage

Figure 3 Bug detected in DUT

Figure 2 Bug Free

**CONCLUSION**

* The main objective of the DUT has been verified with randomized instructions.
* The coverage has been achieved to be **96.93%.**
* The code coverage has been achieved to be **100%.**
* The cover group coverage is **87.5%.**