**interface** processor\_bus ();

logic LdR0, LdR1, LdR2, LdR3, LdR4, LdR5, LdR6, LdR7, LdA, LdG, Add\_sub, IRin;

logic R0\_data\_out, R1\_data\_out, R2\_data\_out, R3\_data\_out, R4\_data\_out, R5\_data\_out, R6\_data\_out, R7\_data\_out, A\_data\_out, Sum, G;

**modport** proc\_bus\_port\_datapath (input LdR0, LdR1, LdR2, LdR3, LdR4, LdR5, LdR6, LdR7, LdA, LdG, Add\_sub, IRin, R0\_data\_out, R1\_data\_out, R2\_data\_out, R3\_data\_out, R4\_data\_out, R5\_data\_out, R6\_data\_out, R7\_data\_out, A\_data\_out, Sum, G);

**modport** proc\_bus\_port\_controlpath (output LdR0, LdR1, LdR2, LdR3, LdR4, LdR5, LdR6, LdR7, LdA, LdG, Add\_sub, IRin, R0\_data\_out, R1\_data\_out, R2\_data\_out, R3\_data\_out, R4\_data\_out, R5\_data\_out, R6\_data\_out, R7\_data\_out, A\_data\_out, Sum, G);

**endinterface**: processor\_bus ();

**module** top ();

processor\_bus GA1 ();

controller\_new GA2 (GA1);

datapath\_register\_array GA3 (GA1);

**endmodule**: top