Test Specification Report

Alessandro Barro, Nicolas Bruscoli, Viviana Ceccarelli, Manuel Cintura, LeonardoChiacchiararelli, Lucia Mariani

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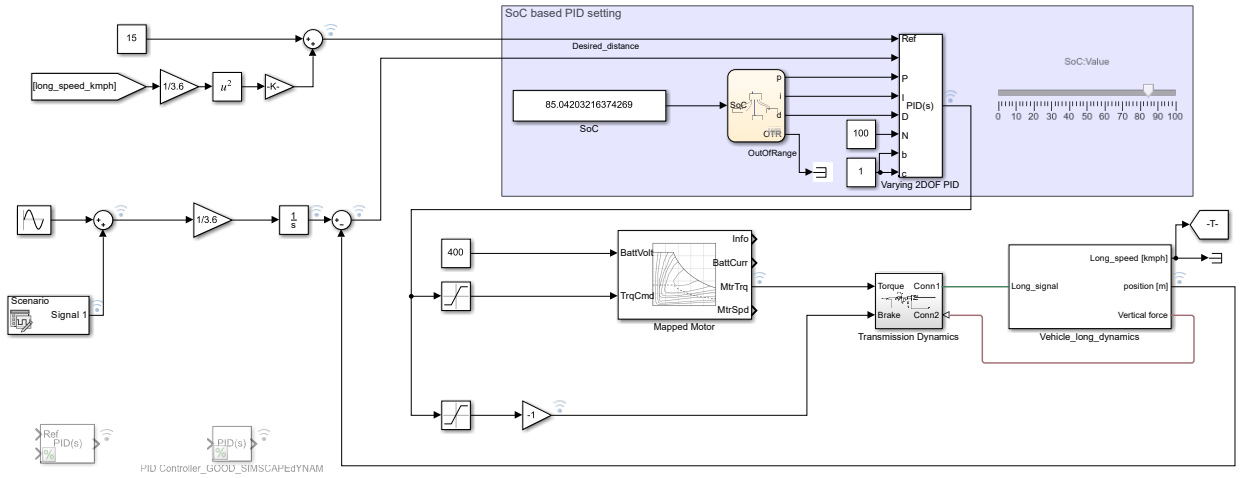
1. SoC_handle_FSM_BaselineTest

Test Details

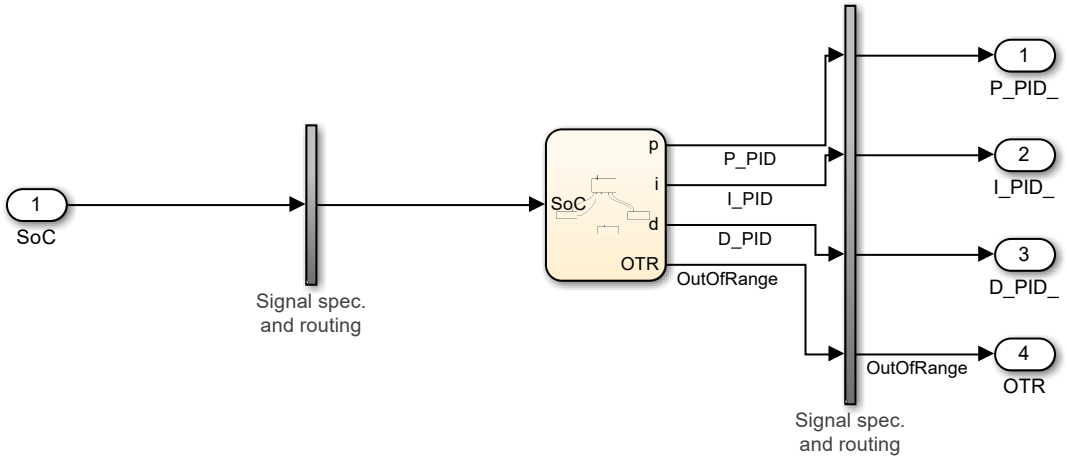
Releases	Current (2019b)

System Under Test

Model Name: Bozza_longitudinal_rev2_19b



Harness Name: Bozza_longitudinal_rev2_19b_Harness3



Simulation Settings Overrides

Simulation Mode	Model Settings

Stop Time	10

External Inputs

Name	File Path	Status
Test_chart_rev2.mat (Active)	D:\Dati\Università\MAGISTRALE\SecondYear\Compliance Design\Test_chart_rev2.mat	Successfully mapped inputs.

Logged Signals

Name	Source	Port Index	Plot Index
Signal Set 1			
• P_PID	Bozza_longitudinal_rev2_19b_Harness-3/Chart	1	
• I_PID	Bozza_longitudinal_rev2_19b_Harness-3/Chart	2	
• D_PID	Bozza_longitudinal_rev2_19b_Harness-3/Chart	3	
• OutOfRange	Bozza_longitudinal_rev2_19b_Harness-3/Chart	4	

Configuration Settings Overrides

Configuration settings	Do not override model settings

Baseline Criteria

Signal Name	Abs Tol	Rel Tol	Leading Tol	Lagging Tol
Baseline_FSM_Testing_rev2.mat (Active)	0	0	0	0

Signal Name	Abs Tol	Rel Tol	Leading Tol	Lagging Tol
• D_PID (Active)	0	0	0	0
• I_PID (Active)	0	0	0	0
• OutOfRange (Active)	0	0	0	0
• P_PID (Active)	0	0	0	0
• P_PID (Active)	0	0	0	0
• I_PID (Active)	0	0	0	0
• D_PID (Active)	0	0	0	0
• OutOfRange (Active)	0	0	0	0