Test Specification Report

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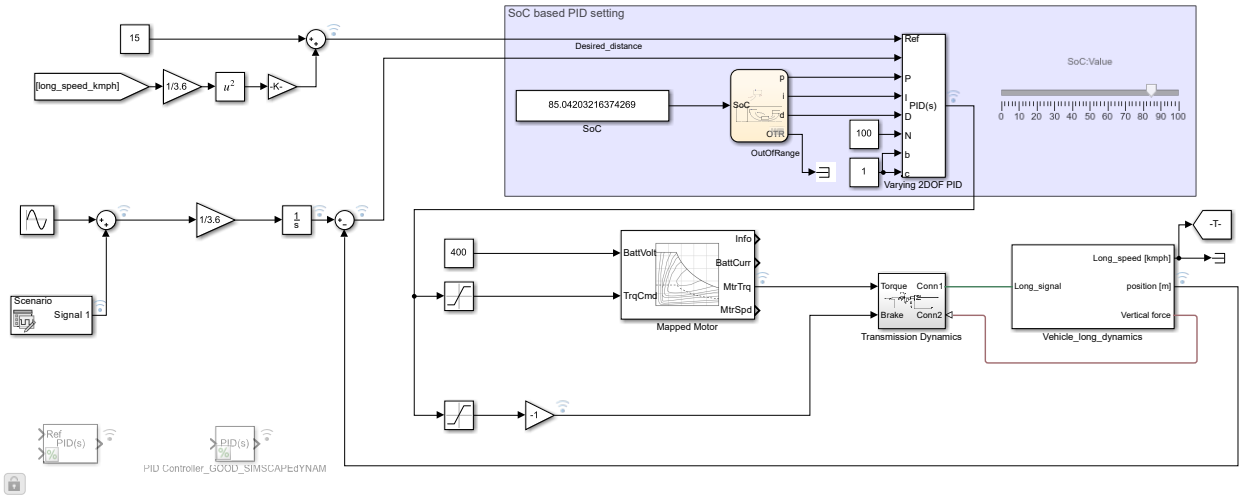
1. SoC_handle_FSM_BaselineTest

Test Details

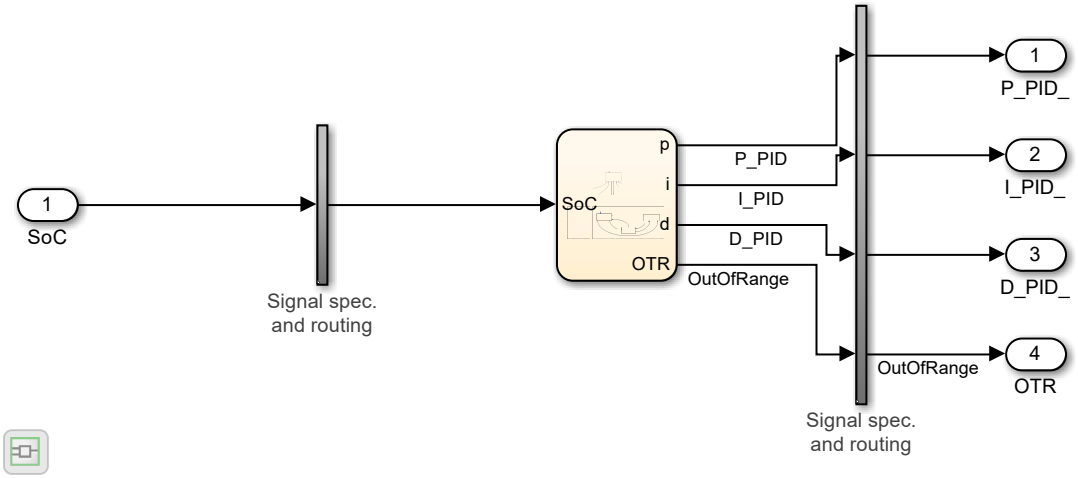
Releases	Current (2019b)

System Under Test

Model Name: Bozza_longitudinal_rev2_19b



Harness Name: Bozza_longitudinal_rev2_19b_Harness3



Simulation Settings Overrides

Simulation Mode	Model Settings

Stop Time	10

External Inputs

Name	File Path	Status
Test_chart_rev2.-mat (Active)	D:\Dati\Università\MAGISTRALE\SecondYe-ar\Compliance Design\Project\Test\FSM_u-nit_test\Test_chart_rev2.mat	Successfully mapped inp-uts.

Logged Signals

Name	Source	Port Index	Plot Index
Signal Set 1			
• P_PID	Bozza_longitudinal_rev2_19b_Harness-3/Chart	1	
• I_PID	Bozza_longitudinal_rev2_19b_Harness-3/Chart	2	
• D_PID	Bozza_longitudinal_rev2_19b_Harness-3/Chart	3	
• OutOfRange	Bozza_longitudinal_rev2_19b_Harness-3/Chart	4	

Configuration Settings Overrides

Configuration settings	Do not override model settings

Baseline Criteria

Signal Name	Abs Tol	Rel Tol	Leading Tol	Lagging Tol
Baseline_FSM_Testing_rev2.mat	0	0	0	0

Signal Name	Abs Tol	Rel Tol	Leading Tol	Lagging Tol
• D_PID (Active)	0	0	0	0
• I_PID (Active)	0	0	0	0
• OutOfRange (Active)	0	0	0	0
• P_PID (Active)	0	0	0	0
Baseline_FSM_Testing_rev3_captured.-mat	0	0	0	0
• D_PID	0	0	0	0
• I_PID	0	0	0	0
• OutOfRange	0	0	0	0
• P_PID	0	0	0	0
• P_PID_:1	0	0	0	0
• I_PID_:1	0	0	0	0
• D_PID_:1	0	0	0	0
• OutOfRange	0	0	0	0
Baseline_FSM_Testing_rev4_captured.-mat (Active)	0	0	0	0.14999-9999999-99999
• D_PID (Active)	0	0	0	0.14999-9999999-99999
• I_PID (Active)	0	0	0	0.14999-9999999-99999

Signal Name	Abs Tol	Rel Tol	Leading Tol	Lagging Tol
• OutOfRange (Active)	0	0	0	0.14999-9999999-99999
• P_PID (Active)	0	0	0	0.14999-9999999-99999
• P_PID_:1 (Active)	0	0	0	0.14999-9999999-99999
• I_PID_:1 (Active)	0	0	0	0.14999-9999999-99999
• D_PID_:1 (Active)	0	0	0	0.14999-9999999-99999
• OutOfRange (Active)	0	0	0	0.14999-9999999-99999