# **Report Generated by Test Manager**

Title: FSM Test: Results report Author: Team 2 (CoDeAS 20/21) Date: 26-Feb-2021 09:35:47

## **Test Environment**

Platform: PCWIN64 MATLAB: (R2020b)

# **Summary**

Sullinal y		<b>.</b>
Name	Outcome	Duration (Seconds)
Results: 2021-Feb-26 09:34:31	27 🥥	28.226
FSM_test	27 🗸	28.226
DEAD	5 🥥	14.777
Dead-Dead	<b>Ø</b>	11.431
Dead-Regen	<b>Ø</b>	0.996
Dead-ED	•	0.815
Dead-NoCharge	•	0.675
Dead-Combined	•	0.794
□ <u>No Charge</u>	6 🕏	3.745
NoCharge-DEAD	•	0.582
NoCharge-Regen	•	0.656
NoCharge-ED	2 🗷	1.256
I <u>Iteration1</u>	•	0.606
I <u>Iteration2</u>	•	0.632
NoCharge-Combined	•	0.582
NoCharge-NoCharge	•	0.613
ED ED	6 🕏	3.642
ED-ED	•	0.576
ED-Regen	•	0.583
ED-DEAD	•	0.587
ED-NoCharge	•	0.58
ED-Combined	2 🗷	1.263
I <u>Iteration1</u>	•	0.62
I <u>Iteration2</u>	•	0.625
Combined	5 🗸	2.985

Combined-Combined	<b>②</b>	0.607
Combined-Regen	<b>Ø</b>	0.577
Combined-DEAD	<b>Ø</b>	0.592
© Combined-ED	<b>Ø</b>	0.583
© Combined-NoCharge	<b>Ø</b>	0.571
Regen	5 🥥	2.973
Regen-Regen	<b>Ø</b>	0.562
Regen-DEAD	<b>Ø</b>	0.589
Regen-ED	<b>Ø</b>	0.586
Regen-NoCharge	<b>Ø</b>	0.583
Regen-Combined	<b>Ø</b>	0.594

## Results: 2021-Feb-26 09:34:31

Result Type: Result Set

Parent: None

Start Time: 26-Feb-2021 09:34:33 End Time: 26-Feb-2021 09:35:01 Outcome: Total: 27, Passed: 27

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## FSM\_test

#### **Test Result Information**

Result Type: Test File Result

Parent: <u>Results: 2021-Feb-26 09:34:31</u>

 Start Time:
 26-Feb-2021 09:34:33

 End Time:
 26-Feb-2021 09:35:01

 Outcome:
 Total: 27, Passed: 27

#### **Test Suite Information**

Name: FSM\_test

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#### **DEAD**

#### **Test Result Information**

Result Type: Test Suite Result

Parent: <u>FSM\_test</u>

Start Time: 26-Feb-2021 09:34:33 End Time: 26-Feb-2021 09:34:48 Outcome: Total: 5, Passed: 5

Description:

This suite contains all the test performed with DEAD as main state. It includes also the transitions from dead to other states.

#### **Test Suite Information**

Name: DEAD

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## **Dead-Dead**

#### **Test Result Information**

Result Type: Test Case Result

Parent: DEAD

Start Time: 26-Feb-2021 09:34:33 End Time: 26-Feb-2021 09:34:44

Outcome: Passed

Description:

State under test: DEAD (0)

Transition under test: DEAD-DEAD

#### **INPUTS:**

- AccPedal: uniformely increasing request

- BrakePedal: 0

- SOC: 0%

- fuelLevel: 0 lt

- SOC: 50%

## **EXPECTED OUTPUT:**

The state should be DEAD for all the testing time.

## **Test Case Information**

Name: Dead-Dead Type: Baseline Test

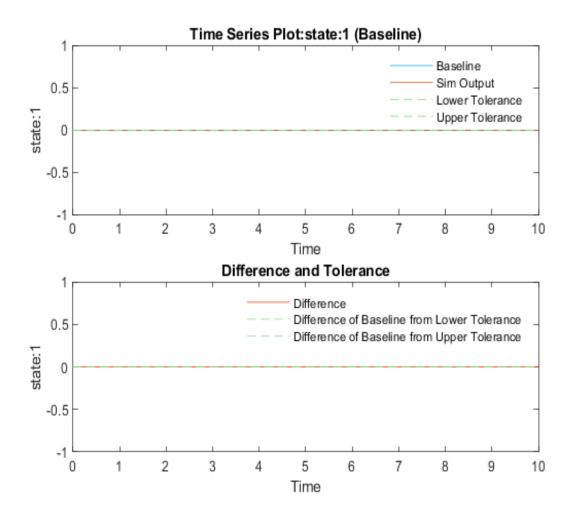
Baseline Name: Dead\_Dead\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\Dead\_Dead\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2		-,	t
state:1	0	0	0	0	0	double			double		Continuous	zoh	union	<u>Link</u>

Name	Abs T	Rel T ol	Lead T	Lag T	Max Di ff	Data Type 1	Units 1	Sample Ti me 1	Data Type 2	Units 2	Sample Time 2 Interp Sync
state:1	0	0	0	0	0	double			double	I	Continuous zoh union



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## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL (

Mode:

Configuration Set: Configuration External Input Name: Dead1.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Dead1.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

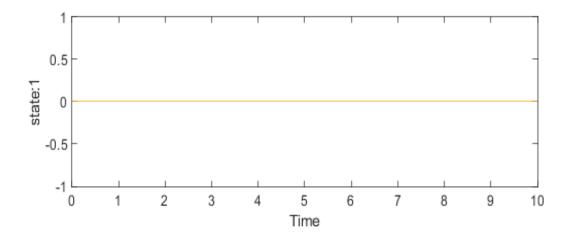
Max Step Size: 0.2000000000000001 Simulation Start Time: 2021-02-26 09:34:33 Simulation Stop Time: 2021-02-26 09:34:44

Platform: PCWIN64

#### **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Dead-Regen**

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

<u>DEAD</u>

26-Feb-2021 09:34:44 Start Time:

End Time: 26-Feb-2021 09:34:45

Outcome: Passed

Description:

State under test: DEAD (0)

Transition under test: DEAD (0) - REGENERATIVE\_BRAKING (4)

#### **INPUT** conditions:

- BrakePedal: != 0 at t = 5s

- Fuel < fuelMin

- SOC< SOCMin

#### **EXPECTED OUTPUT:**

The state should change to REGENERATIVE\_BRAKING (4).

#### **Test Case Information**

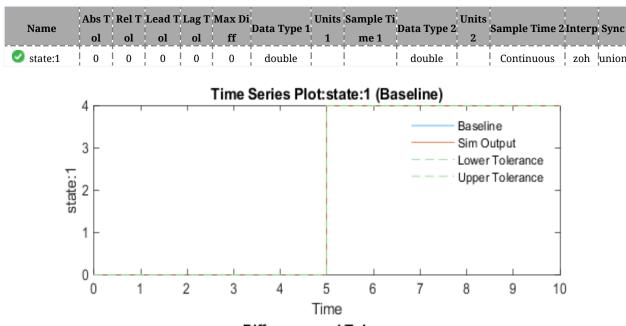
Name: Dead-Regen Type: Baseline Test

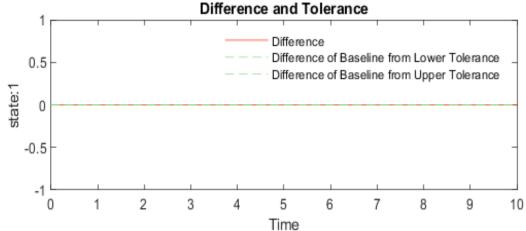
Baseline Name: Dead\_Regen\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\Dead\_Regen\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
Name	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2	interp sync	oy ne	t
state:1	0	0	0	0	0	double			double		Continuous	zoh	union	<u>Link</u>





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## **System Under Test Information**

Model: FSM\_Model Release: Current

Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Dead2.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Dead2.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

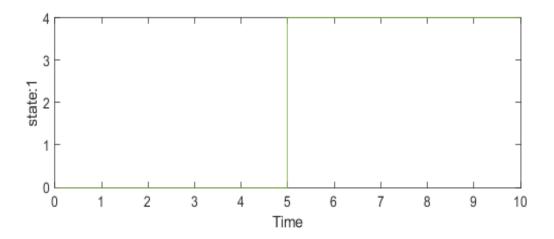
#### **Simulation Output**

Machine Name:

Solver Name:

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double	l	Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Dead-ED**

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

<u>DEAD</u>

26-Feb-2021 09:34:45 Start Time:

End Time: 26-Feb-2021 09:34:46

Outcome: Passed

Description:

State under test: DEAD (0)

Transition under test: DEAD (0) - ELECTRIC\_DRIVE (ED, 2)

#### **INPUT** conditions:

- AccPedal < maxAccMGU

- SOC> SOCMin

- fuelLevel: 10 lt

- BrakePedal: 0

#### **EXPECTED OUTPUT:**

The state should change to ELECTRIC\_DRIVE (ED, 2).

#### **Test Case Information**

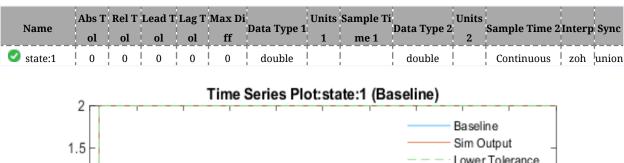
Name: Dead-ED Type: Baseline Test

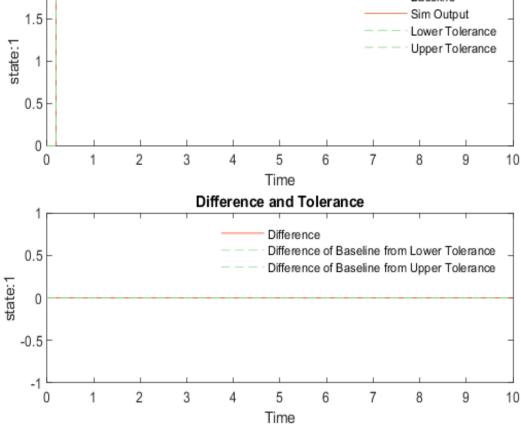
Baseline Name: Dead\_ED\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\Dead\_ED\_baseline.mat

Name	Abs Tol	1				Data Typ e 1	Î	1.	Units 2	Sample Time 2	Interp		Link to Plo t
🕏 state:1	0	0	0	0	0	double		double	I	Continuous	zoh i	union	<u>Link</u>





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**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Dead3.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Dead3.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

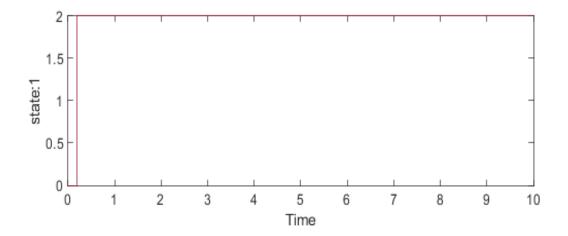
Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:45 Simulation Stop Time: 2021-02-26 09:34:46

Platform: PCWIN64

## **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Dead-NoCharge**

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

<u>DEAD</u>

26-Feb-2021 09:34:46 Start Time:

End Time: 26-Feb-2021 09:34:47

Outcome: Passed

Description:

State under test: DEAD (0)

Transition under test: DEAD (0) - NO\_CHARGE (1)

#### **INPUT** conditions:

- AccPedal < maxAccICE
- SOC < SOCMin
- Fuel > fuelMin
- BrakePedal: 0

#### **EXPECTED OUTPUT:**

The state should change to NO\_CHARGE (1).

#### **Test Case Information**

Name: Dead-NoCharge Type: Baseline Test

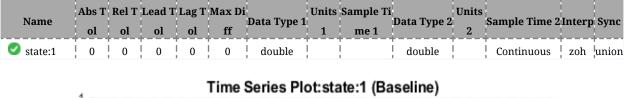
Baseline Name: Dead\_NoCharge\_baseline.mat

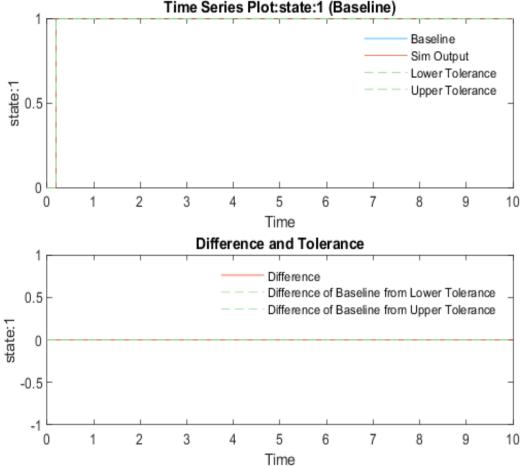
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Baselines\Dead\_NoCharge\_baseline.mat

Name	Abs Tol	1				Data Typ e 1	Î	1.	Units 2	Sample Time 2	Interp		Link to Plo t
🕏 state:1	0	0	0	0	0	double		double	I	Continuous	zoh i	union	<u>Link</u>





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**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Dead4.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Dead4.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Solver Name: VariableStepDiscrete
Solver Type: Variable-Step

Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:46 Simulation Stop Time: 2021-02-26 09:34:47

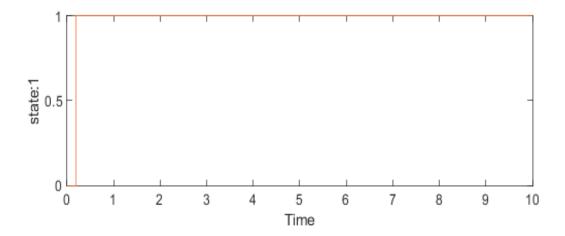
Platform: PCWIN64

## **Simulation Output**

Machine Name:

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Dead-Combined**

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

<u>DEAD</u>

26-Feb-2021 09:34:47 Start Time:

End Time: 26-Feb-2021 09:34:48

Outcome: Passed

Description:

State under test: DEAD (0)

Transition under test: DEAD (0) - COMBINED(3)

#### **INPUT** conditions:

- AccPedal>maxAccMGU

- SOC > SOCMin

- fuel > fuelMin

- BrakePedal: 0

#### **EXPECTED OUTPUT:**

The state should change to COMBINED (3).

#### **Test Case Information**

Name: Dead-Combined Type: Baseline Test

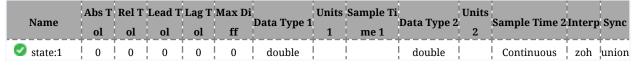
Baseline Name: Dead\_Combined\_baseline.mat

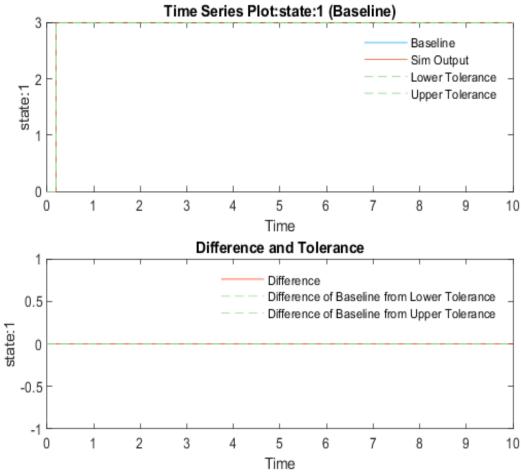
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Baselines\Dead Combined baseline.mat

Name	Abs Tol	1				Data Typ e 1	Î	1.	Units 2	Sample Time 2	Interp		Link to Plo t
🕏 state:1	0	0	0	0	0	double		double	I	Continuous	zoh i	union	<u>Link</u>





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**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Dead5.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Dead5.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

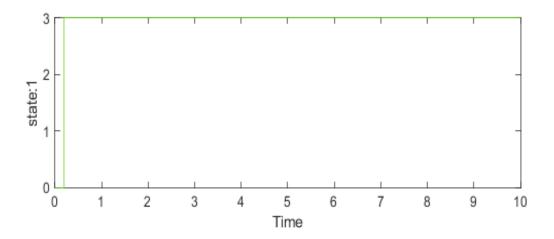
Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:47 Simulation Stop Time: 2021-02-26 09:34:47

Platform: PCWIN64

## **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# No Charge

## **Test Result Information**

Result Type: Parent: Test Suite Result

<u>FSM\_test</u> 26-Feb-2021 09:34:48 Start Time:

End Time: 26-Feb-2021 09:34:51 Outcome: Total: 6, Passed: 6

Description:

From No Charge to all other states. Initially, the FSM starts from DEAD, but soon enters the No Charge state at the first sampling instant.

#### **Test Suite Information**

Name: No Charge

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## **NoCharge-DEAD**

#### **Test Result Information**

Result Type: Test Case Result

Parent: <u>No Charge</u>

Start Time: 26-Feb-2021 09:34:48 End Time: 26-Feb-2021 09:34:48

Outcome: Passed

Description:

State under test: NO\_CHARGE (1)

Transition under test: NO\_CHARGE (1) - DEAD (0)

#### **INPUT** conditions:

- fuel > fuelMin
- BrakePedal: 0

#### **EXPECTED OUTPUT:**

The state should change to DEAD (0).

#### **Test Case Information**

Name: NoCharge-DEAD Type: Baseline Test

Baseline Name: NoChargeToDEAD\_baseline.mat

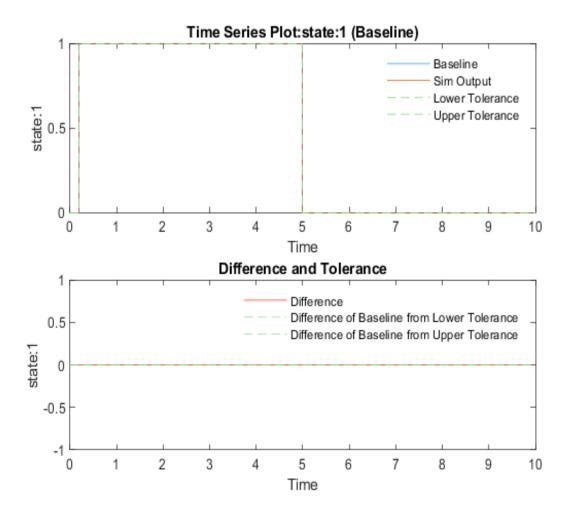
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Baselines\NoChargeToDEAD\_baseline.mat

Name	l	i	l			Data Typ e 1	Units 1	Sample Time 1	1	Units 2	Sample Time 2	Interp		Link to Plo t
state:1	0	. 0	0	0	0	double	 		double	i	Continuous	zoh u	ınion <mark></mark>	<u>Link</u>

Name	ì	Rel T ol	1		Max Di ff	Data Type 1	Units 1	Sample Ti me 1	Data Type 2	Units 2	Sample Time 2 Ir	nterp Sync
state:1	0	0	0	0	0	double	İ	 	double	İ	Continuous	zoh union



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## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL (

Mode:

Configuration Set: Configuration External Input Name: NoCharge1.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\NoCharge1.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

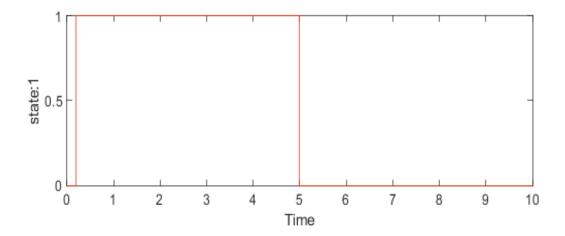
Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:48 Simulation Stop Time: 2021-02-26 09:34:48

Platform: PCWIN64

#### **Simulation Output**

I	Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
	state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# NoCharge-Regen

## **Test Result Information**

Result Type: Parent: Test Case Result

No Charge 26-Feb-2021 09:34:48 Start Time:

End Time: 26-Feb-2021 09:34:49

Outcome: Passed

Description:

State under test: NO\_CHARGE (1)

Transition under test: NO\_CHARGE (1) - REGENERATIVE\_BRAKING (4)

## **INPUT conditions:**

- Fuel > fuelMin

- BrakePedal: 0

#### **EXPECTED OUTPUT:**

The state should change to REGENERATIVE\_BRAKING (4).

#### **Test Case Information**

Name: NoCharge-Regen Type: Baseline Test

Baseline Name: NoChargeToRegen\_baseline.mat

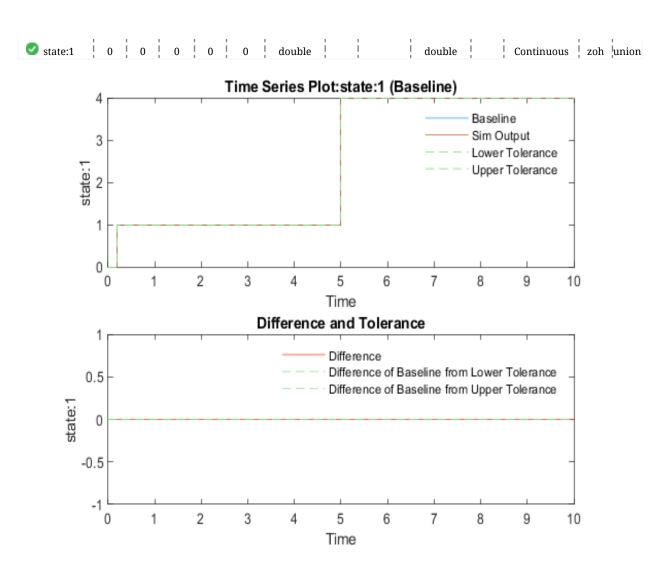
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

 $controller \verb|\Hybrid-controller\Test\FSM|$ 

 $Test \backslash Baselines \backslash NoChargeToRegen\_baseline.mat$ 

Name						Data Typ e 1		Î	Data Typ e 2	Units 2	Sample Time 2	Interp S		Link to Plo t
state:1	0	0	0	0	0	double			double	l	Continuous	zoh ur	nion	<u>Link</u>

1		Abs T Rel T	Lead T Lag T	Max Di		Sample Ti			
1	Name	ol ol	ol ol	ff Dat	ta Type 1	me 1	Data Type 2	Sample Time 2 Interp Syn	c



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## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal Override SIL or PIL

Mode:

Configuration Set: Configuration External Input Name: NoCharge2.mat

0

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\NoCharge2.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

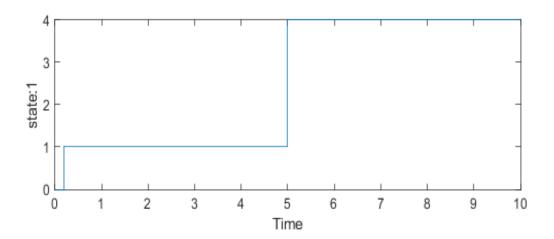
Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:48 Simulation Stop Time: 2021-02-26 09:34:49

Platform: PCWIN64

**Simulation Output** 

Nar	me	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1		double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# NoCharge-ED

## **Test Result Information**

Result Type: Parent: Test Case Result

No Charge 26-Feb-2021 09:34:49 Start Time:

End Time: 26-Feb-2021 09:34:50

Outcome: Passed

Description:

State under test: NO\_CHARGE (1)

Transition under test: NO\_CHARGE (1) - ELECTRIC\_DRIVE (ED, 2)

#### **INPUT** conditions:

- Fuel > fuelMin
- BrakePedal: 0
- SOC < SOCmin for a while, then SOC>SOCmin
- RealSpeed<SpeedEDMax OR Fuel<fuelMin after a while

#### **EXPECTED OUTPUT:**

The state should change to ELECTRIC\_DRIVE (ED, 2).

#### NOTE:

This test is done in two iterations due to the presence of an OR among input conditions.

#### **Test Case Information**

Name: NoCharge-ED Type: Baseline Test

## Iteration1

#### **Test Result Information**

Result Type: Test Iteration Result

Parent: <u>NoCharge-ED</u>

Start Time: 26-Feb-2021 09:34:49 End Time: 26-Feb-2021 09:34:50

Outcome: Passed

#### **Test Case Information**

Name: Iteration1
Type: Baseline Test

Baseline Name: NoCharge\_ED\_baseline\_Iteration1.mat
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

 $controller \verb|\Hybrid-controller\Test\FSM|$ 

Test\Baselines\NoCharge\_ED\_baseline\_Iteration1.

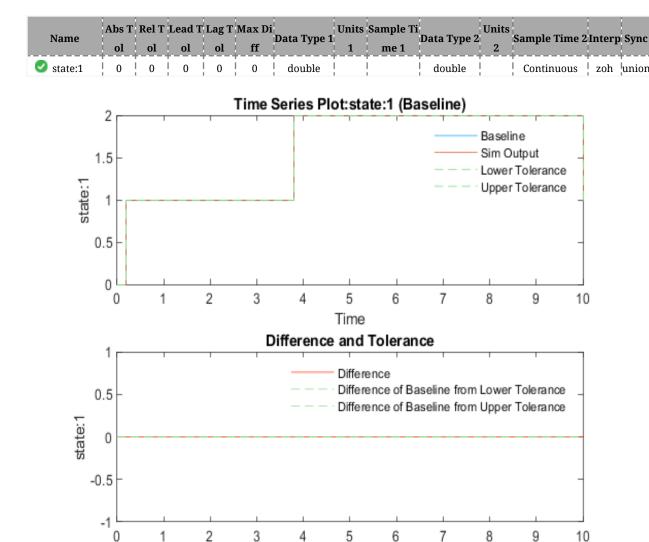
mat

## **Iteration Settings**

#### **Test Overrides**

Parameter Name	Value				
ExternalInput	C:\Users\mordi\Desktop\Materiale				
_	Università\Compliance\hybrid-				
	controller\Hybrid-controller\Test\FSM				
	Test\Inputs\NoCharge3.mat				
Baseline	C:\Users\mordi\Desktop\Materiale				
	Università\Compliance\hybrid-				
	controller\Hybrid-controller\Test\FSM				
	Test\Baselines\NoChargeToED_baseline				
	2.mat\SLBaselineFiles\Iteration1.mat				

Name						71		•	11	Units	Sample Time	Interp		Link to Plo
	Tol	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2		t
state:1	0	0	0	0	0	double			double		Continuous	zoh 1	union	<u>Link</u>



Time

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#### **Simulation**

## **System Under Test Information**

Model: FSM\_Model Release: Current

Simulation Mode: normal

Override SIL or PIL

Mode:

Configuration Set: Configuration External Input Name: NoCharge3.mat

External Input File: C:\Users\mordi\Desktop\Materiale

0

Università\Compliance\hybrid-controller\Hybrid-controller\Test\FSM Test\Inputs\NoCharge3.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

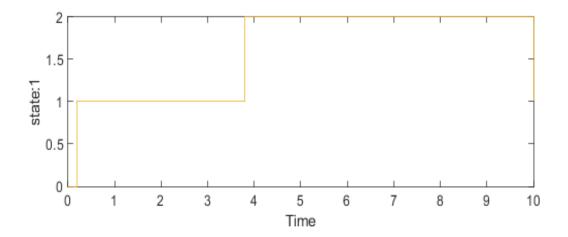
#### **Simulation Output**

Machine Name:

Solver Name:

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double	l	Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Iteration2**

## **Test Result Information**

Result Type: Parent: **Test Iteration Result** 

NoCharge-ED 26-Feb-2021 09:34:50 Start Time:

End Time: 26-Feb-2021 09:34:50

Outcome: Passed

## **Test Case Information**

Name: Iteration2 Type: Baseline Test

Baseline Name: NoCharge\_ED\_baseline\_Iteration2.mat
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

 $controller \verb|\Hybrid-controller\Test\FSM|$ 

Test\Baselines\NoCharge\_ED\_baseline\_Iteration2.

mat

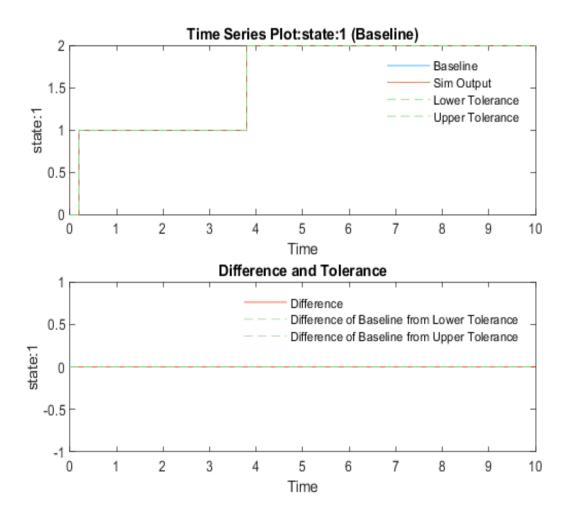
## **Iteration Settings**

#### **Test Overrides**

Parameter Name	Value
ExternalInput	C:\Users\mordi\Desktop\Materiale
_	Università\Compliance\hybrid-
	controller\Hybrid-controller\Test\FSM
	Test\Inputs\NoCharge4.mat
Baseline	C:\Users\mordi\Desktop\Materiale
	Università\Compliance\hybrid-
	controller\Hybrid-controller\Test\FSM
	Test\Baselines\NoChargeToED_baseline
	2.mat\SLBaselineFiles\Iteration2.mat

Name	Abs Tol					Data Typ e 1	1 1	Î	11	Units 2	Sample Time 2	Interp		Link to Plo t
state:1	0	0	0	0	0	double			double		Continuous	zoh	union	<u>Link</u>

Name	Abs T	Rel T	Lead T	Lag T	Max Di ff	Data Type 1	Sample Ti me 1	Data Type 2	Units 2	Sample Time 2 Interp Sync
state:1	0	0	0	0	0	double	İ	double		Continuous zoh union



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## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL

Mode:

Configuration Set: Configuration External Input Name: NoCharge4.mat

External Input File: C:\Users\mordi\Desktop\Materiale

Università\Compliance\hybrid-controller\Hybrid-controller\Test\FSM Test\Inputs\NoCharge4.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

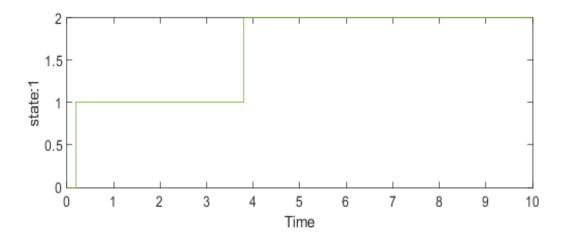
Solver Type: Variable-Step

Max Step Size: 0.2000000000000001 Simulation Start Time: 2021-02-26 09:34:50 Simulation Stop Time: 2021-02-26 09:34:50

Platform: PCWIN64

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# NoCharge-Combined

## **Test Result Information**

Result Type: Parent: Test Case Result

No Charge 26-Feb-2021 09:34:50 Start Time:

End Time: 26-Feb-2021 09:34:51

Outcome: Passed

Description:

State under test: NO\_CHARGE (1)

Transition under test: NO\_CHARGE (1) - COMBINED (3)

#### **INPUT** conditions:

- BrakePedal: 0

- AccPedal> MaxAccICE

- Fuel > fuelMin

- SOC > SOCmin

#### **EXPECTED OUTPUT:**

The state should change to COMBINED (3).

#### **Test Case Information**

Name: NoCharge-Combined

Type: Baseline Test

Baseline Name: NoChargeToCombined\_baseline.mat

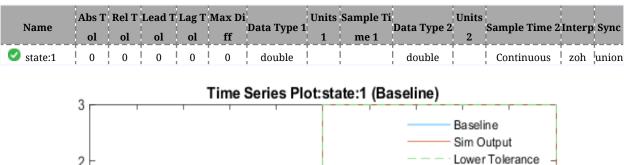
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

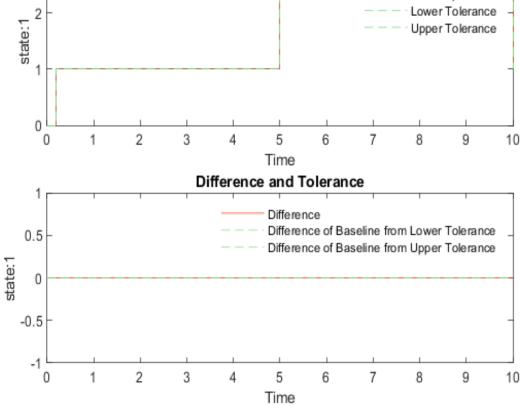
controller\Hybrid-controller\Test\FSM

Test\Baselines\NoChargeToCombined\_baseline.m

at

Name	Abs Tol					Data Typ e 1	•	11	Units	Sample Time	Interp		Link to Plo
	101	UI.	101	101	***	<u> </u>	I IIIIC I			4			
state:1	0	0	0	0	0	double		double		Continuous	zoh i	union	<u>Link</u>





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**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: NoCharge5.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\NoCharge5.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

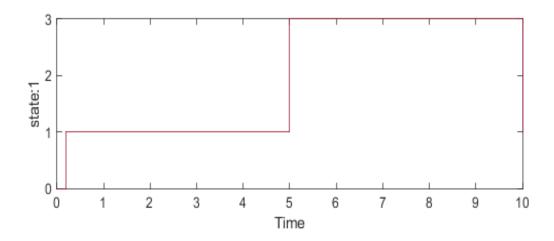
Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# NoCharge-NoCharge

## **Test Result Information**

Result Type: Parent: Test Case Result

No Charge 26-Feb-2021 09:34:51 Start Time:

End Time: 26-Feb-2021 09:34:51

Outcome: Passed

Description:

State under test: NO\_CHARGE (1)

Transition under test: NO\_CHARGE (1) - NO\_CHARGE (1)

## **INPUT conditions:**

- BrakePedal: 0

- AccPedal: uniformly increasing

- Fuel > fuelMin

- SOC < SOCmin

#### **EXPECTED OUTPUT:**

The state should remain to NO\_CHARGE (1).

#### **Test Case Information**

Name: NoCharge-NoCharge

Type: Baseline Test

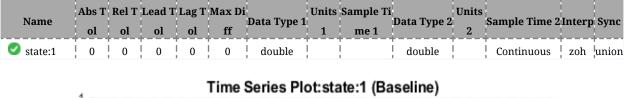
Baseline Name: NoCharge\_NoCharge\_baseline.mat

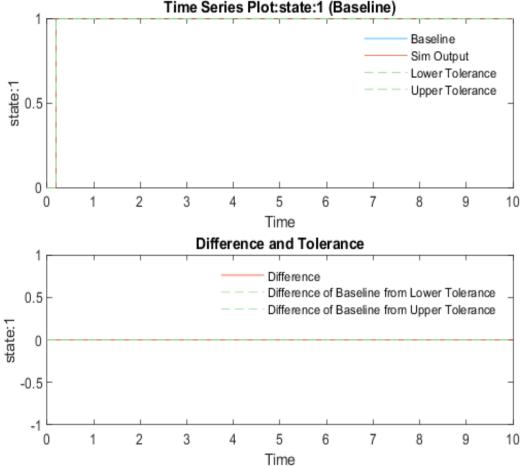
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Baselines\NoCharge\_NoCharge\_baseline.mat

ı	Name	Abs	1	i	i		11		Î	11	Units	Sample Time	Interp		Link to Plo
J		Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2			t
	state:1	. 0	. 0	. 0	0	. 0	double			double		Continuous	zoh	union	Link





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**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: NoCharge6.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\NoCharge6.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

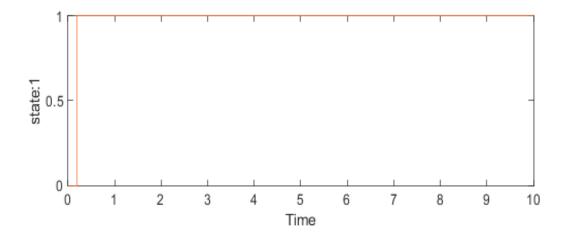
Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# ED

## **Test Result Information**

Result Type: Parent: Test Suite Result

<u>FSM\_test</u> 26-Feb-2021 09:34:51 Start Time:

End Time: 26-Feb-2021 09:34:55 Outcome: Total: 6, Passed: 6

Description:

From Electrical Drive to all other states. Initially, the FSM starts from DEAD, but soon enters the ED state at the first sampling instant.

#### **Test Suite Information**

Name: ED

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#### ED-ED

#### **Test Result Information**

Result Type: Test Case Result

Parent: ED

Start Time: 26-Feb-2021 09:34:51 End Time: 26-Feb-2021 09:34:52

Outcome: Passed

Description:

State under test: ELECTRIC\_DRIVE (ED, 2)

Transition under test: ELECTRIC\_DRIVE (ED, 2) - ELECTRIC\_DRIVE (ED, 2)

#### **INPUT** conditions:

- RealSpeed < SpeedEDMax
- AccPedal < MaxAccMGU
- Fuel > fuelMin
- SOC > SOCmin

## **EXPECTED OUTPUT:**

The state should remain to ELECTRIC\_DRIVE (ED, 2).

#### **Test Case Information**

Name: ED-ED

Type: Baseline Test

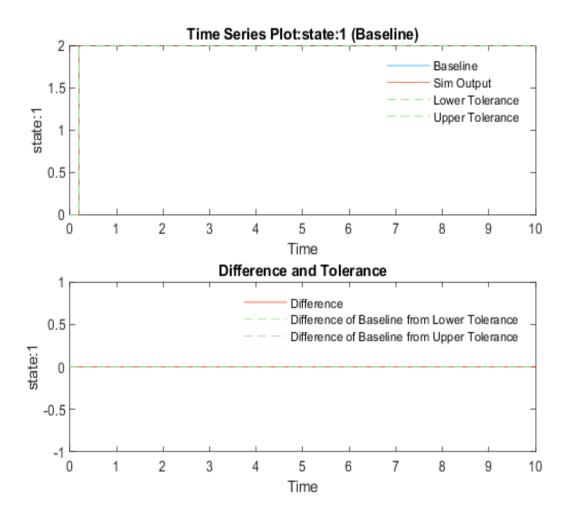
Baseline Name: ED\_ED\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\ED\_ED\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
Nume	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2	inter p	oyne .	t
state:1	0	0	0	0	0	double			double		Continuous	zoh	union	Link

ı	Name	Abs T	Rel T	Lead T	Lag T ol	Max Di ff	Data Type 1		Sample Ti me 1	Data Type 2	Units 2		Interp	Sync
ľ	state:1	0	. 0	0	0	0	double	   		double		Continuous	zoh	union



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## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL (

Mode:

Configuration Set: Configuration External Input Name: ED1.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\ED1.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

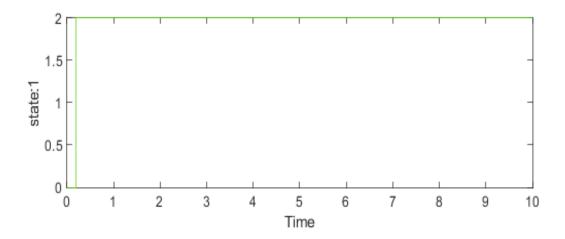
Solver Type: Variable-Step

Max Step Size: 0.2000000000000001 Simulation Start Time: 2021-02-26 09:34:51 Simulation Stop Time: 2021-02-26 09:34:52

Platform: PCWIN64

ı	Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
	state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **ED-Regen**

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

26-Feb-2021 09:34:52 Start Time:

End Time: 26-Feb-2021 09:34:53

Outcome: Passed

Description:

State under test: ELECTRIC\_DRIVE (ED, 2)

Transition under test: ELECTRIC\_DRIVE (ED, 2) - REGENERATIVE\_BRAKING (4)

#### **INPUT** conditions:

- RealSpeed < SpeedEDMax

- AccPedal < MaxAccMGU

- Fuel > fuelMin

- SOC > SOCmin

- BrakePedal: !=0 after 5s

#### **EXPECTED OUTPUT:**

The state should change to REGENERATIVE\_BRAKING (4).

#### **Test Case Information**

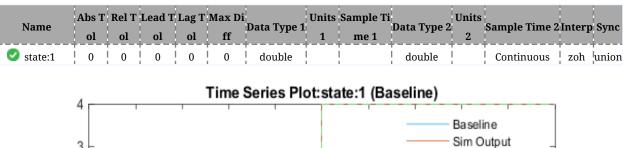
Name: ED-Regen Type: Baseline Test

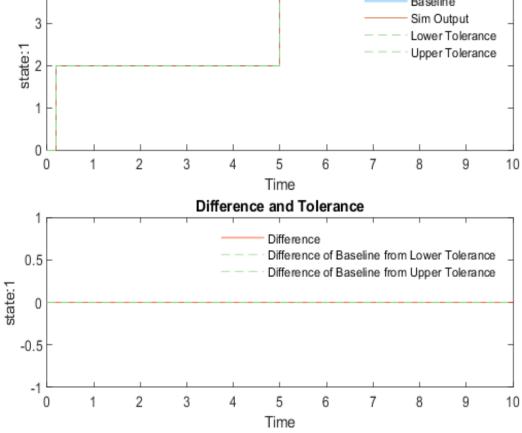
Baseline Name: ED Regen baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\ED\_Regen\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp S	Link to Pl
	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2		t
state:1	0	. 0	0	0	. 0	double			double	l	Continuous	zoh ur	nion Link





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## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration

External Input Name: ED2.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\ED2.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

 $Test \backslash FSM\_Model.slx$ 

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

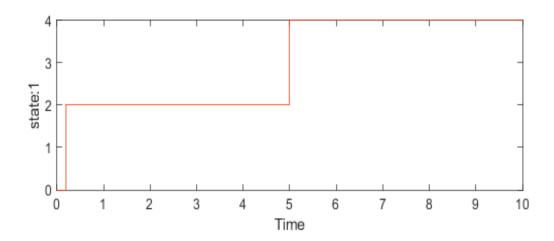
Solver Type: Variable-Step

Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:52 Simulation Stop Time: 2021-02-26 09:34:52

Platform: PCWIN64

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **ED-DEAD**

**Test Result Information** 

Result Type: Test Case Result

Parent: ED

Start Time: 26-Feb-2021 09:34:53 End Time: 26-Feb-2021 09:34:53

Outcome: Passed

Description:

State under test: ELECTRIC\_DRIVE (ED, 2)

Transition under test: ELECTRIC\_DRIVE (ED, 2) - DEAD (0)

#### **INPUT** conditions:

- AccPedal: uniformely increasing request

- Fuel < fuelMin

- SOC < SOCmin

- BrakePedal: 0

#### **EXPECTED OUTPUT:**

The state should change to DEAD (0).

#### **Test Case Information**

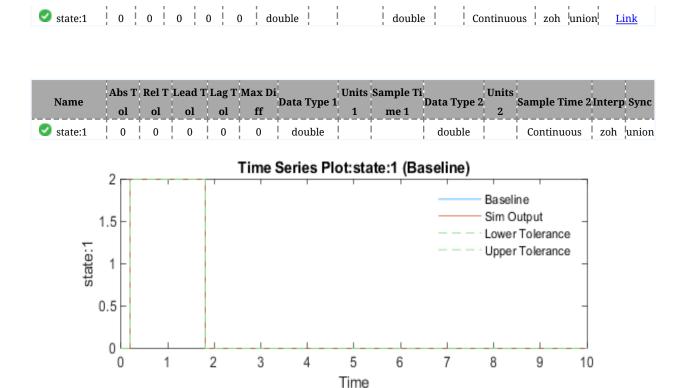
Name: ED-DEAD Type: Baseline Test

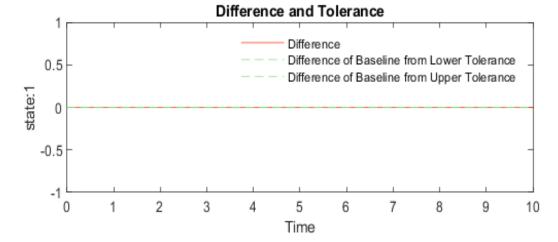
Baseline Name: ED\_Dead\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\ED\_Dead\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp S		Link to Plo
Name	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2	litter p 3	ync	t





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## **System Under Test Information**

Model: FSM\_Model
Release: Current
Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration

External Input Name: ED3.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\ED3.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

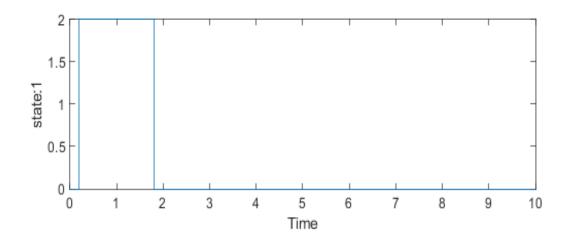
Solver Type: Variable-Step

Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:53 Simulation Stop Time: 2021-02-26 09:34:53

Platform: PCWIN64

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# ED-NoCharge

**Test Result Information** 

Result Type: Test Case Result

Parent: ED

Start Time: 26-Feb-2021 09:34:53 End Time: 26-Feb-2021 09:34:54

Outcome: Passed

Description:

State under test: ELECTRIC\_DRIVE (ED, 2)

Transition under test: ELECTRIC\_DRIVE (ED, 2) - NO\_CHARGE (4)

#### **INPUT** conditions:

- AccPedal < maxAccICE</li>
- Fuel > fuelMin
- SOC < SOCmin
- BrakePedal: 0

#### **EXPECTED OUTPUT:**

The state should change to NO\_CHARGE (1).

#### **Test Case Information**

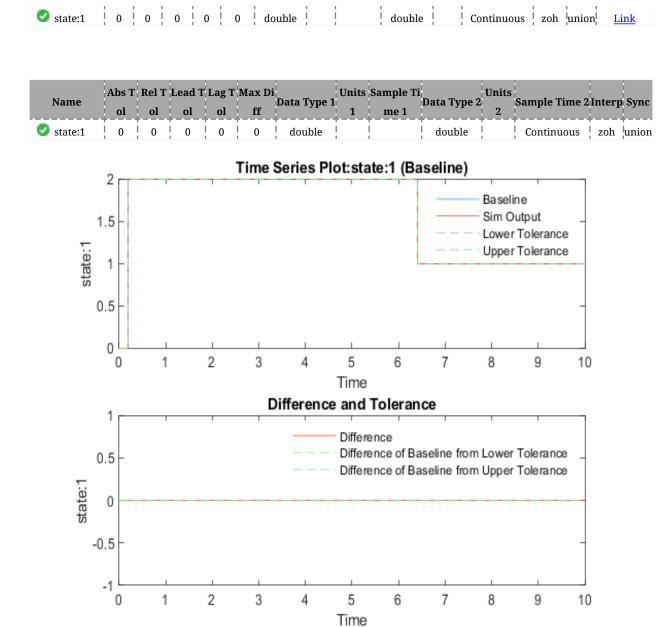
Name: ED-NoCharge Type: Baseline Test

Baseline Name: ED\_NoCharge\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM
Test\Baselines\ED\_NoCharge\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp S		Link to Plo
Name	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2	litter p 3	ync	t



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## **System Under Test Information**

Model: FSM\_Model
Release: Current
Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration

External Input Name: ED4.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\ED4.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

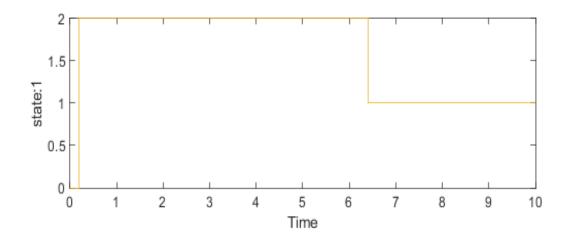
Solver Type: Variable-Step

Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:53 Simulation Stop Time: 2021-02-26 09:34:53

Platform: PCWIN64

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **ED-Combined**

**Test Result Information** 

Result Type: Test Case Result

Parent: ED

Start Time: 26-Feb-2021 09:34:54 End Time: 26-Feb-2021 09:34:55

Outcome: Passed

Description:

State under test: ELECTRIC\_DRIVE (ED, 2)

Transition under test: ELECTRIC\_DRIVE (ED, 2) - COMBINED (3)

#### **INPUT** conditions:

- AccPedal > MaxAccMGU OR RealSpeed > MaxSpeedMGU
- Fuel > fuelMin
- BrakePedal: 0
- SOC > SOCmin

#### **EXPECTED OUTPUT:**

The state should change to COMBINED (3).

#### NOTE:

This test is done in two iterations due to the presence of an OR among input conditions.

#### **Test Case Information**

Name: ED-Combined Type: Baseline Test

## Iteration1

#### **Test Result Information**

Result Type: Test Iteration Result

Parent: ED-Combined

Start Time: 26-Feb-2021 09:34:54 End Time: 26-Feb-2021 09:34:54

Outcome: Passed

#### **Test Case Information**

Name: Iteration1
Type: Baseline Test

Baseline Name: ED\_Comb\_baseline1.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

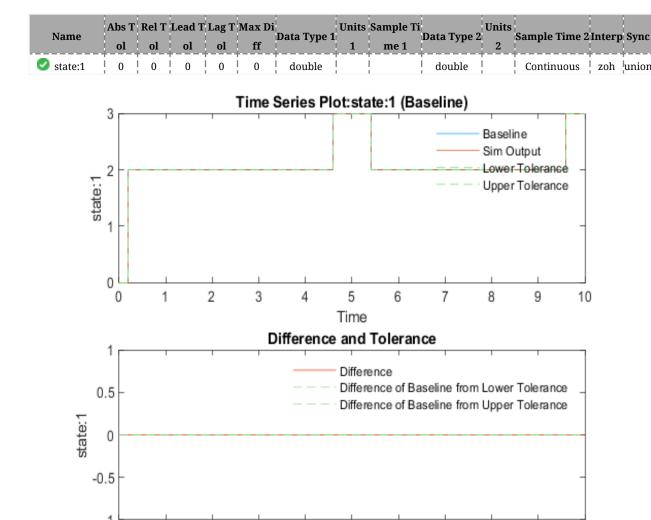
controller\Hybrid-controller\Test\FSM Test\Baselines\ED\_Comb\_baseline1.mat

## **Iteration Settings**

#### **Test Overrides**

Parameter Name	Value
ExternalInput	C:\Users\mordi\Desktop\Materiale
	Università\Compliance\hybrid-
	controller\Hybrid-controller\Test\FSM
	Test\Inputs\ED5.mat
Baseline	C:\Users\mordi\Desktop\Materiale
	Università\Compliance\hybrid-
	controller\Hybrid-controller\Test\FSM
	Test\Baselines\ED_Comb_baseline1.mat

Name	Abs Tol	i	1			1.	l i	•	Data Typ e 2	l	Sample Time 2	Interp Sy	Link to Plo t
state:1	0		. 0	. 0	0	double	I		double	 !	Continuous	zoh un	ion Link



5

Time

6

8

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10

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3

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2

#### **Simulation**

0

## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL

Mode:

Configuration Set: Configuration

External Input Name: ED5.mat

External Input File: C:\Users\mordi\Desktop\Materiale

0

Università\Compliance\hybrid-controller\Hybrid-

controller\Test\FSM Test\Inputs\ED5.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG VariableStepDiscrete

Solver Type: Variable-Step

Platform: PCWIN64

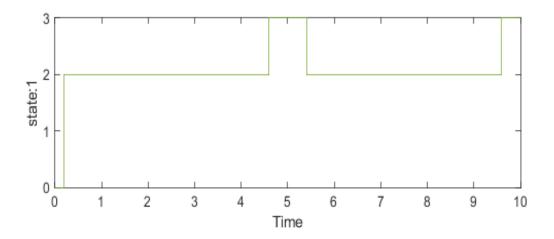
#### **Simulation Output**

Machine Name:

Solver Name:

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Iteration2**

## **Test Result Information**

Result Type: Parent: **Test Iteration Result** 

**ED-Combined** 

26-Feb-2021 09:34:54 Start Time:

End Time: 26-Feb-2021 09:34:55

Outcome: Passed

### **Test Case Information**

Name: Iteration2 Type: Baseline Test

Baseline Name: ED\_Comb\_baseline2.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\ED\_Comb\_baseline2.mat

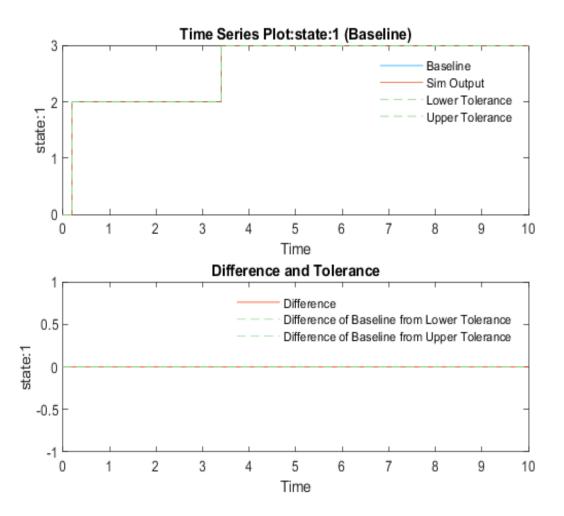
## **Iteration Settings**

#### **Test Overrides**

Parameter Name	Value
ExternalInput	C:\Users\mordi\Desktop\Materiale
	Università\Compliance\hybrid-
	controller\Hybrid-controller\Test\FSM
	Test\Inputs\ED6.mat
Baseline	C:\Users\mordi\Desktop\Materiale
	Università\Compliance\hybrid-
	controller\Hybrid-controller\Test\FSM
	Test\Baselines\ED_Comb_baseline2.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
Name	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2		Tartor P	0,110	t
state:1	0	0	0	0	0	double			double		Continuous	zoh	union	<u>Link</u>

Name	Abs T ol	Rel T ol	Lead T	Lag T	Max Di ff	Data Type 1	Sample Ti me 1	Data Type 2	Units 2	Sample Time 2 Interp Sync
state:1	0	0	0	0	0	double		double	l	Continuous zoh union



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### **Simulation**

## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL (

Mode:

Configuration Set: Configuration

External Input Name: ED6.mat

External Input File: C:\Users\mordi\Desktop\Materiale

Università\Compliance\hybrid-controller\Hybrid-

controller\Test\FSM Test\Inputs\ED6.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

 $controller \verb|\Hybrid-controller\Test\FSM|$ 

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

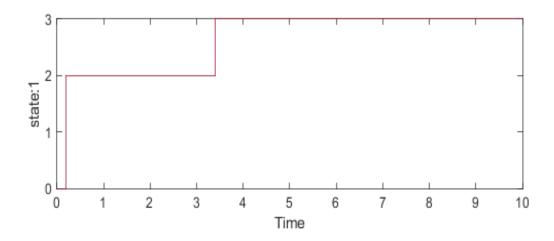
Max Step Size: 0.2000000000000001 Simulation Start Time: 2021-02-26 09:34:55 Simulation Stop Time: 2021-02-26 09:34:55

Platform: PCWIN64

#### **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## Combined

## **Test Result Information**

Result Type: Parent: Test Suite Result

<u>FSM\_test</u> 26-Feb-2021 09:34:55 Start Time:

End Time: 26-Feb-2021 09:34:58 Outcome: Total: 5, Passed: 5

Description:

From Combined to all other states. Initially, the FSM starts from DEAD, but soon enters the Combined state at the first sampling instant.

#### **Test Suite Information**

Name: Combined

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## **Combined-Combined**

#### **Test Result Information**

Result Type: Test Case Result

Parent: <u>Combined</u>

Start Time: 26-Feb-2021 09:34:55 End Time: 26-Feb-2021 09:34:56

Outcome: Passed

Description:

State under test: COMBINED (3)

Transition under test: COMBINED (3) - COMBINED (3)

#### **INPUT** conditions:

- RealSpeed>SpeedEDMax
- Fuel > fuelMin
- BrakePedal: 0
- SOC > SOCmin

#### **EXPECTED OUTPUT:**

The state should remain to COMBINED (3).

### **Test Case Information**

Name: Combined-Combined

Type: Baseline Test

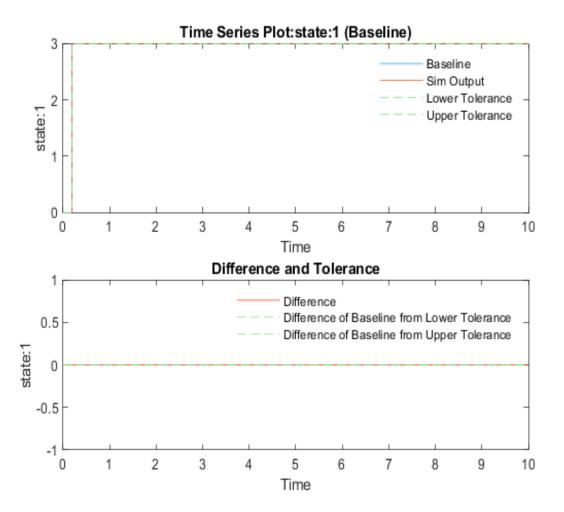
Baseline Name: Comb\_Comb\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM
Test\Baselines\Comb\_Comb\_baseline.mat

	Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
Nume	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2		0,110	t	
	state:1	0	0	0	0	0	double			double		Continuous	zoh	union	<u>Link</u>

Name		Abs T	Rel T	1	i	Max Di ff	Data Type 1	Sample Ti me 1	Data Type 2	Units 2	Sample Time 2 Interp Sync
🕏 state:	1	0	0	0	0	0	double	İ	double		Continuous zoh union



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### **Simulation**

## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL

Mode:

Configuration Set: Configuration External Input Name: Comb1.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Comb1.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

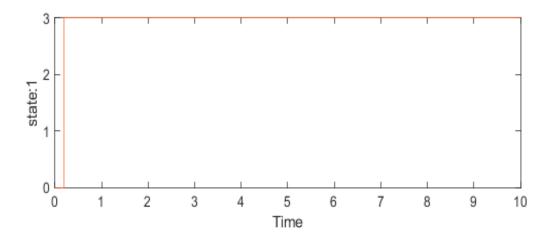
Max Step Size: 0.2000000000000001 Simulation Start Time: 2021-02-26 09:34:55 Simulation Stop Time: 2021-02-26 09:34:55

Platform: PCWIN64

#### **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# **Combined-Regen**

## **Test Result Information**

Result Type: Parent: Test Case Result

Combined 26-Feb-2021 09:34:56 Start Time:

End Time: 26-Feb-2021 09:34:56

Outcome: Passed

Description:

State under test: COMBINED (3)

Transition under test: COMBINED (3) - REGENERATIVE\_BRAKING(4)

### **INPUT conditions:**

- RealSpeed > SpeedMaxED

- Fuel > fuelMin

- BrakePedal: != 0 after t = 5s

- SOC > SOCmin

#### **EXPECTED OUTPUT:**

The state should change to REGENERATIVE\_BRAKING (4).

#### **Test Case Information**

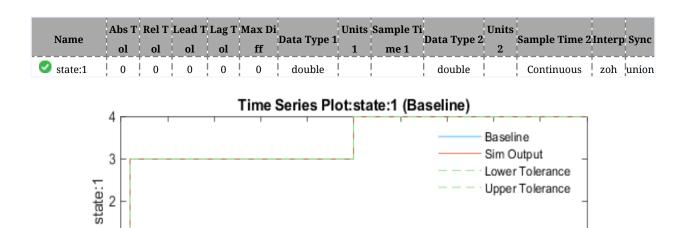
Name: Combined-Regen Type: Baseline Test

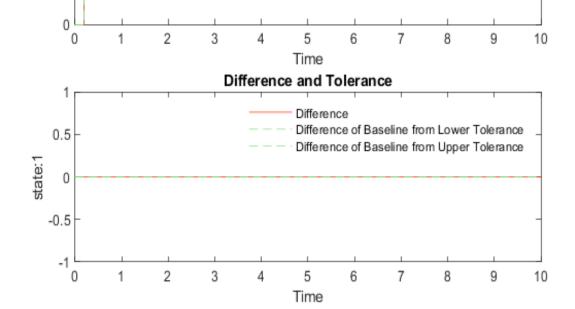
Baseline Name: Comb\_Regen\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM
Test\Baselines\Comb\_Regen\_baseline.mat

Name	Abs Tol	1				Data Typ e 1	Î	1.	Units 2	Sample Time 2	Interp		Link to Plo t
🕏 state:1	0	0	0	0	0	double		double	I	Continuous	zoh i	union	<u>Link</u>





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### **Simulation**

1

**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Comb2.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Comb2.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

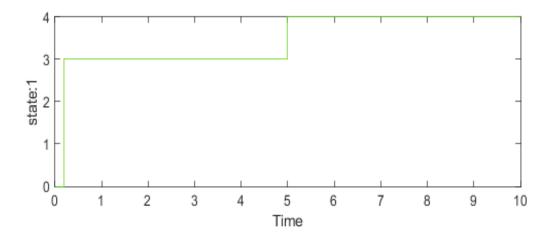
Platform: PCWIN64

### **Simulation Output**

Machine Name:

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Combined-DEAD**

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

Combined 26-Feb-2021 09:34:56 Start Time:

End Time: 26-Feb-2021 09:34:57

Outcome: Passed

Description:

State under test: COMBINED (3)

Transition under test: COMBINED (3) - DEAD (0)

#### **INPUT** conditions:

- Fuel < fuelMin

- SOC < SOCmin

#### **EXPECTED OUTPUT:**

The state should change to DEAD (0).

#### **Test Case Information**

Name: Combined-DEAD Type: Baseline Test

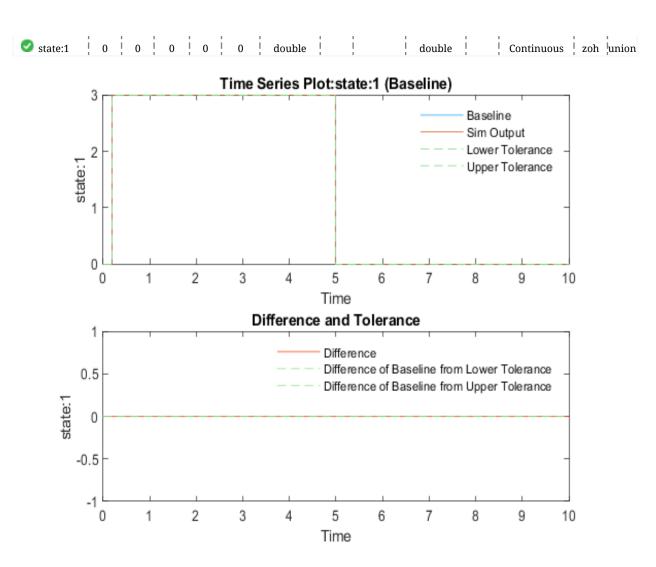
Baseline Name: Comb\_Dead\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM
Test\Baselines\Comb\_Dead\_baseline.mat

Name	Abs Tol		i	i		Data Typ e 1		Î	11	Units 2	Sample Time 2	Interp		Link to Plo t
state:1	. 0	0	0	0	0	double	 		double		Continuous	zoh	union	<u>Link</u>

1		Abs T Rel T	Lead T Lag T	Max Di		Sample Ti			
1	Name	ol ol	ol ol	ff Dat	ta Type 1	me 1	Data Type 2	Sample Time 2 Interp Syn	c



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#### **Simulation**

## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal Override SIL or PIL

Mode:

Configuration Set: Configuration External Input Name: Comb3.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Comb3.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

0

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

 $Test \ FSM\_Model.slx$ 

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

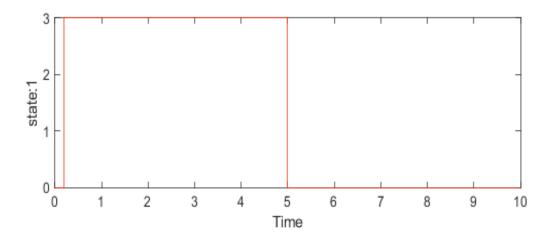
Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:56 Simulation Stop Time: 2021-02-26 09:34:57

Platform: PCWIN64

**Simulation Output** 

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## **Combined-ED**

## **Test Result Information**

Result Type: Parent: Test Case Result

Combined 26-Feb-2021 09:34:57 Start Time:

End Time: 26-Feb-2021 09:34:58

Outcome: Passed

Description:

State under test: COMBINED (3)

Transition under test: COMBINED (3) - ELECTRIC\_DRIVE (ED, 2)

### **INPUT conditions:**

- RealSpeed < SpeedEDMax at t = 5s

- AccPedal < MaxAccMGU after t = 5s

- BrakePedal: 0

- SOC > SOCmin

#### **EXPECTED OUTPUT:**

The state should change to ELECTRIC\_DRIVE (ED, 2).

#### **Test Case Information**

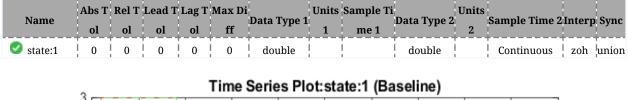
Name: Combined-ED Type: Baseline Test

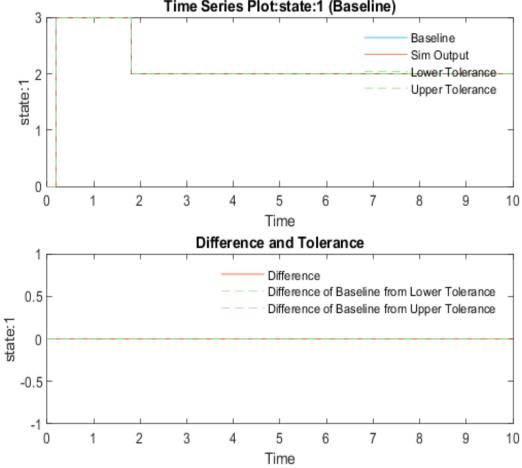
Baseline Name: Comb\_ED\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\Comb\_ED\_baseline.mat

Name						Data Typ e 1	i i	Ť	11	Units 2	Sample Time 2	Interp		Link to Plo t
state:1	0	0	0	0	0	double	l		double	l	Continuous	zoh	union	<u>Link</u>





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### **Simulation**

**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Comb4.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Comb4.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

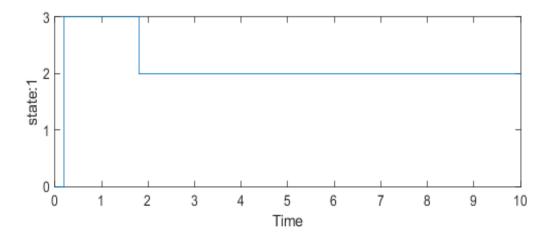
Solver Type: Variable-Step

Platform: PCWIN64

### **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# **Combined-NoCharge**

## **Test Result Information**

Result Type: Parent: Test Case Result

Combined 26-Feb-2021 09:34:58 Start Time:

End Time: 26-Feb-2021 09:34:58

Outcome: Passed

Description:

Combined to No Charge state transition check:

-SOC < SOCMin

-fuel > fuelMin

-AccPedal < maxAccICE

The state should pass from Combined to No Charge

State under test: COMBINED (3)

Transition under test: COMBINED (3) - NO\_CHARGE (1)

**INPUT** conditions:

- AccPedal < maxAccICE
- BrakePedal: 0
- Fuel > fuelMin
- SOC < SOCmin

#### **EXPECTED OUTPUT:**

The state should change to NO\_CHARGE (1).

**Test Case Information** 

Combined-NoCharge Name:

Baseline Test Type:

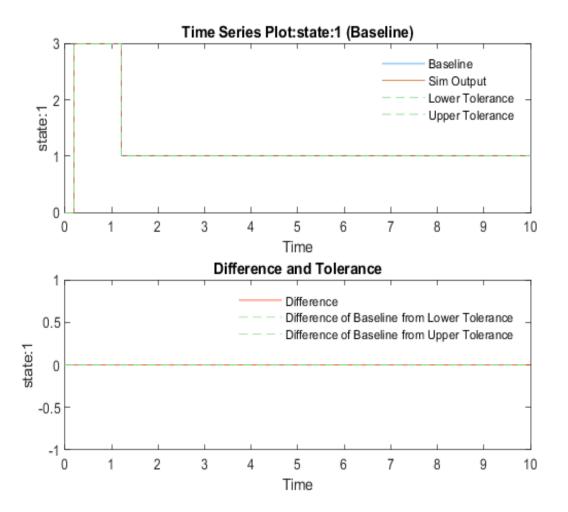
 $Comb\_NoCharge\_baseline.mat$ Baseline Name:

C:\Users\ivane\Documents\GitHub\hybrid-controller\Hybrid-controller\Test\FSM Baseline File:

Test\Baselines\Comb\_NoCharge\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2		5,110	t
state:1	0	0	0	0	0	double		İ	double		Continuous	zoh u	ınion	<u>Link</u>

Name	Abs T	Rel T	Lead T	i	Max Di ff	Data Type 1		Sample Ti me 1	Data Type 2	Units 2	Sample Time 2	Interp Sync
state:1	. 0	. 0	. O	. 0	. 0	double	ļ	<u> </u>	double	i	Continuous	zoh union



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### **Simulation**

## **System Under Test Information**

Model: FSM\_Model
Release: Current
Simulation Mode: normal

Override SIL or PIL

Mode:

Configuration Set: Configuration External Input Name: Comb5.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Comb5.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

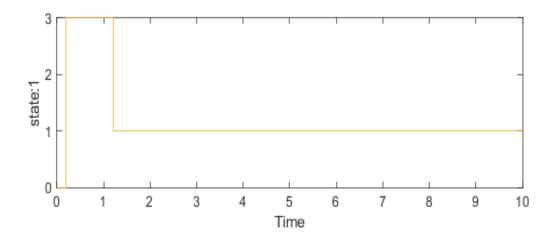
Max Step Size: 0.20000000000000001 Simulation Start Time: 2021-02-26 09:34:58 Simulation Stop Time: 2021-02-26 09:34:58

Platform: PCWIN64

#### **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



## Regen

## **Test Result Information**

Result Type: Parent: Test Suite Result

<u>FSM\_test</u> 26-Feb-2021 09:34:58 Start Time:

End Time: 26-Feb-2021 09:35:01 Outcome: Total: 5, Passed: 5

Description:

From Regenerative Braking to all other states. Initially, the FSM starts from DEAD, but soon enters the Regen state at the first sampling instant.

#### **Test Suite Information**

Name: Regen

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## Regen-Regen

#### **Test Result Information**

Result Type: Test Case Result

Parent: Regen

Start Time: 26-Feb-2021 09:34:58 End Time: 26-Feb-2021 09:34:59

Outcome: Passed

Description:

State under test: REGENERATIVE\_BRAKING (4)

Transition under test: REGENERATIVE\_BRAKING (4) - REGENERATIVE\_BRAKING (4)

#### **INPUT** conditions:

- BrakePedal > 0

#### **EXPECTED OUTPUT:**

The state should remain to REGENERATIVE\_BRAKING (4).

## **Test Case Information**

Name: Regen-Regen Baseline Test Type:

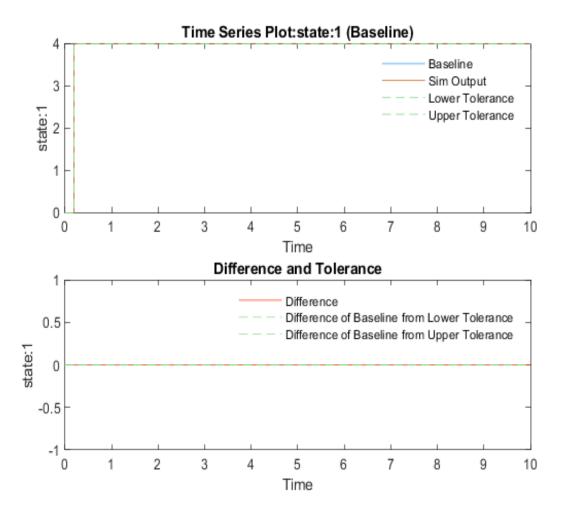
Baseline Name: Regen\_Regen\_baseline.mat

Baseline File:

C:\Users\ivane\Documents\GitHub\hybrid-controller\Hybrid-controller\Test\FSM Test\Baselines\Regen\_Regen\_baseline.mat

	Name	Abs Tol	1			1	1.	•	Data Typ e 2		Sample Time 2	Interp		Link to Plo t
ĺ	state:1	0	0	0	0	0	double		double	I	Continuous	zoh	union	<u>Link</u>

Name	Abs T	Rel T ol	Lead T	Lag T	Max Di ff	Data Type 1		Sample Ti me 1	Data Type 2	Units 2	Sample Time 2 Interp Sync
state:1	0	0	0	0	0	double			double		Continuous zoh union



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### **Simulation**

## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL (

Mode:

Configuration Set: Configuration External Input Name: Regen1.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Regen1.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

Solver Type: Variable-Step

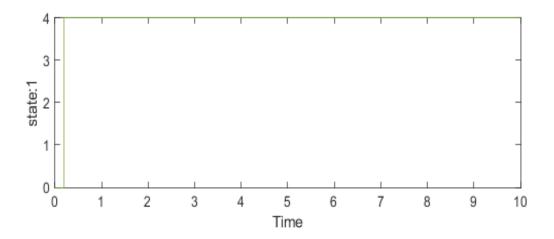
Max Step Size: 0.2000000000000001 Simulation Start Time: 2021-02-26 09:34:58 Simulation Stop Time: 2021-02-26 09:34:58

Platform: PCWIN64

#### **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# **Regen-DEAD**

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

Regen 26-Feb-2021 09:34:59 Start Time:

End Time: 26-Feb-2021 09:34:59

Outcome: Passed

Description:

State under test: REGENERATIVE\_BRAKING (4)

Transition under test: REGENERATIVE\_BRAKING (4) - DEAD (0)

### **INPUT** conditions:

- AccPedal > 0 at t = 5 s

- BrakePedal: 0 at t = 5 s

- Fuel < fuelMin

- SOC < SOCmin

#### **EXPECTED OUTPUT:**

The state should change to DEAD (0).

#### **Test Case Information**

Name: Regen-DEAD Type: Baseline Test

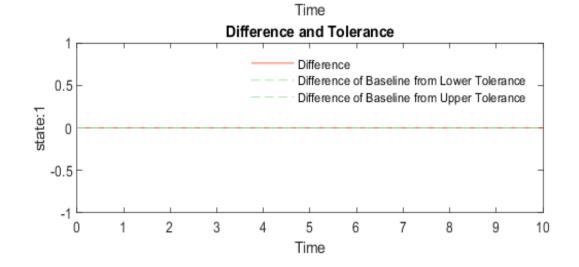
Baseline Name: Regen\_Dead\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM
Test\Baselines\Regen\_Dead\_baseline.mat

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
Nume	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2	interp sync	t	
state:1	0	0	0	0	0	double	i		double		Continuous	zoh	union	<u>Link</u>





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### **Simulation**

**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Regen2.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Regen2.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Solver Name: VariableStepDiscrete
Solver Type: Variable-Step

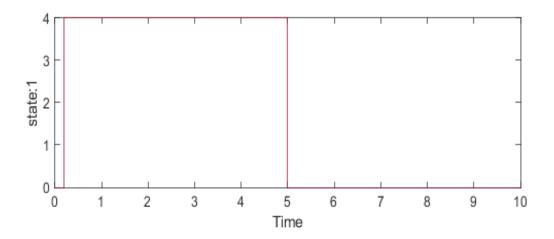
Platform: PCWIN64

**Simulation Output** 

Machine Name:

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



# Regen-ED

## **Test Result Information**

Result Type: Parent: Test Case Result

Regen 26-Feb-2021 09:34:59 Start Time:

End Time: 26-Feb-2021 09:35:00

Outcome: Passed

Description:

State under test: REGENERATIVE\_BRAKING (4)

Transition under test: REGENERATIVE\_BRAKING (4) - ELECTRIC\_DRIVE (ED, 2)

## **INPUT conditions:**

- RealSpeed < SpeedEDMax

- AccPedal: !=0 at t=5 s

- BrakePedal: 0 at t = 5 s

- SOC < SOCmin for a while, then SOC>SOCmin

#### **EXPECTED OUTPUT:**

The state should change to ELECTRIC\_DRIVE (ED, 2).

#### **Test Case Information**

Name: Regen-ED Type: Baseline Test

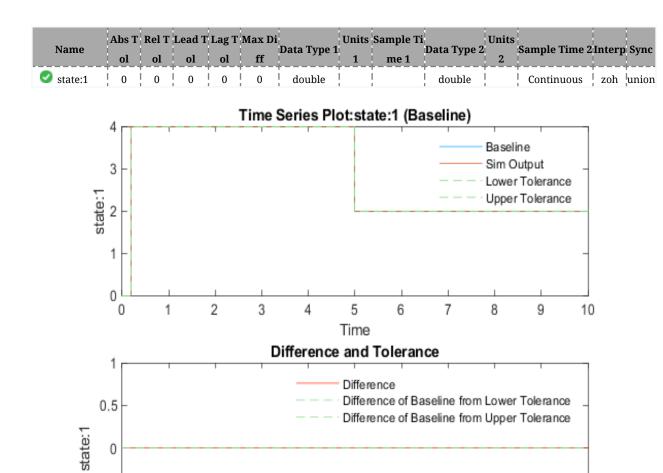
Baseline Name: Regen\_ED\_baseline.mat

Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM Test\Baselines\Regen ED baseline.mat

#### **Baseline Comparison**

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp		Link to Plo
Nume	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2	interp sync	t	
state:1	0	0	0	0	0	double	i		double		Continuous	zoh	union	<u>Link</u>



5

Time

6

8

9

10

7

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2

## **Simulation**

-0.5

0

**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Regen3.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Regen3.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

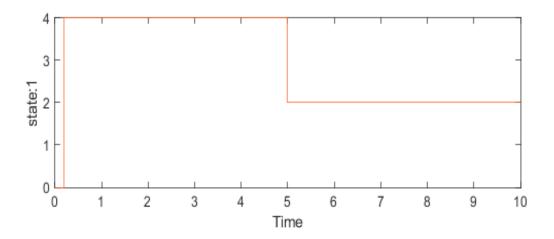
Solver Type: Variable-Step

Platform: PCWIN64

## **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Interp Sync	
state:1	double	l	Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double		Continuous	zoh	union



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# Regen-NoCharge

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

Regen 26-Feb-2021 09:35:00 Start Time:

End Time: 26-Feb-2021 09:35:01

Outcome: Passed

Description:

State under test: REGENERATIVE\_BRAKING (4)

Transition under test: REGENERATIVE\_BRAKING (4) - NO\_CHARGE (1)

## **INPUT** conditions:

- AccPedal: !=0 at t=5 s

- BrakePedal: 0 at t = 5 s

- Fuel > fuelMin

- SOC < SOCmin

#### **EXPECTED OUTPUT:**

The state should change to NO\_CHARGE (1).

#### **Test Case Information**

Name: Regen-NoCharge Type: Baseline Test

Baseline Name: Regen\_NoCharge\_baseline.mat

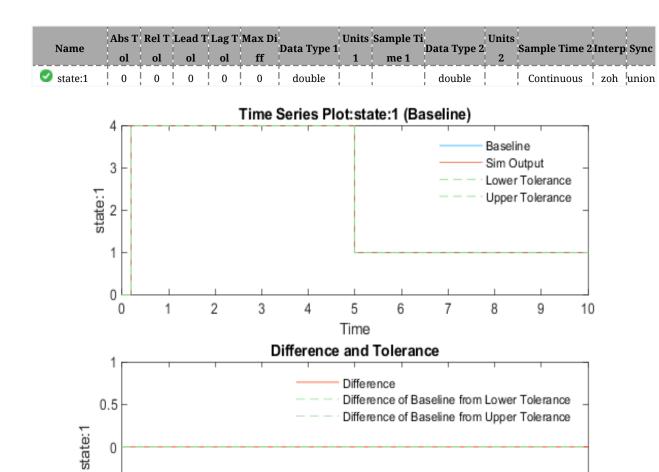
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

 $controller \verb|\Hybrid-controller\Test\FSM|$ 

Test\Baselines\Regen\_NoCharge\_baseline.mat

#### **Baseline Comparison**

Name	Abs Tol	1				Data Typ e 1	i i	Î	1.	Units 2	Sample Time 2	Interp		Link to Plo t
🕏 state:1	0	0	0	0	0	double	I		double	I	Continuous	zoh	union	<u>Link</u>



5

Time

6

8

9

10

7

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2

## **Simulation**

-0.5

0

**System Under Test Information** 

Model: FSM\_Model

Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Regen4.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Regen4.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

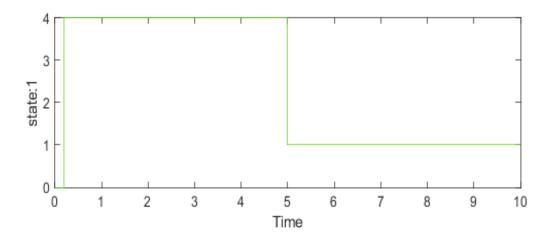
Solver Type: Variable-Step

Platform: PCWIN64

## **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double		Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync
state:1	double	 	Continuous	zoh	union



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# Regen-Combined

## **Test Result Information**

Result Type: Parent: **Test Case Result** 

Regen 26-Feb-2021 09:35:01 Start Time:

End Time: 26-Feb-2021 09:35:01

Outcome: Passed

Description:

State under test: REGENERATIVE\_BRAKING (4)

Transition under test: REGENERATIVE\_BRAKING (4) - COMBINED (3)

## **INPUT conditions:**

- RealSpeed > SpeedMaxMGU

- AccPedal: !=0 at t=5 s

- BrakePedal: 0 at t = 5 s

- Fuel > fuelMin

- SOC > SOCmin

#### **EXPECTED OUTPUT:**

The state should change to COMBINED (3).

#### **Test Case Information**

Name: Regen-Combined Type: Baseline Test

Baseline Name: Regen\_Combined\_baseline.mat

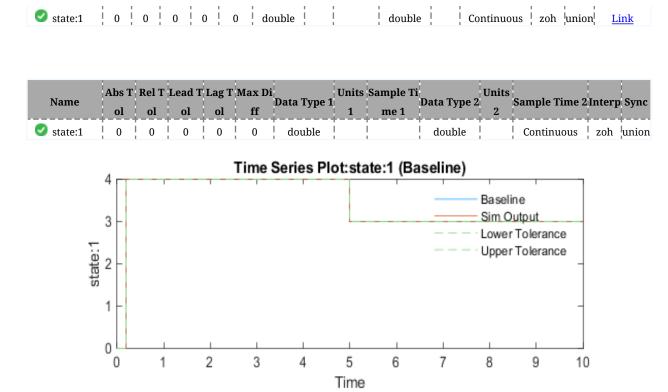
Baseline File: C:\Users\ivane\Documents\GitHub\hybrid-

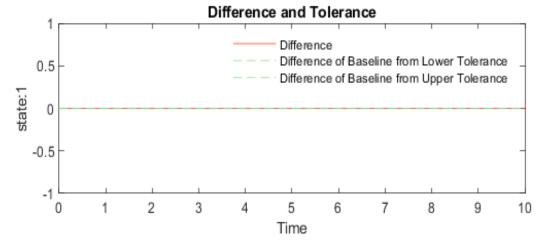
controller\Hybrid-controller\Test\FSM

Test\Baselines\Regen\_Combined\_baseline.mat

## **Baseline Comparison**

Name	Abs	Rel T	Lead	Lag	Max D	Data Typ	Units	Sample	Data Typ	Units	Sample Time	Interp S		Link to Plo
	Tol	ol	Tol	Tol	iff	e 1	1	Time 1	e 2	2	2	litter p 3	ync	t





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#### **Simulation**

## **System Under Test Information**

Model: FSM\_Model Release: Current Simulation Mode: normal

Override SIL or PIL 0

Mode:

Configuration Set: Configuration External Input Name: Regen5.mat

External Input File: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\Inputs\Regen5.mat

Start Time: 0 Stop Time: 10

Checksum: 548314369 3126024374 1648386796 2958348115

Simulink Version: 10.2 Model Version: 1.3 Model Author: mordi

Date: Tue Feb 16 15:30:18 2021

User ID: ivane

Model Path: C:\Users\ivane\Documents\GitHub\hybrid-

controller\Hybrid-controller\Test\FSM

Test\FSM\_Model.slx DESKTOP-MPG8QDG

Machine Name: DESKTOP-MPG8QDG Solver Name: VariableStepDiscrete

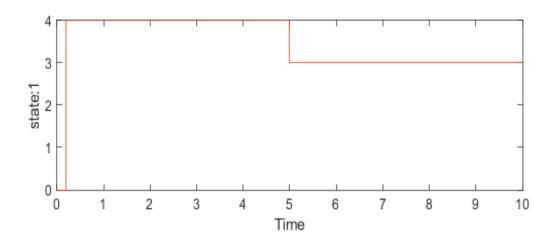
Solver Type: Variable-Step

Platform: PCWIN64

#### **Simulation Output**

Name	Data Type	Units	Sample Time	Interp	Sync	Link to Plo t
state:1	double	 	Continuous	zoh	union	<u>Link</u>

Name	Data Type	Units	Sample Time	Interp	Sync	
state:1	double		Continuous	zoh	union	



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