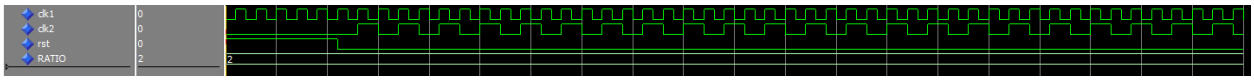
Michelle Emamdie
Lab 4
EEL 4712C

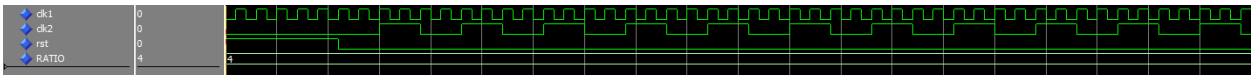
Lab 4 : Sequential Logic and Finite State Machines

Part 1 – Clock Generator

Ratio = 2

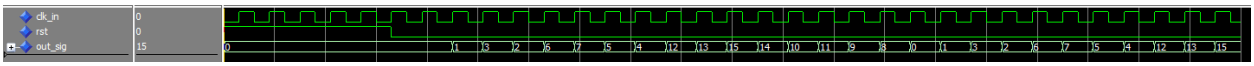


Ratio = 4

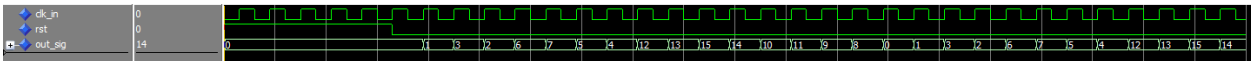


Part 2 – 4-bit Gray code counter

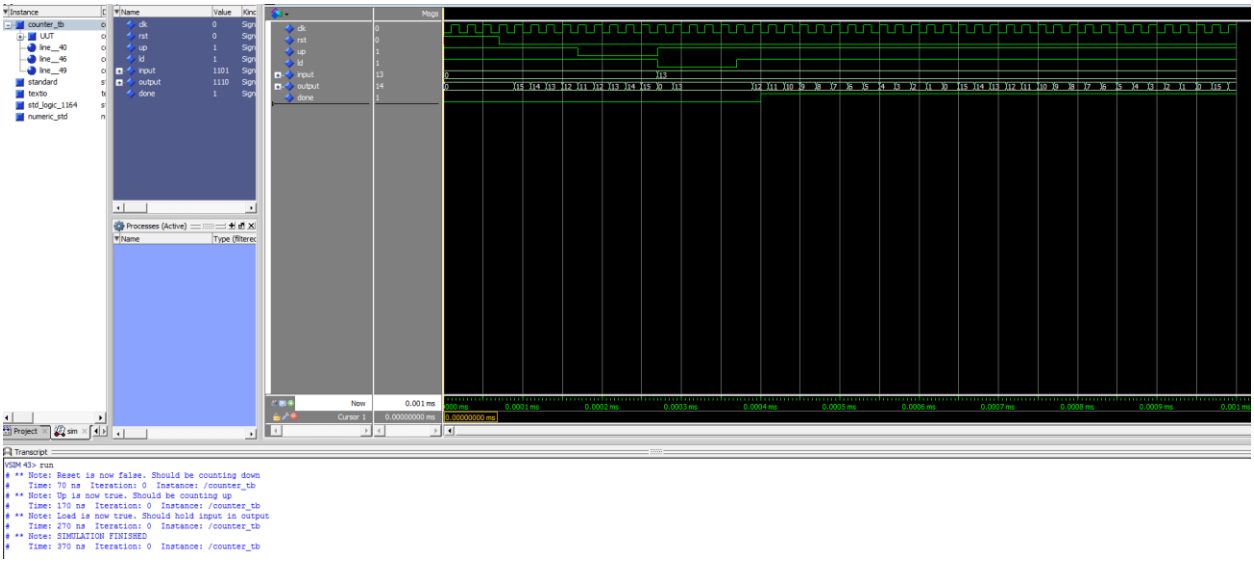
Gray Counter : 1 Process



Gray Counter : 2 Processes



Part 3 – 4-bit Up/Down Counter with Load



Part 4 – Top Level

The top level instantiates a Gray 2 counter, a 4 bit up/down counter, a clock generator, and 4 LEDs. The up for the 4 bit up down counter maps to button 1, and the load maps to button 0, and the button for the clock generator maps to button 2. Then I mapped the reset to switch 0 and the input for the counters are mapped to switches 9 down to 6.