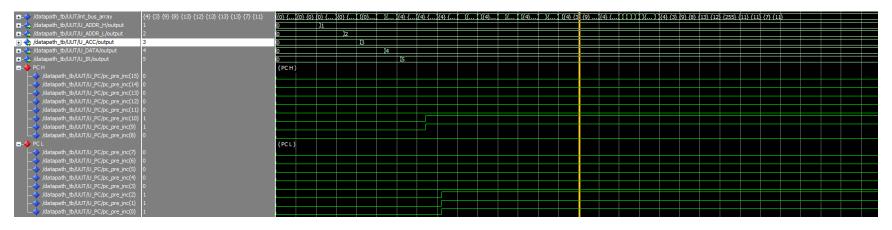


The test bench writes values to each of the registers. Since I combined PC H and PC L into one entity I had to pull their separate signals. The ALU output when enabled transfers the output from the ALU into the ALU register. Then it finishes counting. RAM is the input to the controller.



Here are the signals for PC H and PC L notice that they are where 6 and 7 would be respectively.

	{4} {3} {9} {8} {13} {12} {255} {255} {255} {7} {11}	{ <del>4</del> } {3}	{4}}	4} {3	<b>[4]</b>	3} {9} {	} {13} {12} .	{4} {:	} {9} {		(4)	3	{4} {3} {9	<b>{8} {13</b>	} {12} {	255} {	11} {11}	-{7}{11	}			
- /datapath_tb/UUT/int_bus_array(2)	9	9																				
/datapath_tb/UUT/U_ADDR_H/output	1	1																				
/datapath_tb/UUT/U_ADDR_L/output	2	2																				
	3	3																				
	4	4																				
- /datapath_tb/UUT/U_IR/output	5	5																				
<b>II</b> - <b>◇</b> PC H		(PCH)																				
₩		(PCL)																				
- /datapath_tb/UUT/U_SP_L/output	8	8																				
- /datapath_tb/UUT/U_SP_H/output	9	9																				
/datapath_tb/UUT/U_B_REG/output	11	11																				
III  III  III  III  III  III  III		( ALU OUT	)																			
	12	0	(1	2																		
- /datapath_tb/UUT/U_X_H/output	13	0			(13																	
★ /datapath_tb/UUT/U_STATUS/output	0	0																				
•																						

In this last picture the registers write back to the bus.