

# CS4341: Bec-Man System Design

## The MetaStable Flip-Flops

Carson Page

Husna Chaudhary

Fall 2019

# Contents

<b>1</b>	<b>System Listing</b>	<b>2</b>
1.1	Defined Types . . . . .	2
1.2	Module Descriptions . . . . .	2
1.3	Input List . . . . .	2
1.4	Output List . . . . .	3

# 1 System Listing

## 1.1 Defined Types

We defined multiple new types to assist in development. These are replicated commonly in the next sections.

Type Name	Width	Description
s_width_t	clogb2(SCREEN_WIDTH)	Generated type that fits the visible screen width.
s_height_t	clogb2(SCREEN_HEIGHT)	Generated type that fits the visible screen height.
coord_t	s_width_t + s_height_t	XY Coordinate Pair.
rgb_t	[23:0]	Packed struct representing 8:8:8 RGB color.

## 1.2 Module Descriptions

Each used module is documented here with a high-level description and its function. Detailed port listings follow in the next section.

## 1.3 Input List

Each module has its input(s) name, type, and description listed in a table below. Inputs that are prevalent and share the same semantic meaning are in Table 1.

Table 1: **Common Inputs**

Name	Type	Description
i_clk	logic	Global system clock tree. All logic is driven off of this or a derived clock from a PLL / MMCM module.
i_rst	logic	Active high reset. Module must reset registers and/or outputs to known base state on activation.
i_en	logic	Active high clock enable. Registers part of the data path should only update when activated. Control registers or edge detect registers <i>may</i> not be disabled on a low if necessary for proper function.

Table 2: **Video Timing Generator (vtg)**

Name	Type	Description
ACTIVE_WIDTH	parameter	The width of the visible area of the display.
ACTIVE_HEIGHT	parameter	The height of the visible area of the display.
V_FRONT_PORCH	parameter	Vertical front porch of the timing spec in lines.
V_BACK_PORCH	parameter	Vertical back porch of the timing spec in lines.
V_PULSE	parameter	Length of vertical sync pulse in lines.
V_POL	parameter	Defines if the module outputs a active high/low vertical sync pulse.
H_FRONT_PORCH	parameter	Horizontal front porch of the timing spec in pixels.
H_BACK_PORCH	parameter	Horizontal back porch of the timing spec in pixels.
H_PULSE	parameter	Length of horizontal sync pulse in pixels.
H_POL	parameter	Defines if the module outputs a active high/low horizontal sync pulse.

Table 3: **Game State Engine (game\_state)**

Name	Type	Description
i_joystick	logic [3:0]	Joystick Input, lowest bit represents the left direction. Successive bits represent the next cardinal direction in a counter-clockwise manner. The zero vector represents no input.

## 1.4 Output List