## Indian Institute of Technology (IIT-Bombay)

## AUTUMN Semester, 2024 COMPUTER SCIENCE AND ENGINEERING

CS231: Digital Logic Design + Computer Architecture Lab Lab 3

Full Marks: 100

Time allowed:  $(3 + \epsilon)$  hours

Students who do not follow the naming convention will be awarded no marks. Also, you cannot change the module names and ports for the already defined modules, but you can add your own supporting modules as many as you like. You cannot create any new files.

Add the supporting modules in the same files

- 1. In this lab, you need to create a 32-bit Sequential Karatsuba multiplier, given a single instance of a 16-bit Karatsuba multiplier (Note that having only one multiplier creates a need to reuse it for multiplications). The goal is to understand how to reuse and time-multiplex a given hardware resource to optimize the hardware footprint of a circuit. Follow the instructions given below:
  - 1. The top module of your design will be iterative\_karatsuba\_32\_16(clk, rst, enable, A, B, C). You will have the following submodules instantiated in this top module:
    - Two registers T and Z of 32 and 64 bits. Use the module reg\_with\_enable with proper parameters.
    - A module instantiation of iterative\_karatsuba\_datapath. This is a purely combinational datapath.
    - A module instantiation of iterative\_karatsuba\_control. This is a sequential circuit and the controller of your design.

You have to properly connect all the modules.

- 2. Define the module iterative\_karatsuba\_datapath. All the input and output signals are provided. So you have to instantiate the Muxes and other datapath components.
- 3. Define the module iterative\_karatsuba\_control. All the control inputs and outputs are given, and states are defined. You only have to populate the control signals.

Note: Datapath refers to the combinational part of the sequential circuit and the control refers to the sequential logic part.

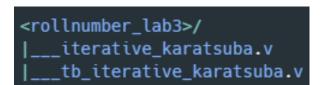


Figure 1: Submission Format