UART configuration

Modurile eUSCI pt UART:

param moduleInstance is the instance of the eUSCI A (UART) module.

Valid parameters vary from part to part, but can include:

- \b EUSCI\_A0\_BASE

- \b EUSCI\_A1\_BASE

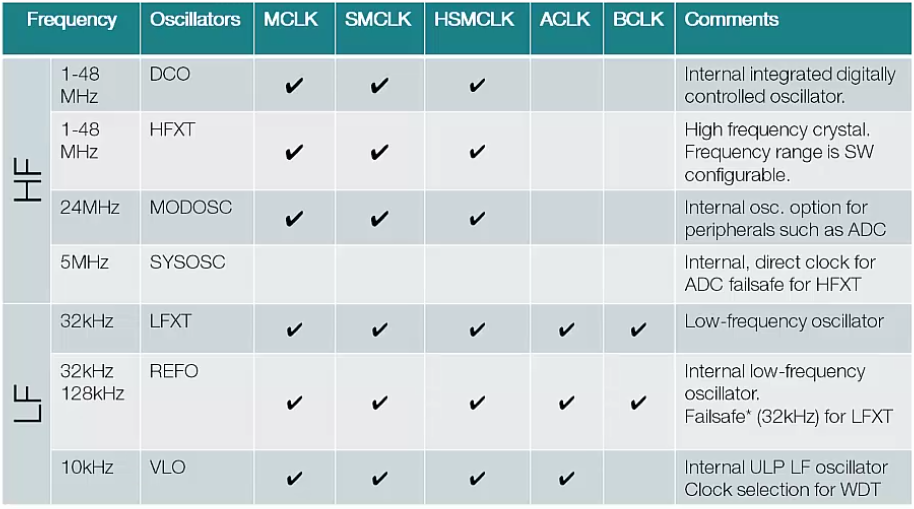
- \b EUSCI\_A2\_BASE

- \b EUSCI\_A3\_BASE

MSP432 Clock System

Are 5 tipuri de clock din 7 surse diferite ( 2 externe si 5 interne).

Are o gama variata de frecvente de operare intre 10kHz si 48 MHz.



param selectClockSource selects Clock source. Valid values are

//! - \b EUSCI\_A\_UART\_CLOCKSOURCE\_SMCLK

//! - \b EUSCI\_A\_UART\_CLOCKSOURCE\_ACLK

Clock Prescaler

//! \param clockPrescalar is the value to be written into UCBRx bits

FirstModeRegister and SecondModeRegister

//! \param firstModReg is First modulation stage register setting. This

//! value is a pre-calculated value which can be obtained from the Device

//! User Guide.This value is written into UCBRFx bits of UCAxMCTLW.

//! \param secondModReg is Second modulation stage register setting.

//! This value is a pre-calculated value which can be obtained from the

//! Device User Guide. This value is written into UCBRSx bits of

//! UCAxMCTLW.

Paritatea

A **parity bit** is a single [bit](http://www.computerhope.com/jargon/b/bit.htm) added to a [binary](http://www.computerhope.com/jargon/b/binary.htm) data transmission used to indicate if whether the 0's and 1's within that data transmission is an even or odd number. The parity bit is used in [parity](http://www.computerhope.com/jargon/p/parity.htm) error checking to find errors that may occur during data transmission.

//! \param parity is the desired parity. Valid values are

//! - \b EUSCI\_A\_UART\_NO\_PARITY [Default Value],

//! - \b EUSCI\_A\_UART\_ODD\_PARITY,

//! - \b EUSCI\_A\_UART\_EVEN\_PARITY

Controlul directiei de schimb de date din Shift Register

//! \param msborLsbFirst controls direction of receive and transmit shift

//! register. Valid values are

//! - \b EUSCI\_A\_UART\_MSB\_FIRST

//! - \b EUSCI\_A\_UART\_LSB\_FIRST [Default Value]

Biti de stop

Stop bits sent at the end of every character allow the receiving signal hardware to detect the end of a character and to resynchronise with the character stream. Electronic devices usually use one stop bit.

//! \param numberofStopBits indicates one/two STOP bits

//! Valid values are

//! - \b EUSCI\_A\_UART\_ONE\_STOP\_BIT [Default Value]

//! - \b EUSCI\_A\_UART\_TWO\_STOP\_BITS

Modul UART

\param uartMode selects the mode of operation

//! Valid values are

//! - \b EUSCI\_A\_UART\_MODE [Default Value],

//! - \b EUSCI\_A\_UART\_IDLE\_LINE\_MULTI\_PROCESSOR\_MODE,

//! - \b EUSCI\_A\_UART\_ADDRESS\_BIT\_MULTI\_PROCESSOR\_MODE,

//! - \b EUSCI\_A\_UART\_AUTOMATIC\_BAUDRATE\_DETECTION\_MODE

Generarea de BAUD

//! \param overSampling indicates low frequency or oversampling baud

//! generation

//! Valid values are

//! - \b EUSCI\_A\_UART\_OVERSAMPLING\_BAUDRATE\_GENERATION

//! - \b EUSCI\_A\_UART\_LOW\_FREQUENCY\_BAUDRATE\_GENERATION