

Comparison Based on Area, Power, and Speed:

SLOW-DIVISION ALGORITHM – RESTORING DIVISION

Resource Usage Summary:

- Logic utilization: 9 ALMs needed out of 32,070 total ALMs on the device (< 1%)
- Total LABs: 2 LABs partially or completely used out of 3,207 total LABs (< 1%)
- Combinational ALUT usage for logic: 17
- Dedicated logic registers: 13
- I/O pins: 20 out of 457 (4%)
- Global clocks: 1 out of 16 (6%)
- Resource Utilization by Entity:

The Slow division entity requires 8.5 ALMs, 17 combinational ALUTs, and 13 dedicated logic registers.

Routing Usage Summary:

- Block interconnects: 27 out of 289,320 (< 1%)
- C2 interconnects: 13 out of 119,108 (< 1%)
- C4 interconnects: 8 out of 56,300 (< 1%)
- Direct links: 3 out of 289,320 (< 1%)
- Global clocks: 1 out of 16 (6%)

Timing Analysis Summary:

- Worst-case slack: Setup: 17.173 ns, Hold: 0.147ns
- Design-wide TNS: 0.0 ns

Power Analysis:

- Average toggle rate: 8.428 million of transitions / sec
- Total thermal power estimate: 425.87 mW

Overall, the slow division algorithm exhibits low resource utilization, reasonable timing slack, and moderate power consumption. It meets the required functionality while utilizing a small portion of the available resources on the device.

Comparison Based on Area, Power, and Speed:

FAST-DIVISION ALGORITHM – RECIPROCAL APPROXIMATION

Resource Usage Summary:

- Logic utilization: 15 ALMs needed out of 32,070 total ALMs on the device (< 1%).
- Total LABs: 3 LABs partially or completely used out of 3,207 total LABs (< 1%).
- Combinational ALUT usage for logic: 29.
- DSP Blocks: 2.
- I/O pins: 16 out of 457 (4%).
- Average interconnect usage: 0.0%.
- Peak interconnect usage: 0.5%.

Routing Usage Summary:

- Block interconnects: 52 out of 289,320 (< 1%).
- C12 interconnects: 4 out of 13,420 (< 1%).
- C2 interconnects: 17 out of 119,108 (< 1%).
- C4 interconnects: 18 out of 56,300 (< 1%).
- Direct links: 5 out of 289,320 (< 1%).
- Local interconnects: 13 out of 84,580 (< 1%).
- R14 interconnects: 28 out of 12,676 (< 1%).
- R14/C12 interconnect drivers: 28 out of 20,720 (< 1%).
- R3 interconnects: 25 out of 130,992 (< 1%).
- R6 interconnects: 33 out of 266,960 (< 1%).

Timing Analysis Summary:

- Worst-case slack: Setup: 1.5 ns, Hold: 0.8 ns
- Design-wide TNS: -0.2 ns

Power Analysis:

- Average toggle rate: 0.000 million transitions per second.
- Total thermal power estimate: 420.79 mW.

Overall, the Fast-Division algorithm demonstrates low resource utilization, indicating efficient usage of available resources. The power consumption is moderate, with an average toggle rate of 0.000 million transitions per second and a total thermal power estimate of 420.79 mW.

Tabulated comparison of the Slow-Division Algorithm (Restoring Division) and the Fast-Division Algorithm (Reciprocal Approximation) based on area, power, and speed:

Algorithm	Slow-Division Algorithm	Fast-Division Algorithm
Resource Utilization		
Logic utilization	9 ALMs (< 1%)	15 ALMs (< 1%)
Total LABs	2 LABs (< 1%)	3 LABs (< 1%)
Combinational ALUTs	17	29
Dedicated logic registers	13	N/A
I/O pins	20 out of 457 (4%)	16 out of 457 (4%)
Routing Usage		
Block interconnects	27 out of 289,320 (< 1%)	52 out of 289,320 (< 1%)
C2 interconnects	13 out of 119,108 (< 1%)	17 out of 119,108 (< 1%)
C4 interconnects	8 out of 56,300 (< 1%)	18 out of 56,300 (< 1%)
Direct links	3 out of 289,320 (< 1%)	5 out of 289,320 (< 1%)
Timing Analysis		
Worst-case slack (Setup)	17.173 ns	1.5 ns
Worst-case slack (Hold)	0.147 ns	0.8 ns
Design-wide TNS	0.0 ns	-0.2 ns
Power Analysis		
Total thermal power estimate	425.87 mW	420.79 mW