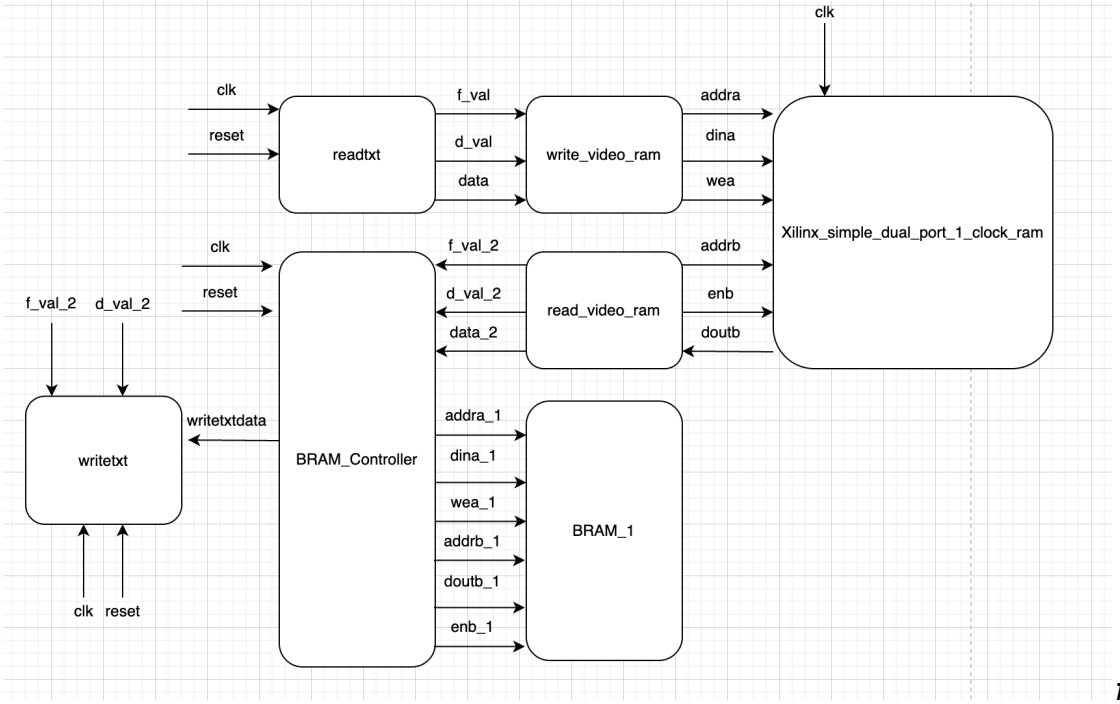
Block Design

During my internship period I designed a real time histogram calculator circuit using VHDL and simulated it on Vivado. The aim is to calculate the histogram of a continuously flowing video data. The histogram has to be calculated with real-time meaning that when a frame comes it needs to be processed before the new frame arrives. This was the most challenging part of my work.



fig

Fig. 1: Schematic of the design

First of all I started my project with a high level design as you can see in fig 1. This is kind of a schematic illustrating the connections between modules while indicating the input and output signals of each module. I followed a step by step process while verifying each step in the Vivado simulation. All of the system is synchronized with connecting the clock (clk) except for block ram (BRAM) modules since it is not needed for BRAMs. There is also a reset signal going through modules which turns the system into the initial state.

“readtxt.vhd” Module

I designed the readtxt module at the first stage. The function of this module is to simulate a camera module. The basic camera gives frame_valid (fval), data_valid (dval), and pixel data (data) signals as outputs. I designed my camera simulator generating 30 frames per second and fval, dval and data signals as output. This module is non-synthesisable since it requires opening the text file including pixel data and this can only be done in the simulation. All the modules are synthesisable except from “readtxt” and “writetxt” modules which open and close the text files as we will see in the following sections.

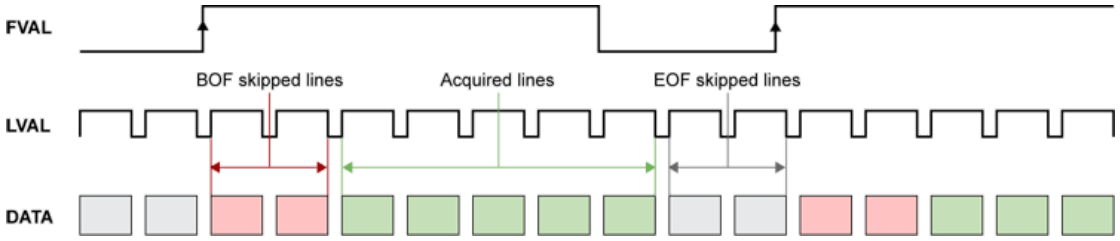


Fig 2: fval and dval signals timing diagram [1].

This pixel data is given as the output signal named “data” while working synchronously with fval and dval signals. “fval” signal only turns on when the frame starts. “dval” signal turns on when pixel data is valid. In figure 2 we can see the fval and lval signals as well as the data. “lval” means the line_valid and it turns on when the data arrives. In some cases it is also named “dval” as in my project.

“write_video_ram” Module

This module takes the fval, dval and data signals and writes the data to BRAM. It generates addra, dina, wea signals. “addra” determines the BRAM address, “dina” is the data that will be written to the BRAM and “wea” is the write enable signal which allows writing operation to the BRAM.

“dual_port_block_ram” Module

This module is a dual port block ram module. Dual port BRAM is used since we can do writing and reading operations from different addresses at the same clock cycle. This feature is required since we are dealing with continuously flowing data and previous frame data has to be processed while a new frame arrives.

“read_video_ram” Module

This module reads the BRAM and generates f_val_2, d_val_2 and data_2 signals. It reads the BRAM with addrb, enb and doubt signals. “addrb” signal determines the address to be read. “enb” is the read enable signal which allows reading data from BRAM. “doutb” is the data sent from BRAM to “read_video_ram” module.

“BRAM_Controller” and “BRAM_1” Modules

These two modules are where histogram calculation is done. BRAM_Controller manages all the operations while BRAM_1 is just a dual port block ram module. Block ram controller takes pixel data from the read_video_ram module and increments that pixel’s BRAM address by one. This operation continues until the frame ends. After the frame ends BRAM_Controller reads each pixel’s BRAM address ,where the total number of occurrences of that particular pixel is held, and gives it as an output signal called “writetxtdata” to the “write_txt” module.

“writetxt” Module

This module is a non-synthesisable module that basically writes histogram data “writetxtdata” signal to “output.txt” file.

Verification Process

I used MATLAB to verify my outcomes. I used MATLAB’s “histogram()” function to do that. After I obtained MATLAB’s histogram data and VHDL’s output data, I compared them with each other again using MATLAB for loop. The tests were successful, meaning I obtained the correct result with my design.