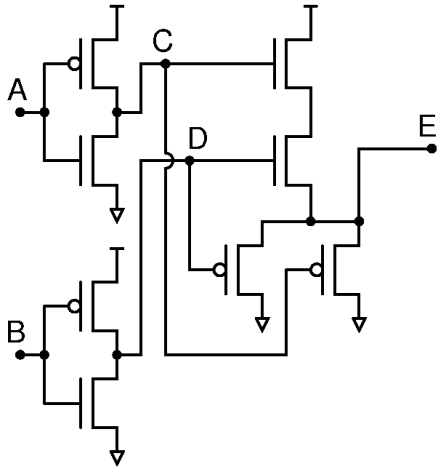
CS 2450 – Final Exam A NAME:_____

THIS IS A SAMPLE. **THIS IS NOT EVERYTHING.** ANYTHING IN THE QUIZZES, ANY DIAGRAMS (INCLUDING MEMORY), ANY PROGRAMMING CONCEPT COULD BE COVERED EVEN THOUGHT THERE MIGHT NOT BE A QUESTION BELOW PERTAINING TO IT SPECIFICALLY.

THIS IS ONLY THE NEW STUFF ADDED SINCE THE MIDTERM. USE THE MIDTERM PRACTICE EXAM FOR THOSE QUESTIONS.

1. A logic circuit whose output depends only upon the current inputs is a _____?
2. An 8 bit adder is created from a series of full adders. How many input and output lines will the 8 bit adder
3. If a computer has 8-bit addressability and uses 6 bits to access a memory location, what is the size of memory in bytes?
4. If a computer has 32-bit addressability and an address space of 1024, how many bytes can be stored?
5. What does R=0, S=0 do on an RS-Latch as discussed in class?
6. What does R=1, S=0 do on an RS-Latch as discussed in class?

   For the next three it could be anything block diagram for a device we have studied such as decoder, multiplexer, encoder, adder, memory, latch, etc…
7. What is the name of the circuit block diagram shown in Image 1?
8. In Image 1, Given some number of input lines, how many lines are required of the output O?
9. In Image 1, Given some number of output lines, how many lines are required for input S?
10. Given a transistor level circuit, fill out a truth table.



A	B	C	D	E
0	0			
0	1			
1	0			
1	1			

11. For the circuit above, what does E represent?
    a) and b) nand c) xor d) xnor e) None/All

12. Draw a two bit state diagram for a circuit that counts up and repeats when the switch is in 1 and flashes both-on / both-off when the switch is in zero. When transitioning from counting to flashing, all unspecified transitions should go to the both-off state.

Fill in the truth table completely and transfer 1s or 0s to your answer sheet for the numbered cells.

S1	S2	SW	D1	D0
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

13. Build the circuit associated with D1 (or D0).

    Build D1 (or D0) using a universal circuit.

Translate the given code into hexadecimal. Assume it has been assembled and loaded into a simulator. (I will give you a program to translate.)

14. What is stored in memory location x3000?
15. What is stored in memory location x3001?
16. What is stored in memory location x3002?

17. In Figure 2, attached at end of test, which instructions uses the data line numbered (1-20) while finding the operand(s) (fetch)?
18. In Figure 2, attached at end of test, the _____ instruction uses which of the following numbered data line(s) while finding the operand(s)?
19. Which of the following instructions use line (1-20) from Figure 2 while executing?
20. Which of the following instructions need _____MUX control to be 0 or 1?
21. In Figure 2, attached at end of test, which of the following numbered data line(s) are used while reading from memory location _____ (one of the memory mapped instructions)?
22. An example instruction which would cause the ALU labeled + in Figure 2 to perform a computation is_____?
23. Which of the following instructions require 2 memory accesses to process (including the fetch)?
24. Addressing mode in which the operand can be found _____is
25. Number of bits needed to represent a register in an instruction if the number of registers on the machine is some power of 2. (the LC3 is 8)
26. Number of bits needed to represent an opcode in an instruction if the number of instructions implemented by the machine _____? (some number of instructions)

27. Largest positive value that can be represented in the IMM field of an instruction if the IMM field is x bits and is used to hold a 2's complement number

28. When using memory mapping for IO, what happens to the mapped memory location?
29. When calling TRAP x22 what is the significance of the x22?
30. What would I need to do to make my own Trap for the LC3?
31. If R0 = 65 and R1 = MEMORY_MAPPED and the following is executed STR R0, R1, #0, where does the 65 get stored?
32. When does the interrupt status get checked?
33. When can an interrupt get executed?
    a) between instructions b) in the middle of an instruction c) only at the end of the program
    d) only at the beginning of the program e) None/All
34. Why is RTI required instead of RET when returning from an interrupt?
    a) RTI must restore R7 and RET does not b) RTI must restore the DSR and RET does not
    c) RTI must restore the PSR and RET does not d) Either RTI or RET would actually work
    e) None/All

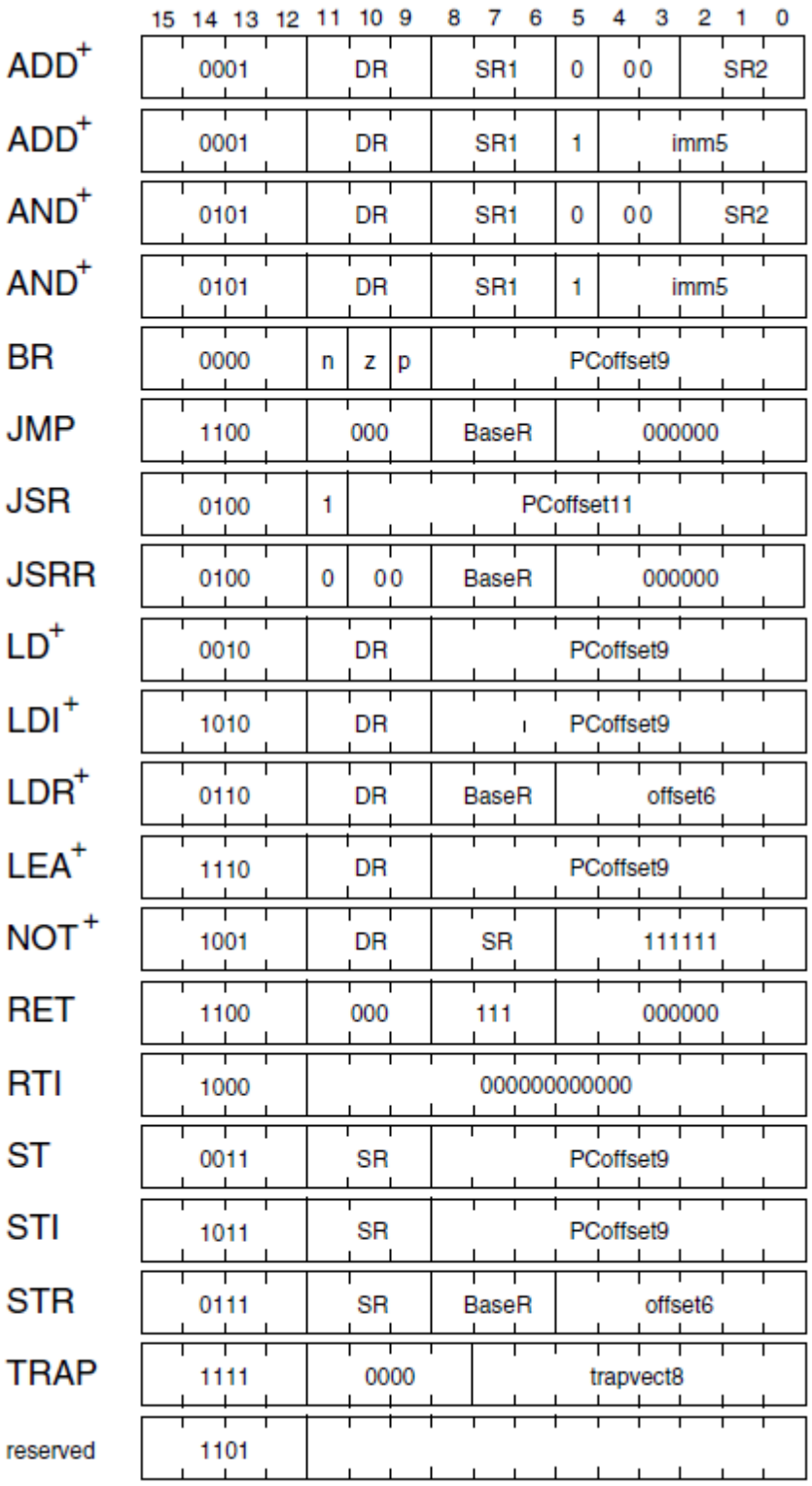


Figure 1

TRAPS

GETC	x20
OUT	x21
PUTS	x22
IN	x23
PUTSP	x24
HALT	x25

Memory Mapping

xFE00	KBSR
xFE02	KBDR
xFE04	DSR
xFE06	DDR

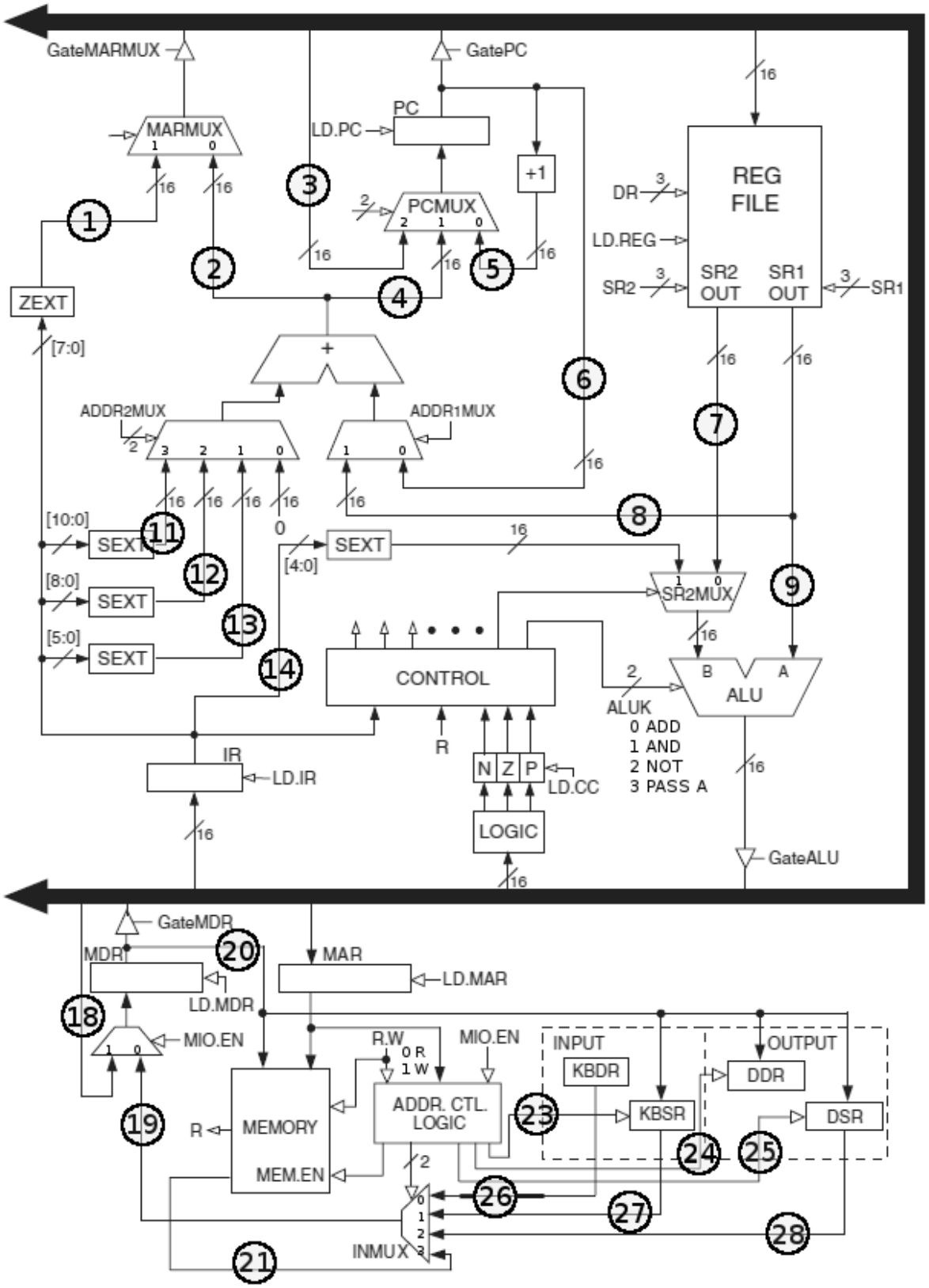

GateMARMUX
GatePC
MARMUX
PC
LD.PC
+1
PCMUX
REG FILE
DR
LD.REG
SR2
SR2 OUT
SR1 OUT
SR1
ZEXT
[7:0]
+
ADDR2MUX
ADDR1MUX
[10:0]
[8:0]
[5:0]
SEXT
[4:0]
SR2MUX
CONTROL
ALU
ALUK
0 ADD
1 AND
2 NOT
3 PASS A
IR
LD.IR
R
N Z P
LD.CC
LOGIC
GateALU
GateMDR
MDR
MAR
LD.MAR
LD.MDR
MIO.EN
R.W
0 R
1 W
INPUT
OUTPUT
KBDR
DDR
KBSR
DSR
MEMORY
MEM.EN
ADDR. CTL. LOGIC
INMUX

Figure 2