REVISION	DESCRIPTION	DATE	APPROVED

Root

RELEASED

SCHEMATIC STATUS: **RELEASED**

VARIANT:

TEMPLATE NOTES

Set Project Parameters

1– Go to View –> Pge Preview Setting
2– Set Parameters based on the following Info
COMMENT 1: Project Version
COMMENT 2: Document Status
COMMENT 3: Doc. Approval Eng.
COMMENT 4: BOM Ref. DOC.
COMMENT 5: PCB Ref. DOC.
COMMENT 6: GBR Ref. DOC.
COMMENT 7: ASM Ref. DOC.
COMMENT 8: Variant Name
COMMENT 9: Revision Description

Symbols and Lables

Mark Not Fitted Components as –> **DNF**
Differential Signal Example
Net Class Example

SCHEMATIC STATUS:

DRAFT	– Very Early Stage of Schematic
PRELIMINARY	– Close to Final Schematic
CHECKED	– There Should Not Be Any Mistakes
RELEASED	– A Board with This Schematic Has Been Produced

DESIGN CONSIDERATION

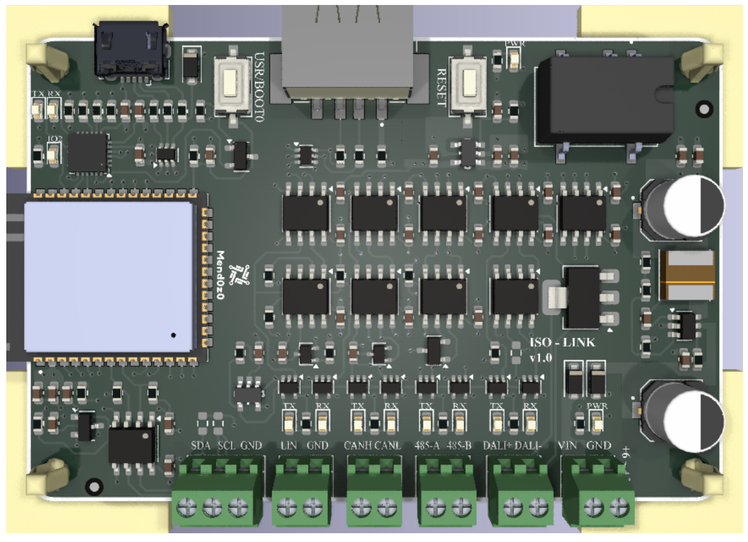
INFO: Example text for informational design notes.

CAUTIONARY: Example text for cautionary design notes.

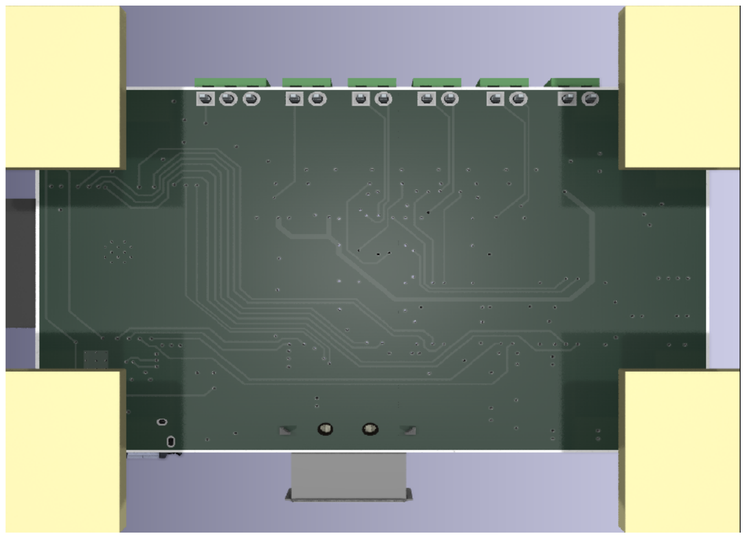
DESIGN NOTE: Example text for critical design notes.

LAYOUT NOTE: Example text for critial layout guidlines.

3D Preview TOP



3D Preview BOTTOM



Board Statistics
Stackup Info

SHOULD BE ADDED

AFTER RELEASE

APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	
REFERENCE DOCUEMNTS	
SCH Ref. DOC.: _HW_ESP32–IsoLink.kicad_sch	
BOM Ref. DOC.:	
PCB Ref. DOC.:	
GBR Ref. DOC.:	
ASM Ref. DOC.:	

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

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Find the Right License?

TITLE: Root

FILE NAME: _HW_ESP32–IsoLink.kicad_sch

SHEET 1 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH ARE ALL OPEN-SOURCE AND THERE IS NO RESPONSIBILITY FOR PROBABLE FAILURE OR INJURY

REVISION	DESCRIPTION	DATE	APPROVED

BLOCK DIAGRAM

RELEASED

CLEAN SIDE

+3.3VDC LDO REG.
+3.3V
3V_OUT
V_IN
VCC
File: [06]_+3.3VDC LDO REG..kicad_sch

+5VDC ISOLATED DCDC CONV.
3V_OUTPUT
V_IN
+5V
File: [10]_+5VDC ISOLATED DCDC CONV..kicad_sch

+5VDC BUCK REG.
3V_OUTPUT
File: [17]_+5VDC BUCK REG..kicad_sch

20 UIN-DIR ISOLATOR
ISO6520_INA_3.3V
ISO6520_INB_3.3V
ISO6520_OUTA_5VD
ISO6520_OUTB_5VD
File: [07]_20 UIN-DIR ISOLATOR.kicad_sch

10Hz ASTABLE OSCILLATOR
CLOCKD
File: [15]_10Hz ASTABLE OSCILLATOR.kicad_sch

USB OTG
USBD-
USBD+
File: [05]_USB OTG.kicad_sch

MCU Driver
USBD-
USBD+
RS485_SELD
CAN_ENB
UART_TXDD
UART_RXD
CAN_TXDD
CAN_RXD
LIN_TXDD
LIN_RXD
DALI_TXD
DALI_RX
SCL
SDA
ESP32_TXD
ESP32_RXD
RTS
DTR
File: [03]_MCU Driver.kicad_sch

1-1 BI-DIR ISOLATOR
ISO6521_INB_3.3V
ISO6521_OUTA_3.3V
ISO6521_OUTB_5VD
ISO6521_INA_5V
File: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

1-1 BI-DIR ISOLATOR1
ISO6521_INB_3.3V
ISO6521_OUTA_3.3V
ISO6521_OUTB_5VD
ISO6521_INA_5V
File: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

1-1 BI-DIR ISOLATOR2
ISO6521_INB_3.3V
ISO6521_OUTA_3.3V
ISO6521_OUTB_5VD
ISO6521_INA_5V
File: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

1-1 BI-DIR ISOLATOR3
ISO6521_INB_3.3V
ISO6521_OUTA_3.3V
ISO6521_OUTB_5VD
ISO6521_INA_5V
File: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

I2C BUS ISOLATOR
ISO1640_SCL_3.3V
ISO1640_SDA_3.3V
File: [09]_I2C BUS ISOLATOR.kicad_sch

USB to UART Bridge
CP2105_RXD
CP2105_TXD
CP2105_RTS
CP2105_DTR
File: [04]_USB to UART Bridge.kicad_sch

RS485 DRIVER
CLOCK
THVD_E
THVD_D
THVD_R
File: [11]_RS485 DRIVER.kicad_sch

CAN DRIVER
CLOCK
ATA6561_STBY
ATA6561_TXD
ATA6561_RXD
File: [12]_CAN DRIVER.kicad_sch

IT DOESN'T SUPPORT CANFD!!!

LIN DRIVER
CLOCK
TLIN_TXD
TLIN_RXD
File: [13]_LIN DRIVER.kicad_sch

DALI ISOLATOR
CLOCK
DALI_TX
DALI_RX
File: [14]_DALI ISOLATOR.kicad_sch

APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [02] - BLOCK DIAGRAM.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

Mend0z0

Find the Right License?

PRJ VER:	DOC VER:	DOC REV:

TITLE: BLOCK DIAGRAM

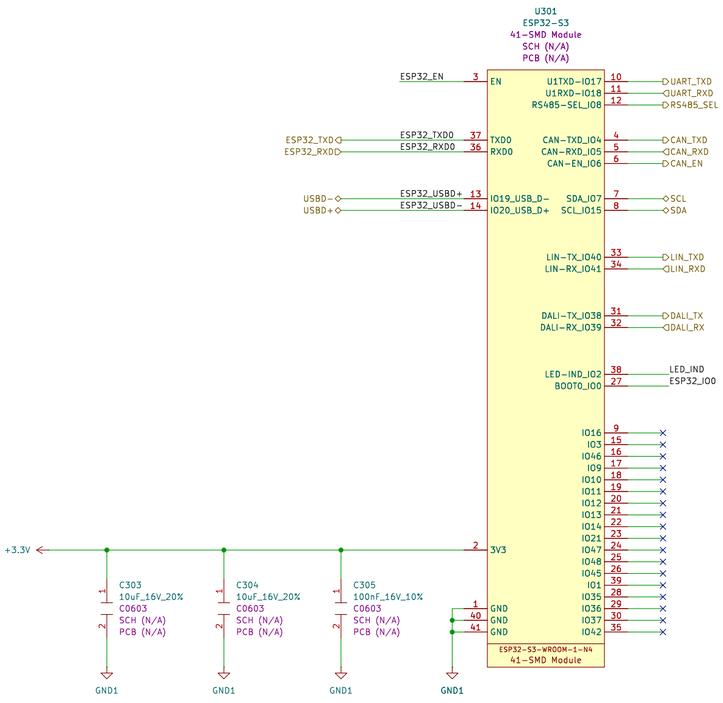
FILE NAME: [02] - BLOCK DIAGRAM.kicad_sch

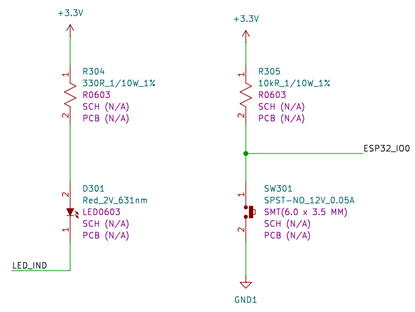
SHEET 2 OF 24	SIZE: C	SCALE: 1:1	VARIANT NAME:

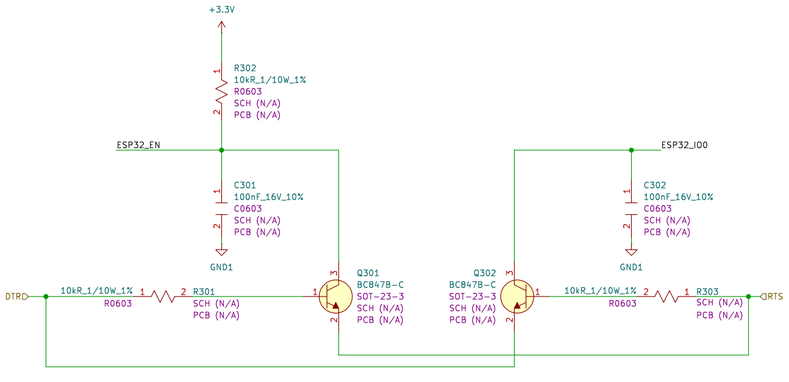
REVISION	DESCRIPTION	DATE	APPROVED

MCU Driver

RELEASED







AUTO PROGRAMMING

DTR	RTS	EN	IO0
1	1	1	1
0	0	1	1
1	0	0	1
0	1	1	0

https://docs.espressif.com/projects/esptool/en/latest/esp32/advanced-topics/boot-mode-selection.html

APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [03]_MCU Driver.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: MCU Driver

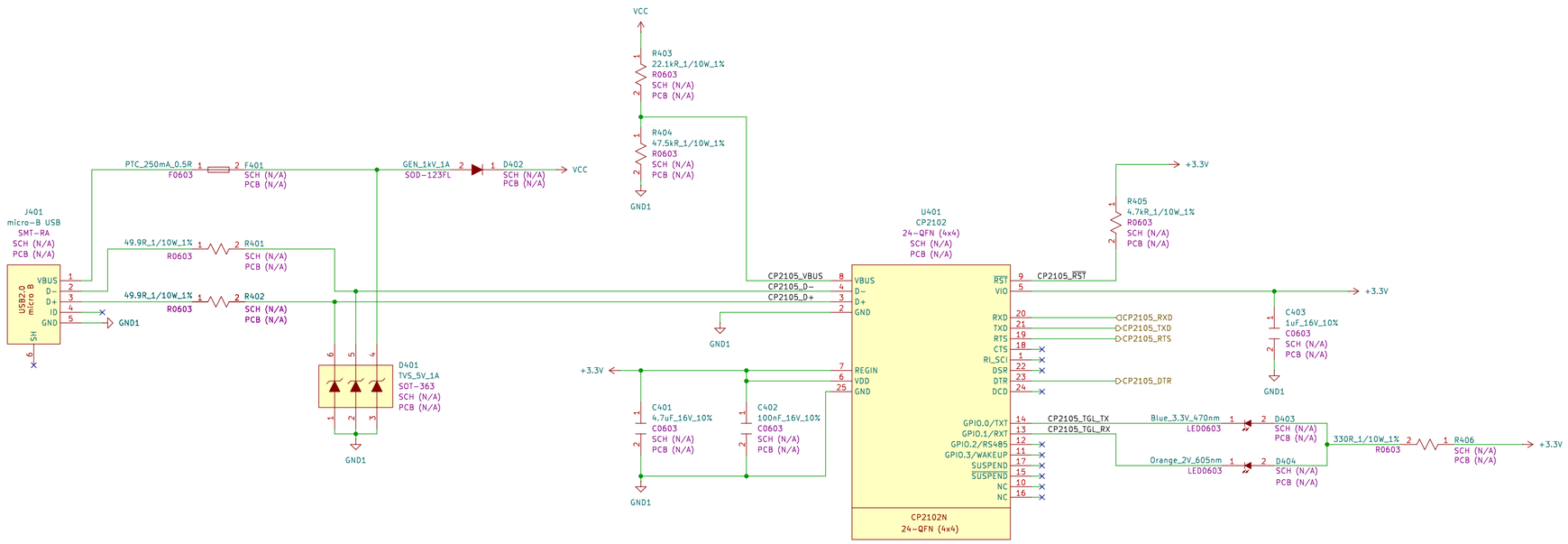
FILE NAME: [03]_MCU Driver.kicad_sch

SHEET 3 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

USB to UART Bridge

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [04]_USB to UART Bridge.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: USB to UART Bridge

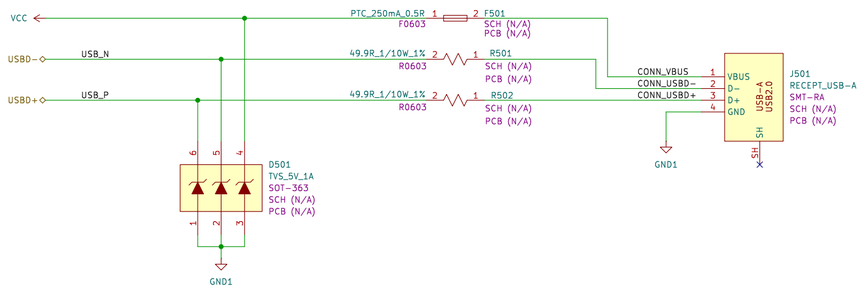
FILE NAME: [04]_USB to UART Bridge.kicad_sch

SHEET 4 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

USB OTG

RELEASED



APPROVALS	DATE
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DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [05]_USB OTG.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: USB OTG

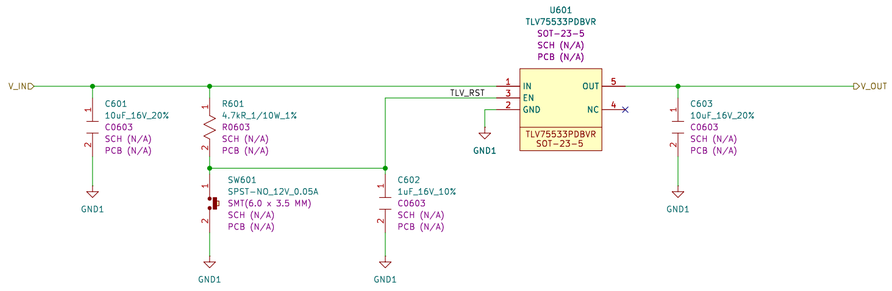
FILE NAME: [05]_USB OTG.kicad_sch

SHEET 5 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

+3.3VDC LDO REG.

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [06]_+3.3VDC LDO REG..kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

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Find the Right License?

TITLE: +3.3VDC LDO REG.

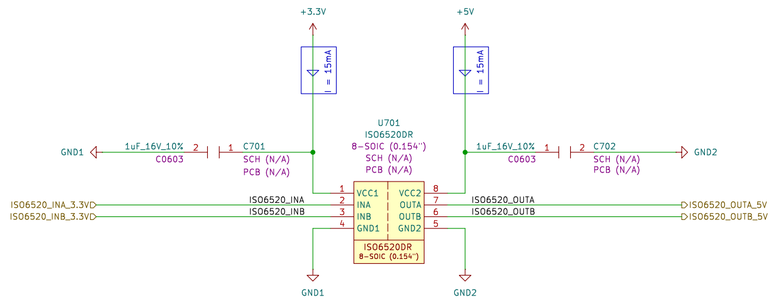
FILE NAME: [06]_+3.3VDC LDO REG..kicad_sch

SHEET 6 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

20 UIN-DIR ISOLATOR

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [07]_20 UIN-DIR ISOLATOR.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

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TITLE: 20 UIN-DIR ISOLATOR

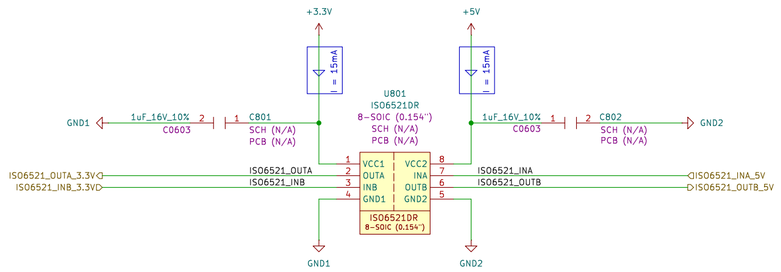
FILE NAME: [07]_20 UIN-DIR ISOLATOR.kicad_sch

SHEET 7 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

1-1 BI-DIR ISOLATOR

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [08]_1-1 BI-DIR ISOLATOR.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

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Find the Right License?

TITLE: 1-1 BI-DIR ISOLATOR

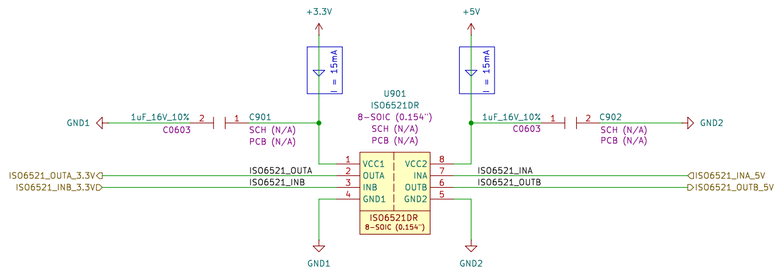
FILE NAME: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

SHEET 8 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

1-1 BI-DIR ISOLATOR1

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [08]_1-1 BI-DIR ISOLATOR.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: 1-1 BI-DIR ISOLATOR1

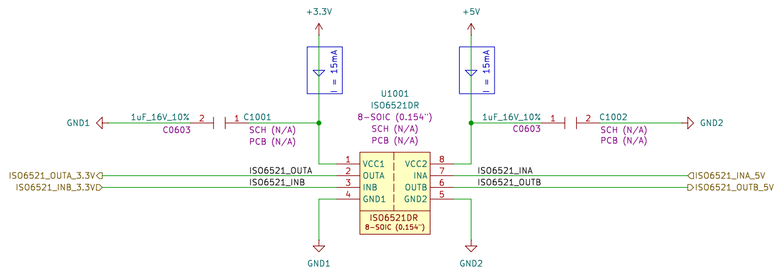
FILE NAME: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

SHEET 9 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

1-1 BI-DIR ISOLATOR2

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
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BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

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Find the Right License?

TITLE: 1-1 BI-DIR ISOLATOR2

FILE NAME: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

SHEET 10 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

1-1 BI-DIR ISOLATOR3

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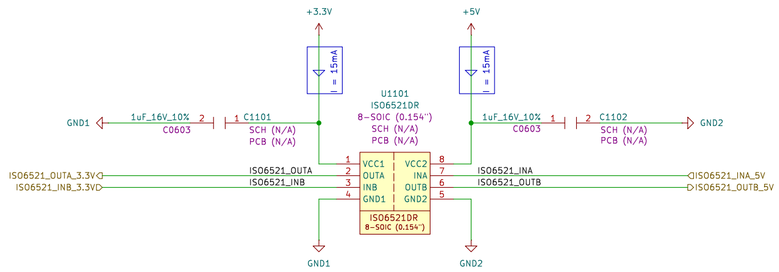


APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [08]_1-1 BI-DIR ISOLATOR.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: 1-1 BI-DIR ISOLATOR3

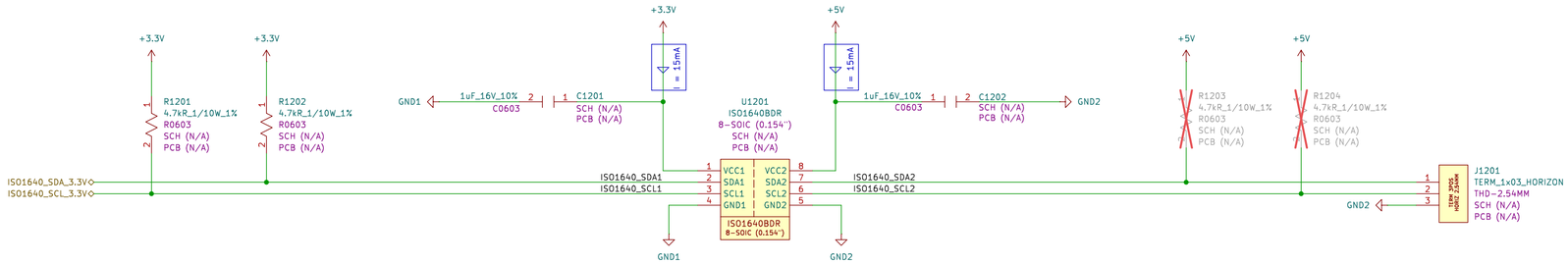
FILE NAME: [08]_1-1 BI-DIR ISOLATOR.kicad_sch

SHEET 11 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

I2C BUS ISOLATOR

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [09]_I2C BUS ISOLATOR.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: I2C BUS ISOLATOR

FILE NAME: [09]_I2C BUS ISOLATOR.kicad_sch

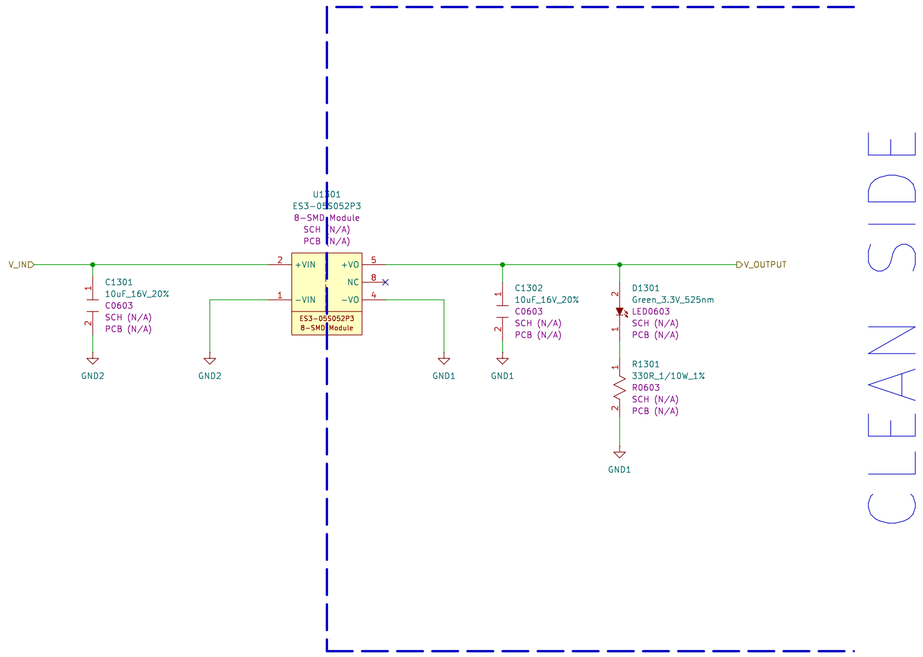
SHEET 12 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH ARE ALL OPEN-SOURCE AND THERE IS NO RESPONSIBILITY FOR PROBABLE FAILURE OR INJURY

REVISION	DESCRIPTION	DATE	APPROVED

+5VDC ISOLATED DCDC CONV.

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [10]_+5VDC ISOLATED DCDC CONV..kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: +5VDC ISOLATED DCDC CONV.

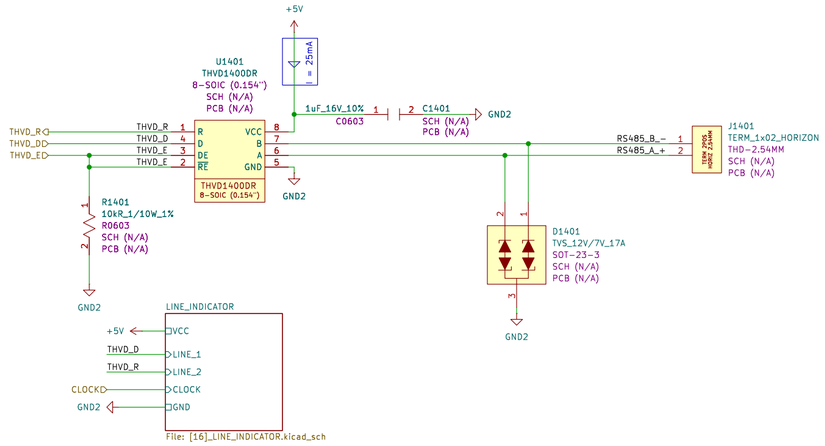
FILE NAME: [10]_+5VDC ISOLATED DCDC CONV..kicad_sch

SHEET 13 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

RS485 DRIVER

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [11]_RS485 DRIVER.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: RS485 DRIVER

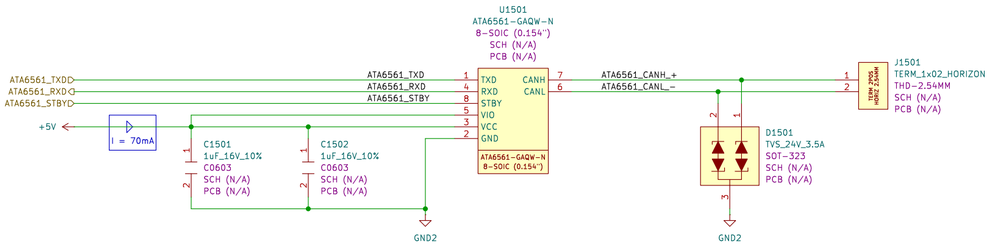
FILE NAME: [11]_RS485 DRIVER.kicad_sch

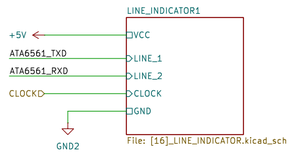
SHEET 14 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

CAN DRIVER

RELEASED





APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [12]_CAN DRIVER.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

Mend0z0

Find the Right License?

TITLE: CAN DRIVER

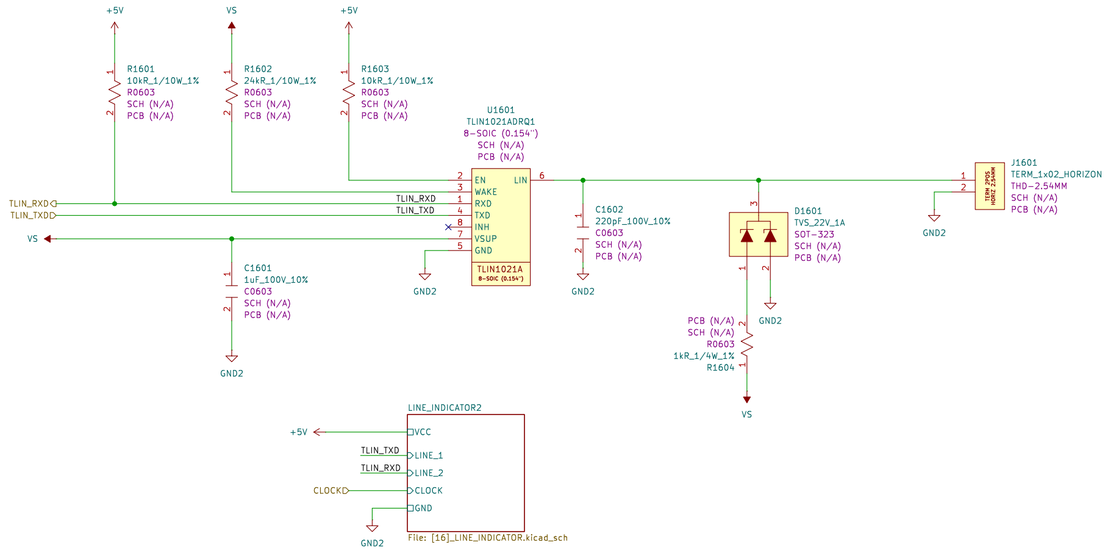
FILE NAME: [12]_CAN DRIVER.kicad_sch

SHEET 15 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

LIN DRIVER

RELEASED



APPROVALS	DATE
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DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [13]_LIN DRIVER.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

PRJ VER: | DOC VER: | DOC REV:

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TITLE: LIN DRIVER

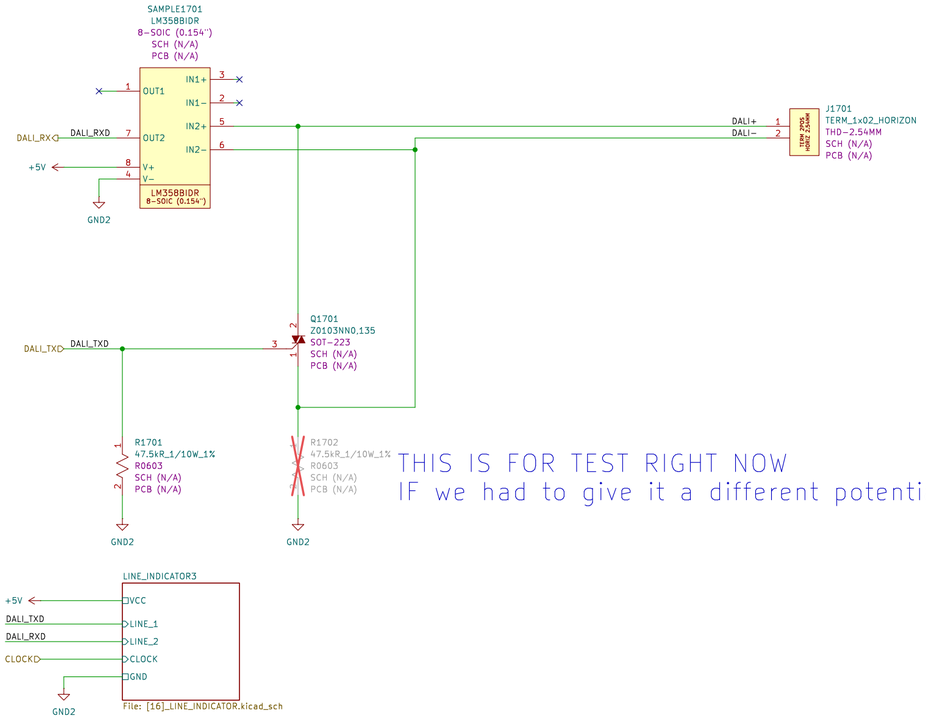
FILE NAME: [13]_LIN DRIVER.kicad_sch

SHEET 16 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

DALI ISOLATOR

RELEASED



DALI SPEC.

IEC60929

• Short specification
- Maximum 64 individual addressable ballasts within one system
- The ballast can not act as a master controller
- Multiple ballast groups
– Bi-phase coding for error detection (see E.4.3.6, Pulse diagram)
– Asynchronous start-stop transmission protocol
– Low information rate: 1 200 bit/s
– Allowed cable voltage drop: 2 V
– No ground-loops because of isolation in the ballast
The tolerance at all mentioned timing specifications in this document shall be ±10 % if minimum/maximum are not specified.

Impedance control terminals (see Figure E.1): Rin ≥ 8 KΩ static at typical high input voltage
Cin ≤ 1 nF
Lin ≤ 1 mH

The robustness can be increased with the optional implementation of:
– polarity insensitive interface input;
– overvoltage protection for accidental mains voltage between the control wires.
• Transmission characteristics
The transmission rate, expressed in bandwidth, is specified with 1 200 Hz for the forward channel and for the backward channel.
All specified voltage and current levels refer to the terminals of the electronic ballast.

Voltage rating (IEC60929)

In general, the interface voltage is high if there is no communication (idle state).
The slopes of the received and transmitted data signal shall be 10 µs ≤ tfall ≤ 100 µs and 10 µs ≤ trise ≤ 100 µs at the ballast terminals of the digital interface.
The voltage range shall be between 9,5 V and 22,5 V for "high level" and between −6,5 V and +6,5 V for "low level" respectively. Between 6,5 V and 9,5 V, the level is undefined.

Current rating (IEC60929)

In non-active state, the sink current of the ballast shall not exceed 2 mA at ≤22,5 V because of the actual maximum number of ballasts per control unit. This shall be guaranteed by each ballast manufacturer.
The ballast shall be able to sink at least 250 mA at ≤ 4,5 V at active state. The ballast shall keep the interface voltage lower than 4,5 V.
The interface power supply shall limit the supply current to max. 250 mA under all circumstances.
This current limitter circuit has to react faster than 10 µs
The interface specification at the ballast terminals shall be:
- active state: low voltage level ≤ 4,5 V; high current level ≤ 250 mA (lim. by the power supply);
- non-active state: high voltage level ≤ 22,5 V, low voltage level ≤ 6,5 V; high current ≤ 2 mA.

APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [14]_DALI ISOLATOR.kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

PROJECT:

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TITLE: DALI ISOLATOR

FILE NAME: [14]_DALI ISOLATOR.kicad_sch

SHEET 17 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

10Hz ASTABLE OSCILLATOR

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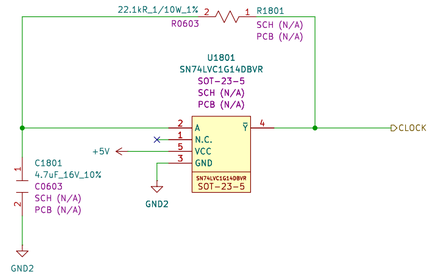
expecting around 10Hz output
formula is a simple RC charge curve in considering the schmit triger lvl



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ENG: Siavash Taher Parvar	
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REFERENCE DOCUEMNTS
SCH Ref. DOC.: [15]_10Hz ASTABLE OSCILLATOR.kicad_sch
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ASM Ref. DOC.:

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TITLE: 10Hz ASTABLE OSCILLATOR

FILE NAME: [15]_10Hz ASTABLE OSCILLATOR.kicad_sch

SHEET 18 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

LINE_INDICATOR

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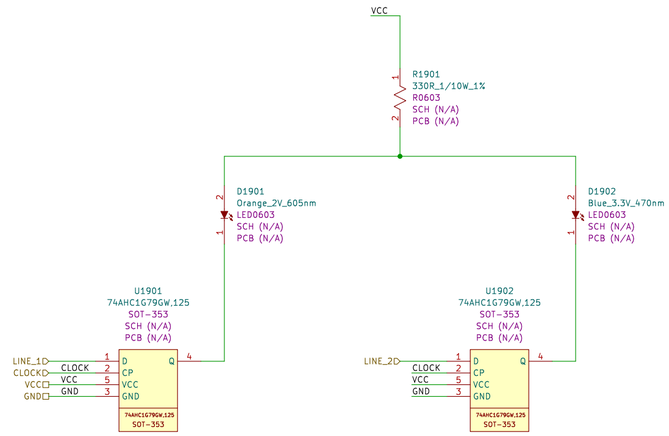

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DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [16]_LINE_INDICATOR.kicad_sch
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TITLE: LINE_INDICATOR

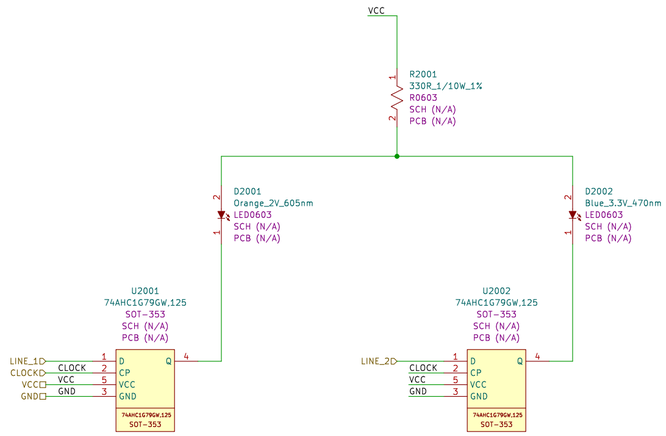
FILE NAME: [16]_LINE_INDICATOR.kicad_sch

SHEET 19 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

LINE_INDICATOR1

RELEASED



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DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
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TITLE: LINE_INDICATOR1

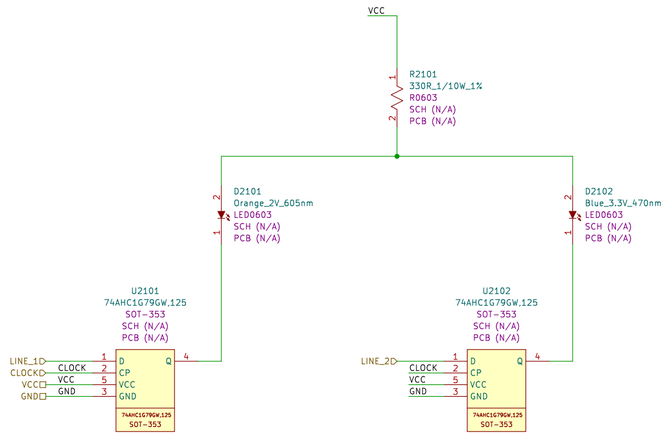
FILE NAME: [16]_LINE_INDICATOR.kicad_sch

SHEET 20 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

LINE_INDICATOR2

RELEASED



APPROVALS	DATE
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DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

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TITLE: LINE_INDICATOR2

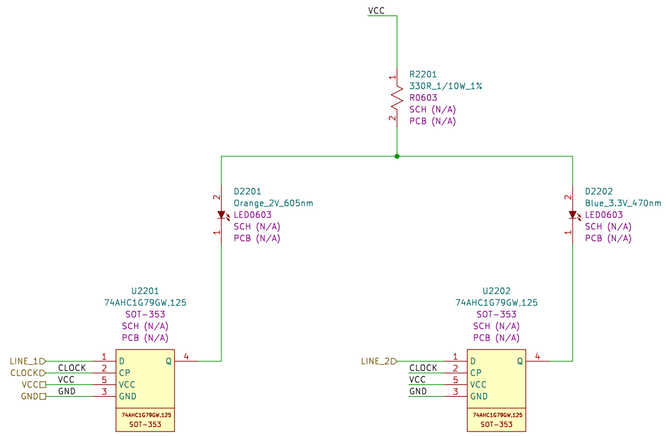
FILE NAME: [16]_LINE_INDICATOR.kicad_sch

SHEET 21 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

LINE_INDICATOR3

RELEASED



APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

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SCH Ref. DOC.: [16]_LINE_INDICATOR.kicad_sch
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TITLE: LINE_INDICATOR3

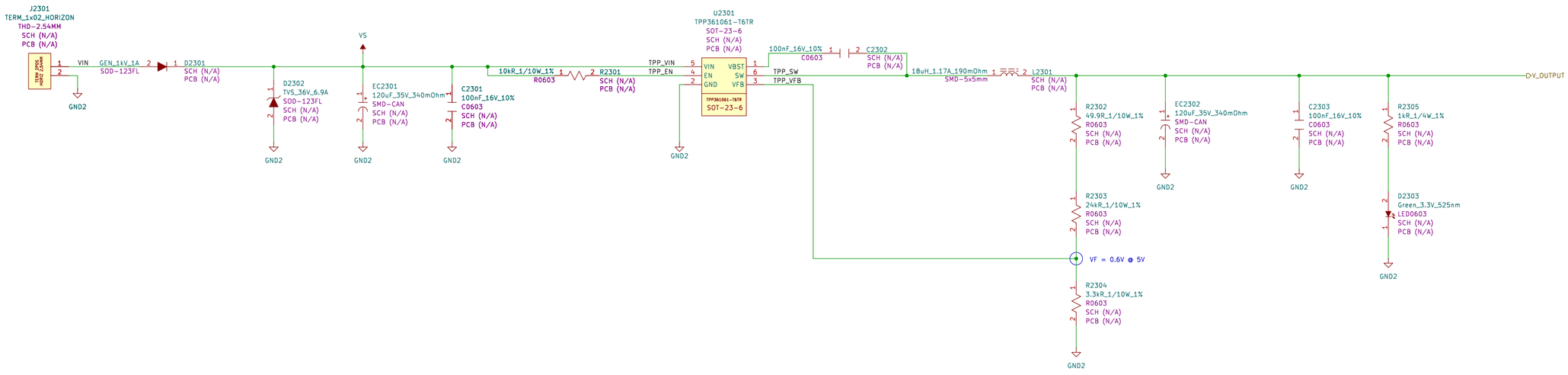
FILE NAME: [16]_LINE_INDICATOR.kicad_sch

SHEET 22 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

REVISION	DESCRIPTION	DATE	APPROVED

+5VDC BUCK REG.

RELEASED



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ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

REFERENCE DOCUEMNTS
SCH Ref. DOC.: [17]_+5VDC BUCK REG..kicad_sch
BOM Ref. DOC.:
PCB Ref. DOC.:
GBR Ref. DOC.:
ASM Ref. DOC.:

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TITLE: +5VDC BUCK REG.

FILE NAME: [17]_+5VDC BUCK REG..kicad_sch

SHEET 23 OF 24 | SIZE: C | SCALE: 1:1 | VARIANT NAME:

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MECHANICAL PARTS

RELEASED

LBL2401
LOGO_MEND0Z0
Legend Layer
SCH (N/A)
PCB (N/A)

MH2401
M3-DIN695
THD-M3
SCH (N/A)
PCB (N/A)

MH2403
M3-DIN695
THD-M3
SCH (N/A)
PCB (N/A)

FD2401
D1MM
SMT
SCH (N/A)
PCB (N/A)

MH2402
M3-DIN695
THD-M3
SCH (N/A)
PCB (N/A)

MH2404
M3-DIN695
THD-M3
SCH (N/A)
PCB (N/A)

FD2402
D1MM
SMT
SCH (N/A)
PCB (N/A)

MECH2401
SNAP-IN STANDOFF
N/a
SCH (N/A)
PCB (N/A)

MECH2403
SNAP-IN STANDOFF
N/a
SCH (N/A)
PCB (N/A)

MECH2402
SNAP-IN STANDOFF
N/a
SCH (N/A)
PCB (N/A)

MECH2404
SNAP-IN STANDOFF
N/a
SCH (N/A)
PCB (N/A)

APPROVALS	DATE
ENG: Siavash Taher Parvar	
DSN: Siavash Taher Parvar	
CHK: Siavash Taher Parvar	

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SCH Ref. DOC.: [18]_MECHANICAL PARTS.kicad_sch
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