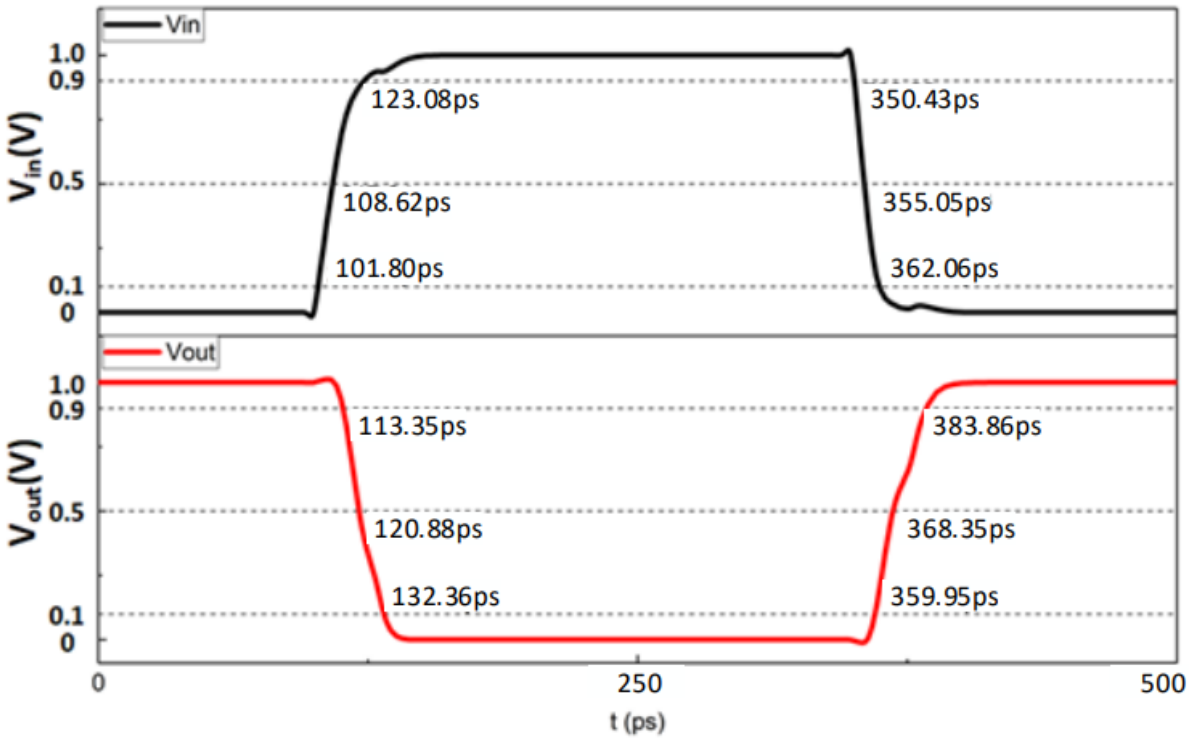
National University of Singapore
Electrical and Computer Engineering

CG2027 (Transistor-Level Digital Circuits)
Assignment #1

AY25/26 Semester 1
Issued: 8th Oct 2025 Due: 11th Oct 2025; 11:59 pm

Problem 1: Delay Calculation **[40 marks]**

The objective of this problem is to figure out correct delay / risetime / falltime of a CMOS inverter, based on the information given from the waveform.



a) What is the rise time (t_r), fall time (t_f) of the output waveform V_{out}?

$t_r = 383.86\,ps - 359.95\,ps = \boxed{23.91\,ps}$; $t_f = 132.36\,ps - 113.35 = \boxed{19.01\,ps}$

b) What is the high-to-low propagation delay (t_{pHL}) of the logic?

$t_{pHL} = 120.88\,ps - 108.62\,ps = \boxed{12.26\,ps}$

c) What is the low-to-high propagation delay (t_{pLH}) of the logic?

$t_{pLH} = 368.35\,ps - 355.05\,ps = \boxed{13.3\,ps}$

d) If the given waveform V_{in} is a part of a clock signal with **20%** duty, what is the clock frequency?

$T_H = 355.05\,ps - 108.62\,ps = 246.43\,ps$

$\because Duty = \frac{T_H}{T_{cycle}} \Rightarrow T_{cycle} = \frac{T_H}{Duty} = \frac{246.43\,ps}{20\%} = 1232.15\,ps$

$\because Frequency = \frac{1}{T_{cycle}}$

$\therefore Frequency \approx \boxed{0.8116\,GHz = 8.1 \times 10^8\,Hz}$

Problem 2: On-resistance **[30 marks]**

A designer must realize a pMOS and an nMOS that exhibit the same on-resistance. Both transistors come from the same process node, have the same channel length L, and the same gate-oxide material/thickness.

In this process, when gate width $W = 5\,\mu$m:

- On resistance of n-MOSFET: $R_n(5\,\mu\text{m}) = 10\ \text{k}\Omega$
- On resistance of p-MOSFET: $R_p(5\,\mu\text{m}) = 20\ \text{k}\Omega$

Propose two different sizing approaches (assuming you can only vary width W) that achieve equal resistance for the nMOS and pMOS.

[Hint: Adjust for P and N respectively, keeping the other transistor same.]

Sol: ① Adjust pMOS width, keep NMOS unchanged, (target is 10 kΩ)

$\because R \propto \frac{1}{W}$ and when $W = 5\,\mu m$, $R_p = 20\,k\Omega$

$\therefore$ W should become 10 μm for R_p to become 10 kΩ

$\therefore$ nMOS width : 5 μm
pMOS width : 10 μm

② Adjust nMOS width, but keep pMOS width unchanged

$\because R \propto \frac{1}{W}$

$\therefore$ W should become 2.5 μm for R_n to become 20 kΩ.

$\therefore$ nMOS width : 2.5 μm
pMOS width : 5 μm

Problem 3: Gate capacitance **[30 marks]**

An n-channel MOSFET is designed with a gate length of 1 µm, gate width of 1 µm, and a gate oxide thickness $t_{ox} \approx 20\,\text{nm}$. $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, $\varepsilon_r = 3.9$

(a) Determine the gate capacitance per unit area and total gate capacitance.

Suppose that, during MOSFETs process fabrication, only 10 nm of gate oxide was actually deposited.

(b) Determine the gate capacitance per unit area and total gate capacitance in this case.

(c) How would this change in C_{ox} affecting the drain current?

Sol. (a) per unit area: $C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}} = \boxed{1.72575 \times 10^{-3}\ F/m^2}$

total capacitance: $C_{gate} = \frac{\varepsilon_{ox}}{t_{ox}} \cdot WL = C_{ox} \cdot WL = 1.72575 \times 10^{-12} \times 10^{-6} \times 10^{-6} = \boxed{1.72575 \times 10^{-15}\ F}$

(b) $t_{ox} = 10 \times 10^{-9}$ nm now

$\therefore$ per unit, $C_{ox} = \frac{\varepsilon_r \varepsilon_0}{t_{ox}} = \boxed{3.4515 \times 10^{-3}\ F/m^2}$

total capacitance: $C_{gate} = C_{ox} \cdot WL = \boxed{3.4515 \times 10^{-15}\ F}$

(c) As we know that, I_D is proportional to C_{ox} in both linear and saturation region.

now C_{ox} doubled

$\therefore$ I_D will also double