# 计算机组织与体系结构实习报告 Lab3.1

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## PART 1 - 单层Cache模拟

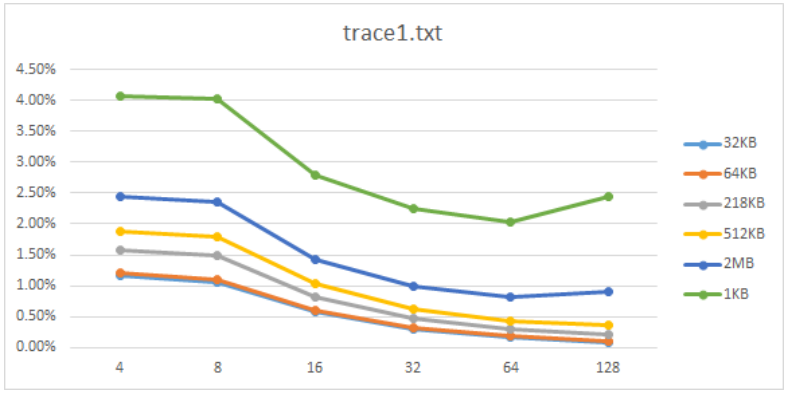
使用附件中所给模拟器框架，使用给定的测试trace，完成单层cache的模拟。

1. 在不同的 Cache Size的条件下， Miss Rate 随 Block Size变化的趋势，收集数据并绘制折线图。并说明变化原因。至少有4个不同的size大小对应的折线图。

   写回设置为write back + write allocate，取associativity为4，当cache size分别为32KB, 16KB, 8KB, 4KB, 2KB, 1KB时，所得到的的miss rate随block size的变化趋势如下：

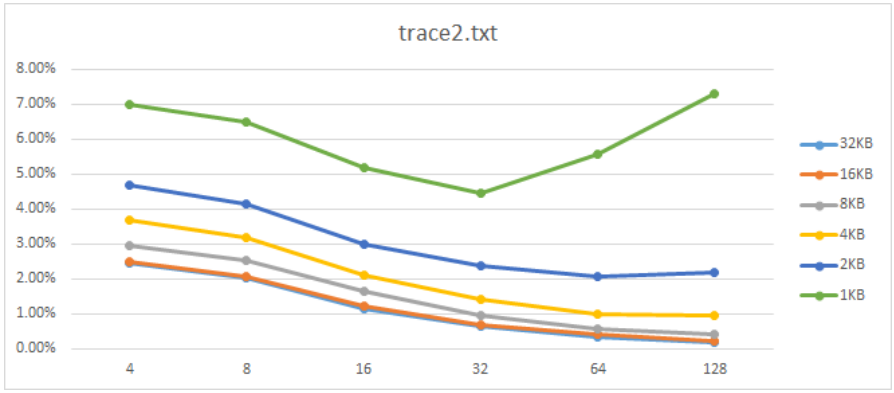
   trace1.txt:

| cache size = 32KB | | cache size = 16KB | | cache size = 8KB | | cache size = 4KB | | cache size = 2KB | | cache size = 1KB | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| block size | miss rate | block size | miss rate | block size | miss rate | block size | miss rate | block size | miss rate | block size | miss rate |
| 4 | 1.16% | 4 | 1.20% | 4 | 1.58% | 4 | 1.89% | 4 | 2.44% | 4 | 4.06% |
| 8 | 1.05% | 8 | 1.10% | 8 | 1.48% | 8 | 1.80% | 8 | 2.36% | 8 | 4.03% |
| 16 | 0.57% | 16 | 0.61% | 16 | 0.82% | 16 | 1.04% | 16 | 1.43% | 16 | 2.79% |
| 32 | 0.30% | 32 | 0.33% | 32 | 0.47% | 32 | 0.63% | 32 | 0.99% | 32 | 2.24% |
| 64 | 0.17% | 64 | 0.19% | 64 | 0.29% | 64 | 0.42% | 64 | 0.81% | 64 | 2.04% |
| 128 | 0.09% | 128 | 0.11% | 128 | 0.21% | 128 | 0.37% | 128 | 0.90% | 128 | 2.45% |




   trace2.txt:

| cache size = 32KB | | cache size = 16KB | | cache size = 8KB | | cache size = 4KB | | cache size = 2KB | | cache size = 1KB | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| block size | miss rate | block size | miss rate | block size | miss rate | block size | miss rate | block size | miss rate | block size | miss rate |
| 4 | 2.46% | 4 | 2.49% | 4 | 2.95% | 4 | 3.67% | 4 | 4.69% | 4 | 6.98% |
| 8 | 2.04% | 8 | 2.08% | 8 | 2.54% | 8 | 3.18% | 8 | 4.13% | 8 | 6.51% |
| 16 | 1.15% | 16 | 1.20% | 16 | 1.63% | 16 | 2.09% | 16 | 2.97% | 16 | 5.18% |
| 32 | 0.62% | 32 | 0.67% | 32 | 0.95% | 32 | 1.41% | 32 | 2.36% | 32 | 4.45% |
| 64 | 0.34% | 64 | 0.39% | 64 | 0.58% | 64 | 0.99% | 64 | 2.05% | 64 | 5.58% |
| 128 | 0.19% | 128 | 0.23% | 128 | 0.42% | 128 | 0.96% | 128 | 2.17% | 128 | 7.31% |




注：当cache size取更大值（如64KB）时，miss rate的折线图与32KB时基本重合，故不再绘制。

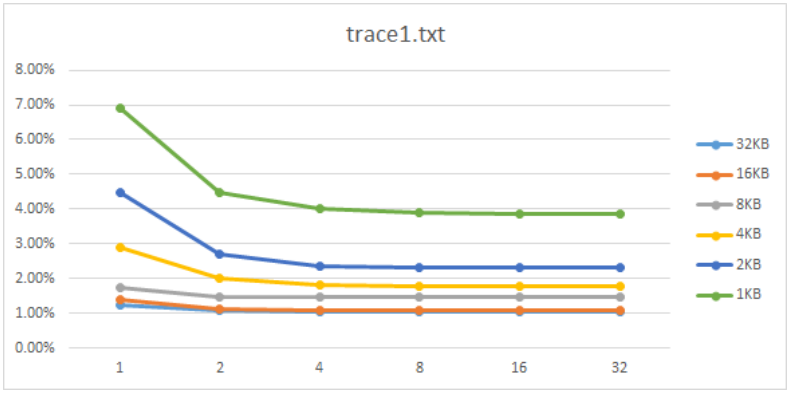
数据分析：总体而言，cache size相同时，block size越大，miss rate越低，由于程序的局部性，增大block size在多次访问地址相近的区域时有较好的hit rate。当block size一定时，cache size越大，miss rate越低，因为更大的cache size能容纳更多的数据。当cache size过小且block size过大时，由于组相联度不变，导致set数量减少，cache中容纳的数据段数量变少，miss rate有上升的趋势。

2. 在给定 Cache Size 的条件下，Miss Rate 随 Associativity变化的趋势，收集数据并绘制折线图。并说明变化原因。至少有2、4、8、16、32对应的折线图。

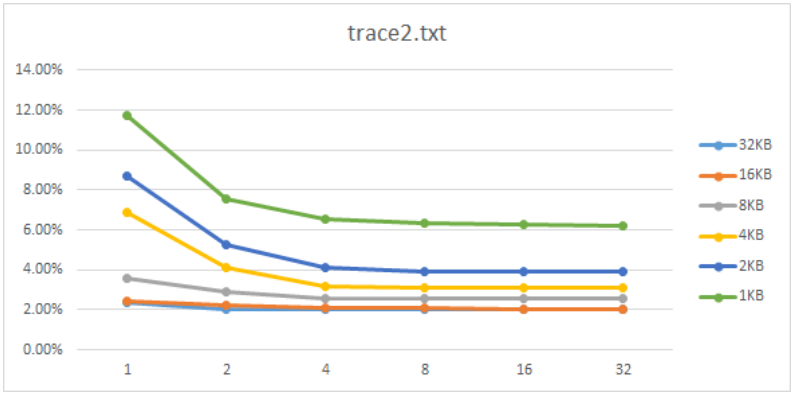
   写回设置为write back + write allocate，取block size为8，当cache size分别为32KB, 16KB, 8KB, 4KB, 2KB, 1KB时，所得到的miss rate随associativity变化的趋势如下：

   trace1.txt:

| cache size = 32KB | | cache size = 16KB | | cache size = 8KB | | cache size = 4KB | | cache size = 2KB | | cache size = 1KB | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| associativity | miss rate | associativity | miss rate | associativity | miss rate | associativity | miss rate | associativity | miss rate | associativity | miss rate |
| 1 | 1.25% | 1 | 1.39% | 1 | 1.75% | 1 | 2.90% | 1 | 4.47% | 1 | 6.91% |
| 2 | 1.07% | 2 | 1.11% | 2 | 1.46% | 2 | 2.00% | 2 | 2.69% | 2 | 4.47% |
| 4 | 1.06% | 4 | 1.10% | 4 | 1.48% | 4 | 1.80% | 4 | 2.36% | 4 | 4.03% |
| 8 | 1.06% | 8 | 1.10% | 8 | 1.49% | 8 | 1.77% | 8 | 2.32% | 8 | 3.90% |
| 16 | 1.06% | 16 | 1.10% | 16 | 1.49% | 16 | 1.77% | 16 | 2.31% | 16 | 3.85% |
| 32 | 1.06% | 32 | 1.10% | 32 | 1.48% | 32 | 1.76% | 32 | 2.32% | 32 | 3.85% |




| associativity | miss rate | associativity | miss rate | associativity | miss rate | associativity | miss rate | associativity | miss rate | associativity | miss rate |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 2.36% | 1 | 2.43% | 1 | 3.58% | 1 | 6.85% | 1 | 8.70% | 1 | 11.75% |
| 2 | 2.05% | 2 | 2.20% | 2 | 2.88% | 2 | 4.10% | 2 | 5.24% | 2 | 7.54% |
| 4 | 2.04% | 4 | 2.08% | 4 | 2.54% | 4 | 3.18% | 4 | 4.13% | 4 | 6.51% |
| 8 | 2.04% | 8 | 2.06% | 8 | 2.56% | 8 | 3.13% | 8 | 3.93% | 8 | 6.31% |
| 16 | 2.04% | 16 | 2.05% | 16 | 2.59% | 16 | 3.10% | 16 | 3.91% | 16 | 6.25% |
| 32 | 2.04% | 32 | 2.05% | 32 | 2.58% | 32 | 3.10% | 32 | 3.90% | 32 | 6.23% |



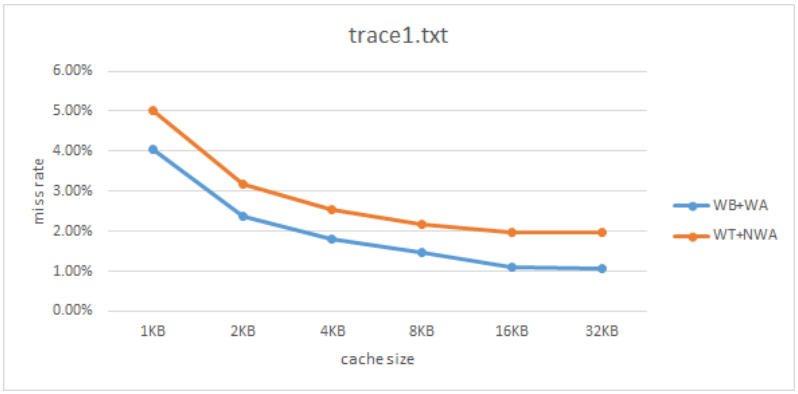

数据分析：总体而言，当cache size固定时，组相联度越高，miss rate越低，原因可能是trace文件中的局部性比较明显，有很多访存地址都有相似的前缀因此也有相近的set index；当组相联度固定时，cache size越大，miss rate越低，因为更大的cache size能容纳更多的数据；当组相联度过高时miss rate不再下降，可能是因为set数量减少所致。

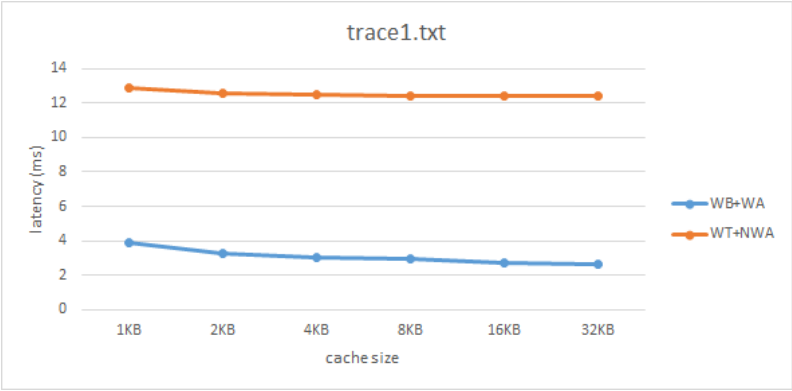
3. 比较 Write Through + No-write Allocate，Write Back + Write allocate 这两种访存策略的总访问延时的差异。

   取block size = 8, associativity = 4, cache latency = 1 cycle，当cache size取1, 2, ..., 32KB时，分别采用两种访存策略对miss rate和访问延迟进行统计如下：

   trace1.txt:

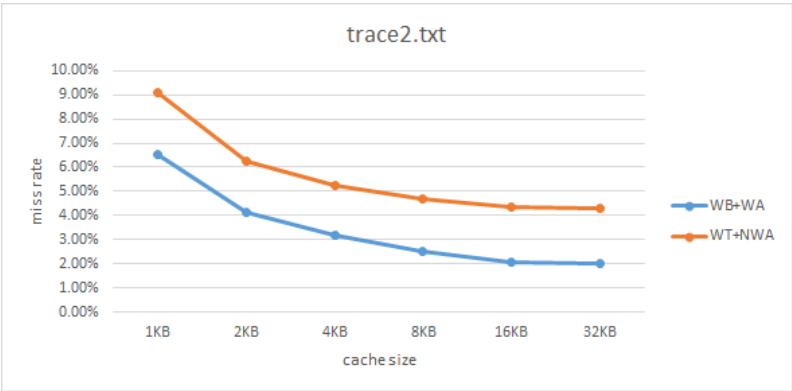
| write back + write allocate | | | write through + no write allocate | | |
|---|---|---|---|---|---|
| cache size | miss rate | latency (ms) | cache size | miss rate | latency (ms) |
| 1KB | 4.03% | 3.92 | 1KB | 5.00% | 12.84 |
| 2KB | 2.36% | 3.27 | 2KB | 3.17% | 12.56 |
| 4KB | 1.80% | 3.05 | 4KB | 2.55% | 12.46 |
| 8KB | 1.48% | 2.93 | 8KB | 2.17% | 12.39 |
| 16KB | 1.10% | 2.75 | 16KB | 1.97% | 12.37 |
| 32KB | 1.06% | 2.64 | 32KB | 1.96% | 12.37 |

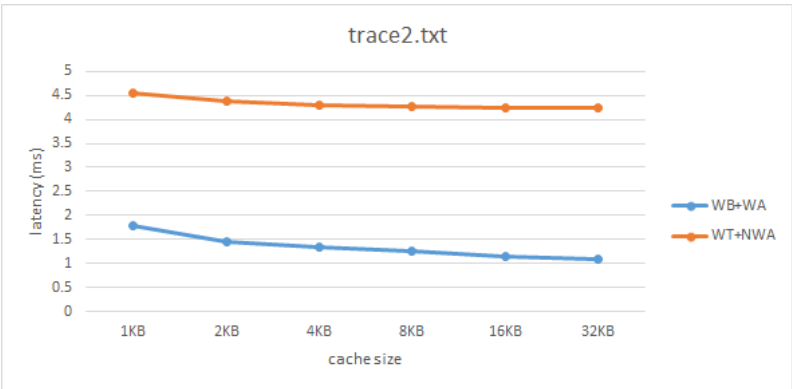





trace2.txt:

| write back + write allocate | | | write through + no write allocate | | |
|---|---|---|---|---|---|
| cache size | miss rate | latency (ms) | cache size | miss rate | latency (ms) |
| 1KB | 6.51% | 1.78 | 1KB | 9.10% | 4.55 |
| 2KB | 4.13% | 1.46 | 2KB | 6.23% | 4.38 |
| 4KB | 3.18% | 1.35 | 4KB | 5.24% | 4.31 |
| 8KB | 2.54% | 1.26 | 8KB | 4.70% | 4.27 |
| 16KB | 2.08% | 1.14 | 16KB | 4.33% | 4.25 |
| 32KB | 2.04% | 1.08 | 32KB | 4.31% | 4.25 |




数据分析：当访存策略不变时，增加cache size有助于降低miss rate并略微降低访存延迟；当cache size不变时，write back + write allocate的访存策略组合带来的性能明显高于write through + no-write allocate的组合，不仅降低了miss rate，更大幅度降低了访存延迟，这证明了write back的延迟写回方法以及write allocate的“先读进cache再写入”的方式都有助于cache性能

的提升。