Computer Organization and Architecture

18 Final Review

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Concept

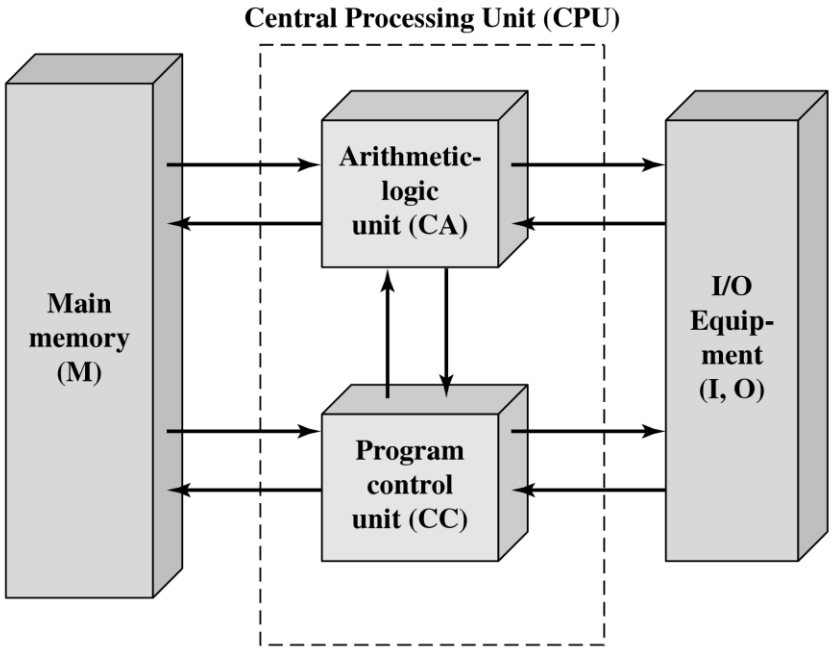
- **Computer**
  - General-purpose electronic digital computer
- **Architecture** (visible to programmer)
  - The attributes have a direct impact on the logical execution of a program
  - Instruction set, the number of bits to represent data type, …
    - E.g.: Is there a multiply instruction?
- **Organization** (transparent to programmer)
  - The operational units and their interconnections
  - Control signals, memory technology, …
    - E.g.: Implement multiply by a hardware unit or repeated addition?

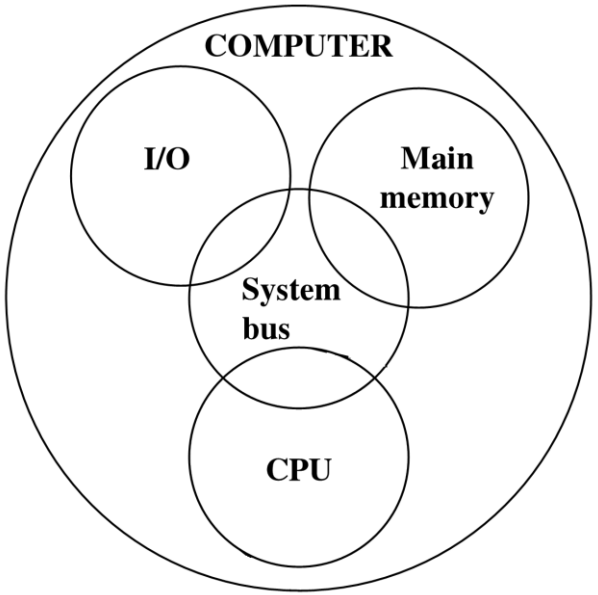
Computer Performance

- Performance evaluation
  - CPU: speed
  - Memory: capacity, speed
  - I/O: speed, capacity
- The main goal / driver is the increase of CPU speed
  - System clock
  - Instruction execution
  - Million Instructions Per Second (MIPS)
  - Million Floating Point Operations Per Second (MFLOPS)

The von Neumann machine

- Idea: main memory storing programs and data





Computer Function

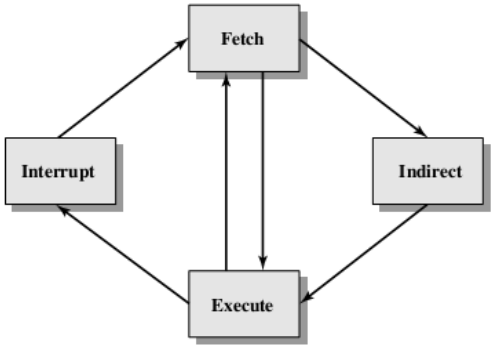
- Execution of a program, which consists of a set of instructions stored in memory

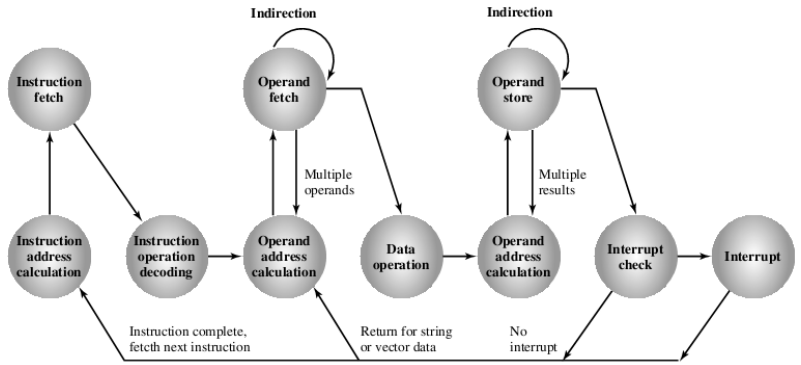
Instruction

- Instruction format
  - Opcode
  - Operand reference: addressing
- Instruction set design

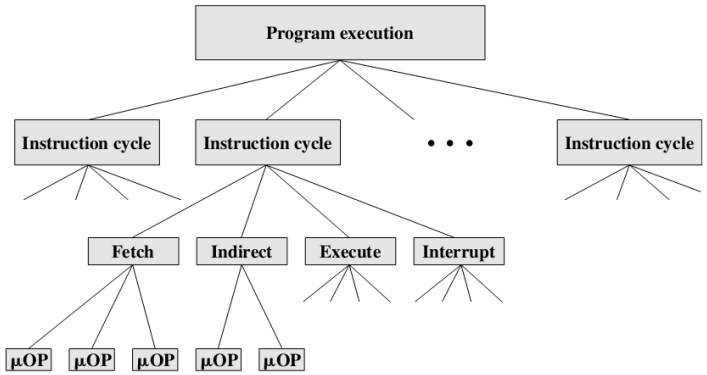
Instruction Execution

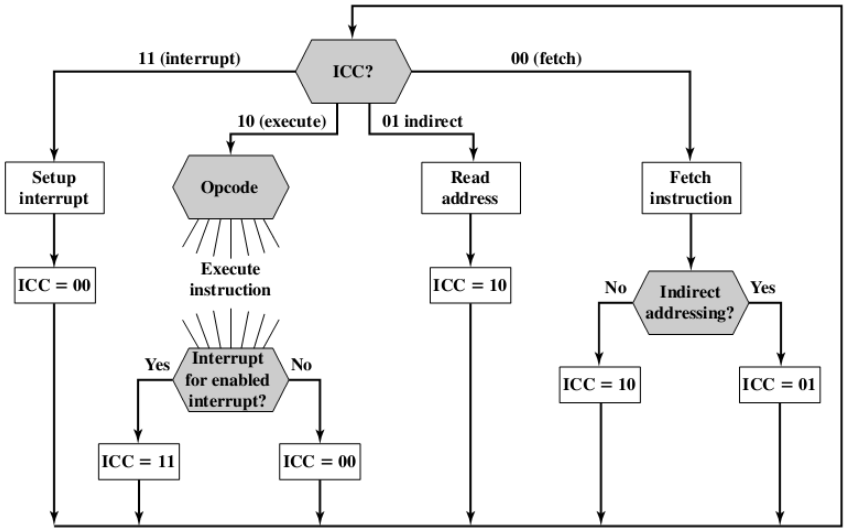
- Instruction cycle





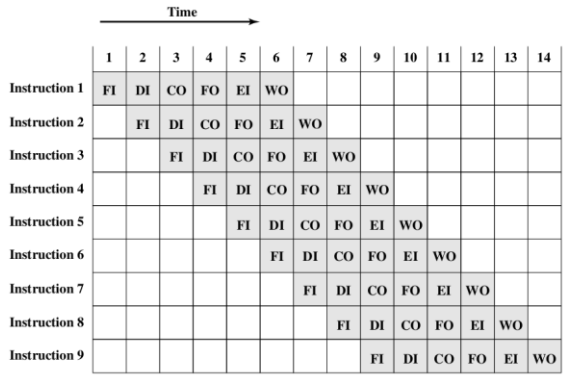
- Micro-operations
  - Concept, different cycles

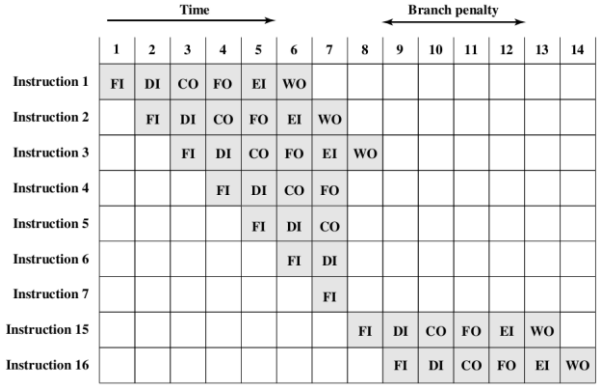




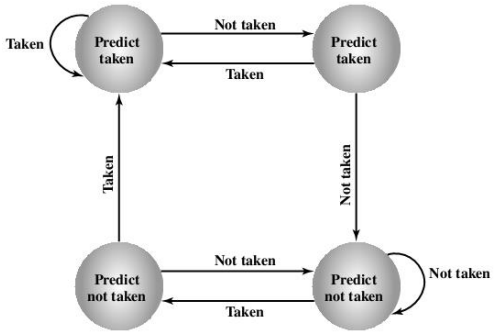
Instruction Pipelining

- Concept





- Performance: speedup factor
- Hazard
  - Structure hazard / hardware resource conflict
  - Data hazard / data dependency
  - Control hazard

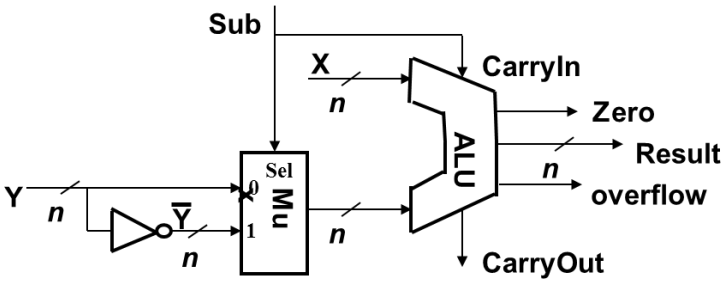


Task of CPU

- The processor does the actual work by executing instructions specified in the program
- Detailed
  - Fetch instruction, Interpret instruction, Fetch data, Process data, Write data
- More detailed
  - ALU: algorithm and logical operations
  - Control unit: generate control signals

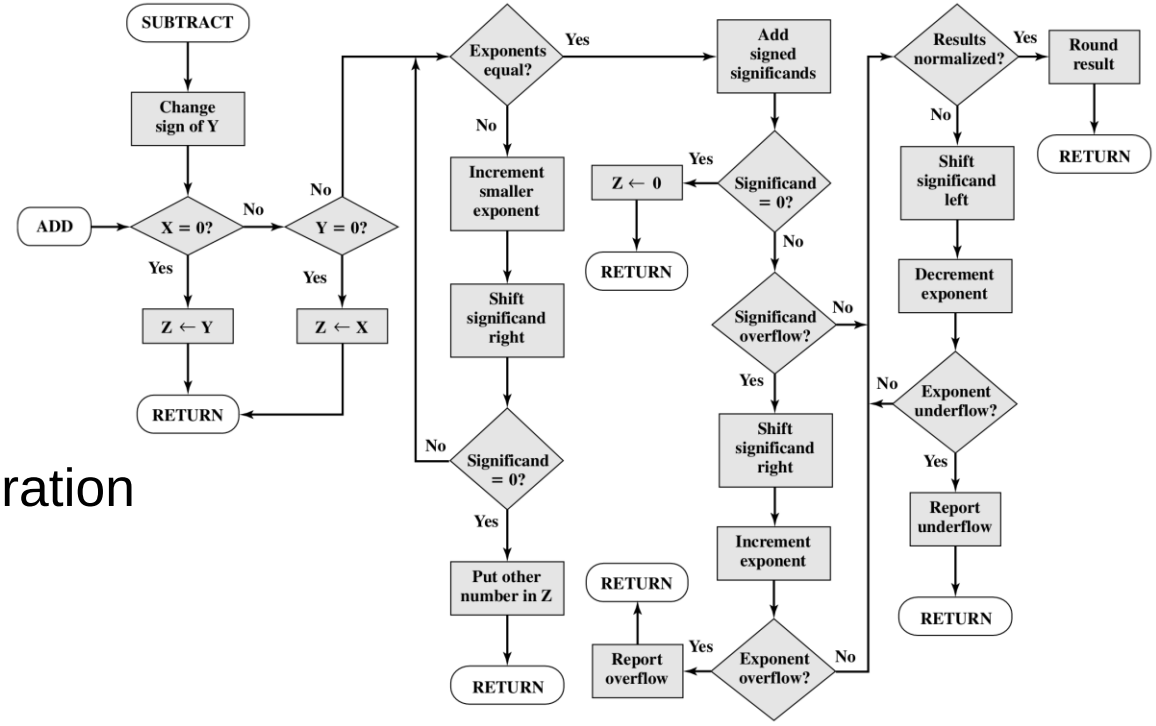
CPU: ALU

- Integer arithmetic
  - Integer representation: complement
  - Full adder, serial carry adder, carry look ahead adder
  - Operation
    - Addition: overflow
    - Subtraction
    - Multiplication: partial product, Booth's algorithm
    - Division: recover remainder, not recover remainder



CPU: ALU (cont.)

- Floating-point arithmetic
  - Floating-point representation
  - Operation
    - Addition
    - Subtraction
    - Multiplication
    - Division
  - Precision consideration
    - Guard bits
    - Rounding

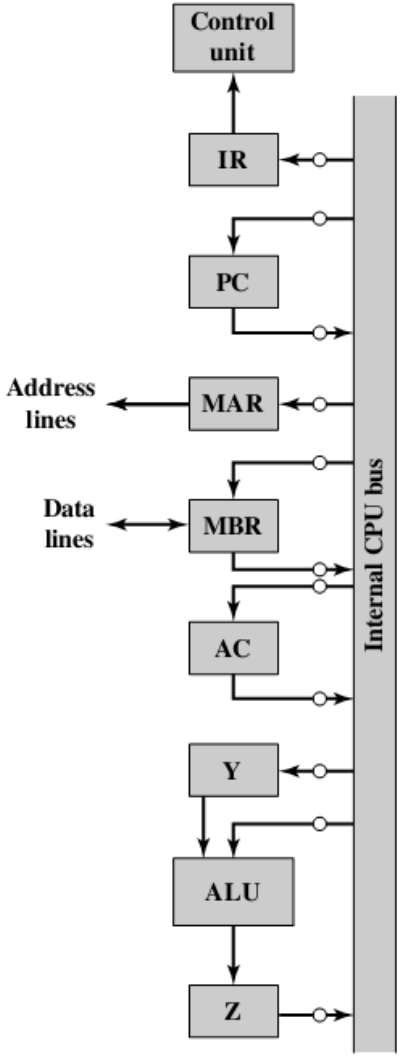


CPU: ALU (cont.)

- Decimal arithmetic
  - Decimal representation
  - Operation
    - Addition
    - Subtraction

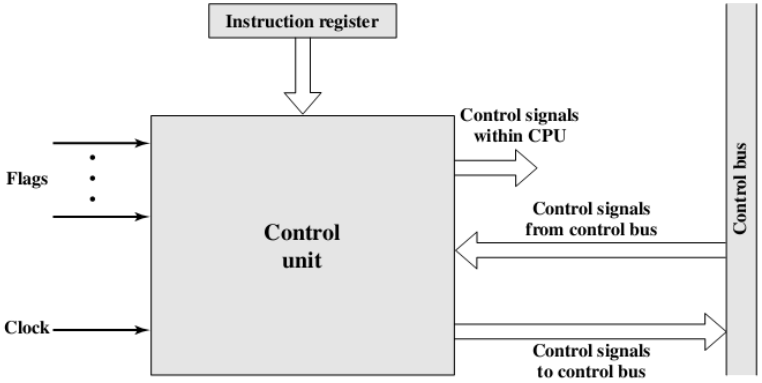
CPU: Register

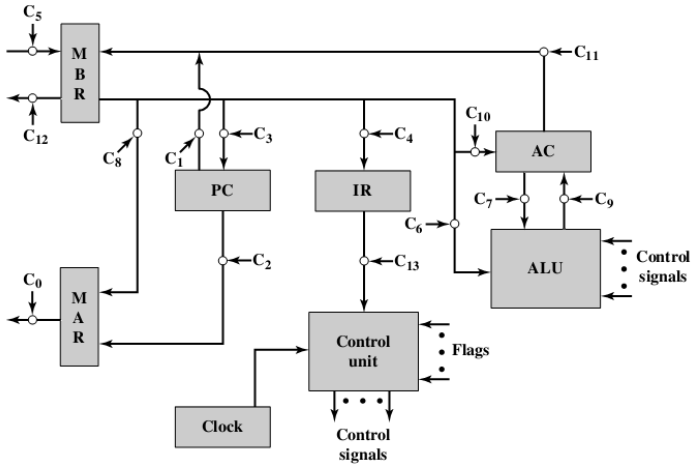
- User-visible registers
  - Enable the machine- or assembly language programmer to minimize main memory references by optimizing use of registers
  - General purpose register, data register, address register, condition codes register
- Control and status registers
  - Used by the control unit to control the operation of the processor and by privileged, operating system programs to control the execution of programs
  - Program counter (PC), instruction register (IR), memory address register (MAR), memory buffer register (MBR), program status word (PSW)



CPU: Control Unit

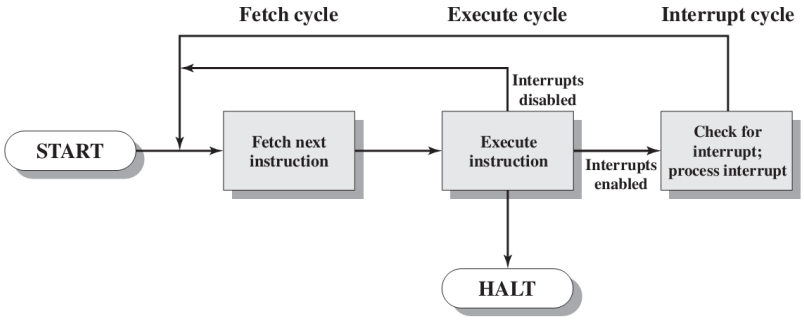
- Input / output of control unit
  - Control signal
- Implementation
  - Hardwired
  - Micro-programmed

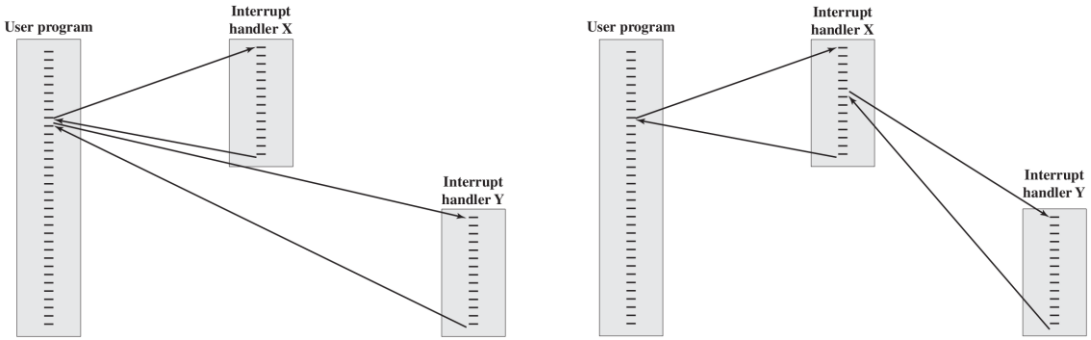




CPU: Interrupt

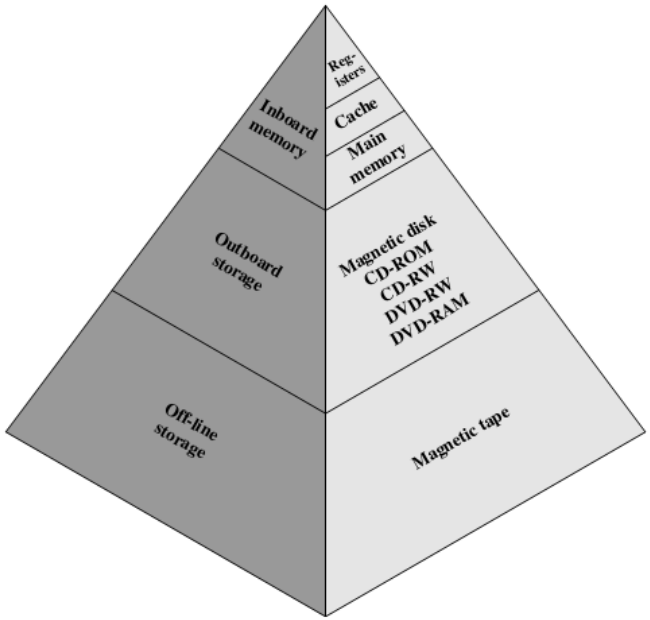
- A mechanism by which other modules (e.g. I/O) may interrupt normal sequence of processing
- Multiple interrupts

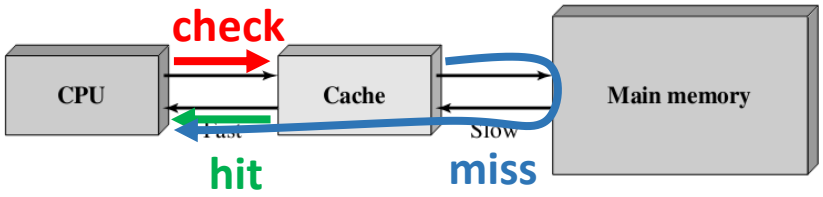




Memory: Cache

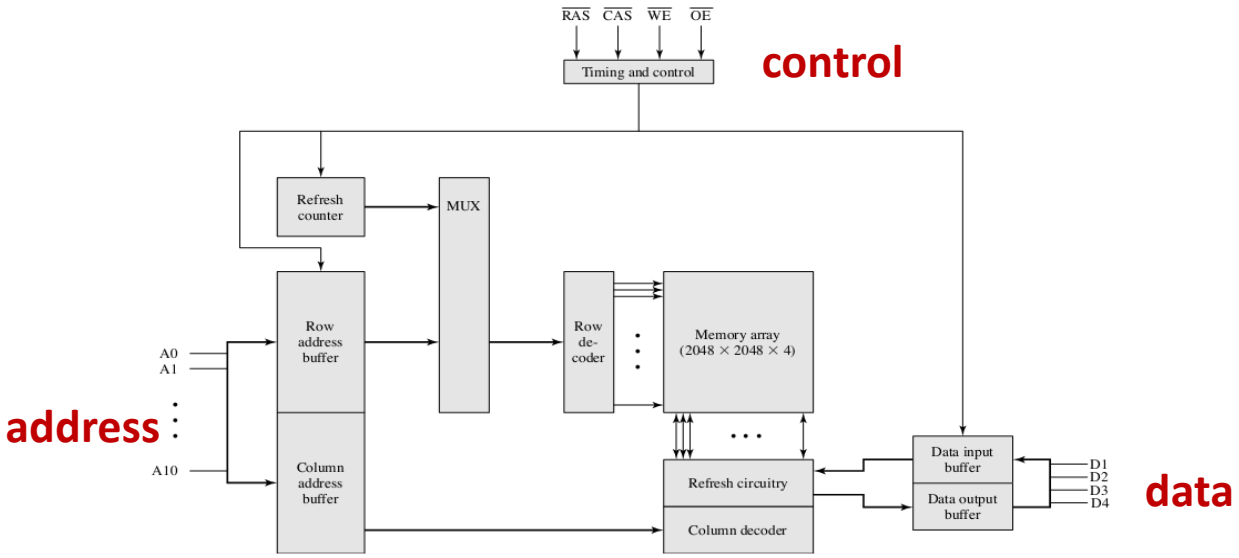
- Principle
- Average access time
- Design elements
  - Cache size
  - Mapping function
  - Replacement algorithm
  - Write policy
  - Line size
  - Number of caches





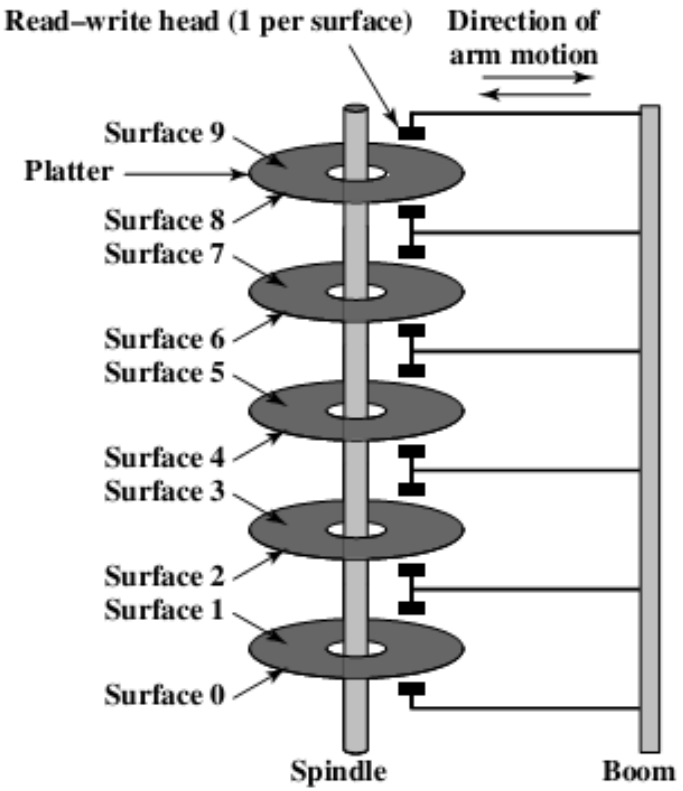
Memory: Main Memory

- Memory cell
- Semiconductor memory types
- Memory array



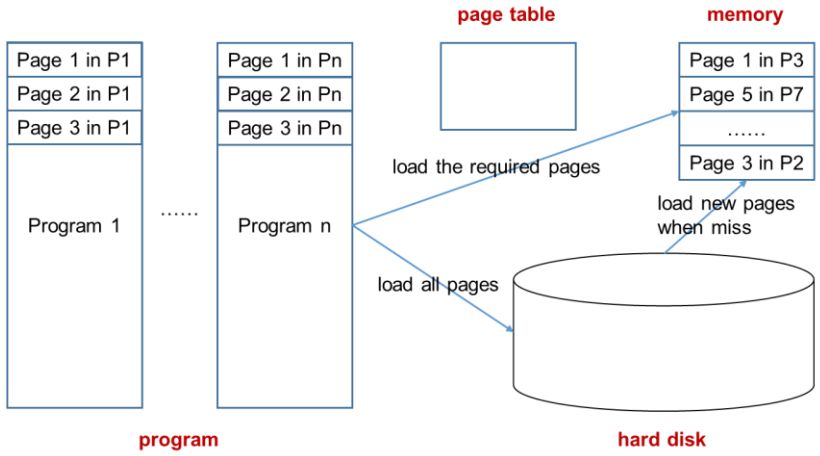
Memory: External Memory

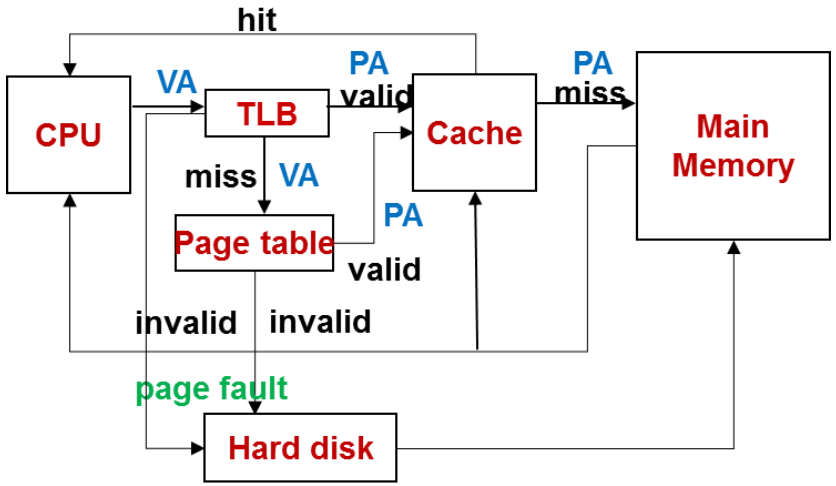
- Magnetic disk
  - Data organization, formatting, read and write mechanism, physical characteristics, timing of a disk transfer
  - Timing of a disk transfer
  - Head scan algorithm
    - FCFS, SSTF, SCAN, C-SCAN, LOOK
- Optical memory
- Magnetic tape
  - Parallel vs. serial



Memory: Virtual Memory

- Partitioning vs. paging
- Virtual memory
  - Size of page
  - Mapping function
  - Write policy
  - TLB





Memory: Error

- Basic idea
  - Add some bits to store additional information for correction
- Process
- Type
  - Parity checking
  - Hamming code
  - Cyclic redundancy check

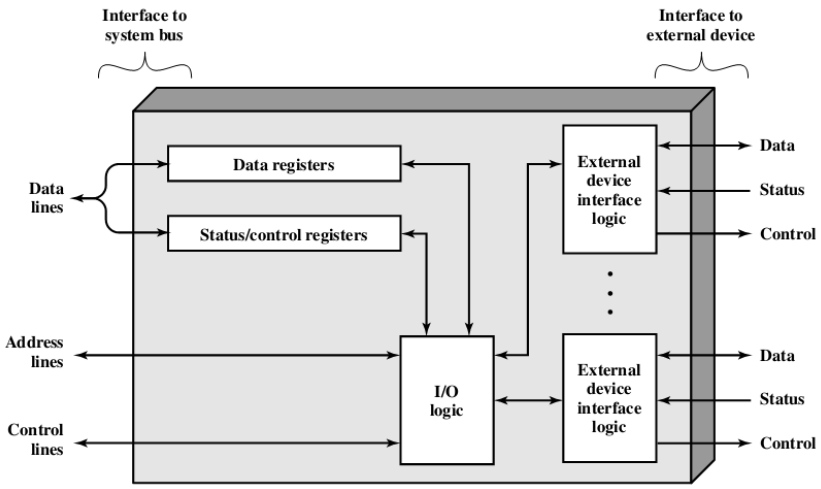
Memory: RAID

- Redundant Array of Independent Disks
- Basic idea
- Characteristic

Category	Level	Description	Disks Required	Data Availability	Large I/O Data Transfer Capacity	Small I/O Request Rate
Striping	0	Nonredundant	N	Lower than single disk	Very high	Very high for both read and write
Mirroring	1	Mirrored	$2N$	Higher than RAID 2, 3, 4, or 5; lower than RAID 6	Higher than single disk for read; similar to single disk for write	Up to twice that of a single disk for read; similar to single disk for write
Parallel access	2	Redundant via Hamming code	$N + m$	Much higher than single disk; comparable to RAID 3, 4, or 5	Highest of all listed alternatives	Approximately twice that of a single disk
	3	Bit-interleaved parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 4, or 5	Highest of all listed alternatives	Approximately twice that of a single disk
Independent access	4	Block-interleaved parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 3, or 5	Similar to RAID 0 for read; significantly lower than single disk for write	Similar to RAID 0 for read; significantly lower than single disk for write
	5	Block-interleaved distributed parity	$N + 1$	Much higher than single disk; comparable to RAID 2, 3, or 4	Similar to RAID 0 for read; lower than single disk for write	Similar to RAID 0 for read; generally lower than single disk for write
	6	Block-interleaved dual distributed parity	$N + 2$	Highest of all listed alternatives	Similar to RAID 0 for read; lower than RAID 5 for write	Similar to RAID 0 for read; significantly lower than RAID 5 for write

I/O

- External device
- I/O module: function, evolution, structure
- I/O operation technique
  - Programmed I/O
  - Interrupt driven I/O
  - Direct memory access
    - Stop CPU, cycle stealing, …
- External interface: serial vs. parallel



Bus

- A communication pathway connecting two or more devices
- Key characteristic
- Component: address, data, control
- Design elements
  - Arbitration: daisy chain, query by a counter, independently request, self selection, collision detection
  - Timing: synchronous, asynchronous, semi-synchronous, split bus transaction
  - Bus bandwidth

Thank You

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