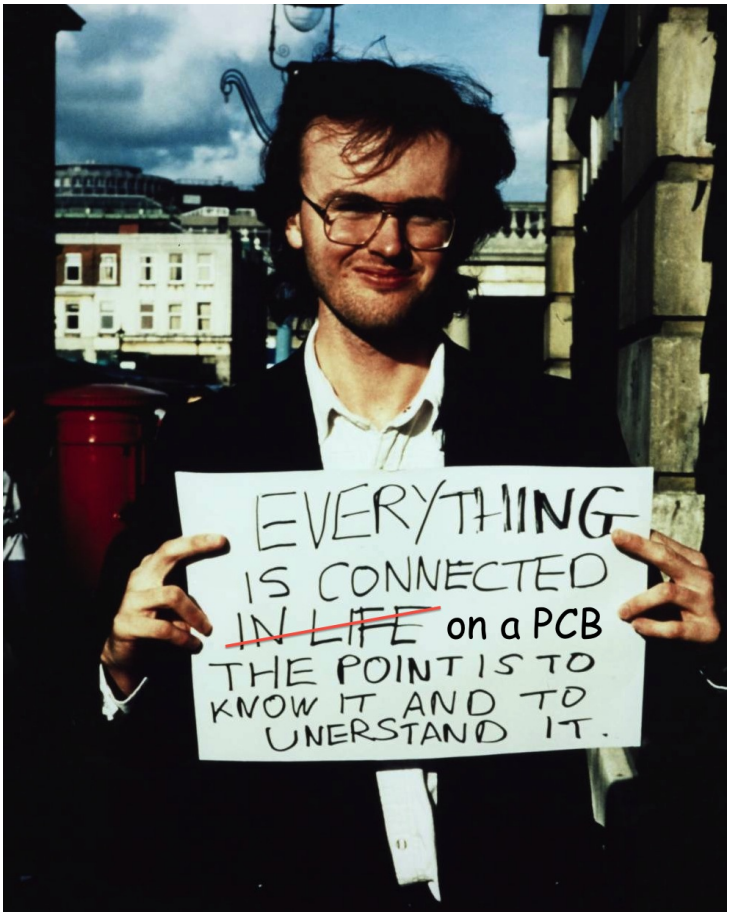
# X7

## PCB Layout

In this lab exercise you will design a two-layer PCB to realise a mixed-signal circuit using EAGLE PCB CAD software. The exercise will lead you through the steps necessary for preparing footprints for devices that are not in the standard libraries, capturing a schematic, and designing the PCB layout. In the subsequent lab, X8, you will build and test your PCB that you design in this exercise.



## Schedule

| | | |
|---|---|---|
| Preparation Time | : | 5 hours |
| Lab Time | : | 3 hours |

## Items provided

| | | |
|---|---|---|
| Tools | : | |
| Components | : | |
| Equipment | : | |
| Software | : | CadSoft EAGLE PCB Design Software, eagleUp, SketchUp |

## Items to bring

Patience

Concentration

Creativity

Identity card

Laboratory logbook

Version: February 24, 2014

Steve R. Gunn and David Oakley
Electronics and Computer Science
University of Southampton

Before entering the laboratory you should read through this document and complete the preparatory tasks detailed in section 2.

> **Academic Integrity** – *If you wish you may undertake the preparation jointly with other students. If you do so it is important that you acknowledge this fact in your logbook. Similarly, you will probably want to use sources from the internet to help answer some of the questions. Again, record any sources in your logbook.*

You will undertake the exercise working with your laboratory partner. However, there is a lot to learn and much to do. As such, it is recommended that you each create one of the footprints in section 2.4 and explain the difference between SMT and THT device design to your partner.

During the exercise you should use your logbook to record your observations, which you can refer to in the future – perhaps to write a formal report on the exercise, or to remind you about the procedures. As such it should be legible, and observations should be clearly referenced to the appropriate part of the exercise. As a guide the ✎ symbol has been used to indicate a mandatory entry in your logbook. However, you should always record additional observations whenever something unexpected occurs, or when you discover something of interest.

## Notation

This document uses the following conventions:

✎ An entry should be made in your logbook

# 1 Introduction

This laboratory exercise aims to:

- Introduce you to mixed-signal PCB design

## 1.1 Outcomes

At the end of the exercise you should be able to:

- Configure the CAD software
- Create new library parts
- Draw schematics
- Understand the concept of layers
- Work with interchangeable grids
- Work with ground fills
- Determine suitable trace widths
- Build print-inductors
- Make good use of the rule checkers
- Understand how to separate analogue and digital elements
- Manually route a two-layer PCB

and optionally

- Produce realistic 3D models of your design

## 1.2 Primer

The following is taken from Steve Jobs folklore:

> *The first Mac prototypes were hand-made using a technique called "wire-wrapping", where each individual signal is routed by wrapping an individual wire around two pins. Burrell wire-wrapped the first prototype himself, and then others were done by Brian Howard and Dan Kottke. But wire-wrapping is time consuming and error prone.*
>
> *By the spring of 1981, the Mac's hardware design was stable enough for us to make a printed circuit board, which would allow us to make prototypes much more quickly. We recruited Collete Askeland from the Apple II group to lay out the board, and after working with Burrell and Brian for a couple of weeks, she taped out the design and sent it off for a limited production run of a few dozen boards.*
>
> *We started having weekly management meetings in June 1981, which were attended by most of the team, where we discussed the issues of the week. At the second or third meeting, Burrell presented an intricate blueprint of the PC board layout, which had already been used to build a few working prototypes, blown up to four times the actual size.*
>
> *Steve started critiquing the layout on a purely aesthetic basis."That part's really pretty", he proclaimed. "But look at the memory chips. That's ugly. The lines are too close together".*
>
> *George Crow, our recently hired analog engineer, interrupted Steve. "Who cares what the PC board looks like? The only thing that's important is how well that it works. Nobody is going to see the PC board."*
>
> *Steve responded strongly. "I'm gonna see it! I want it to be as beautiful as possible, even if it's inside the box. A great carpenter isn't going to use lousy wood for the back of a cabinet, even though nobody's going to see it."*
>
> *George started to argue with Steve, since he wasn't on the team long enough to know that it was a losing battle. Fortunately, Burrell interrupted him.*
>
> *"Well, that was a difficult part to layout because of the memory bus.", Burrell responded. "If we change it, it might not work as well electrically".*
>
> *"OK, I'll tell you what," said Steve. "Let's do another layout to make the board prettier, but if it doesn't work as well, we'll change it back."*
>
> *So we invested another $5,000 or so to make a few boards with a new layout that routed the memory bus in a Steve-approved fashion. But sure enough, the new boards didn't work properly, as Burrell had predicted, so we switched back to the old design for the next run of prototypes.*

### 1.3 Principles

As with all design there are hard and soft constraints that must be met. To help you, the following principles should be used when designing a PCB. They have been ordered in terms of priority:

**Signal integrity** Ultimately your job is to connect the components together with zero impedance traces and no interaction between them – this is an ideal which is impossible to meet.

**Short tracks** All tracks have a finite resistance which is inversely proportional to their width, and a finite inductance which is related to the number of vias and the bending of the traces. Traces laid next to each other will introduce a capacitive and inductive coupling.

**Avoid sharp corners** Sharp outside corners of a bend can cause issues at higher frequencies as the points can act as mini antennas and radiate signals.

**Minimise vias** Vias have inductance.

**Remove least copper** Environmentally it reduces the amount of chemicals involved in manufacture, but it can also be put to good use as a ground or power plane.

**Make good use of the silkscreen** If you are already using it to label parts, it is free to use the remaining space for additional information that might normally be placed in a manual.

**Minimise number of sides to be soldered** Manufacturing costs can be minimised by restricting the soldering to a single side of the PCB.

**Aesthetics** As Steve Jobs rightfully said, a PCB should look beautiful, but not at the expense of signal integrity.

## 2 Preparation

### 2.1 Technology

Answer the following questions:

1. What is the standard thickness of a PCB? 
2. What is the standard thickness of a copper layer on a PCB? 
3. What is a solder mask? 
4. What is a silkscreen? 
5. What is the trace width, and what are the sizes that you will use in this exercise? 
6. What is a ground fill? 
7. What is a via and what size and shape will you use in this exercise? 

## 2.2 CAD Software

Answer the following questions with respect to the EAGLE PCB CAD software:

### Library

8. Explain the concepts of a *device*, a *symbol* and a *package*.
9. How many symbols and packages can a device have?
10. How can you instruct EAGLE to use a new library?

### Schematic

11. How do you add new components to a schematic?
12. There are two methods that can be used to wire the components together in the schematic: a) by drawing a wire between them; b) by giving separate nets the same name. Describe how both of these methods are accomplished.
13. How do you change the value of a component?
14. If you wish to perform the same operation on a number of components, such as moving, how is this achieved?
15. What is the ERC and when should it be used?

### Board

16. What is an autorouter?
17. Which layer determines the outline of the board?
18. Which layers are used for routing the copper traces on a two-layer board?
19. Which layers are used for drawing the silkscreens on a two-layer board?
20. Which layers determine the soldermasks on a two-layer board?
21. Which layers can you use to provide additional design information that will not be used by the board house for production?
22. What is a grid and how are the standard dimensional units configured?
23. What are design rules, and how can you configure them for the board house that you will use?
24. What is the DRC and when should it be used?

## 2.3 Software Configuration

Follow the instructions below to configure the PCB CAD software:

1. Download and install the EAGLE PCB Software.
2. Download the eagle.zip archive containing additional files that you require for the exercise and uncompress under your home directory.
3. Start EAGLE.
4. Select *Options → Directories...* from the menu bar.
5. The archive that you downloaded contains a local copy of additional libraries, design rules, user language programs, scripts, CAM jobs and projects. It is advantageous to separate these from the main program directories, as when you upgrade to a future version they will remain intact. Change each of the lines in the Directories dialog to include your local version before the main version. This way, your libraries will be searched first. For example change the libraries from[1] `$(EAGLEDIR)/lbr` to `$(HOME)/eagle/lbr;$(EAGLEDIR)/lbr`. Repeat for the five remaining directories.
6. Select *Options → User interface...* from the menu bar.
7. Check the *Always vector font* and ensure the the layout background is black and the schematic background is white.

## 2.4 Library Preparation

One of the best things about EAGLE is that there are a large range of components already available to you. However, it is very common that in any design there will be one or two components that do not exist in the standard libraries. Consequently, you will need to create the library part for these devices. In this exercise the buzzer (BZ1), the LCD (LCD1), and the inductor (L1) do not exist and you are required to create these parts. To help you a little the symbols and the devices for these parts have been implemented in the library files `Speaker.lbr`, `Opto.lbr` and `Passives.lbr` in your local EAGLE directory. You are required to implement the package for these devices and then add them to the device and connect them to the symbol. For the preparation you should prepare the buzzer and the LCD; the inductor will be created in the lab.

### 2.4.1 SMT Buzzer Footprint

Open up the copy of the buzzer datasheet and navigate to the page which describes the recommended footprint on the PCB. Open your local copy of the `Speaker.lbr` file from within EAGLE and create a new package called *KSSGJ4D20* by selecting *Library → Package* from the menu. You should now place four SMD pads with the appropriate size and position, using the *Draw → SMD* command.

[1] On a Mac change `$EAGLEDIR/lbr` to `$HOME/eagle/lbr:$EAGLEDIR/lbr`.

Here it is best to use the origin as the centre of the footprint and you can set the grid and units from *View→Grid...*. Draw the silkscreen outline of the buzzer on the *tPlace* layer using the *Draw→Wire* command[2]. Add the buzzer part name on the *tNames* layer by using the *Draw→Text...* command with text *>NAME* and add the buzzer value on the *tValues* layer with text *>VALUE*.

Now go to the device, *Library→Device*, and select BUZZER. Click *New* and select your *KSSGJ4D20* package. Now select *Connect* and tell EAGLE which pins on the symbol connect to which pins on the package. Here, the polarity is not important and you can connect the buzzer either way round. You can connect multiple pins on the package to one on the symbol by using the [SHIFT] key. Save your modified library.

### 2.4.2 THT LCD Footprint

You will now create a footprint for a device that uses through-hole technology. Repeat the steps from the previous section, but using the LCD data sheet, `Opto.lbr` for the library, *NHD-C0216CIZ-FSW-FBW-3V3* for the package name and the *Draw→Pad* command. Use pads with a drill size of **0.6mm** and a diameter of **auto** for the main LCD connections and pads with a drill size of **0.8mm** and a diameter of **auto** for the LED backlight. Draw the outline of the package on the *tPlace* layer as before, or if you prefer, draw it on the *tDocu* layer which will not appear on the silkscreen but can be used for reference in the design stage. Complete the device by selecting the device *NHD-C0216CIZ-FSW-FBW-3V3*, adding your package and connect the pins to the symbol. Save your modified library.

> *You are now about to embark upon the schematic capture of your circuit. There is one very important aspect of* EAGLE *which you should be aware of.* EAGLE *uses two separate files to store the schematic (`.sch`) and the board (`.brd`).* **When using the software you should always have both the schematic window and the board window open at all times.** *If only one is open, changes to one are not communicated to the other and* EAGLE *can get itself into a state whereby it is unable to resolve any differences. As you draw the schematic components will appear on the board. Do not get distracted by this until you have completed the schematic. Package types can easily be changed at a later time.*

## 2.5 Schematic Capture

In the final part of the preparation you will draw the schematic of your circuit (appendix A). To help you get started you have been provided with a partially filled out schematic (figure 1) which can be located in the `eagle/projects/RFID/Rev A` directory. Load up the `rfid.sch` file. Since the `rfid.brd` file exists in this directory EAGLE should also load this. You should check by looking under the *Window* menu. Your task is to fill in the *RFID detector*, *Microcontroller*, *16×2 LCD*, *Input/Output* and complete the *Power Supply*. First tell EAGLE which additional libraries to use by selecting *Library*

[2] To be very professional you should ensure that your lines do not cross the pads, however all board houses will mask out any silkscreen over-running any pads. You will receive a non-fatal error from the DRC if you do not do this.

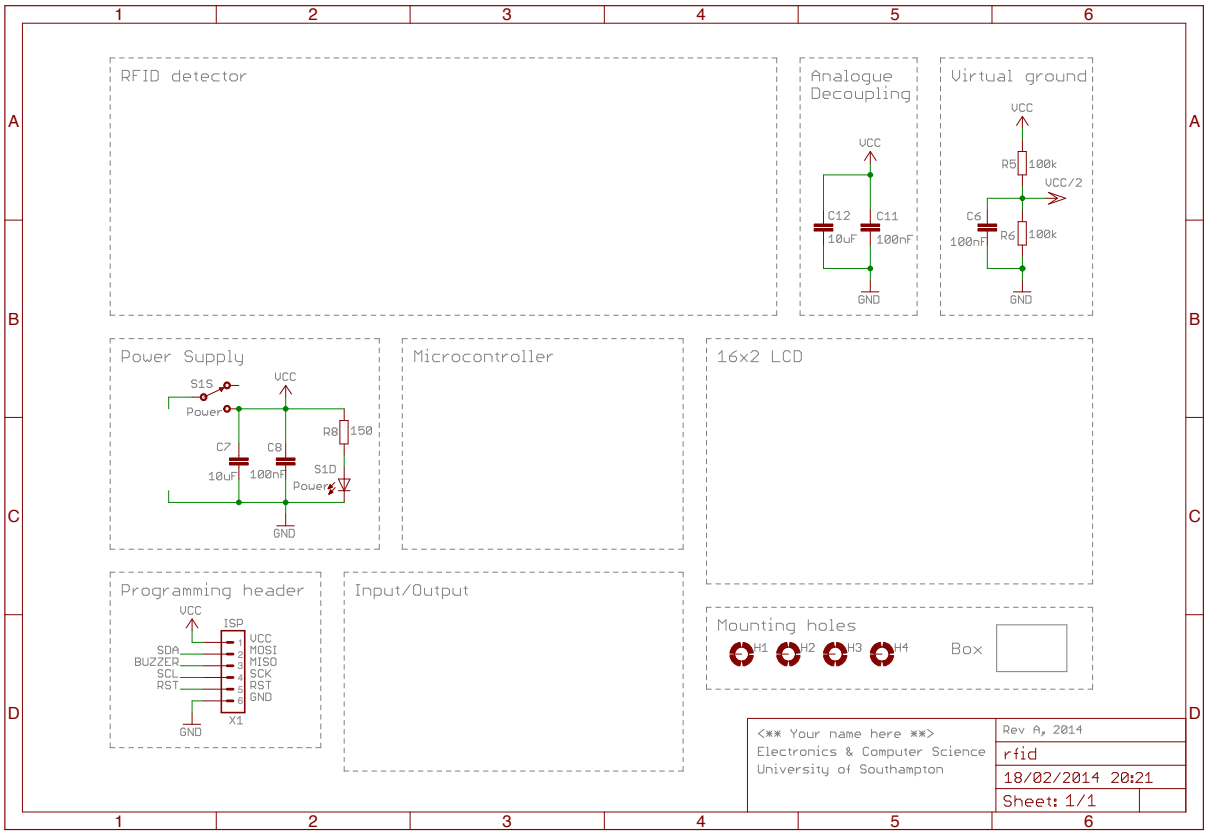



FIGURE 1: Starting schematic

→*Use...*. You should select all of the libraries in your local `eagle/lbr` directory. Now you can add components to the schematic using *Edit*→*Add...*. All of the components that you require are in your local libraries[3] except for the VCC and GND parts, which can be found in the *supply1* library. Alternatively, these can just be copied and pasted from the existing symbols on the schematic. Components can be rotated by right clicking before placement, and mirrored by selecting *Edit*→*Mirror*. Components should be joined together using the *Draw*→*Net* command, and for a more professional look you can use the *Draw*→*Label* command to show the net name and the *Edit*→*Name* command to change the net name; this way wires with the same net name will be connected without having to be joined together, which often aids the readability of a schematic.

Part names and component values can be set using the *Edit*→*Name* and *Edit*→*Value* commands respectively. If you wish to fine tune the position of these you can use the *Edit*→*Smash* command.

You are almost complete, except that it is very easy to leave a wire unconnected or mis-configure something. To help you, EAGLE provides an *Electrical Rule Check (ERC)* to help identify many problems. You should now run this on your completed schematic. You will receive some warnings about power pin connections, missing value for C1A and unconnected pin for the mounting holes. These can be ignored but you should try to resolve any others before arriving at the lab.

When you have finished, zip up your local `eagle` directory and uncompress it under your home directory on your network filestore, so that it will be accessible from the lab machines.

[3] Since they begin with a capital letter they will appear at the top of the library list.

# 3 Laboratory Work

In the laboratory you will design your PCB. There are two main aspects to routing a PCB: component placement and track routing. Placement is typically done manually. Routing can be undertaken manually or with the aid of an auto-router, where the software determines how to connect all of the placed components. Routing is a high-dimensional, non-convex optimisation problem and auto-routers vary in their degree of sophistication and success. The auto-router in EAGLE is not the best and for this exercise you will be using manual routing – this is good experience to understand the challenges involved. Regardless, most production boards will have some manual intervention in the routing aspects. The design typically proceeds with an initial coarse placement of the packages followed by routing. It will then be necessary to adjust the placement of many of the components to accommodate the correct space for the routed tracks.

## 3.1 Software configuration

Perform the following steps:

1. Ensure that all of your local EAGLE files are under your home directory.
2. Repeat the software configuration described in section 2.3 from point 3.
3. Open your `rfid.brd` file.
4. Each board house has its own set of capabilities, such as minimum track width/clearance, minimum via size, etc. In order that EAGLE can verify that your design is compatible with the board house you need to tell it what design rules it should use. To do this select *Edit → Design rules...* and then *Load* the file `PCB-POOL Standard.dru` which can be found under your local `dru` directory. This configures the rules for PCB-POOL where your board will be manufactured.

## 3.2 Dimensional Units

PCB design is one discipline which has not been entirely metricised. Many component packages are designed using imperial spacing and many using the metric system. As such you must become comfortable working simultaneously with both measurement systems. The standard units which are commonly employed are **inches** or **mm**, and often it is more convenient to work with **mils** (1/1000 **inch**). In this exercise you will be using **mils** for trace widths and **mm** for drill sizes.

## 3.3 Board outline

The board outline describes the physical shape and size of the PCB. It is drawn on the *Dimension* layer and should be drawn with a zero width line. To help you, this has already been done for you. Right angle exterior corners are fine, but rounded corners make handling of the PCB more comfortable. Interior corners should always be rounded as the board house will have a minimum milling radius. The board shape is fixed for this exercise to match the enclosure and should not be changed.

### 3.4 Mounting holes

A PCB will typically need to be fixed inside an enclosure. To accomplish this four **M3** mounting holes have been placed on the board. In this exercise these match up with the **0.2in** spaced dots on the base of the enclosure. If you wish you may move these, but only on a **0.2in** grid. This is easily done by first setting the grid to **0.2in** and then any movement will be restricted to a valid location.

### 3.5 Packages

Many components have multiple packages. At this point you should review all of the packages on the board and confirm that they match up with the components that you will be using (appendix B). You can use the *View→Info* tool to see the current package. At this point the correct package for L1 has not been created and you should select the *SDR0403* package; when it needs to be changed you can use the *Edit→Change...* command.

### 3.6 Placement

Here are the design requirements:

- Divide the board area into three regions: antenna (40%), batteries (20%) and circuitry (40%)
- LCD on the top layer
- Antenna on top and/or bottom layer
- Remaining components on the bottom layer
- S1 and S2 should be placed symmetrically about the centre of the board and **48mm** apart
- BZ1 and X1 should be placed near the edge of the board
- Sub-divide the circuitry area into two separate regions for analogue and digital elements

> *Do not rush this part of the exercise. Good placement is the secret to successful PCB design. However, many aspects will come with experience and you should aim to complete the placement after one hour in the laboratory.*

On viewing your board you will see that all of the components with the exception of S1 are not in the correct position. Begin by locating S2, LCD1, BZ1 and X1. By default components are placed on the top layer. They can be moved to bottom layer by using the *Edit→Mirror* command. You can use the *View→Info* tool to see the precise properties of an object and can adjust the position from there by directly typing in the co-ordinates – sometimes this is preferable to moving with the mouse and grid.

Set the grid to **0.025in** or **25mil**. Most of the components that you are placing are 0603 passives and a good rule of thumb is to place these on a grid of **0.125in** × **0.175in** (or 5×7 on a **25 mil** grid); this gives enough space for routing, hand soldering and labelling the component values on the silkscreen.

Now that you have located the I/O components this should give you some idea of where to locate the digital section (IC2, R9-12, C7-10) whilst keeping the routing short, because many of the digital signals connect to X1 and LCD1. The signals to be routed are shown as a ratsnest. After you have moved components you can run the *Tools → Ratsnest* command to update the connections. The decoupling capacitors (C7, C8) should be placed as close as possible to the power pins on IC2.

Now locate the analogue section (C1-6, C11, C12, R1-6, D1, IC1). Again the decoupling capacitors (C11, C12) should be placed as close as possible to the power pins on IC1, and the other components should be arranged to keep the routing as short as possible.

## 3.7 Routing

Now we come on to the detailed work of wiring up all of the components. You are working with a two-layer board which gives you the opportunity to switch tracks back and forth on both sides of the PCB by the use of vias to ease the challenges in routing. For this exercise you should use a round via with a **0.5mm** drill and **auto** diameter. The tracks should have a trace width of **10mil** for signals and any power routing that cannot be accommodated by the ground and power planes should use a **20mil** trace width (appendix C and D give details on how these sizes are justified). It is important to avoid sharp corners in the routing and therefore all tracks should be routed with 45° routing.

Manual routing is achieved with the *Edit → Route* command, and errors can be corrected with the *Edit → Ripup* command. Select the *Edit → Route* command and you will see a toolbar appear. Ensure that the via size and shape are set correctly and select between either *Wire Bend Style 1* or *Wire Bend Style 3* which enforce 45° routing. You will need to select one as you leave a component and switch to the other in the final move before connecting to the second component to ensure that tracks leave and arrive at the centre of the component pads. When a net has more than two connections you will need to use *Wire Bend Style 0* or *Wire Bend Style 4* to form a 'T' junction. If you need to switch layers in order to route your track you can use the middle mouse button to achieve this.

Keep the **0.025in** grid that you set in the placement operation, but you might like to add **0.0125in** as the alternative grid, which can be activated by holding down the [ALT] key.

> *At this point do not connect any of the power and ground connections as you will use the plane fill feature in section 3.8 to achieve this.*

Begin by routing the digital section and try to keep the tracks as short as possible, the number of bends and vias to a minimum.

Now move to routing the analogue section using the same techniques.

You can use the *Tools → Ratsnest* command to update and report the number of signals left to route.

### 3.8 Ground and Power Planes

*One of the challenges in PCB design is to provide a low impedance ground connection to all components to avoid ground bounce in digital circuits and provide a good reference signal in analogue circuits. A ground plane is a good way to meet this challenge. On boards with four or more layers you will often find dedicated layers to power and ground.*

You will use a ground plane on the bottom layer of the PCB and a power plane on the top layer to make the power connections. Since these planes will interfere with the operation of the antenna they should not cover the antenna area. It is optional if you want to cover the battery area with them.

EAGLE provides the ability to fill in an entire area of copper leaving an isolation gap around any existing tracks. You can use the *Draw → Polygon* command to draw these on the top and bottom layers. By naming the plane with the *Edit → Name* command it is possible to connect the plane to a net in the schematic.

Draw a polygon on the top layer surrounding the circuitry area and name it VCC. Draw an identical polygon on the bottom layer and name it GND. When done, select the *Tools → Ratsnest* command to activate the fills[4].

To complete the power routing you can now add vias and name them VCC to drop down power connections at the appropriate point in the circuit.

### 3.9 DRC

With the exception of the inductor, your board should now be routed. It is a good time to use the *Design Rule Checker* to validate your design meets the board house requirements. Run the command *Tools → DRC...*. At this point you should aim to remove all errors. However, if you receive errors related to your silkscreen over-running the stop mask you may ignore these for now.

### 3.10 Print Inductor

The inductor, L1, acts as the antenna of the device to inductively couple with the tag. Here you will draw a spiral track on the PCB of between 50-150 turns to create an inductive coupler. The actual value is not too critical as you can tune your circuit by adjusting the value of C1 and C1A; when you come to testing in lab X8 we will provide you with a range of capacitors to do this. However, to give you some idea of what inductance value you will get you can use Wheeler's approximation,

$$L = 31.33\mu_0 N^2 \frac{r^2}{8r + 11w}$$

[4] When EAGLE loads a board, fills are not activated and you will need to run the *Tools → Ratsnest* command to see them.

where $\mu_0 \approx 1.26 \times 10^{-6}$, $N$ is the number of turns, $r$ is the mean radius (m) and $w$ is the trace width (m). A higher inductance will potentially give your circuit better range, but at the expense of being more sensitive to tuning.

You will add a new package to the inductor library for your antenna. Start by measuring how much space you have in the antenna area on your PCB. Now open up the library `Passives.lbr` and create a new package called *ANTENNA*. In this package draw a rectangular outline on the *tDocu* layer, centred on the origin, equivalent to the antenna area.

EAGLE provides a *Tools→Calculate print inductor...* command to do the hard work for you. You can use either the *Ferrit* or *Spiral* models and you will need to experiment with the parameters to get the correct size and number of turns; if you use the *Ferrit* make sure to delete the rectangles from the dimension layer after you are done. You may prefer the *Edit→Group* and *Edit→Delete* commands to retry different parameters over the *Edit→Undo* command. It is advisable not to spiral right to the centre, but to leave 10-20% of the total area empty.

When you have a suitable shape you have the option of doubling your inductance, by copying and mirroring the spiral onto the bottom layer. To finish up you should provide two pads (**0.6mm** drill, **auto** diameter) for your connections. You will also need a single via to route the centre back to a pad, or if you have spiralled both sides, to connect the two spirals in the centre. Use a pad with **0.5mm** drill and **auto** diameter. Go to the inductor device, add your new package, and make the two connections.

Save your library. Go back to your board and tell EAGLE to reload the library by using the *Library→Update...* and select your modified `Passives.lbr` file. You can now use the *Edit→Change...* command to select your new package for L1.

### 3.11 Test Points

During testing it is often necessary to inspect signals in the circuit. To aid this task it is possible to add test points to the PCB for probing or attaching wires. In your design you will need to inspect the signals either side of L1 and at the DEMOD input to the microcontroller during testing. You can use the pads on the inductor as test points, so you only need to add a test point for DEMOD and a test point for GND. Go back to the schematic and add these two test points from the *Testpoint* library. Switch to the board view and locate them in a suitable position, close to the relevant signals and if possible with access from both sides of the board.

### 3.12 Silkscreen

The top silkscreen is produced from the elements on the *tPlace* and *tNames* layers and *bPlace* and *bNames* for the bottom silkscreen. Your part names are probably in a mess, so you can move these by using the *Edit→Smash* command and then *Edit→Move*. If you cannot get the name into the correct orientation, check that the *Mirror* and *Spin* attributes are checked using the *View→Info* command.

Use the *Draw→Text...* tool to add your names, revision and date to the *tPlace* layer. Also label the two pads of the inductor with test point labels.

### 3.13 Finishing up

It is good practice to *tent your vias* which lets the solder mask run over them. To do this go to *Edit → Design rules...* and select the *Masks* tab. Change the *Limit* to **0.55mm** which will cover any hole smaller than this with the stop mask.

Run the *Tools → Ratsnest* a final time and confirm that there are no more airwires left to route as reported in the status bar.

Run the *Tools → DRC...* a final time and satisfy yourself that any remaining errors are acceptable. You will likely receive three overlap errors from your print inductor which can be ignored.

Finally, you should print out your board at true size and confirm that the major parts match up with their footprints. To do this run the *File → Run ULP...* command and select the file `cam2print.ulp`, and then the file `print-tb-layout.cam`. This will create two life-size PDFs of the top and bottom of the board. Print them out – you might be surprised how small your board is after you have been staring at it magnified for many hours!

### 3.14 Board Submission

Historically board houses only accepted designs in Gerber format. This can be done in EAGLE by using the CAM processor. However, nowadays most board houses will accept an EAGLE `.brd` file, which is what you will submit. One submission should be made per lab pair to the hand-in system by 16:00, 5 March. You are required to submit: `rfid.brd`, `rfid.sch`, `Passives.lbr`, `Speaker.lbr` and `Opto.lbr`.

# 4 Optional Additional Work

## 4.1 Silkscreen Image

It is also possible to add images that are stored as bitmaps to the silkscreen using `import-bmp.ulp`.

## 4.2 Bill of Materials

The bill of materials in appendix B was exported using `bom.ulp`. You can also export a simple parts list by using the *File → Export* and selecting *Partlist*.

## 4.3 3D Visualisation

Although PCBs are inherently two-dimensional the components and any enclosure are not. It can be helpful to visualise how everything will fit together in three dimensions. To achieve this visualisation you can use the eagleUp tool and SketchUp Make. These have been configured on the laboratory machines, but if you wish to set this up on your own machine you can follow the eagleUp installation instructions.

On the lab machines go to *Window → Control Panel*, select the *User Language Programs* and select the second *ulp* folder (system). Navigate and find the `eagleUp_export.ulp` and execute it. Select *set for Windows* and change the models path to point to your local `skp` directory which contains all of the models for your components. Click OK. Select 1200dpi and click OK.

Start SketchUp and select the *Engineering (Metric)* template. For best resolution go to *SketchUp → Preferences* and ensure that all of the options under the *OpenGL* item are checked. Select *Plugins → eagleUp* and select the file `rfid.eup` in the `eagleUp` directory under your board design. Wait a little bit . . . and you should see a model similar to that shown in figure 2. It is possible to select and hide or delete the case to fully inspect your board.

## 4.4 3D Rendering

If you really want to go to extremes you can try the Kerkythea tool for life-like rendering of your SketchUp models.

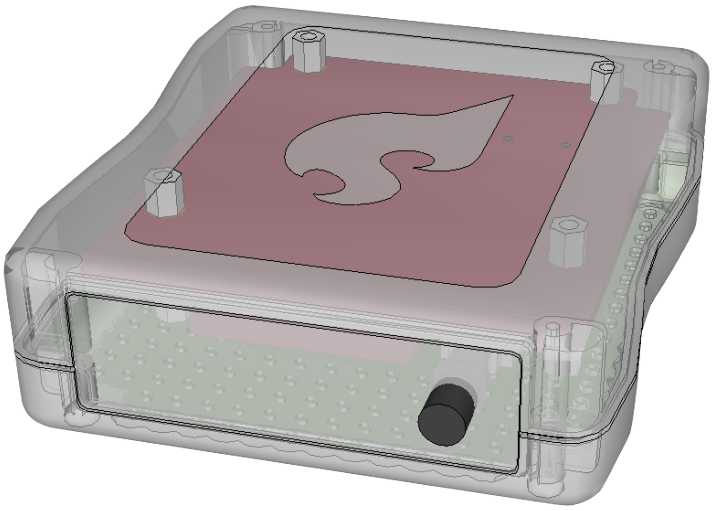
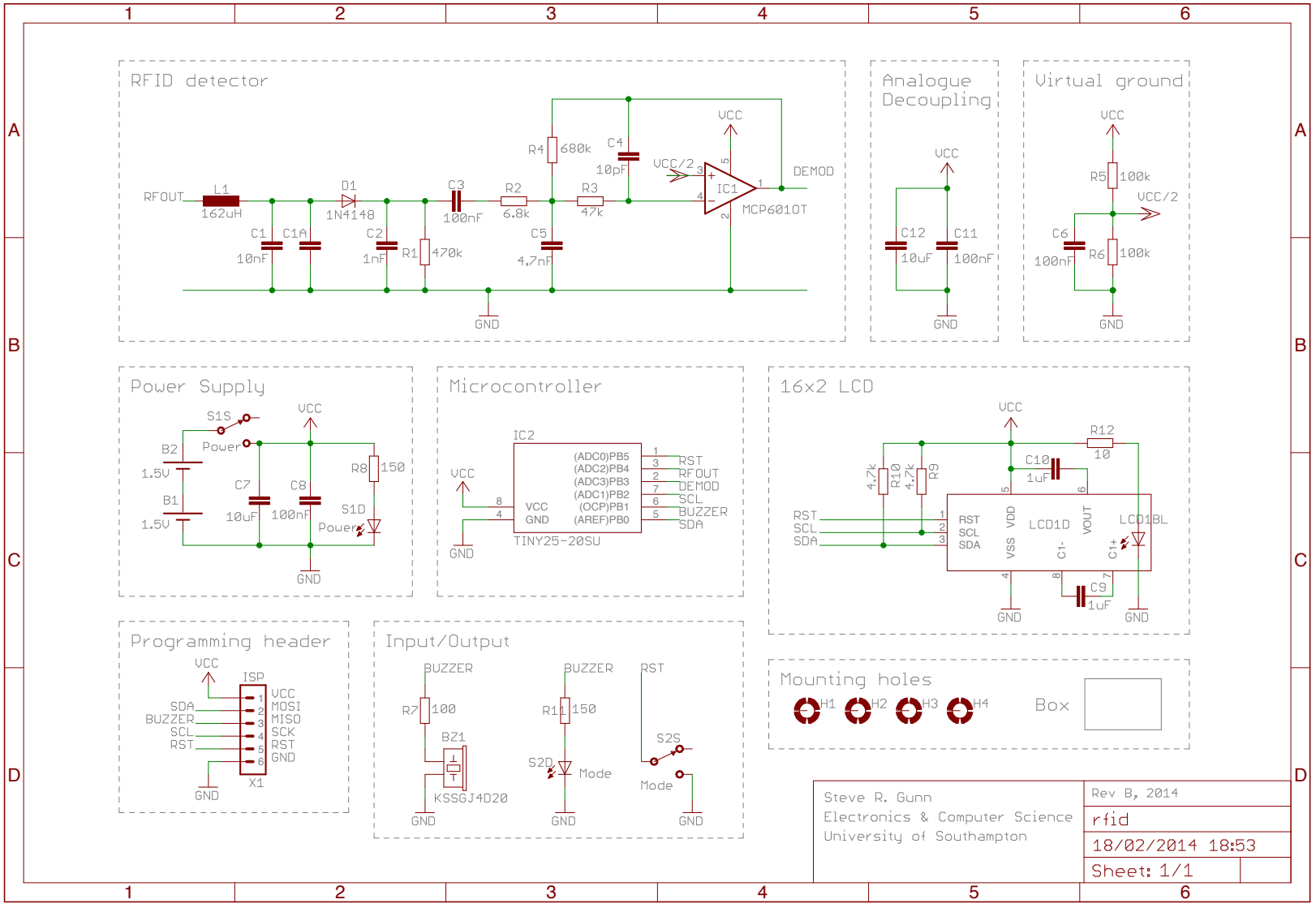


FIGURE 2: Final Product

# A Schematic


RFID detector
RFOUT
L1
162uH
D1
1N4148
C1
10nF
C1A
C2
1nF
R1
470k
C3
100nF
R2
6.8k
R4
680k
C4
10pF
R3
47k
C5
4.7nF
VCC/2
IC1
MCP6010T
VCC
DEMOD
GND
Analogue Decoupling
C12
10uF
C11
100nF
Virtual ground
R5
100k
R6
100k
C6
100nF
Power Supply
S1S
B2
1.5V
B1
1.5V
Power
C7
10uF
C8
100nF
R8
150
S1D
Microcontroller
IC2
TINY25-20SU
(ADC0)PB5
(ADC2)PB4
(ADC3)PB3
(ADC1)PB2
(OCP)PB1
(AREF)PB0
RST
RFOUT
DEMOD
SCL
BUZZER
SDA
16x2 LCD
R12
10
C10
1uF
R10
4.7k
R9
4.7k
RST
SCL
SDA
LCD1D
LCD1BL
VSS
VDD
C1-
VOUT
C1+
C9
1uF
Programming header
ISP
X1
MOSI
MISO
SCK
Input/Output
R7
100
BZ1
KSSGJ4D20
R11
150
S2D
Mode
S2S
Mounting holes
H1
H2
H3
H4
Box
Steve R. Gunn
Electronics & Computer Science
University of Southampton
Rev B, 2014
rfid
18/02/2014 18:53
Sheet: 1/1

## B Bill of Materials

| Qty | Value | Type | Parts | Package | Supplier | Supplier Part No. |
|---|---|---|---|---|---|---|
| 4 | | Battery | B1, B2 | AAA-HOLDER-SMT-CLIPS | Mouser | 534-055 |
| 1 | KSSGJ4D20 | Buzzer | BZ1 | KSSGJ4D20 | Onecall | 2215091 |
| 1 | 10nF | Capacitor | C1 | C0603 | Onecall | 1759003 |
| 2 | 1$\mu$F | Capacitor | C9, C10 | C0603 | Onecall | 1759399 |
| 4 | 100nF | Capacitor | C3, C6, C8, C11 | C0603 | Onecall | 1759016 |
| 2 | 10$\mu$F | Capacitor | C7, C12 | C0603 | Onecall | 1759393 |
| 1 | 1nF | Capacitor | C2 | C0603 | Onecall | 1759088 |
| 1 | 10pF | Capacitor | C4 | C0603 | Onecall | 1759053 |
| 1 | 4.7nF | Capacitor | C5 | C0603 | Onecall | 1759098 |
| 1 | 1N4148 | Diode | D1 | SOD123 | Onecall | 1469425 |
| 1 | MCP601OT | Op-amp | IC1 | SOT23-5 | Onecall | 9758631 |
| 1 | TINY25-20SU | Microcontroller | IC2 | SOIC8 | Onecall | 1636951 |
| 1 | 162$\mu$H | Inductor | L1 | Integrated on PCB | | |
| 1 | | Display | LCD1 | NHD-C0216CIZ-FSW-3V3 | Mouser | 763-C0216CIZFSWFBW3V |
| 1 | 470kΩ | Resistor | R1 | R0603 | Onecall | 2333613 |
| 2 | 4.7kΩ | Resistor | R9, R10 | R0603 | Onecall | 2008340 |
| 2 | 150Ω | Resistor | R8, R11 | R0603 | Onecall | 2333549 |
| 1 | 10Ω | Resistor | R12 | R0603 | Onecall | 2321756 |
| 1 | 6.8kΩ | Resistor | R2 | R0603 | Onecall | 2333614 |
| 1 | 47kΩ | Resistor | R3 | R0603 | Onecall | 2333548 |
| 1 | 680kΩ | Resistor | R4 | R0603 | Onecall | 2335945 |
| 2 | 100kΩ | Resistor | R5, R6 | R0603 | Onecall | 2333553 |
| 1 | 100Ω | Resistor | R7 | R0603 | Onecall | 2008332 |
| 1 | | Switch | S1 | MCPLSL-P26-MZ-CS | Onecall | 2146936 |
| 1 | | Switch | S2 | MCPLS7-P23-MZ-CS | Onecall | 2146923 |
| 1 | | Switch Cap | S1 | 957C00000 | Mouser | 611-957C00000 |
| 1 | | Switch Cap | S2 | 956C02000 | Digikey | CKN9457-ND |
| 1 | | Connector | X1 | MH06-1-SMD | Toby | TSM-106-01-T-SH-A |
| 1 | | Box | | Clear case | Sparkfun | WIG-08632 |
| 4 | M3-18mm | Stand-off | | Female-Male | Toby | TP-18 |
| 4 | M3-6mm | Stand-off | | Female-Female | Toby | HP-6 |

# C Continuous current capacity

The relationship of current and change in temperature of a PCB trace can be approximated[5] as

$$I \approx k w^{\alpha} d^{\beta} \triangle^{\gamma}$$

where $I$ is the current (A), $w$ is the trace width (m), $d$ is the trace thickness (m), $\triangle$ is the temperature change (K), $\alpha = 0.76, \beta = 0.54, \gamma = 0.44$ and $k = 29840$.[6]

## C.1 Trace

For a two-layer board, 1oz copper (35$\mu$m), a tolerable increase in temperature of $\triangle = 15$, and expressing $w$ in units of **mil**, the formula can be simplified to,

$$I \approx \frac{w^{\alpha}}{8}$$

Hence, a 10mil trace can carry a 0.7A current, and a 20mil trace 1.2A.

## C.2 Via

A simple approximation equates a cylindrical via of drill diameter $v$ with a trace of width $\pi v$. Assuming a plating thickness of 35$\mu$m and noting that the plating is rarely as uniform as a track we derate the formula by 40% to give an expression in terms of the drill diameter, $v$, in **mm** as

$$I \approx 3 v^{\alpha}$$

Hence, a via with a 0.5mm drill can carry a 1.8A current.

[5] Temperature Rise in PCB Traces, Douglas Brooks, UltraCAD Design, Inc., 1998.

[6] For interior layers on multi-layer boards a derating of 50% is recommended to compensate for the poorer thermal characteristics of these layers.

# D Resistance

The resistance of a conductor can be calculated using

$$R \approx \rho \frac{l}{wd} (1 + \theta(T - 20))$$

where $R$ is the resistance ($\Omega$), $\rho$ is the resistivity ($\Omega$m), $l$ is the length (m), $w$ is the width (m), $d$ is the thickness (m), $\theta$ is the temperature coefficient ($K^{-1}$) and $T$ is the temperature (K).

For copper $\rho \approx 1.7 \times 10^{-8}$ and $\theta \approx 0.0039$.

## D.1 Trace

At room temperature, $T = 20$, using 1oz copper (35$\mu$m), the resistance simplifies to

$$R \approx \frac{1}{2000} \frac{l}{w}$$

where the ratio can be computed using any consistent unit. Hence, a 10mil trace has $R \approx 50$m$\Omega$/inch.

## D.2 Via

In practice plated copper has a higher resistivity than pure copper and $\rho \approx 1.9 \times 10^{-8}$ is more realistic. For a via of length 1.6mm on a two-layer board, with drill diameter, $v$, in **mm**

$$R \approx \frac{1}{4000} \frac{1}{v}$$

Hence, a 0.5mm via has a resistance of approximately 0.5m$\Omega$.