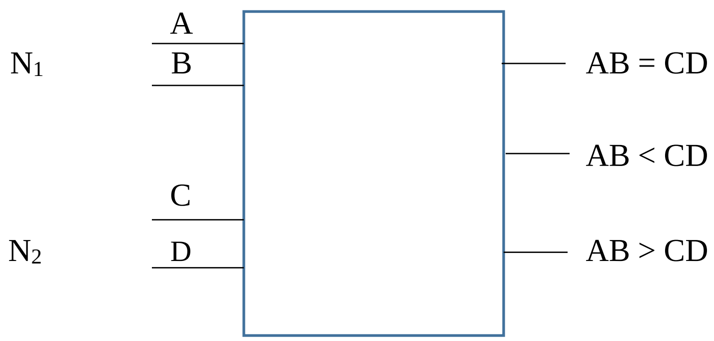
Two Bit Comparator Circuit

Design a circuit that takes as input two 2-bit numbers N_1 and N_2 to be compared and generates three outputs:- one output for $N_1=N_2$, one for $N_1< N_2$ and one for $N_1>N_2$.

The outputs are logic 1 if the corresponding condition is true and logic 0 otherwise.

A block diagram of the circuit is given below:-



The simplest way to describe the behaviour of the functions is with a truth table:-

A	**B**	**C**	**D**	**F_{eq}**	**F_{lt}**	**F_{gt}**
0	**0**	**0**	**0**	**1**	**0**	**0**
0	0	0	1	0	1	0
0	0	1	0	0	1	0
0	0	1	1	0	1	0
0	**1**	**0**	**0**	**0**	**0**	**1**
0	1	0	1	1	0	0
0	1	1	0	0	1	0
0	1	1	1	0	1	0
1	**0**	**0**	**0**	**0**	**0**	**1**
1	0	0	1	0	0	1
1	0	1	0	1	0	0
1	0	1	1	0	1	0
1	**1**	**0**	**0**	**0**	**0**	**1**
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	1	0	0

The next step is to prepare K-maps for each of the function outputs:-

CD \ AB	00	01	11	10
00	1	0	0	0
01	0	1	0	0
11	0	0	1	0
10	0	0	0	1

F_{eq}

CD \ AB	00	01	11	10
00	0	0	0	0
01	1	0	0	0
11	1	1	0	1
10	1	1	0	0

F_{lt}

CD \ AB	00	01	11	10
00	0	1	1	1
01	0	0	1	1
11	0	0	0	0
10	0	0	1	0

F_{gt}

Switching Equations

Derive the minimal sum of products expressions for each function from the respective K-Maps above.

In the case of the Feq function, simplify the sum of products expression so that the function can be expressed in two levels using two 2-input XNOR gates and one 2-input AND gate instead. Show your workings.
(Note that A’B+AB’ = A EXOR B and A’B’ + AB = A XNOR B)

Logic Schematics

Create the comparator circuit from the switching equations you derived from the k-maps.

In the case of the equality function (N1=N2), implement both the sum-of-products form and the form which uses XNOR gates.
Verify that both implementations of the equality function produce the same outputs for all combinations of inputs. (Hint: Use the same input switches for both implementations to simplify testing.)