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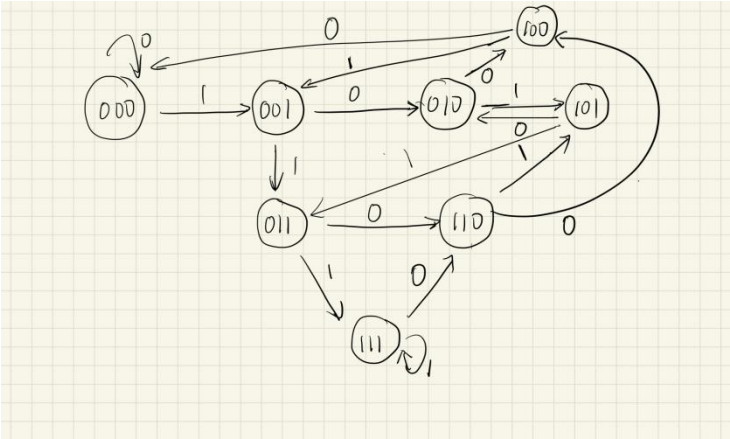
**CS220 Computer Architecture**
**Digital Logic Design**
**Practical 8**

***state diagram:***




***Transition Table:***

| | | | X = 0 | | | X = 1 | | |
|---|---|---|---|---|---|---|---|---|
| ***y2*** | ***y1*** | ***y0*** | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| | | | ***y2 y1 y0*** | | | ***y2 y1 y0*** | | |

***Modified Transition Table:***

| ***Prenent State*** | | | ***X*** | ***Next State*** | | | ***J2*** | ***K2*** | ***J1*** | ***K1*** | ***J0*** | ***K0*** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ***0*** | ***0*** | ***0*** | ***0*** | ***0*** | ***0*** | ***0*** | ***0*** | ***1*** | ***0*** | ***1*** | ***0*** | ***1*** |
| ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***1*** | ***0*** | ***0*** | ***1*** |
| ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***1*** |
| ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** |
| ***1*** | ***0*** | ***0*** | ***0*** | ***0*** | ***0*** | ***0*** | ***0*** | ***1*** | ***0*** | ***1*** | ***0*** | ***1*** |
| ***1*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***1*** | ***0*** | ***0*** | ***1*** |
| ***1*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***1*** |
| ***1*** | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** |
| ***0*** | ***0*** | ***0*** | ***1*** | ***0*** | ***0*** | ***1*** | ***0*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** |
| ***0*** | ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***1*** | ***0*** | ***1*** | ***0*** |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |

***K-Maps and Excition Equations for J-K Flip Flops:***

$J_2$:

| y2.y1<br>y0.X | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 1 | 1 | 0 |
| 01 | 0 | 1 | 1 | 0 |
| 11 | 0 | 1 | 1 | 0 |
| 10 | 0 | 1 | 1 | 0 |

$J_2 = y1$

$K_2 = \overline{y1}$

$J_1$ :

| y2.y1<br>y0.X | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 1 | 1 | 1 | 1 |

$J_1 = y0$

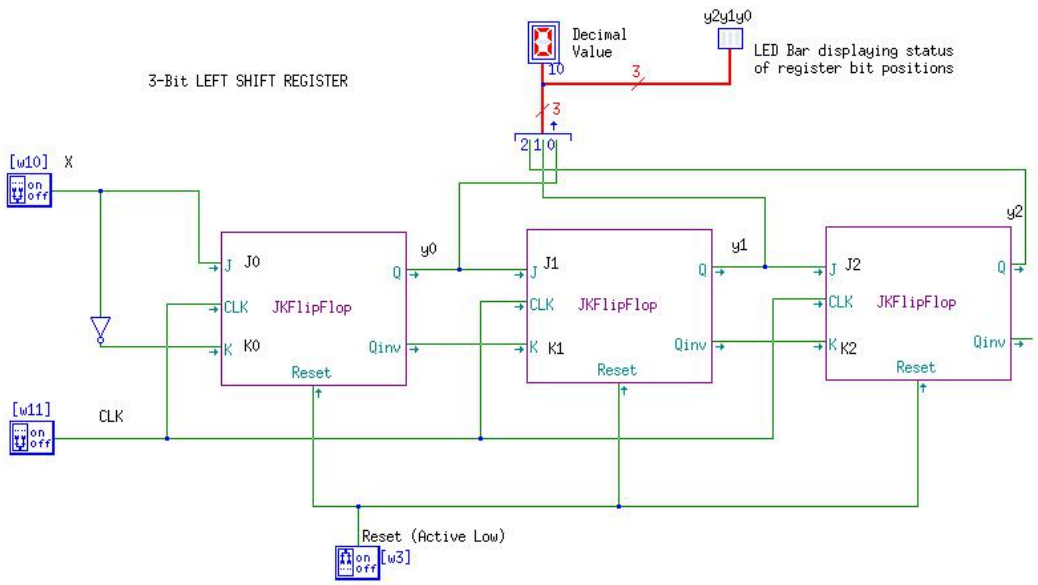
$K_1 = \overline{y0}$

$J_0$ :

| y2.y1<br>y0.X | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | 1 | 1 | 1 | 1 |
| 11 | 1 | 1 | 1 | 1 |
| 10 | 0 | 0 | 0 | 0 |

$J_0 = X$

$K_0 = \overline{X}$


3-Bit LEFT SHIFT REGISTER
Decimal
Value
10
3
y2y1y0
LED Bar displaying status
of register bit positions
3
2 1 0
[w10]
X
J
J0
Q
y0
CLK
JKFlipFlop
K
K0
Qinv
Reset
J
J1
Q
y1
CLK
JKFlipFlop
K
K1
Qinv
Reset
J
J2
Q
y2
CLK
JKFlipFlop
K
K2
Qinv
Reset
[w11]
CLK
Reset (Active Low)
[w3]