CS220 Computer Architecture
Digital Logic Design
Practical 7

The TkGate Logic Simulator under Linux is used to implement these practicals.
Boot Linux, log in and launch the TkGate application.

In this practical, you will design and implement a synchronous sequential circuit for pattern recognition. You will need to do the design before you can construct the circuit. The paper design will be part of the mark for the practical.

PROBLEM
Design a synchronous sequential circuit that has a single input X and a single output Z.
Z is to turn on when the pattern 100 is sampled on X (on successive clock pulses).
Z is then to remain on until X is sampled as 1.

Use Master Slave Pulse Triggered J-K Flip Flops to implement the design.
Note you created a module for the J-K flip flop circuit in a previous practical and if it was operational, you can use instances of that module to build the circuit (AFTER YOU HAVE COMPLETED THE DESIGN). You can also download a working version from moodle "lab7shell.v" and complete the circuit after you have completed the design on paper.

Design the circuit on paper leading to a logic schematic. Your notes must show these workings and you must understand and be able to explain your own design.

Using 2xJ-K flip-flop modules and any other necessary logic gates, implement the logic schematic on the TkGate simulator and verify its operation.

Using phone/camera to reecord an 1 to 3 minutes video(720p or 1080p) to demonstrate your working circuit on the simulator and upload on Moodle. Half of the marks will be for a full design of your circuit on your report.