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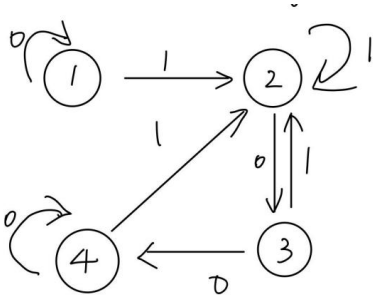
CS220 Computer Architecture
Digital Logic Design
Practical 7

state diagram



state/output table:

	X		Z
	0	1	
1	1	2	0
2	3	2	0
3	4	2	0
4	4	2	1

make secondary state assignment

y_1	y_0	State	Z
0	0	1	0
0	1	2	0
1	0	3	0
1	1	4	1

Transution table

		X			
y_1	y_0	0		1	
0	0	0	0	0	1
0	1	1	0	0	1
1	0	1	1	0	1
1	1	1	1	0	1

excitation table

		X			
y_1	y_0	0		1	
0	0	0	0	0	I
0	1	I	Φ	0	1
1	0	1	I	Φ	I
1	1	1	1	Φ	1

y_1	y_0	y_1	y_0

excitation equcations:

	00	01	11	10
0	0	I	1	1
1	0	0	Φ	Φ

$J_1 = \overline{X} y_0 \qquad K_1 = X$

	00	01	11	10
0	0	Φ	1	I
1	I	1	1	I

$J_0 = X + y1 \qquad K_0 = \overline{X}\,\overline{y_1}$

output eqations：

z	y_1	y_0
0	0	0
0	0	1
0	1	0
1	1	1

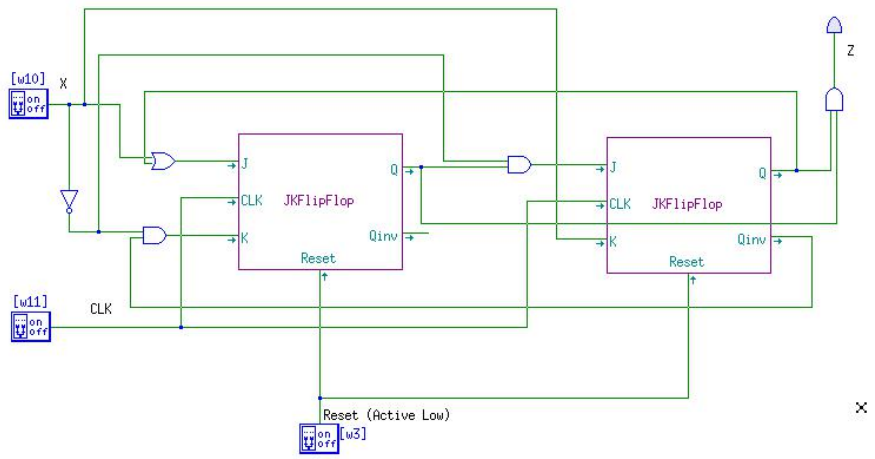
$Z = y_0 y_1$

Where y0 is the output of our first JK Flip Flops and y1 is the output of our second JK Flip Flops.
Where X is the input of whole circuit.

the circuit:

$Z = y_0 y_1$

$J_0 = X + y1 \qquad K_0 = \overline{X}\,\overline{y_1} \qquad J_1 = \overline{X} y_0 \qquad K_1 = X$



X is on the left top of the screen.
the JK Flip Flops left is the first Flip Flops.
and the JK Flip Flops right is the second Flip Flops.
Z is on the right top of the screen.
CLK is an switch which is controlled by myself.

the verify of this circuit is recorded by a video
And the circuit works in accordance with the words specification.