CMP301 Fall 2021 Project

Phase 1

Team 2

- **Instructions format**
  I. One-Operand instructions

Instruction	Op code From 0 to 4	1st bits group From 5 to 7	2nd bits group From 8 to 10	3rd bits group From 11 to 13
NOP	00000 (0)	XXX	XXX	XXX
HLT	00001 (1)	XXX	XXX	XXX
SETC	00010 (2)	XXX	XXX	XXX
NOT	00011 (3)	Rdst	XXX	Rdst
INC	00100 (4)	Rdst	XXX	Rdst
OUT	00101 (5)	Rsrc	XXX	XXX
IN	00110 (6)	XXX	XXX	Rdst

II. Two-Operands instructions

Instruction	Op code From 0 to 4	1st bits group From 5 to 7	2nd bits group From 8 to 10	3rd bits group From 11 to 13
MOV	00111 (7)	Rsrc	XXX	Rdst
ADD	01000 (8)	Rsrc1	Rsrc2	Rdst
SUB	01001 (9)	Rsrc1	Rsrc2	Rdst
AND	01010 (10)	Rsrc1	Rsrc2	Rdst
IADD - part1	01011 (11)	Rsrc	XXX	Rdst
IADD - part2	**IMMEDIATE VALUE**			From 0 to 15

III. Memory Operations

Instruction	Op code From 0 to 4	1st bits group From 5 to 7	2nd bits group From 8 to 10	3rd bits group From 11 to 13
PUSH	01100 (12)	Rsrc	XXX	XXX
POP	01101 (13)	XXX	XXX	Rdst
LDM -patr1	01110 (14)	XXX	XXX	Rdst
LDM -part2	**IMMEDIATE VALUE**		**ALU**	From 0 to 15
LDD -part1	01111 (15)	Rsrc	XXX	Rdst
LDD -part2	**OFFSET**		From 0 to 15	
STD -part1	10000 (16)	Rsrc1	Rsrc2 (offset)	XXX
STD -part2	**OFFSET**		From 0 to 15	

IV. Branch and Change of Control Operations

Instruction	Op code From 0 to 4	1st bits group From 5 to 7	2nd bits group From 8 to 10	3rd bits group From 11 to 13
JZ	10001 (17)	Rsrc	XXX	XXX
JN	10010 (18)	Rsrc	XXX	XXX
JC	10011 (19)	Rsrc	XXX	XXX
JMP	10100 (20)	Rsrc	XXX	XXX
CALL	10101 (21)	Rsrc	XXX	XXX
RET	10110 (22)	XXX	XXX	Rdst
INT	10111 (23)	**INTERR**	**UPTI**	**NDEX** From 5 to15
RTI	11000 (24)	XXX	XXX	XXX

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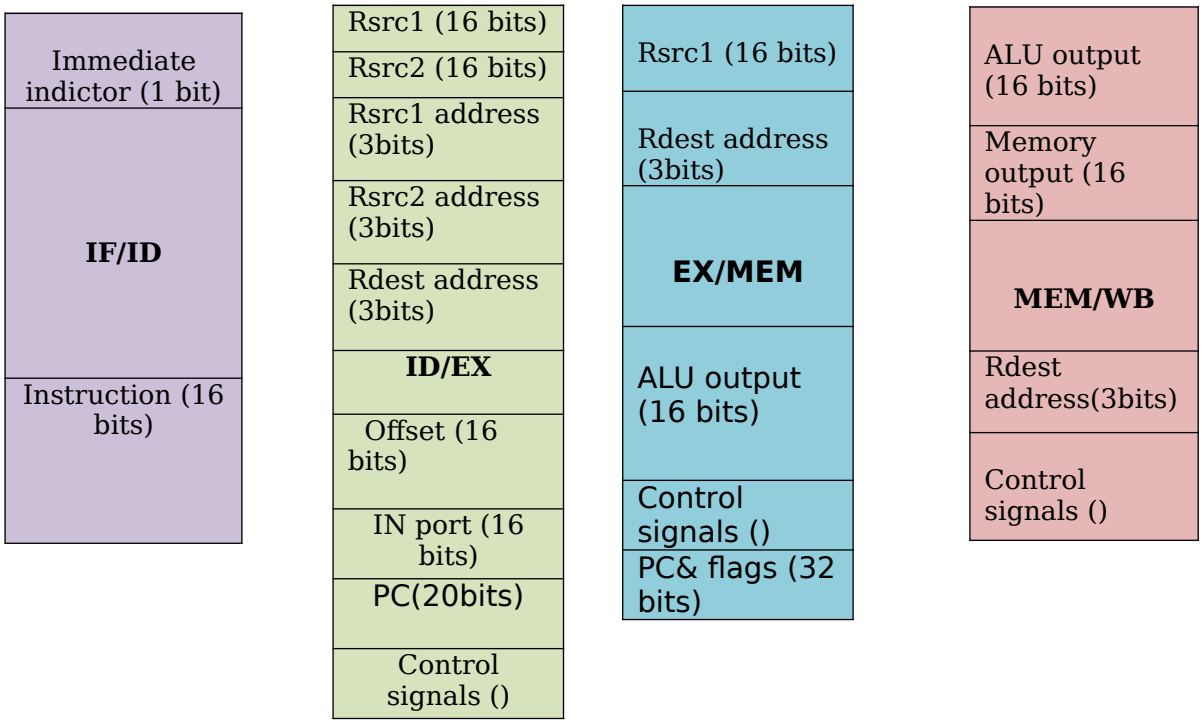
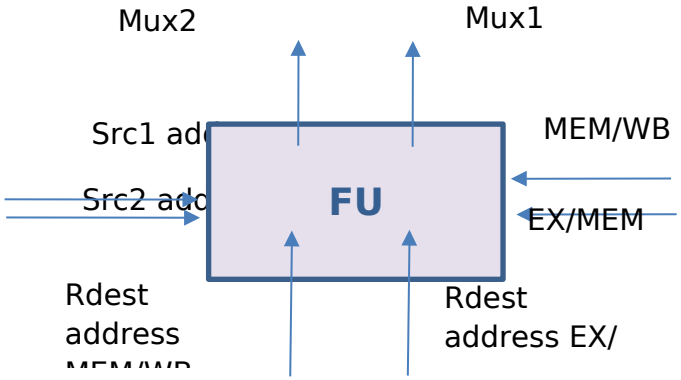
Pipeline registers details



- **Data Forwarding**



- **Static branch prediction**

  Assume to be untaken always.