VLSI PROJECT
SMART HOME

3/1/2022

PROPOSED TO: SANDRA WAHEED

Done by:

Name	Sec	B.N.
Menna Allah Ahmed Ali	2	30
Nada Elsayed Mohamed	2	33
Raghad Khaled AbdElhay	1	31
Reem Emad Ramadan	1	34

WORK OVERVIEW

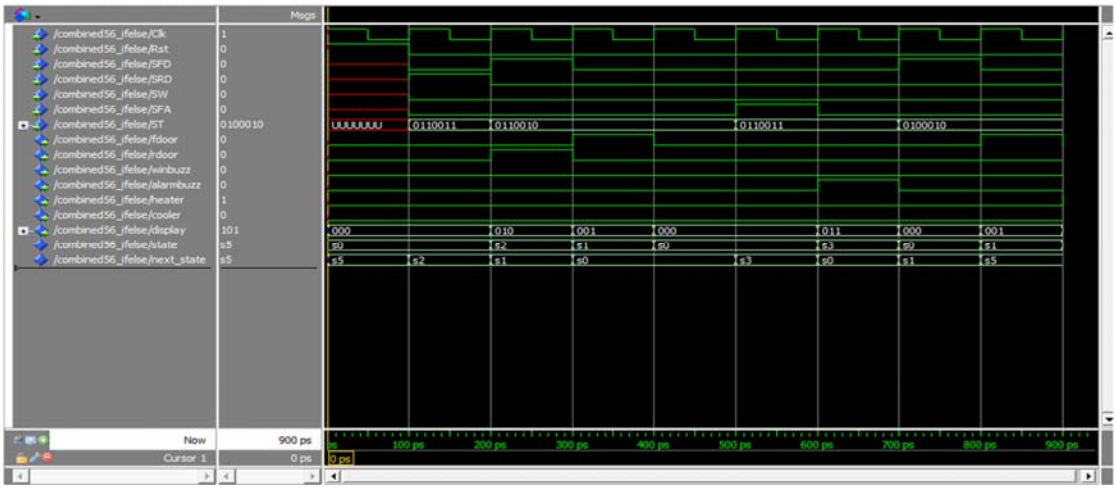
We have done many scenarios until we have reached the best design for the overall equation:

1. combined56IfElse

This is the chosen design.

Moore Finite State Machine is used

We combined the states 5(heater) and state 6(cooler) together



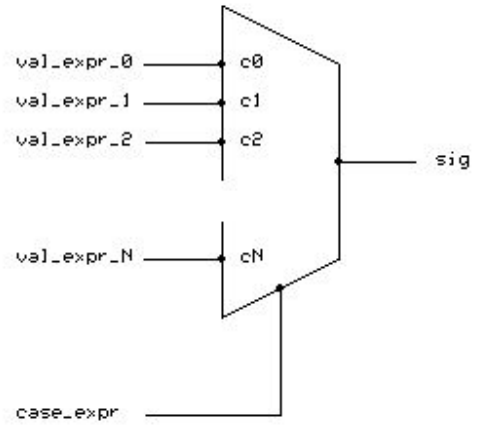
pre-synthesis combined56IfElse

post-synthesis combined56IfElse

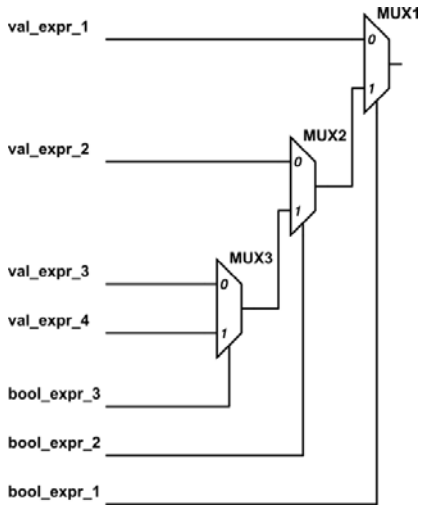
2. combined56

This design has same idea as *Combined56IfElse* but here we used Case When instead of Else If which differs in all aspects(area-slack-power).

Combined56IfElse gives better overall result over *combined56* because When Case has big mux



When case hardware



If Else hardware

These two figures show Case when has less area but gives low slack and vice versa for the if else

So case has better area but worse slack so gives less time while if else has bigger area with better slack.

So briefly combined56_ifelse is best than combine_56; why?

because combined56_ifelse uses smaller multiplexers each one does its process in a small time and they all parallel so the total arrival time, in the end, is smaller than one big mux does all process.

the trade-off here was time vs area and power; but why do we choose the time?

cause the overall equation spots on time; because time has the larger value between all other values so even it scaled to 30% and area scaled to 50% but still time has the bigger value

3. combined56TriBuffer

Instead of using muxes in *Combined56*, we implemented tristate buffers to put signals with 0s in signals and Zs in other states, we imagined that it will have less area but this wasn't achieved

4. combined56_v1

Instead of using two processes in *Combined56*, we used one process to see if it would give better effect but it wasn't

5. separate56

We separated states 5(heater) and 6(cooler), each as an independent state, this wasn't efficient as it costs more hardware while they are both related to temperature, so it was better to combine them.

6. separate56IfElse

This design has same idea as *separate56* but here we used Else If instead of Case When which differs in aspects (area -power) but slack is not better so still its overall wasn't better than *combined56IfElse*

7. keep_H_C_value

We still using Moore and states 5 and 6 are combined as one sensor but we keep the values of heater and cooler however the state is, don't put high impedance(Z) on them. They are only changed at states 5 and 6 if they need to be changed.

8. Keep_H_C_valueIfElse

This design has same idea as *Keep_H_C_value* but here we used Else If instead of Case When seeking for better result and its overall was better than *Keep_H_C_value* but still not better than *combined56IfElse*

9. Mealy

All previous designs were using Moore, we tried to use Mealy here but it gives very big area and very small slack so subsequently it gives worst overall value.

STATISTICS FOR ALL DESIGNS

Best design is highlighted

Overall is calculated using the following equation:

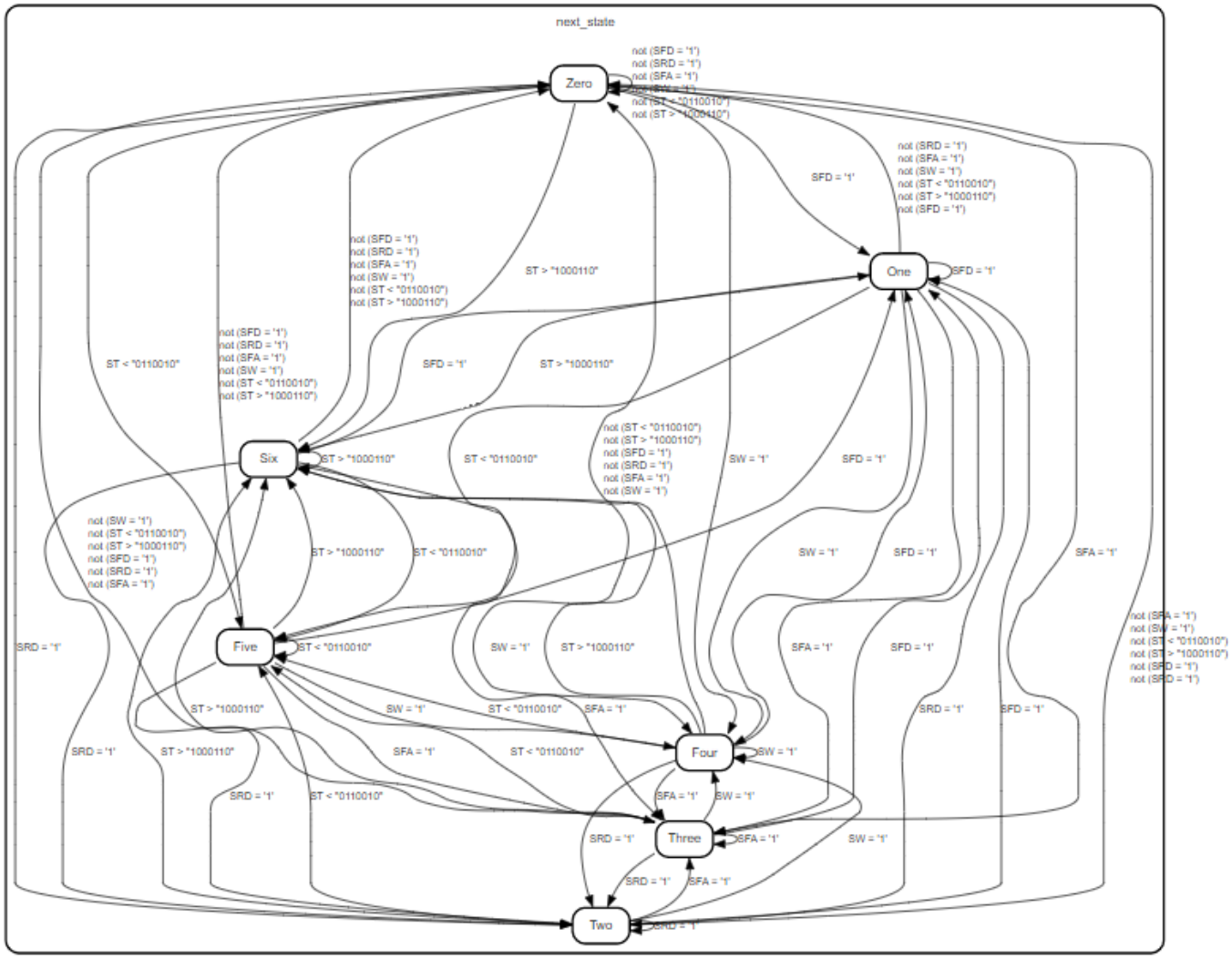
*0.5*Movable Cell Area in squm+0.3*(clock period in ps-worst case slack in ps)+0.2*total power in uw*

Clock Period = 1500 ps

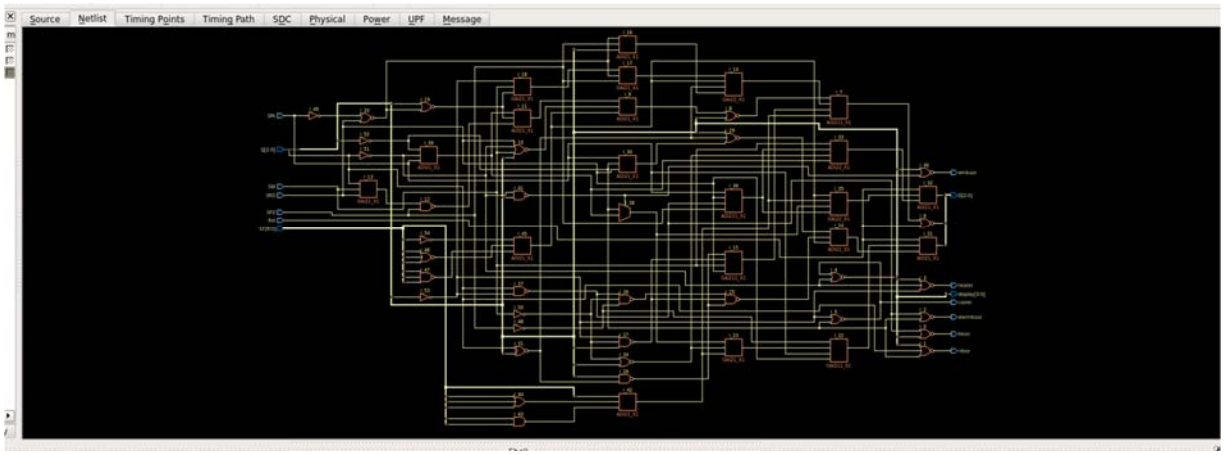
Design Name	Movable Area (squm)	Worst Slack (ps)	Total Power (uW)	Overall
combined56	60	469.2	113.894569	362.0189137
combined56IfElse	68	521.9	146.587	356.7474
combined56TriBuffer	75	336.5	157.07912	417.965824
combined56_v1	66	225.7	151.430786	445.57615719999995
Mealy	80	20.7	226.08139	529.006278
keep_H_C_value	70	467.5	101.418640	365.033728
keep_H_C_value_ifElse	69	540.9	142.133652	350.6567304
separate56	72	459.2	154.296753	379.0993506
seperate56IfElse	66	456.7	142.144745	374.418949

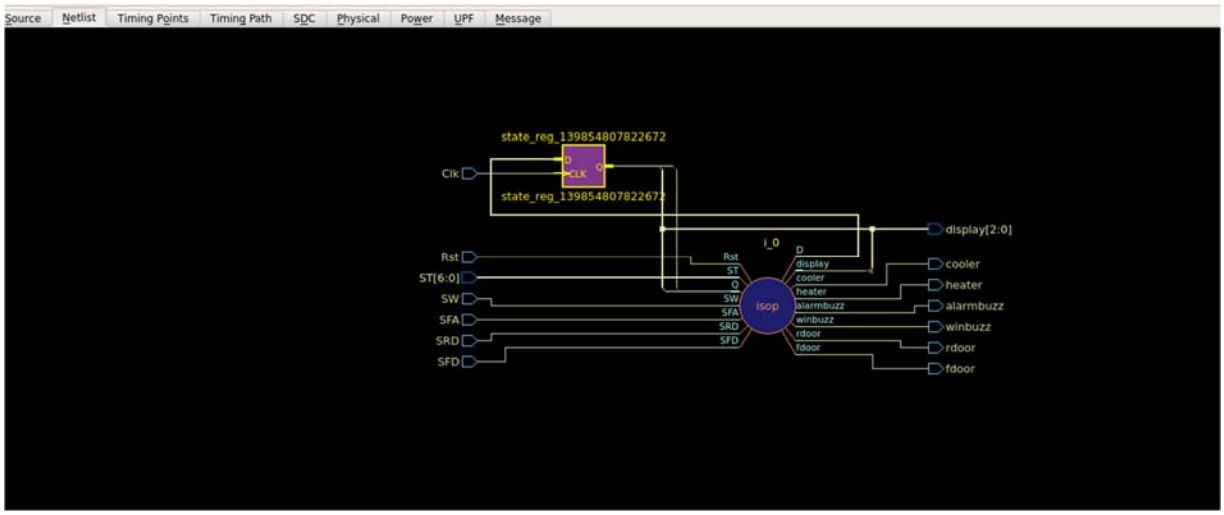
ALL FOLLOWING IS FOR COMBINED56IFELSE DESIGN

DESIGN SCHEMA

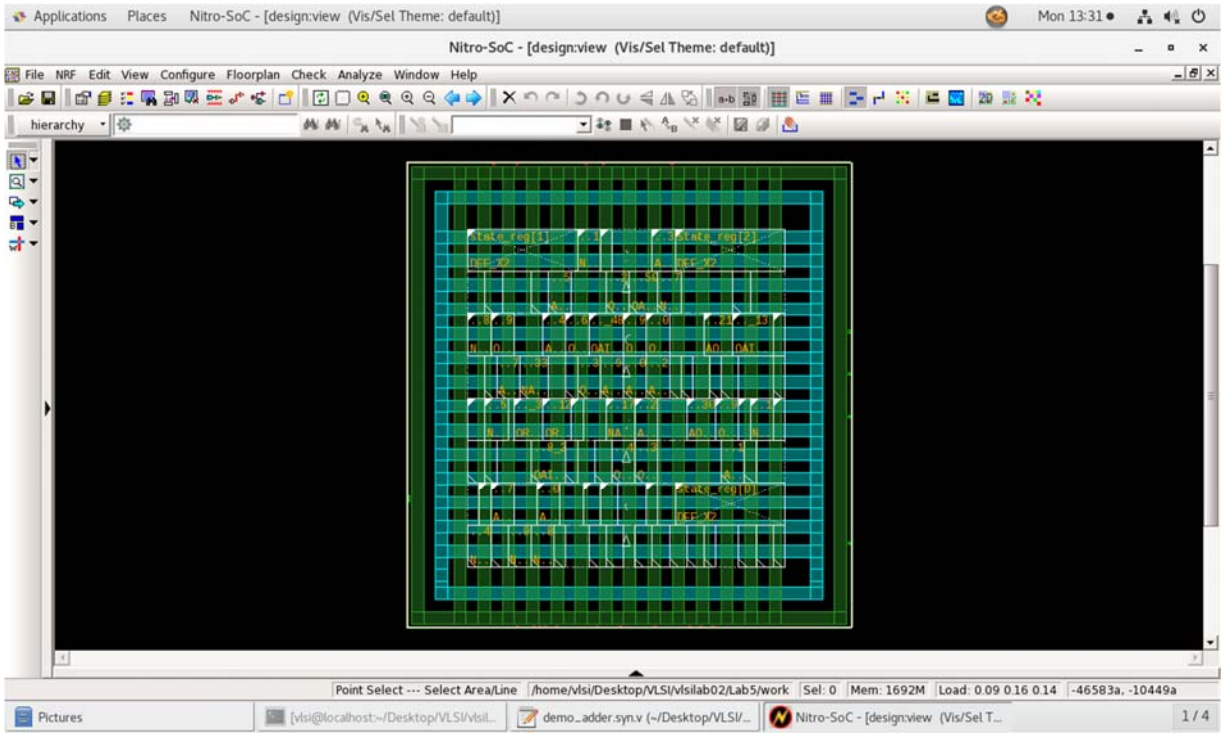


SCHEMATIC OF THE DESIGN AFTER SYNTHESIS

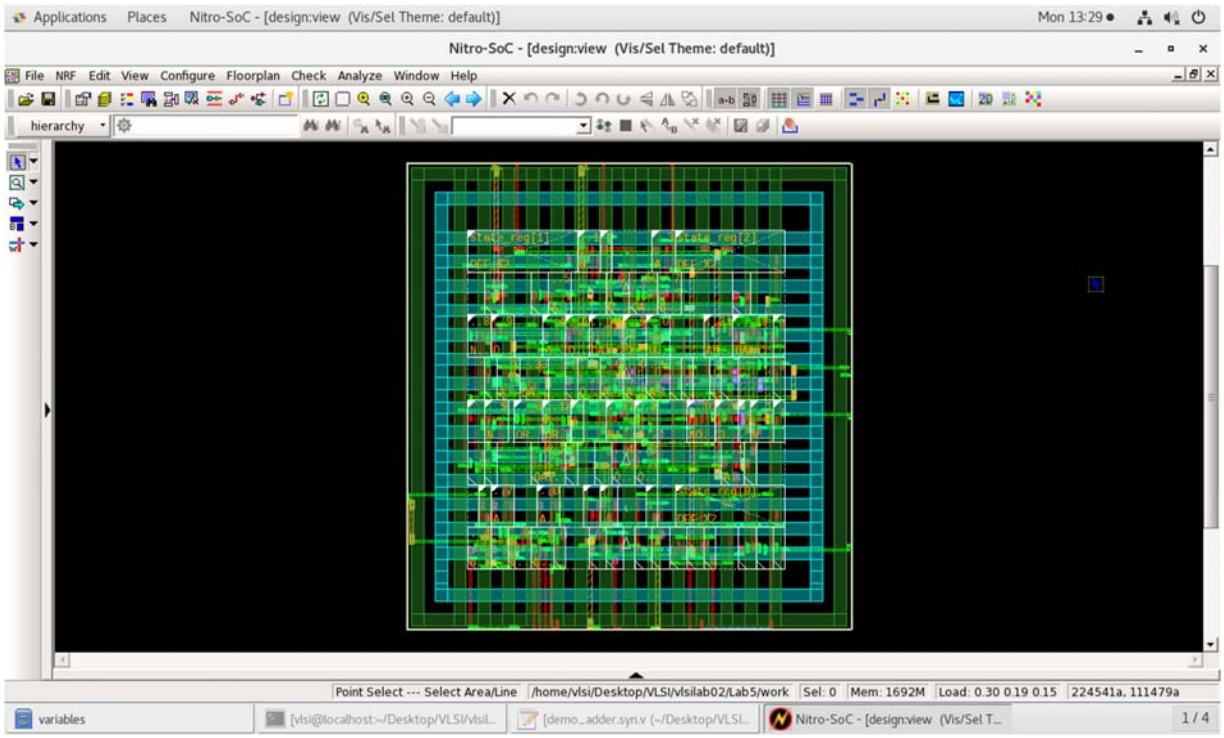




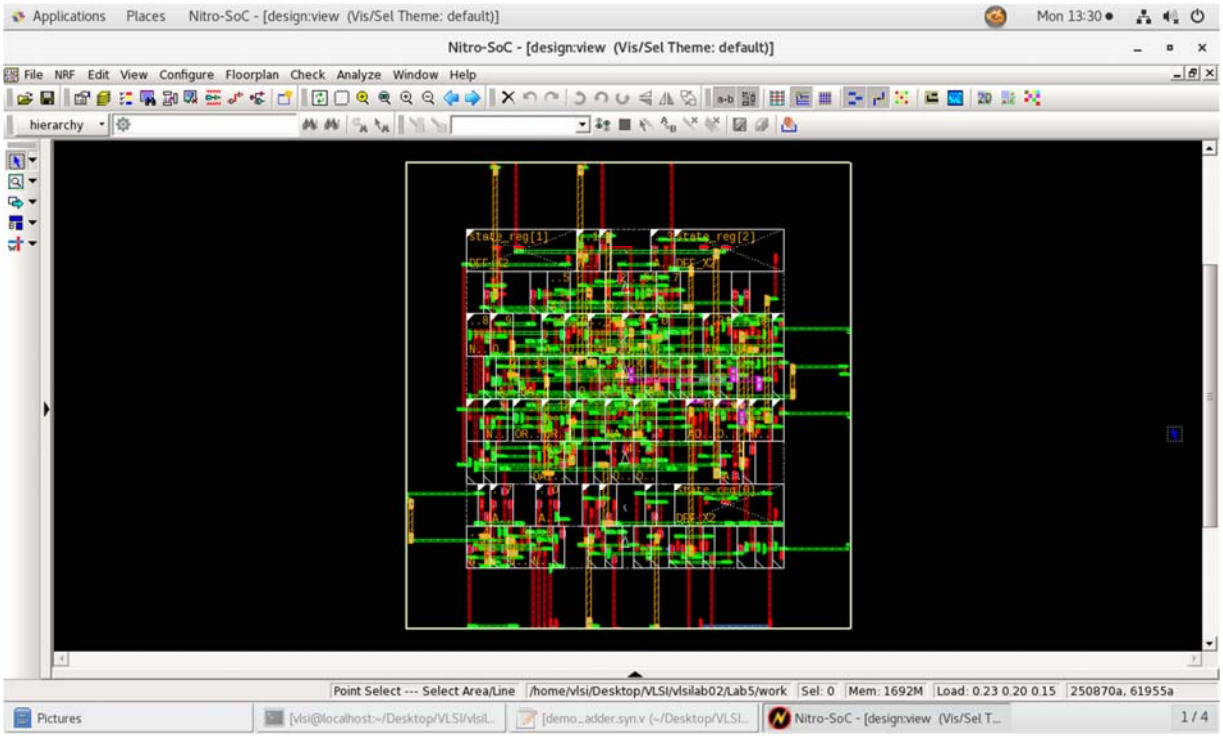
CHIP SCHEMATIC



Chip before routing



Chip after routing



Routing only

synthesis reports

design.rpt

```
Report Physical info:
-------------------------+------------------+-----------+------------
                         |                  |Area (squm)|Leakage (uW)
-------------------------+------------------+-----------+------------
Design Name              |combined56_ifelse|           |
  Total Instances        |                58|         68|       1.537
    Macros               |                 0|          0|       0.000
    Pads                 |                 0|          0|       0.000
    Phys                 |                 0|          0|       0.000
    Blackboxes           |                 0|          0|       0.000
    Cells                |                58|         68|       1.537
      Buffers            |                 0|          0|       0.000
      Inverters          |                 7|          4|       0.100
      Clock-Gates        |                 0|          0|       0.000
      Combinational      |                48|         51|       1.199
      Latches            |                 0|          0|       0.000
      FlipFlops          |                 3|         14|       0.237
       Single-Bit FF     |                 3|         14|       0.237
       Multi-Bit FF      |                 0|          0|       0.000
       Clock-Gated       |                 0|           |
       Bits              |                 3|         14|       0.237
         Load-Enabled    |                 0|           |
         Clock-Gated     |                 0|           |
  Tristate Pin Count     |                 0|           |
Physical Info            |Placed            |           |
  Chip Size (mm x mm)    |0.072 x 0.072     |       5113|
  Fixed Cell Area        |                  |          0|
    Phys Only            |                 0|          0|
  Placeable Area         |                  |        128|
  Movable Cell Area      |                  |         68|
  Utilization (%)        |                53|           |
  Chip Utilization (%)   |                53|           |
  Total Wire Length (mm)|             0.794|           |
  Longest Wire (mm)      |             0.037|           |
  Average Wire (mm)      |             0.036|           |
-------------------------+------------------+-----------+------------
```

power.rpt

```
warning: No library characterized for (process = 1.00 voltage = 0.85 temperature = 25.00) can be found in the database for power domain '/PD_TOP'  [NL-174]
Report Power (instances with prefix '*' are included in total) :
```

	Instance	Internal Power(uw)	Switching Power(uw)	Leakage Power(uw)	Total Power(uw)
1	*state_reg[2]	1.957324	10.207888	0.079112	12.244324
2	*state_reg[1]	2.211625	11.522768	0.079112	13.813505
3	*state_reg[0]	2.586482	8.104404	0.079112	10.769998
4	*i_0_0_0	0.274646	1.781972	0.021200	2.077817
5	*i_0_0_1	0.451280	2.247871	0.026832	2.725983
6	*i_0_0_2	0.122470	0.786647	0.021200	0.930317
7	*i_0_0_3	0.182038	0.882597	0.026832	1.091466
8	*i_0_0_4	0.457787	2.608953	0.021200	3.087940
9	*i_0_0_5	0.102919	0.860898	0.021200	0.985016
10	*i_0_0_6	0.427156	0.321039	0.021200	0.769395
11	*i_0_0_7	0.661561	0.896709	0.034566	1.592836
12	*i_0_0_8	0.441136	0.585723	0.021200	1.048058
13	*i_0_0_9	0.670947	0.974232	0.027858	1.673037
14	*i_0_0_10	0.277417	0.324623	0.032601	0.634642
15	*i_0_0_11	0.569586	0.925564	0.027858	1.523009
16	*i_0_0_12	0.577018	0.913637	0.017393	1.508048
17	*i_0_0_13	0.592636	0.692029	0.022619	1.307284
18	*i_0_0_14	0.651717	0.608611	0.034026	1.294355
19	*i_0_0_15	0.817378	0.628325	0.022039	1.467742
20	*i_0_0_16	0.636351	0.866163	0.027858	1.530372
21	*i_0_0_17	0.522902	0.726867	0.022619	1.272388
22	*i_0_0_18	0.673275	0.898769	0.022619	1.594663
23	*i_0_0_19	0.453690	1.882601	0.021200	2.357491
24	*i_0_0_20	0.594893	3.189688	0.021200	3.805780
25	*i_0_0_21	0.477128	0.298464	0.027858	0.803450
26	*i_0_0_22	0.676711	0.781512	0.022039	1.480262
27	*i_0_0_23	0.456700	0.750171	0.022619	1.229490
28	*i_0_0_24	0.560371	0.917620	0.027858	1.505850
29	*i_0_0_25	0.566168	0.874056	0.018105	1.458329
30	*i_0_0_26	0.359140	0.616738	0.018105	0.993983
31	*i_0_0_27	0.228129	0.736928	0.018105	0.983162
32	*i_0_0_28	0.193765	0.740835	0.017393	0.951993
33	*i_0_0_29	0.447336	0.686054	0.026832	1.160222
34	*i_0_0_30	0.649958	0.800621	0.027858	1.478437
35	*i_0_0_31	0.822577	2.774698	0.036441	3.633716
36	*i_0_0_32	0.341481	0.216868	0.027858	0.586208
37	*i_0_0_33	0.414230	0.489719	0.032612	0.936560
38	*i_0_0_34	0.422726	1.785446	0.021200	2.229372
39	*i_0_0_35	0.559106	0.704939	0.034026	1.298071
40	*i_0_0_36	0.422719	1.073614	0.034566	1.530899
41	*i_0_0_37	0.371225	2.861120	0.017393	3.249738
42	*i_0_0_38	0.832456	1.403080	0.035928	2.271465
43	*i_0_0_39	0.389486	1.368006	0.027858	1.785350
44	*i_0_0_40	0.145532	0.881707	0.021200	1.048439
45	*i_0_0_41	0.176198	0.616382	0.017393	0.809973
46	*i_0_0_42	1.038554	3.745965	0.027858	4.812378
47	*i_0_0_43	1.187018	1.103167	0.025066	2.315252
48	*i_0_0_44	0.704582	0.628889	0.024415	1.357886
49	*i_0_0_45	0.978482	5.861842	0.027858	6.868182
50	*i_0_0_46	0.502233	0.629489	0.026832	1.158554
51	*i_0_0_47	0.549525	0.651865	0.018105	1.219496
52	*i_0_0_48	0.928418	2.932264	0.014353	3.875035
53	*i_0_0_49	1.029130	1.457717	0.014353	2.501200
54	*i_0_0_50	0.845870	4.357310	0.014353	5.217534
55	*i_0_0_51	0.287280	4.256230	0.014353	4.557864
56	*i_0_0_52	0.245469	4.030383	0.014353	4.290205
57	*i_0_0_53	0.217337	3.230895	0.014353	3.462585
58	*i_0_0_54	1.035796	1.370355	0.014353	2.420503
59					
60	*TOTAL	35.977070	109.073540	1.536510	146.587112

Path.rpt

```
Report Path Groups:
-----+-------+------+---------+---------
     | Path  |Weight|Critical |Worst
     | Group |      |Range(ps)|Slack(ps)
-----+-------+------+---------+---------
1    |default| 1.000|      0.0|   1083.0
2    |I2R    | 1.000|      0.0|    521.9
3    |I2O    | 1.000|      0.0|<ill>
4    |R2O    | 1.000|      0.0|    810.4
-----+-------+------+---------+---------
```