PCI (Peripheral Component Interconnect)

Presented by

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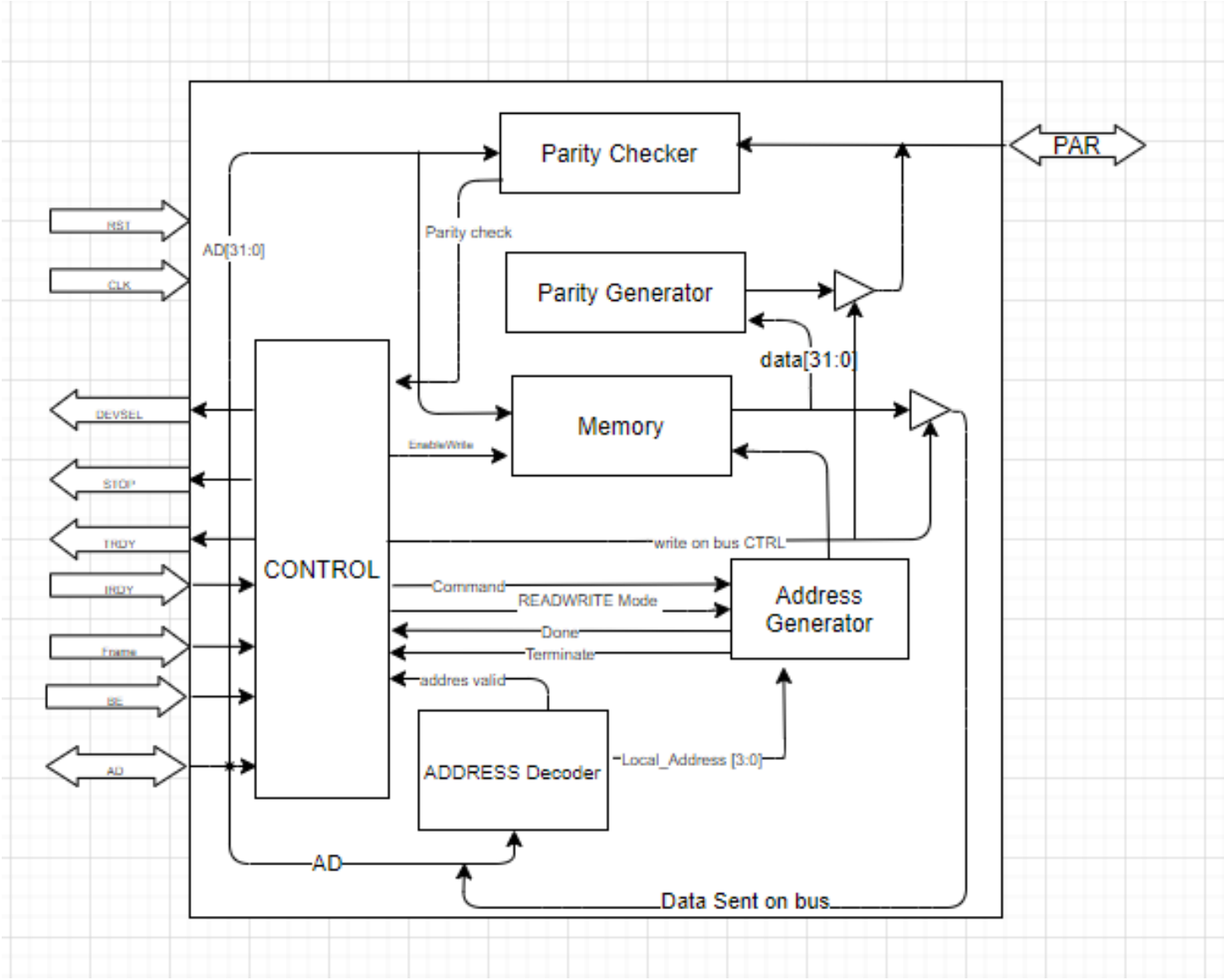
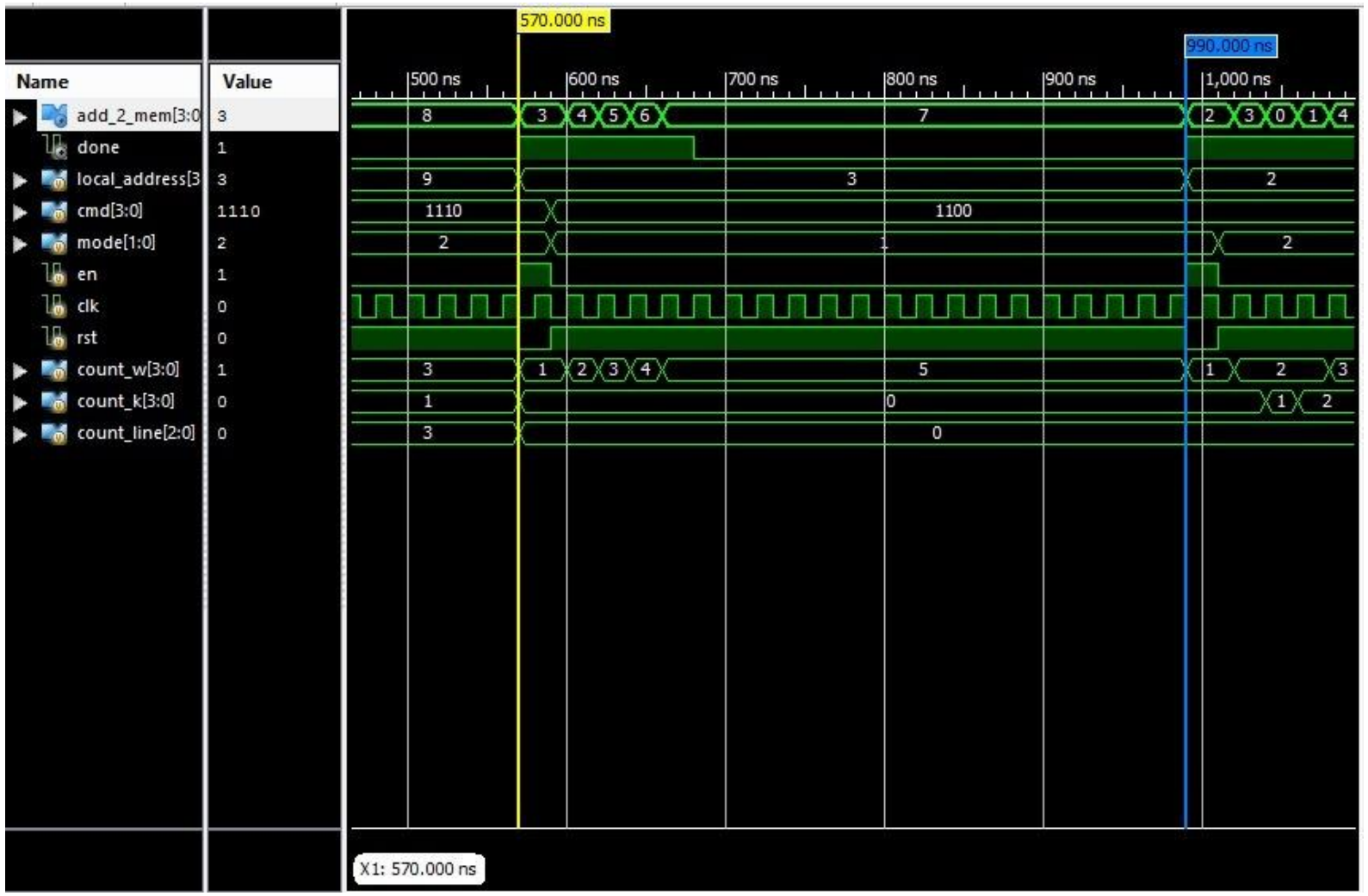
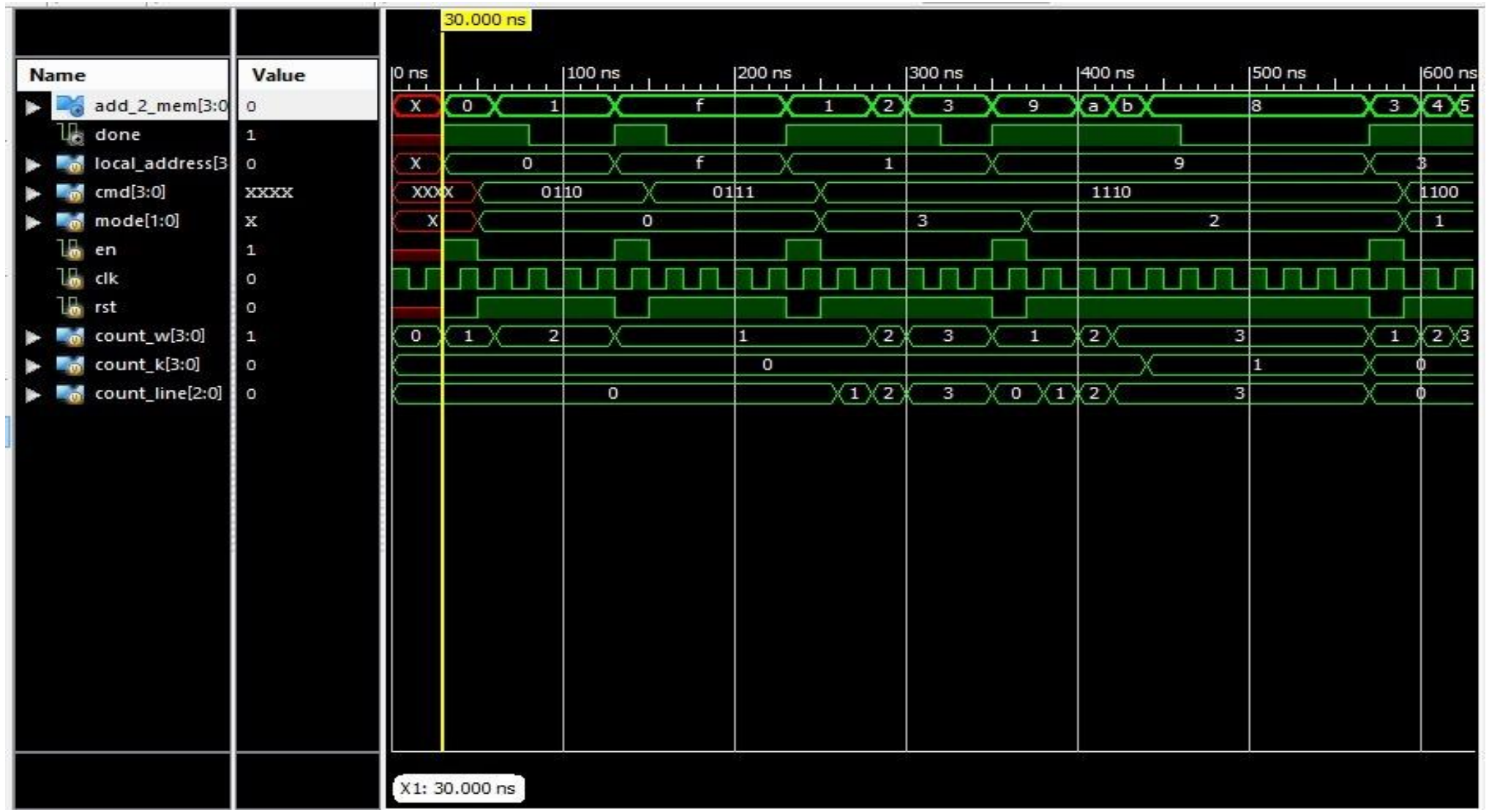
- PCI Target Architecture

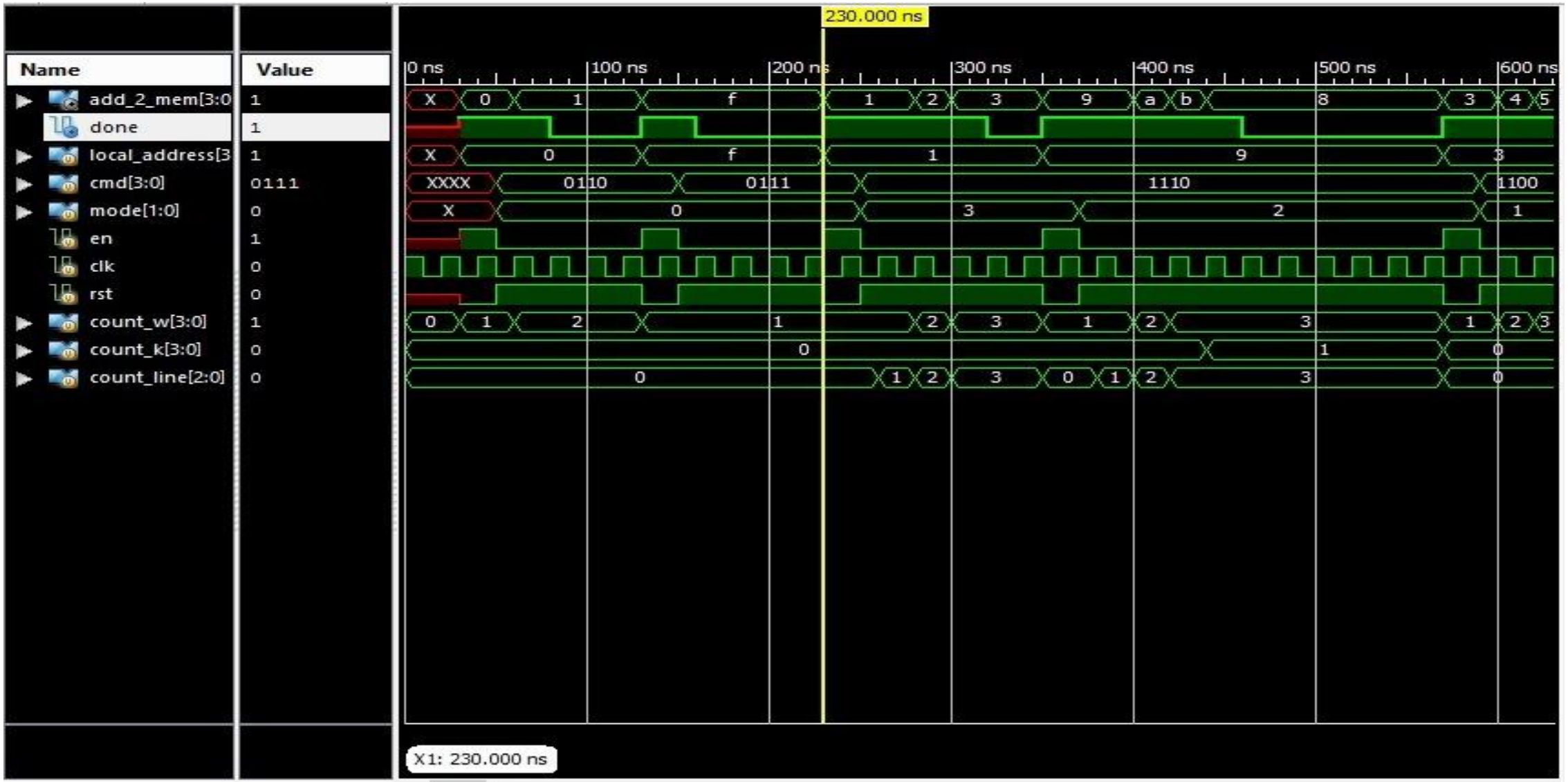


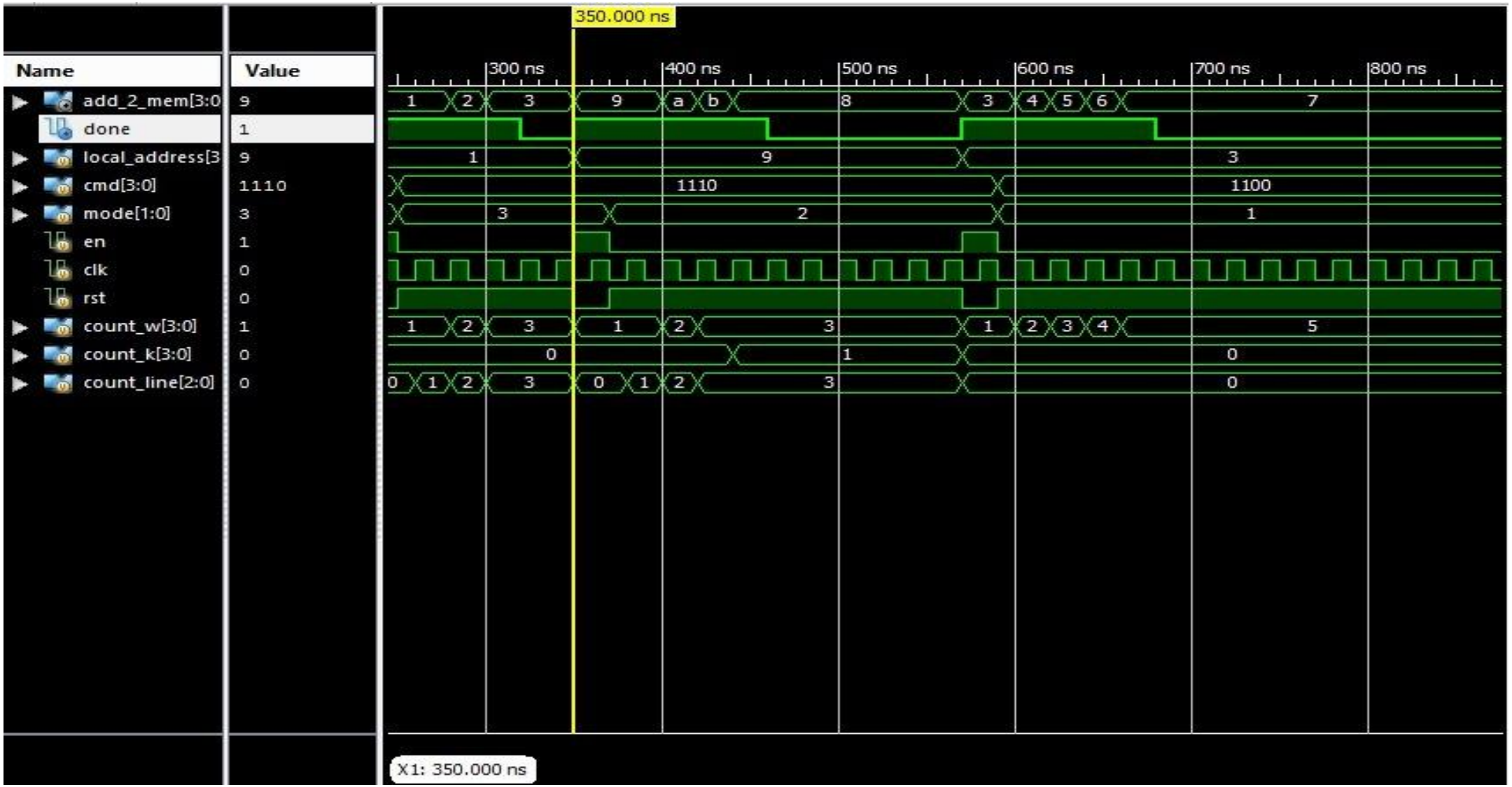
Address Generator Simulation Results



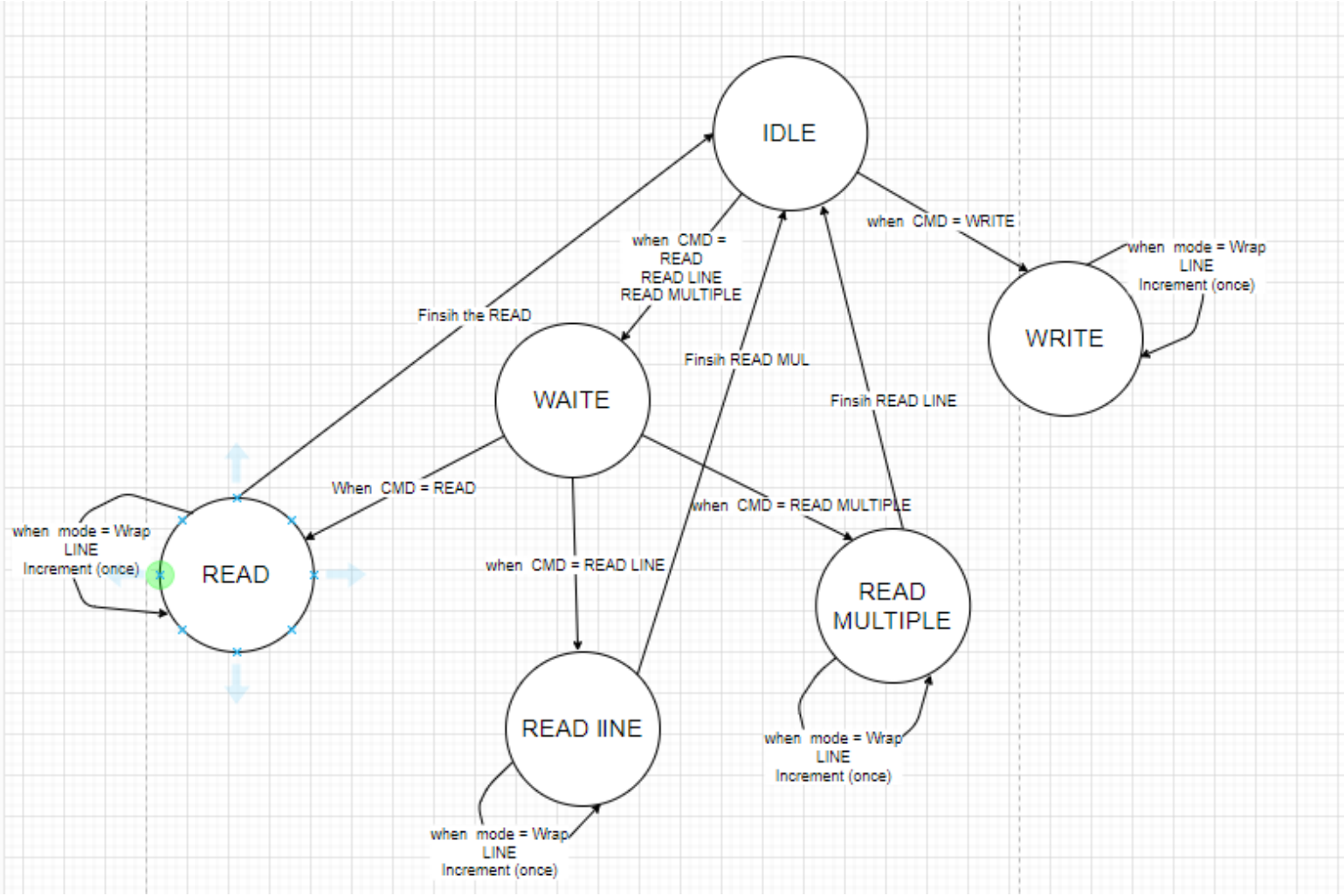

ame
Value
add_2_mem[3:0
7
done
1
local_address[3
2
cmd[3:0]
1100
mode[1:0]
2
en
0
clk
0
rst
1
count_w[3:0]
6
count_k[3:0]
2
count_line[2:0]
0
990.000 ns
1,158.230 ns
800 ns
900 ns
1,000 ns
1,100 ns
1,200 ns
X1: 1,158.230 ns


30.000 ns
Name
Value
add_2_mem[3:0
0
done
1
local_address[3
0
cmd[3:0]
xxxx
mode[1:0]
x
en
1
clk
0
rst
0
count_w[3:0]
1
count_k[3:0]
0
count_line[2:0]
0
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
X1: 30.000 ns


230.000 ns
Name
Value
add_2_mem[3:0
1
done
1
local_address[3
1
cmd[3:0]
0111
mode[1:0]
0
en
1
clk
0
rst
0
count_w[3:0]
1
count_k[3:0]
0
count_line[2:0]
0
0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
X1: 230.000 ns

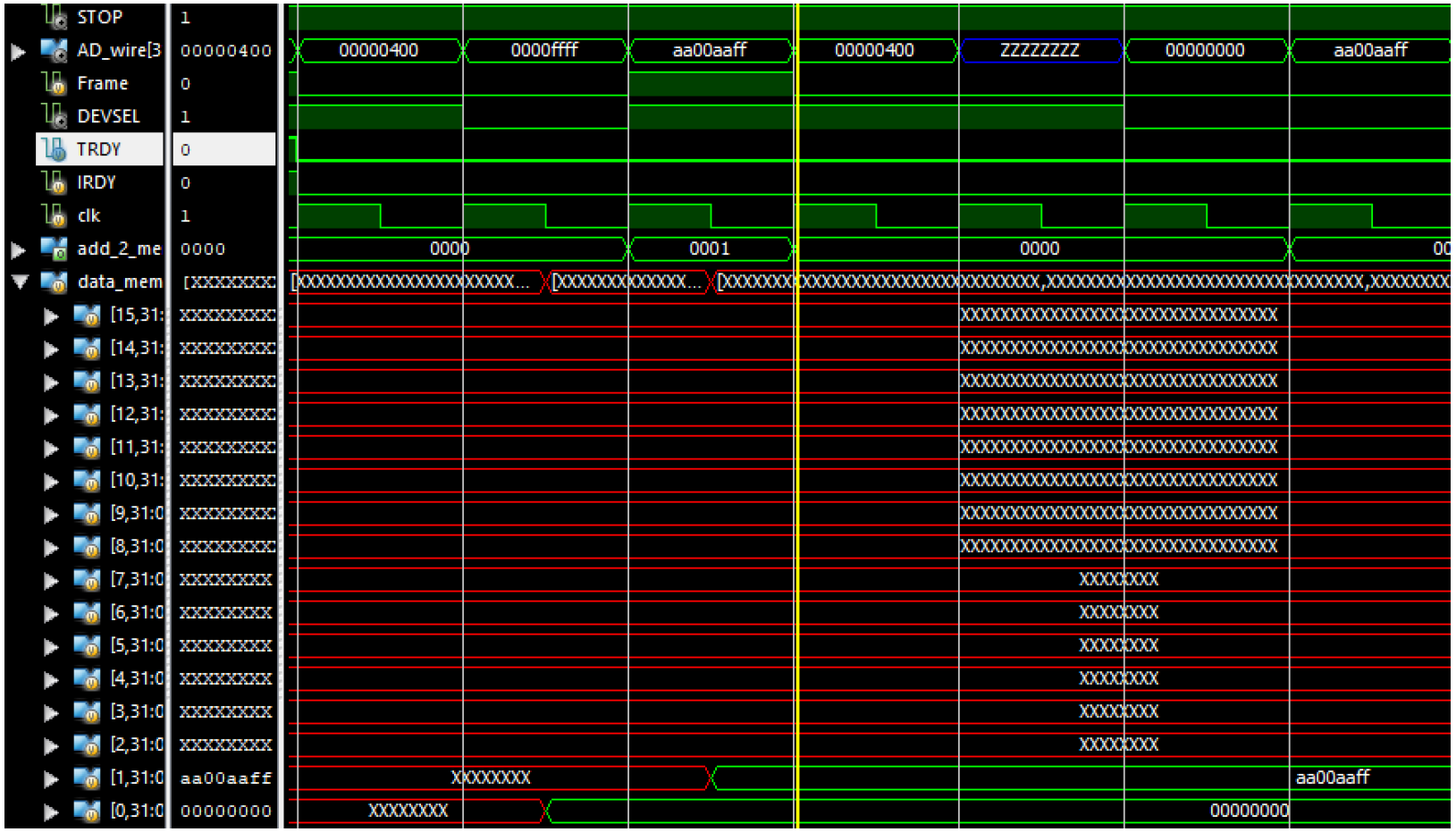

350.000 ns
Name
Value
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
add_2_mem[3:0
9
done
1
local_address[3
9
cmd[3:0]
1110
mode[1:0]
3
en
1
clk
0
rst
0
count_w[3:0]
1
count_k[3:0]
0
count_line[2:0]
0
X1: 350.000 ns

- PCI Target Finite state Machine



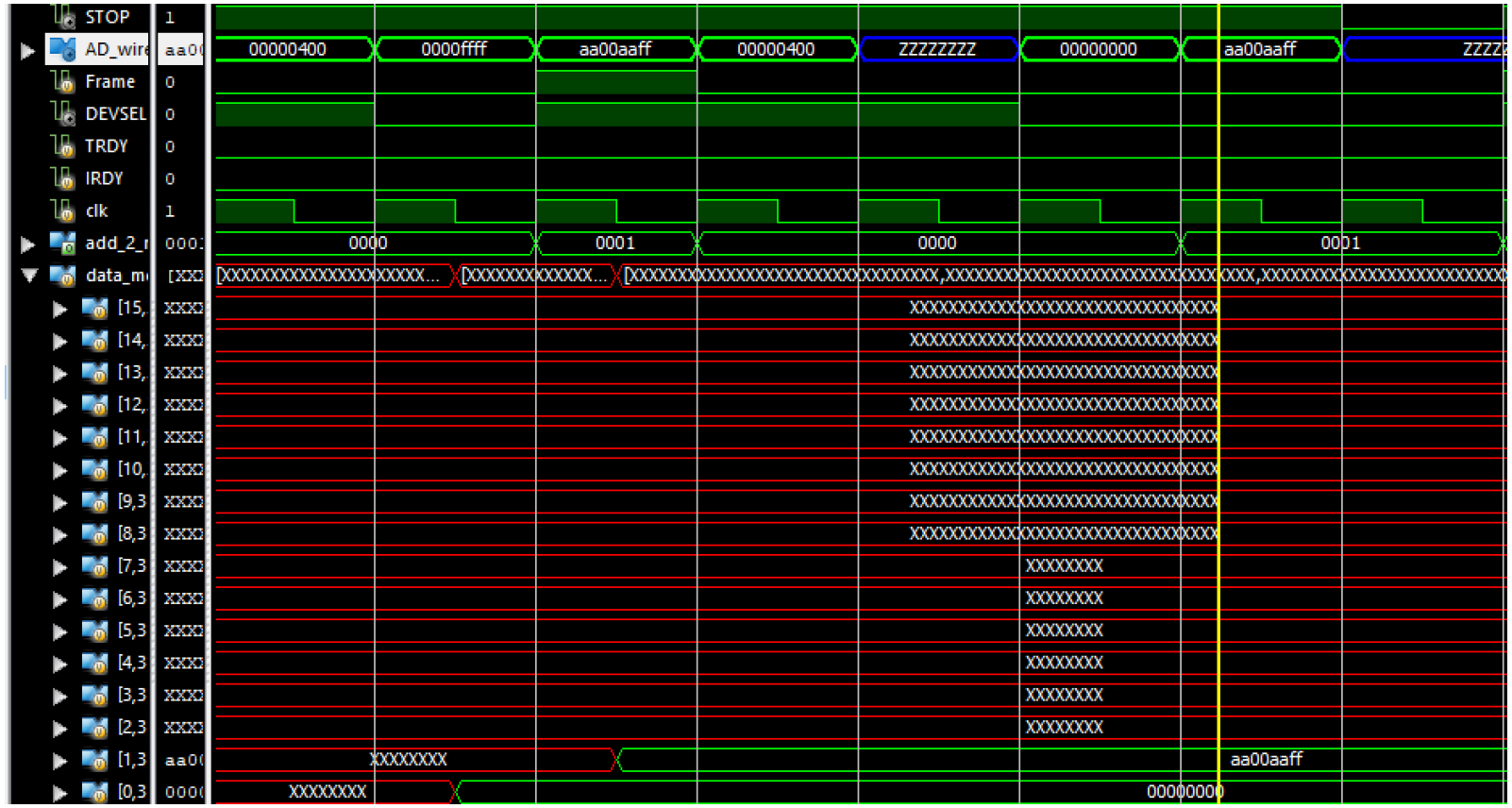
Read Memory and Write (Increment Mode)

- Termination from master



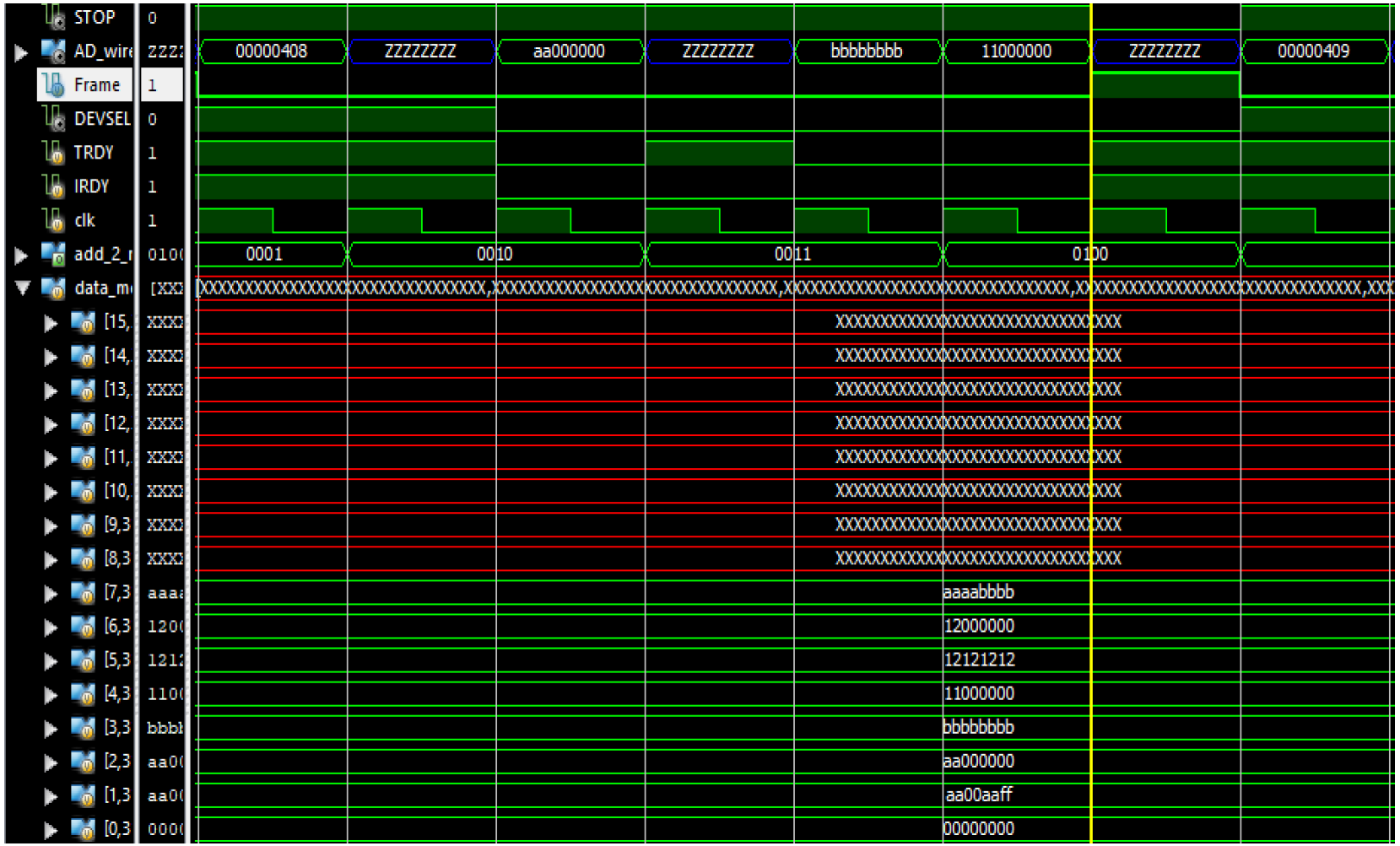
Read Memory and Write (Increment Mode)

- Termination from target

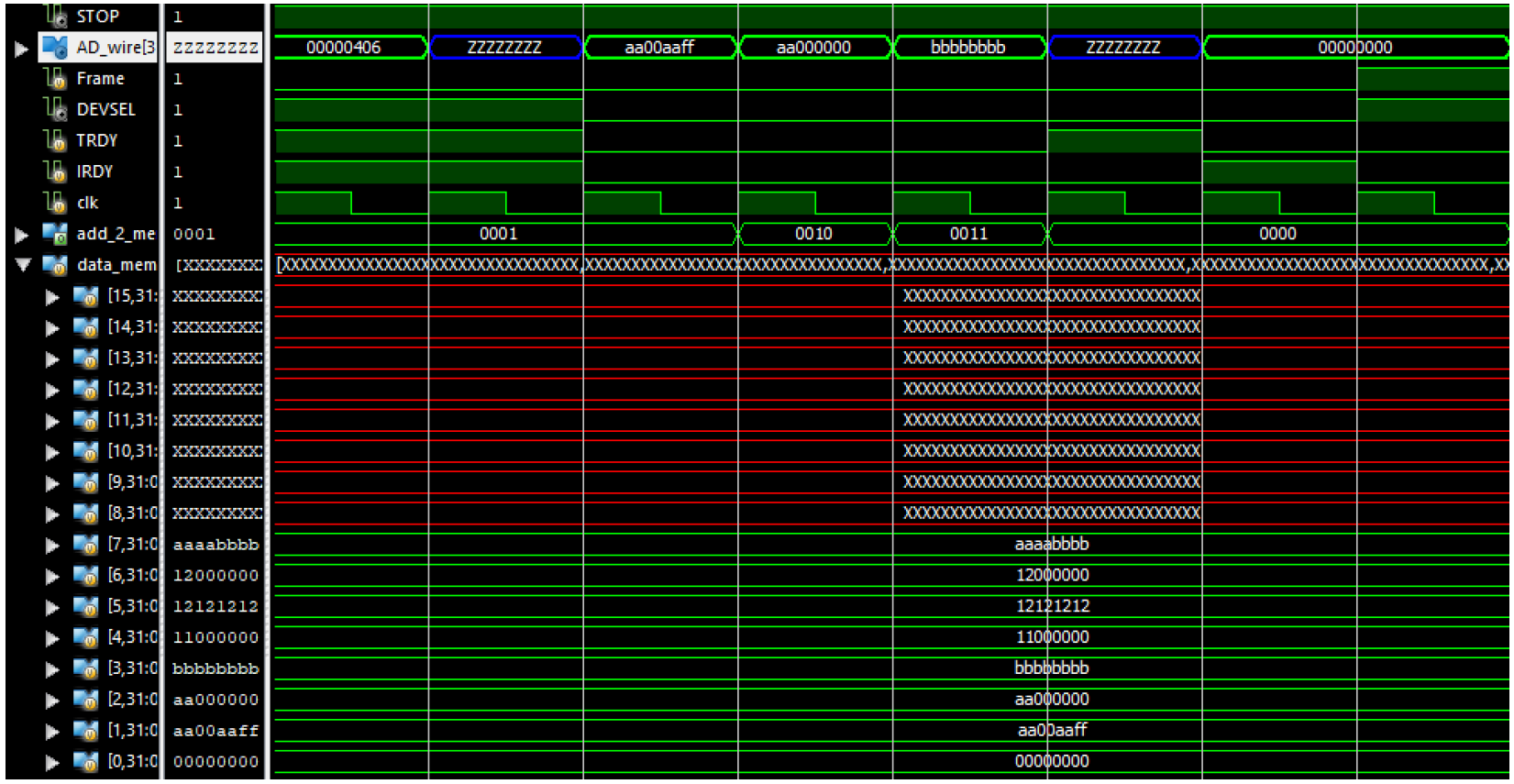


Read Line (Reserved Mode)

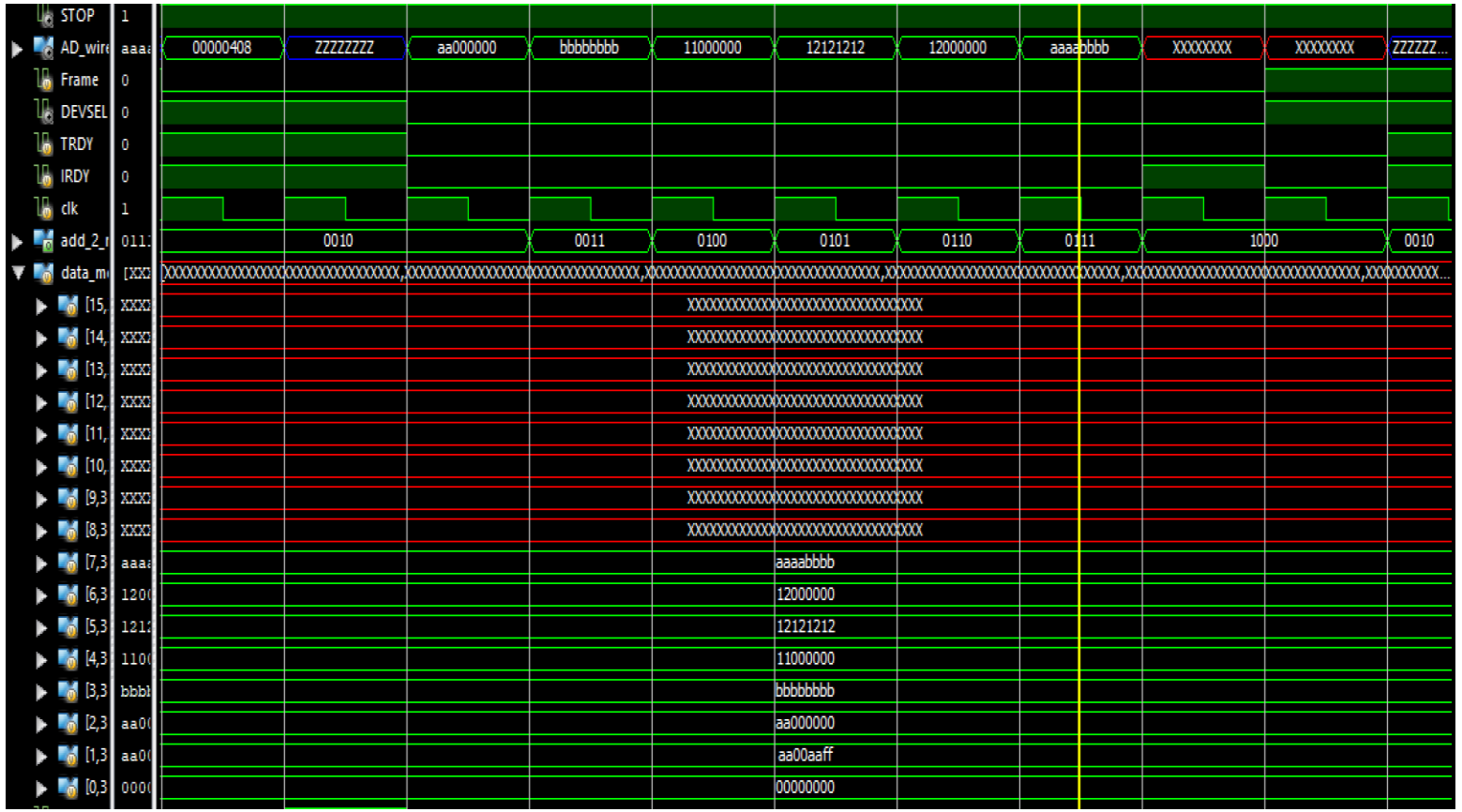
Read Line (Increment Mode)



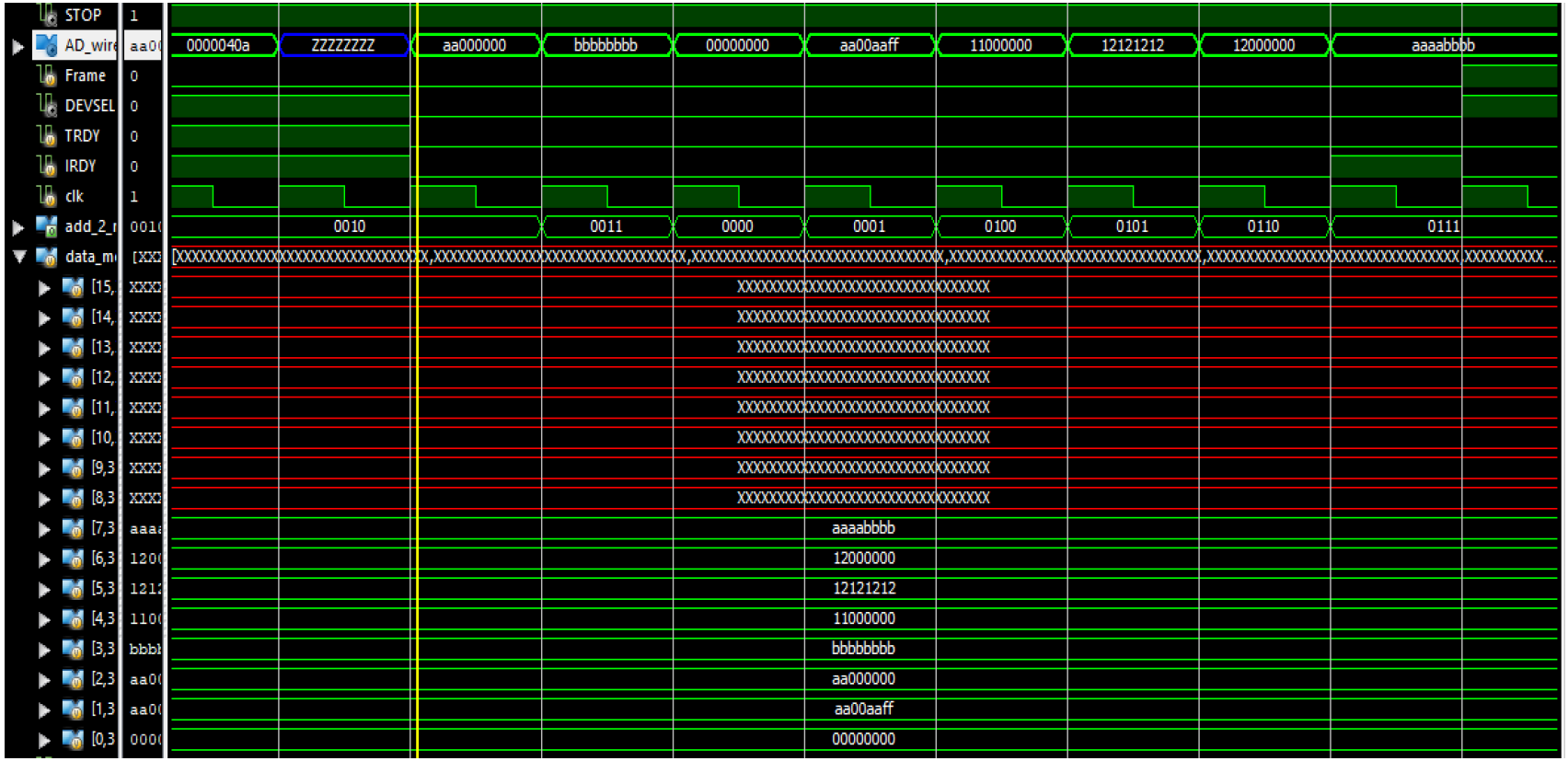
Read Line (Wrap Mode)



Read Multiple (Increment Mode)



Read Multiple (Wrap Mode)



Thank You