

Programação Paralela: das *threads* aos FPGAs

Computação Reconfigurável

Prof. Ricardo Menotti
menotti@ufscar.br

Prof. Maurício Accocia Dias
macccdias@gmail.com

Prof. Helio Crestana Guardia
helio.guardia@ufscar.br

Departamento de Computação
Universidade Federal de São Carlos

Atualizado em: 6 de maio de 2020

Conteúdo

Introdução

FPGAs

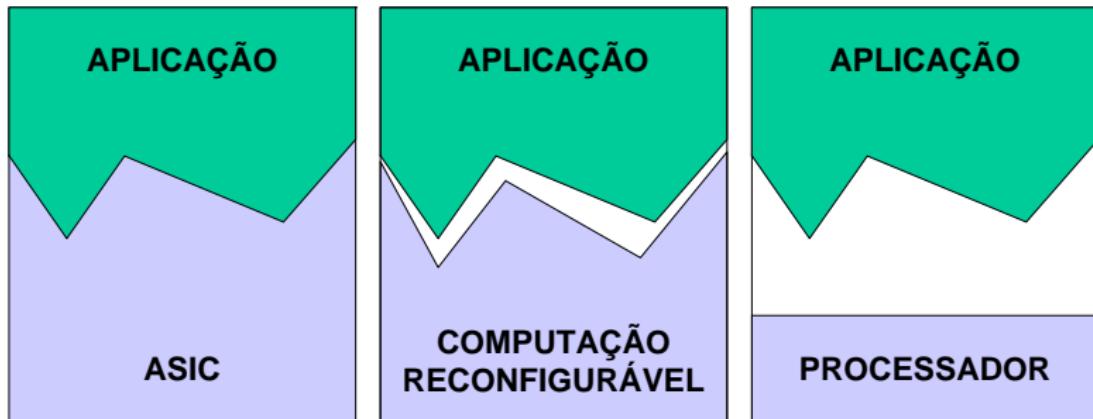
Desenvolvimento

Aplicações

Bibliografia

Métodos de computação

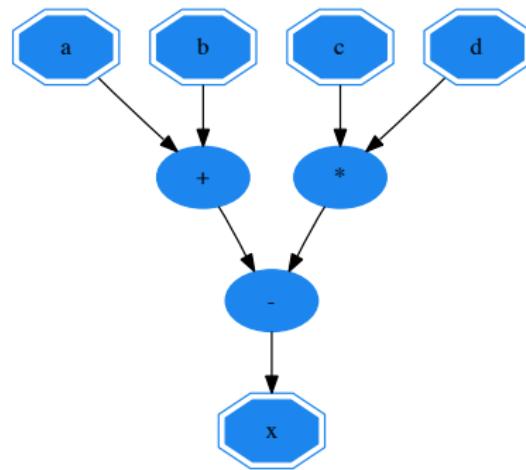
[Menotti(2010)]



Métodos de computação

[Menotti(2010)]

Espacial



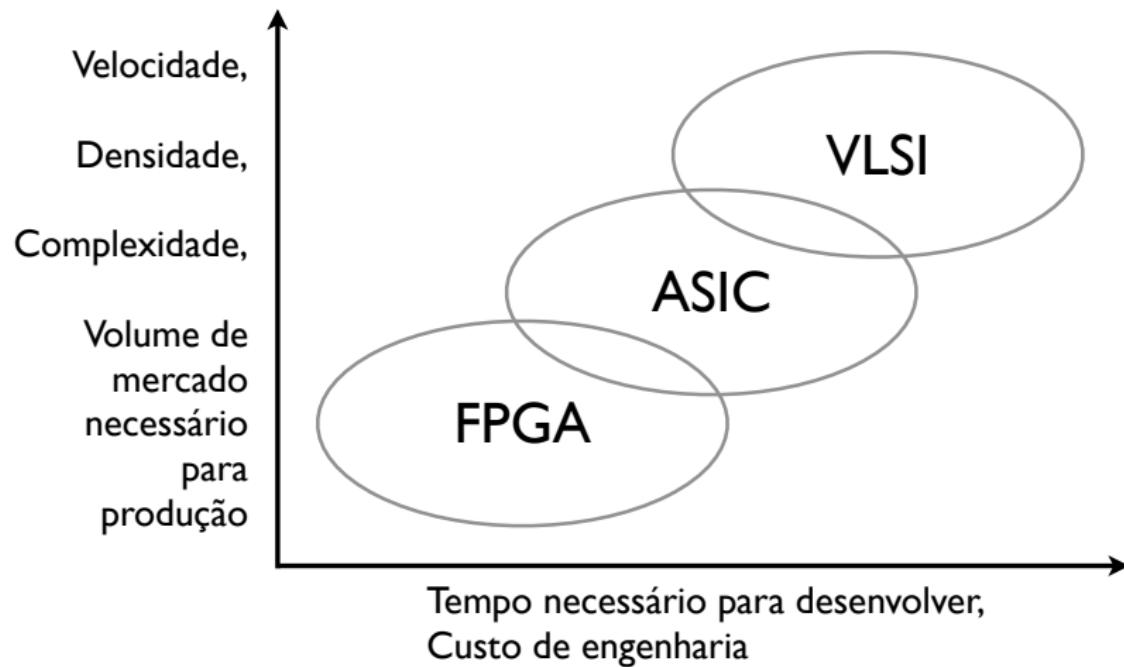
Temporal

```
1 x = a + b - c * d;
```

```
1 t1 = a + b  
2 t2 = c * d  
3 x = t1 - t2
```

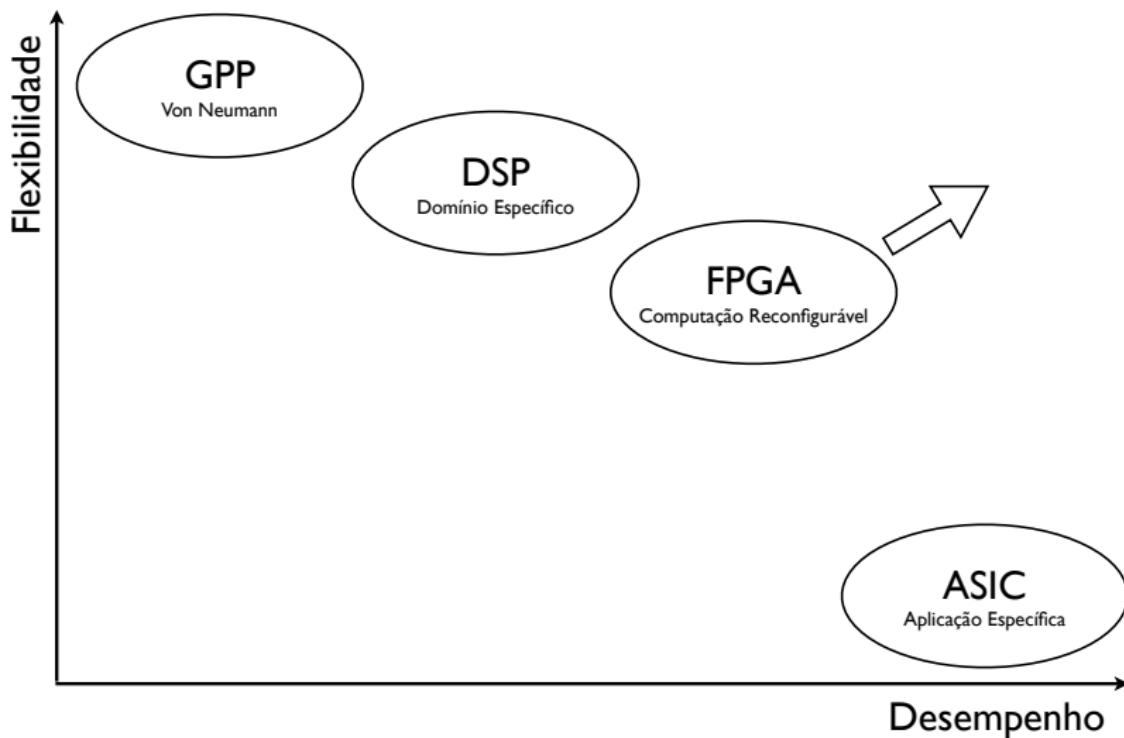
Mercado de lógica digital

[Hamblen and Furman(2001)]

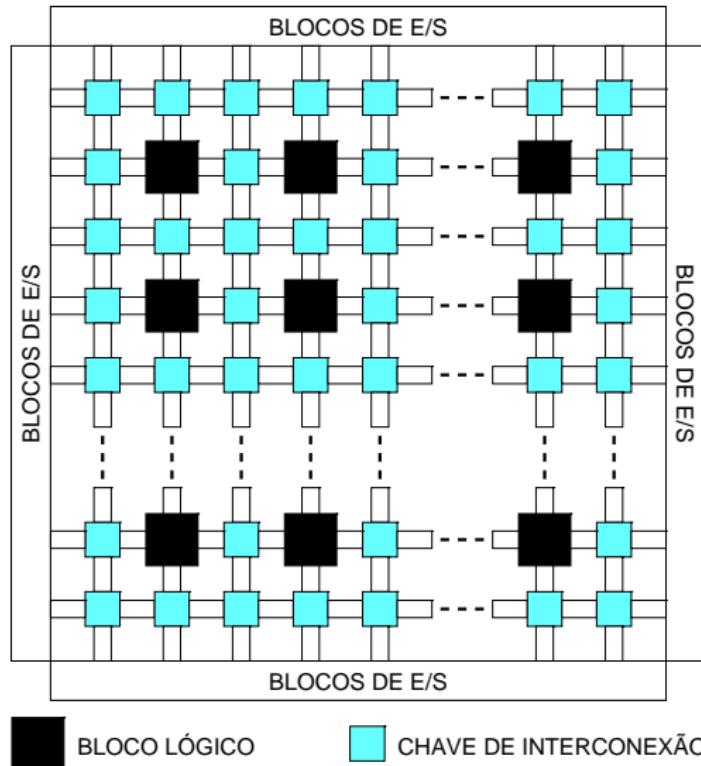


Relação entre flexibilidade e desempenho

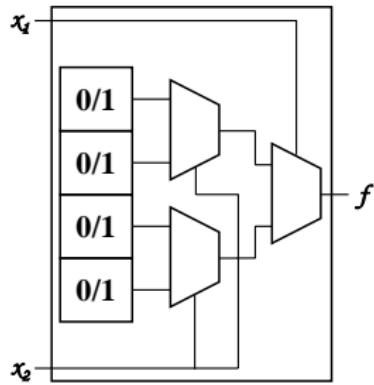
[Bobda(2007)]



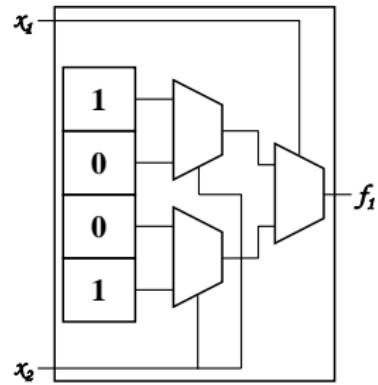
Estrutura básica de um FPGA



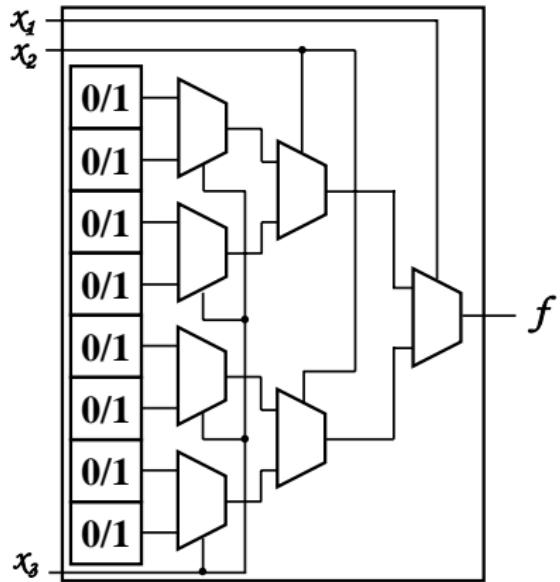
Uso de LUTs para implementação de funções lógicas



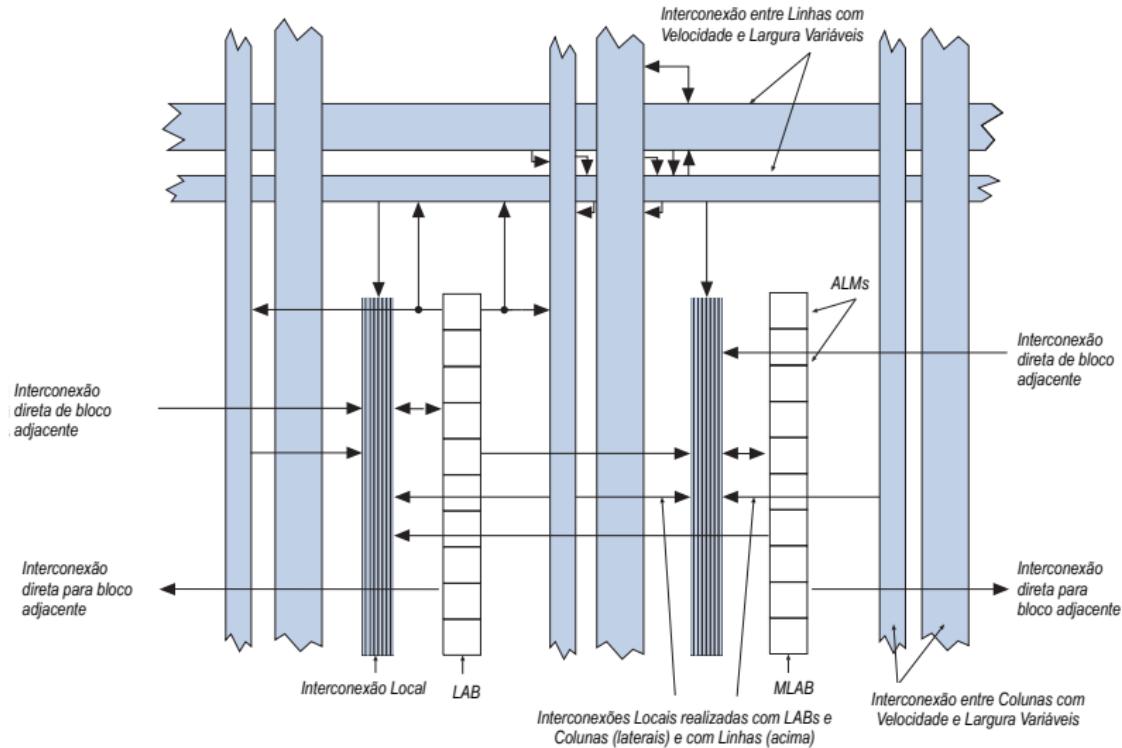
x_1	x_2	f_1
0	0	1
0	1	0
1	0	0
1	1	1



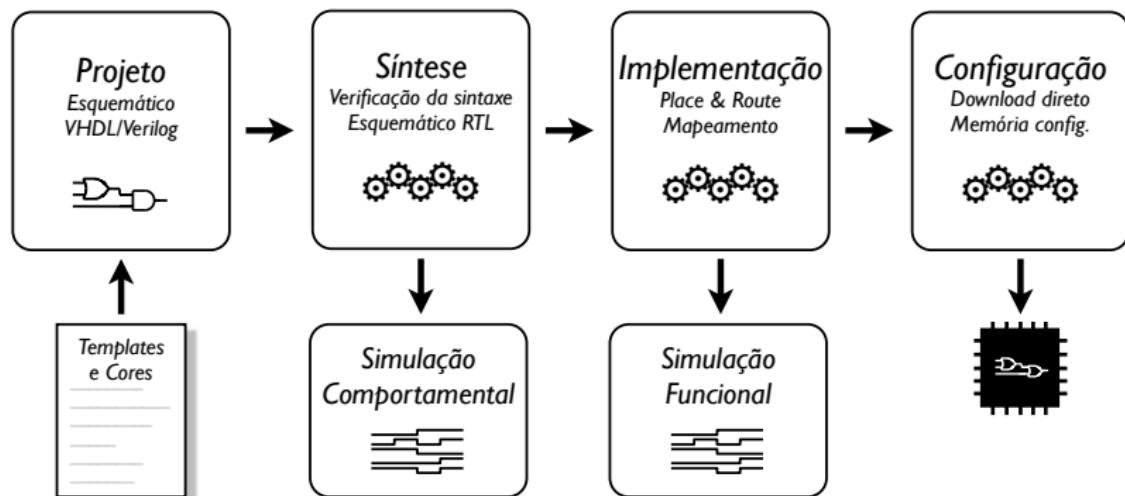
Circuito de uma LUT de três entradas



Elementos Lógicos



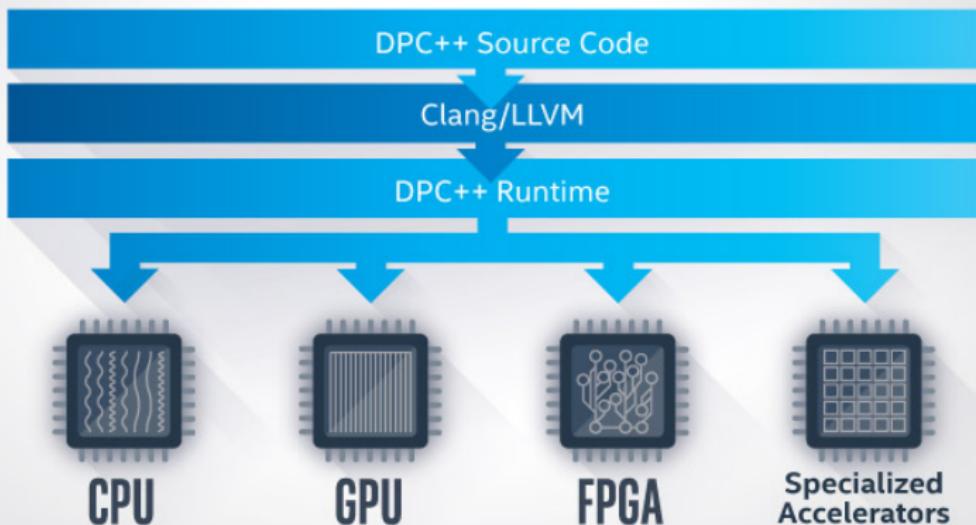
Desenvolvimento: Fluxo clássico



<https://www.edaplayground.com/x/5TaK>

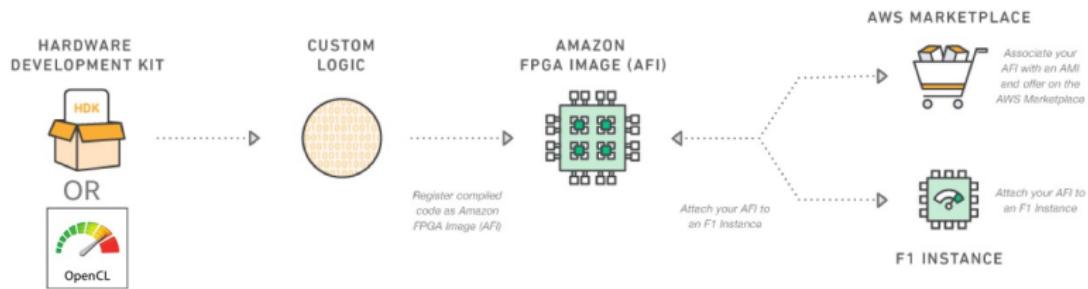
Desenvolvimento: oneAPI

OneAPI DPC++ Compiler and Runtime



<https://software.intel.com/en-us/oneapi/dpc-compiler>

Desenvolvimento: Amazon AWS F1



<https://aws.amazon.com/ec2/instance-types/f1/>

<https://github.com/aws/aws-fpga>

Desenvolvimento: HardCloud



HardCloud
FPGA Computing Made Easy!

Home Wiki Video Blog Publications Contact

HardCloud

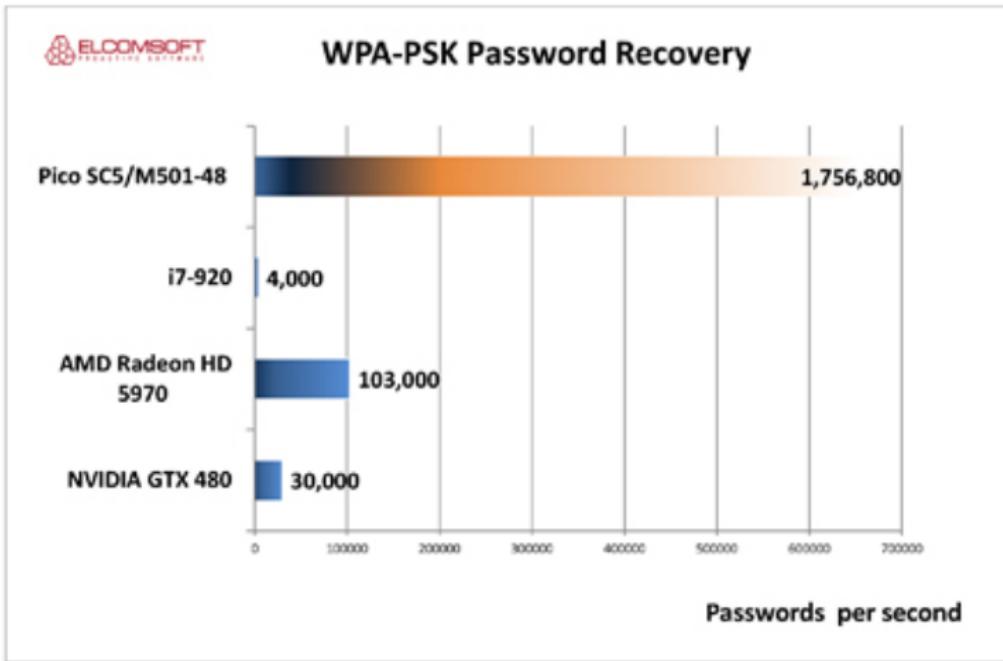
The computing industry has recently proposed the use of FPGAs as a way to improve performance and energy efficiency in modern cloud clusters. Unfortunately, using such FPGA clusters is a very hard and complex task. In this context, we present HardCloud a novel and simple mechanism to offload computation to the FPGAs available in the Intel HARP2 platform and AWS F1 instances. HardCloud extends OpenMP directives in such a way that the FPGA becomes just another OpenMP acceleration device that can be used directly from any user program.

Offloading a pre-synthesized module

```
#pragma omp target device(HARP | AWSF1) map(to: X) map(from: Y)
#pragma omp parallel for use(hrw) module(loopback)
// Software version of the loopback hardware module.
for (int i = 0; i < NI; i++) {
    Y[i] = X[i];
}
```

<https://omphardcloud.github.io/>

Aplicações: Password Crack

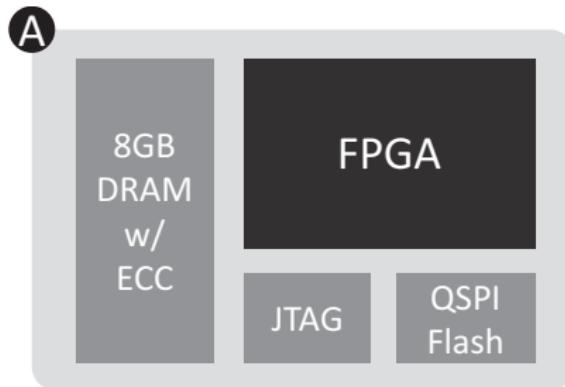


Aplicações: Password Crack



Aplicações: Catapult – Bing – Microsoft

[Putnam et al.(2014) Putnam, Caulfield, Chung, Chiou, Constantinides, Demme, Esmaeilz]



Aplicações: CERN

The screenshot shows a web browser displaying the CERN openlab website. The title bar reads "ESR 2 Position: FPGA | CERN openlab". The page header includes the CERN logo and the tagline "Accelerating science". Navigation links include "Sign in" and "Directory". A banner image features the CERN openlab logo and three people working in a technical environment. Below the banner is a navigation menu with links: Home, News | Events, About CERN openlab, Competence Centres | Projects, Publications, Education, Resources, Industry Members, and Jobs. A search bar is also present. The main content area displays a job listing for an "ESR 2 Position: FPGA". The job description asks if the reader wants to work on high-speed reconfigurable logic at CERN and at Intel. It mentions the ICE-DIP project and its goal of seeking bright candidates in computer science and engineering for doctoral training. The "The Challenge" section provides a brief overview of CERN's role in particle physics research.

ESR 2 Position: FPGA | CERN openlab

CERN Accelerating science

Sign in Directory

CERN openlab

Home News | Events About CERN openlab Competence Centres | Projects Publications Education Resources Industry Members Jobs

Search Jobs » ICE-DIP Positions » ESR 2 Position: FPGA

ESR 2 Position: FPGA

Do you want to work on high-speed reconfigurable logic at CERN and at Intel?

ICE-DIP is the Intel-CERN European Doctorate Industrial Program, a Marie Curie Actions project within the European Union's 7th Framework Programme. For its newly opened research posts, ICE-DIP is seeking bright candidates in the areas of computer science and engineering to undertake doctoral training.

The Challenge

CERN is the European Organization for Nuclear Research – a world-wide particle physics laboratory in Geneva, Switzerland and home to the largest machine ever built by man, the Large Hadron Collider (LHC). Every year, the four major LHC experiments collect over 25 petabytes of data. These collaborations are now planning upgrades which will increase data

Aplicações: LNLS



CNPEM

Centro Nacional de Pesquisa
em Energia e Materiais



Laboratório Nacional
de Luz Síncrotron

Vaga de estágio

O PROJETO SIRIUS

O Laboratório Nacional de Luz Síncrotron (LNLS), integrante do Centro Nacional de Pesquisa em Energia e Materiais (CNPEM), está projetando um complexo de aceleradores de partículas para abrigar a nova fonte de luz síncrotron brasileira, o Sirius. O novo anel de armazenamento, já em construção em Campinas, possuirá circunferência de aproximadamente 500 metros, por onde circulará um feixe de elétrons com energia de 3 GeV viajando a 99,9999% da velocidade da luz. Com uma emitância de 0,28 nm.rad, o Sirius figurará como uma das máquinas do gênero mais competitivas em escala internacional.



Visão artística do novo acelerador de partículas, Sirius.

Bibliografia I

-  [Christophe Bobda.](#)
Introduction to Reconfigurable Computing: Architectures, Algorithms and Applications.
Springer, 2007.
-  [J. O. Hamblen and M. D. Furman.](#)
Rapid Prototyping of Digital Systems.
Kluwer, 2001.
-  [Ricardo Menotti.](#)
LALP: uma linguagem para exploração do paralelismo de loops em computação reconfigurável.
PhD thesis, Universidade de São Paulo, 2010.

Bibliografia II



Andrew Putnam, Adrian M. Caulfield, Eric S. Chung, Derek Chiou, Kypros Constantinides, John Demme, Hadi Esmaeilzadeh, Jeremy Fowers, Gopi Prashanth Gopal, Jan Gray, Michael Haselman, Scott Hauck, Stephen Heil, Amir Hormati, Joo-Young Kim, Sitaram Lanka, James Larus, Eric Peterson, Simon Pope, Aaron Smith, Jason Thong, Phillip Yi Xiao, and Doug Burger.

A reconfigurable fabric for accelerating large-scale datacenter services.

In *Computer Architecture (ISCA), 2014 ACM/IEEE 41st International Symposium on*, pages 13–24, June 2014.
doi: 10.1109/ISCA.2014.6853195.

Programação Paralela: das *threads* aos FPGAs

Computação Reconfigurável

Prof. Ricardo Menotti
menotti@ufscar.br

Prof. Maurício Accocia Dias
macccdias@gmail.com

Prof. Helio Crestana Guardia
helio.guardia@ufscar.br

Departamento de Computação
Universidade Federal de São Carlos

Atualizado em: 6 de maio de 2020