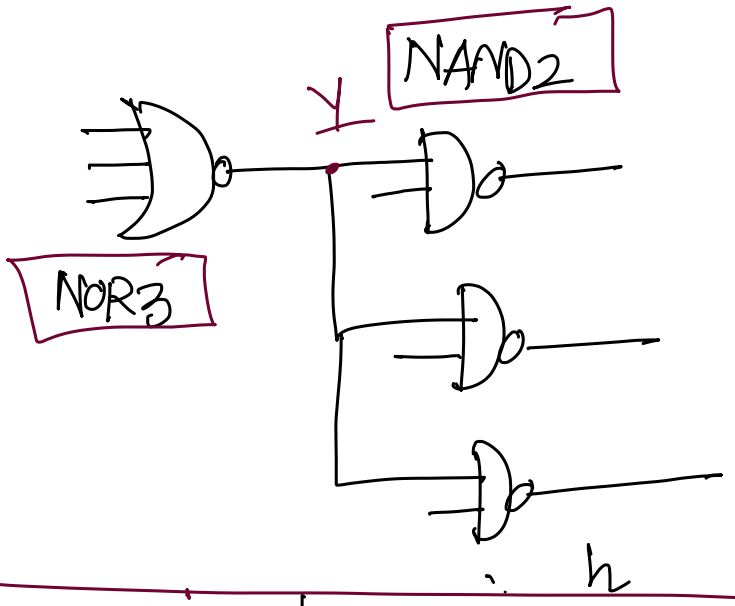
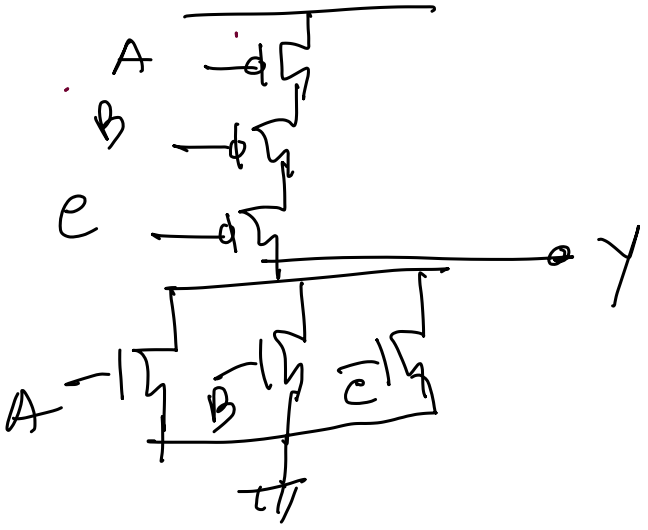
if $\mu_n = 3\mu_p$, find all the delays at node Y where the output of NOR3 gate drives h identical NAND2 gates (single input).





if $\mu_n = 3\mu_p \rightarrow R_n = R_p/3$

$\therefore R_p = 3R_n = 3R$

PMOS → $3R/k_p$,

NMOS → R/k_n

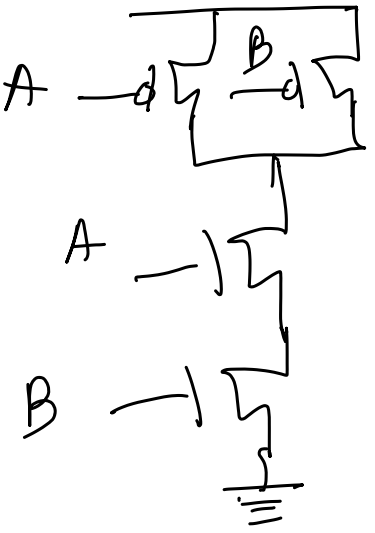
$R_{rise} = R_{fall} = R$

worst case (1 nmos on)

$3 \times \frac{3R}{k_p} = \frac{R}{k_n} = R$

$\Rightarrow k_p = 3, \; k_n = 1$

NOR3



$R_{rise} = R_{fall} = R$

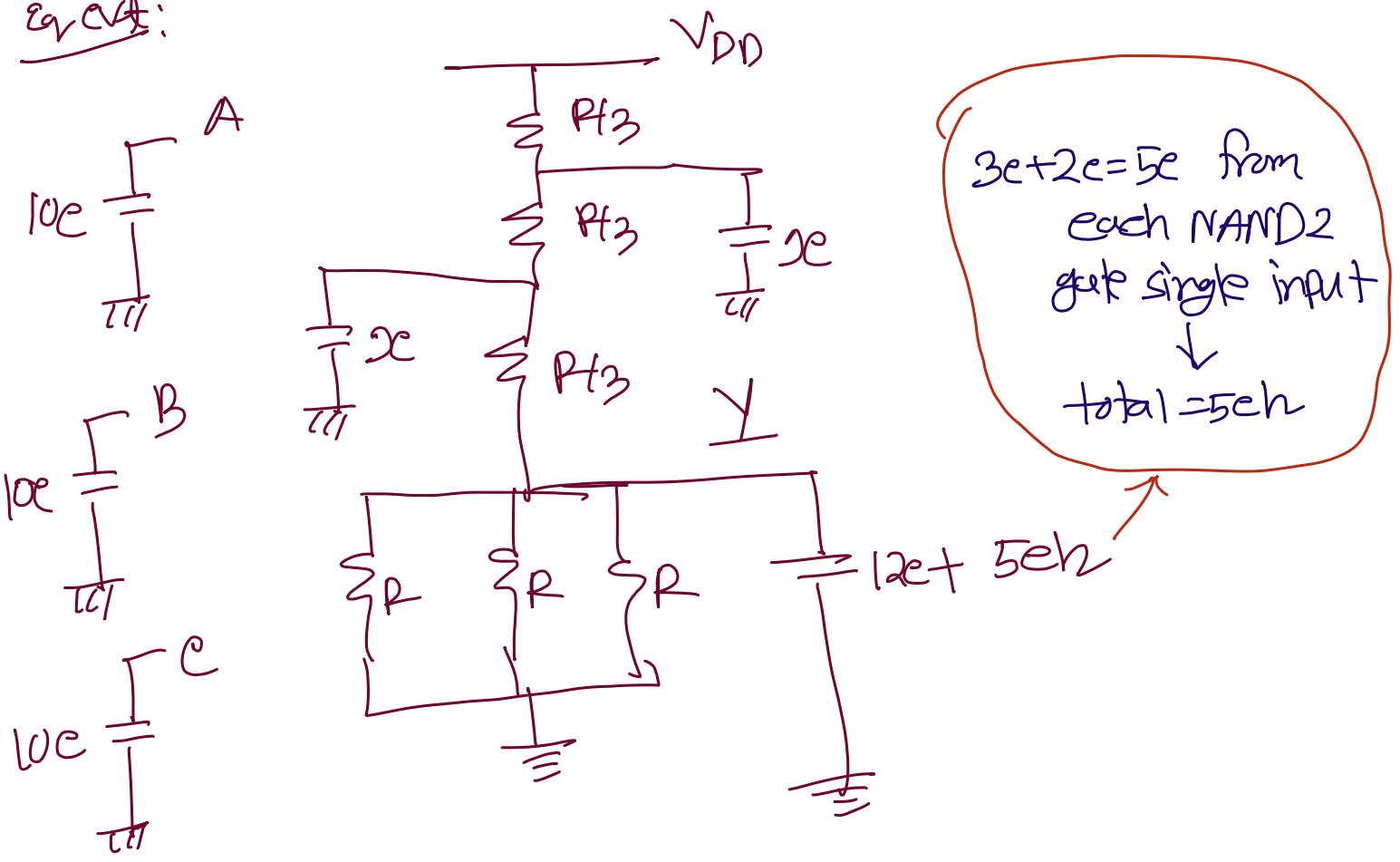
worst case (1 pmos on)

$\frac{3R}{k_p} = \frac{2R}{k_n} = R$

$\therefore k_p = 3, \; k_n = 2$

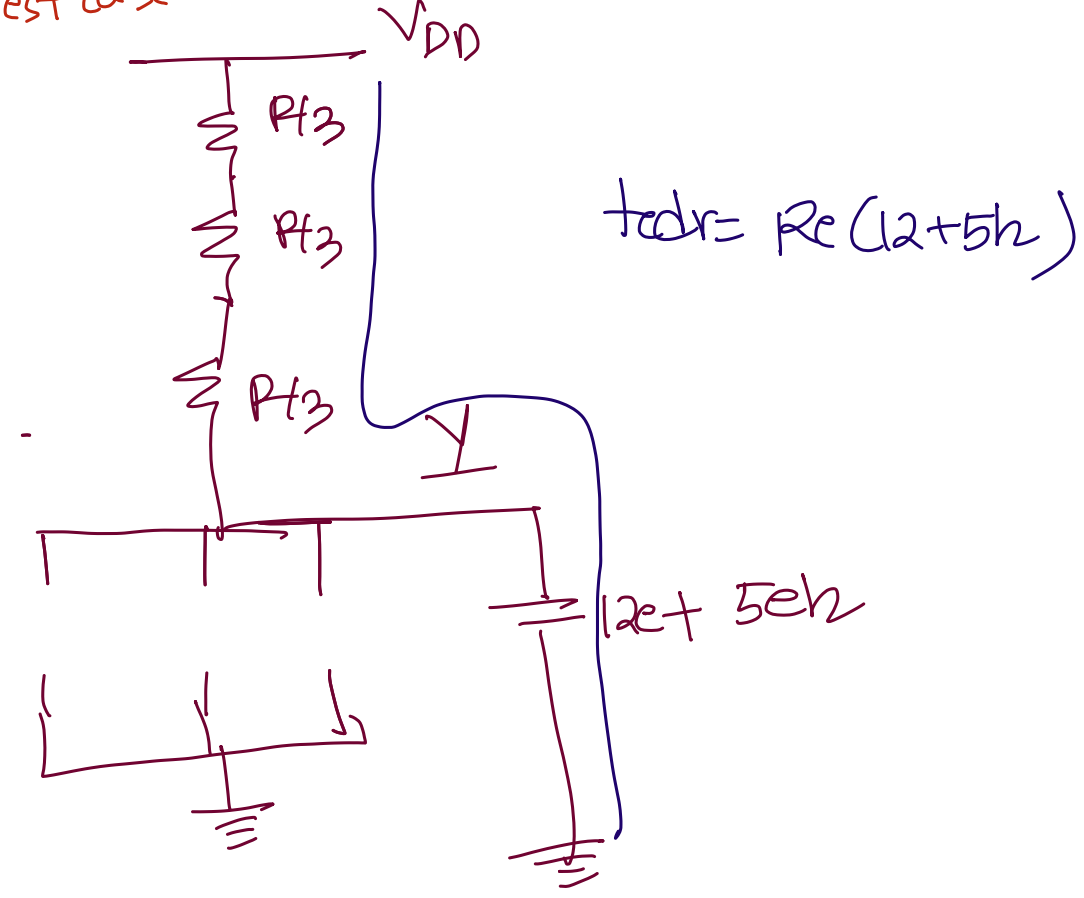
NAND2

Eg cont:



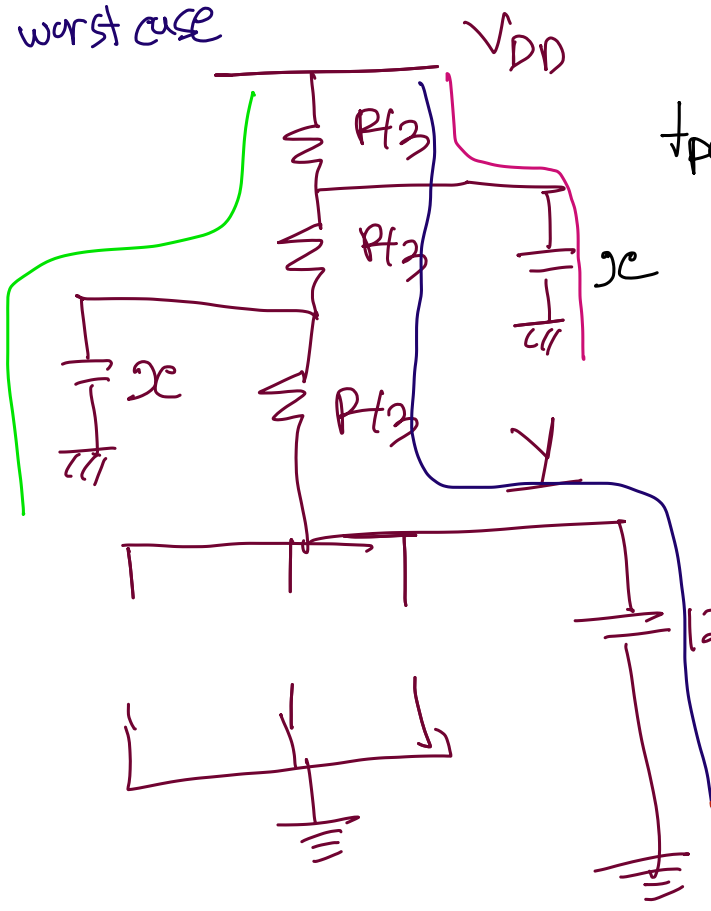
3c+2c=5c from each NAND2 gate single input
↓
total =5ch

tedr : best case



tedr= Rc(12+5h)

t_{pdr} : worst case



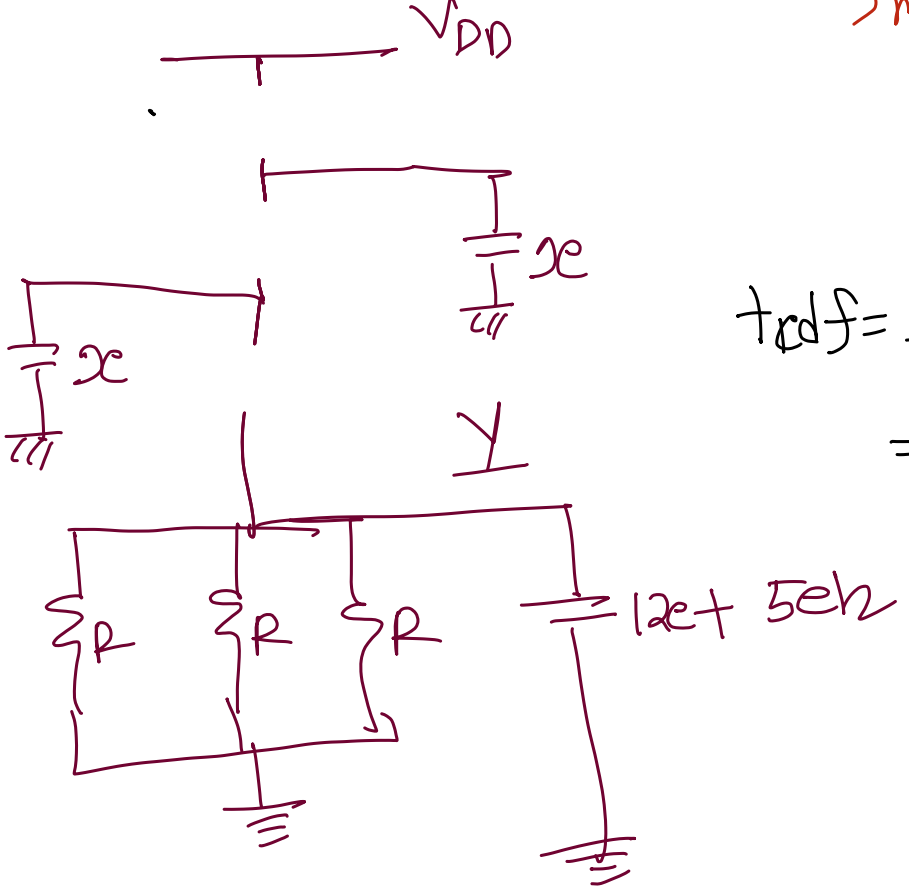
$t_{pdr} = R(12c+5h) + \frac{R}{3} \times 3c + \left(\frac{R}{3} + \frac{R}{3}\right) \times c$

$= Rc(21 + 5h)$

Same for 12c Delay & Elmore Delay model

main propagation path

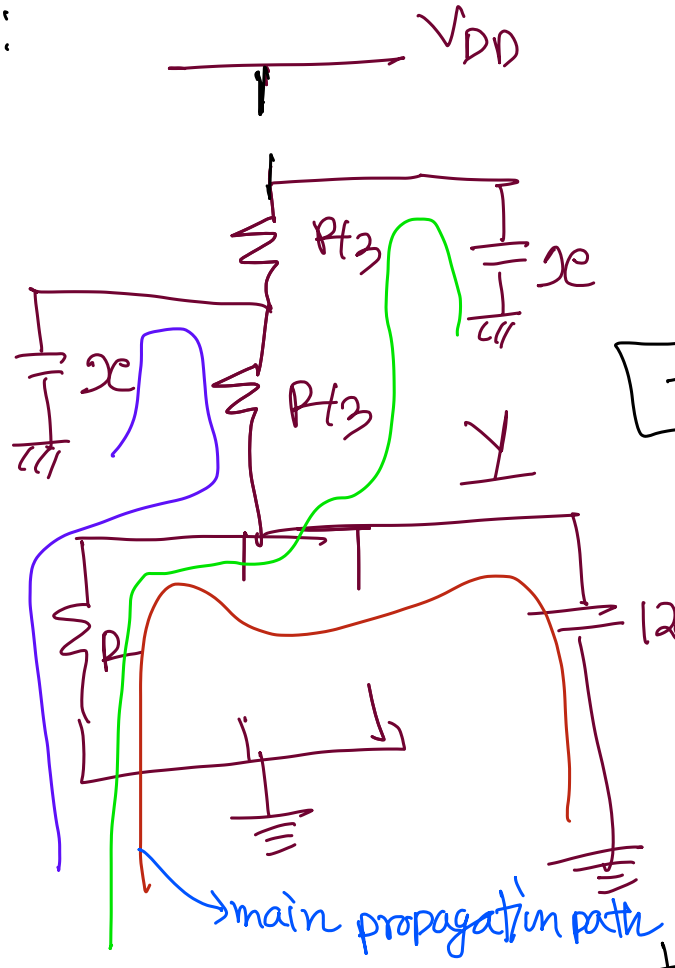
t_{cdf} :



$t_{cdf} = \frac{R}{3}(12c+5ch)$

$= Rc\left(4 + \frac{5}{3}h\right)$

t_{pdf} :



Elmore

$t_{pdf} = R(12c+5ch) + Rx2c + Rx2c$

$t_{pdf} = Rc(30+5h)$

Rc delay

$t_{pdf} = R(12c+5ch) + (R+\frac{R}{3})2c + (R+\frac{R}{3}+\frac{R}{3})2c$

$= Rc(12+5h) + 12Rc + 15Rc$

$t_{pdf} = Rc(39+5h)$

*** For NAND gate t_{pdr} is different for Rc delay & Elmore delay. And for NOR gate t_{pdf} is different for Rc delay & Elmore Delay.