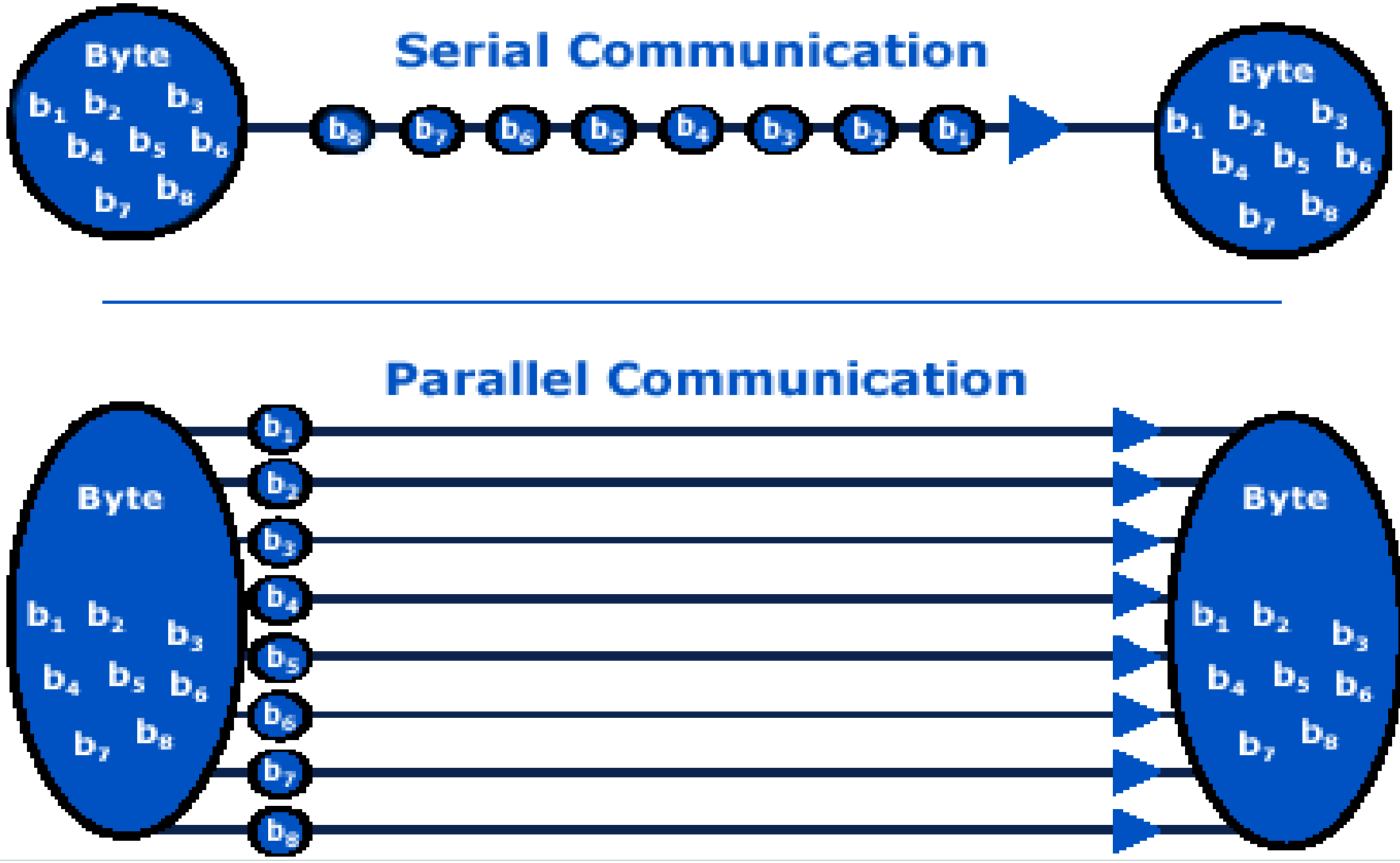
PRIORITY INTERRUPT

- A priority interrupt is a system that establishes a priority over the various source to determine which condition is to be survived first when two or more request arrive simultaneously.

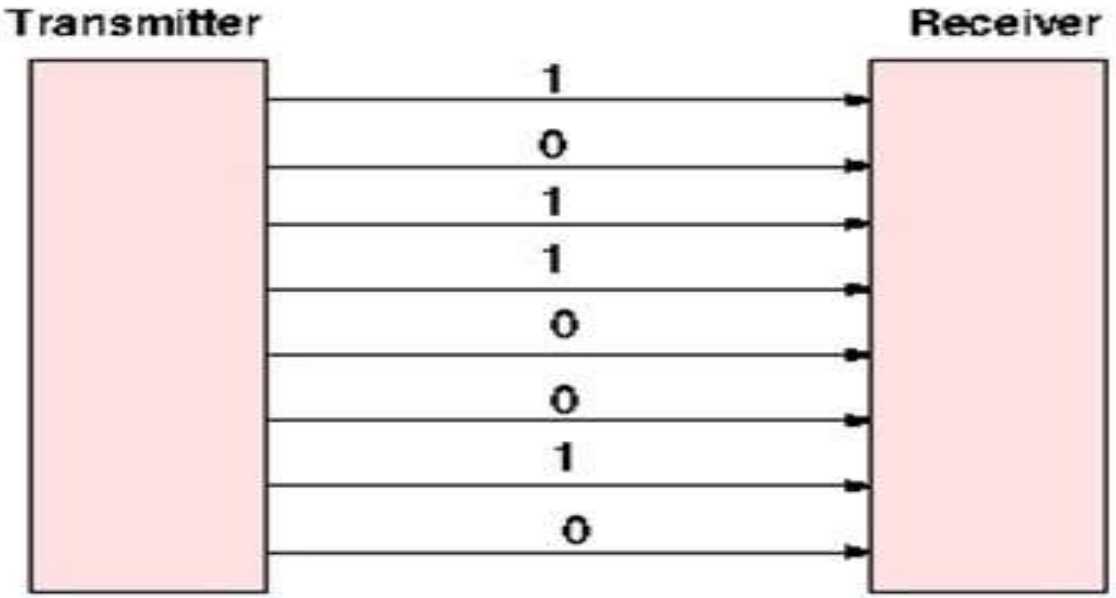
- Devices with high speed transfer such as magnetic disk are given highest priority.

Polling

- Establishing the priority of simultaneous interrupt can be done by software or hardware.
- A polling procedure is used to identify the highest priority by the software.
- The hard ware priority interrupt unit function as an overall manager in the system environment.
- The hardware priority function can be established by either serial or parallel connection line.


Serial Communication
Byte
b1 b2 b3
b4 b5 b6
b7 b8
b8 b7 b6 b5 b4 b3 b2 b1
Byte
b1 b2 b3
b4 b5 b6
b7 b8
Parallel Communication
Byte
b1 b2 b3
b4 b5 b6
b7 b8
b1
b2
b3
b4
b5
b6
b7
b8
Byte
b1 b2 b3
b4 b5 b6
b7 b8

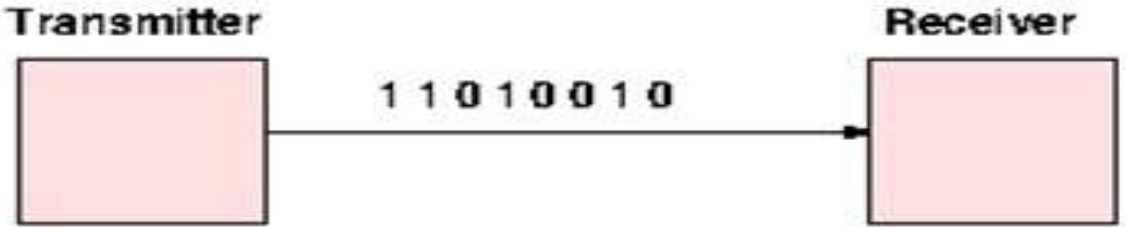
Parallel Transmission



Message: 10110010

All bits are sent at once

Serial Transmission



Message: 11010010

bits are transmitted one at a time

DAISY CHAINING PRIORITY

- The daisy chaining method of establishing priority consists of a serial connection of all devices that request an interrupt.
- The interrupt request line is common to all devices and forms a wired logic connection if any devices The daisy chaining method of establishing priority consist of a serial connection of all devices that has its interrupt signal in the low-level state .

- the CPU response to an interrupt request by enabling the interrupt acknowledgement line.
- If device 1 has a pending interrupt it shows the acknowledgment signal from the next devices by placing a PI and the PO output.

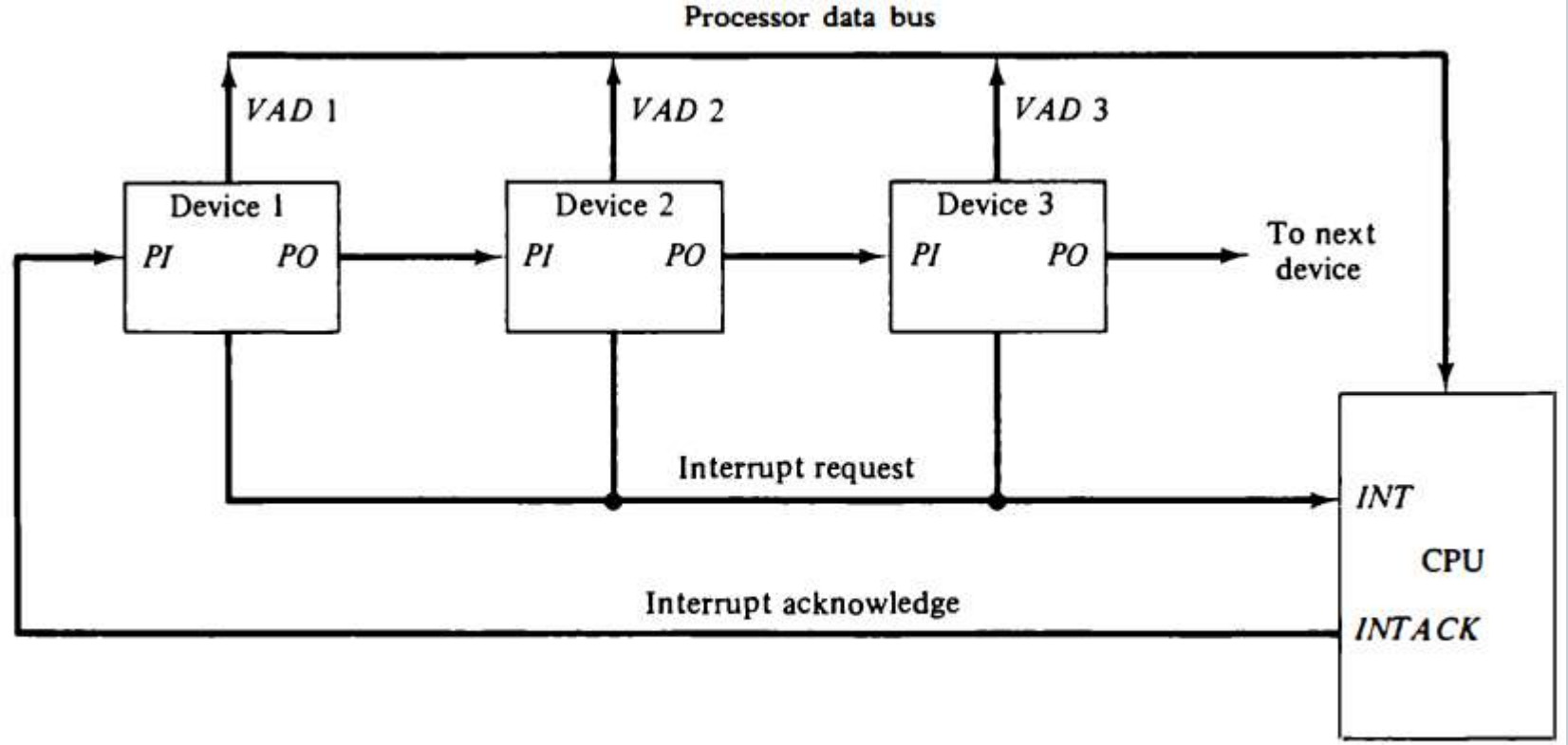


Figure 12 Daisy-chain priority interrupt.

PARALLEL PRIORITY INTERRUPT

- The parallel priority interrupt method uses a register whose bits are separated from each device
- Priority is established according to the position of the bits in the register.
- The interrupt register may include a mask register to control the status of interrupt request.
- The priority logic for a system have the four interrupt sources.
- It consist of an interrupt register which the bits are represented by the program.

- Next the printer reader and the keyboard by the means of program instruction
- It is possible to set or reset any bit in the mask register.
- The INT ACK signal from the CPU enable the bus in the output register and a vector address (VAD) is placed in to the databus.

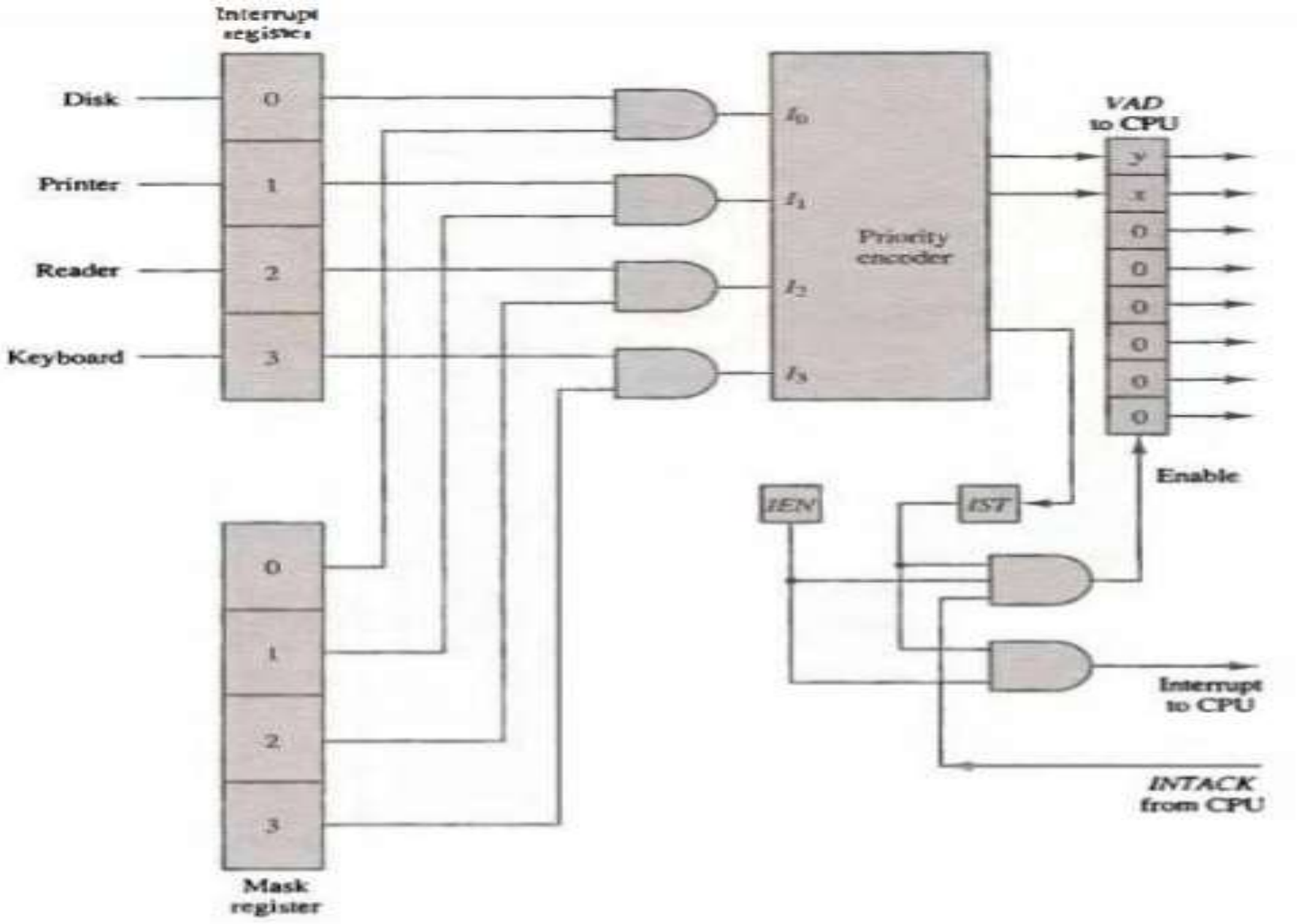


Figure 14 Priority interrupt hardware.

DMA (DIRECT MEMORY ACCESS)

- **Direct memory access** (**DMA**) is a feature of **computer** systems that allows certain hardware subsystems to **access** main system **memory** (random-**access memory**) independent of the central processing unit (CPU). **DMA** can also be used for "**memory** to **memory**" copying or moving of data within **memory**.

- The transfer of data between a fast storage devices such as a magnetic disk and memory is linked by the speed of CPU.
- Removing the CPU from the path and giving the peripheral devices manage the memory bus directly to improve the speed of transfer this technique is called Direct Memory Access.
- DMA controller takes over the bus to manage the transfer directly between the input devices memory

- The bus request BR (bus request) is used by DMA controller to request the CPU to relinguish control of buses.
- The CPU activate the bus grant output to inform the external DMA .The CPU disables the bus grant,takes control of the buses,and returns to its normal operations.
- The burst transfer consisting of a number of words is transferred into the memory bus.
- The techniques cycle stealing is used for the data transfer that cannot be stopped or slow down until the entire block is transferred .

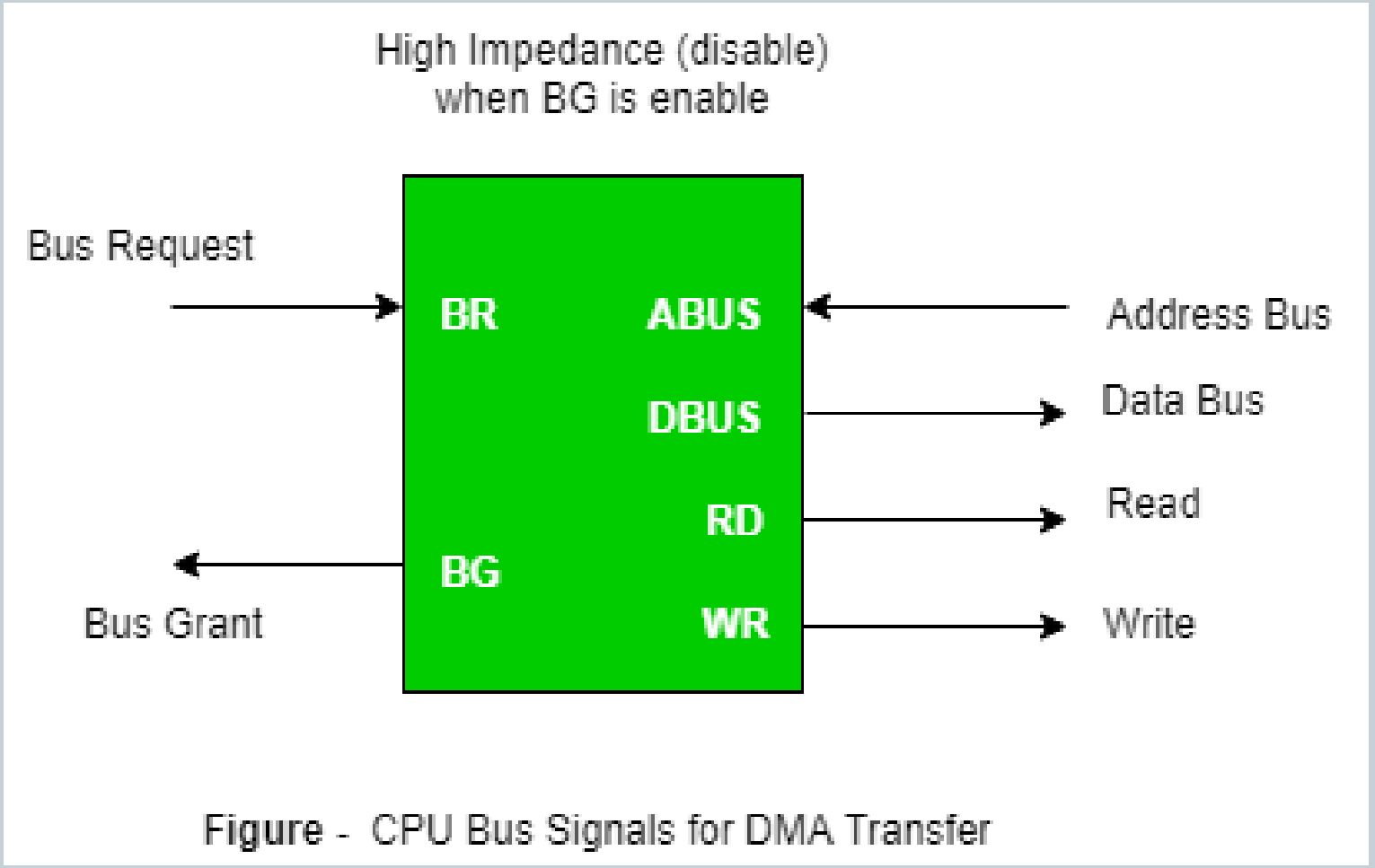
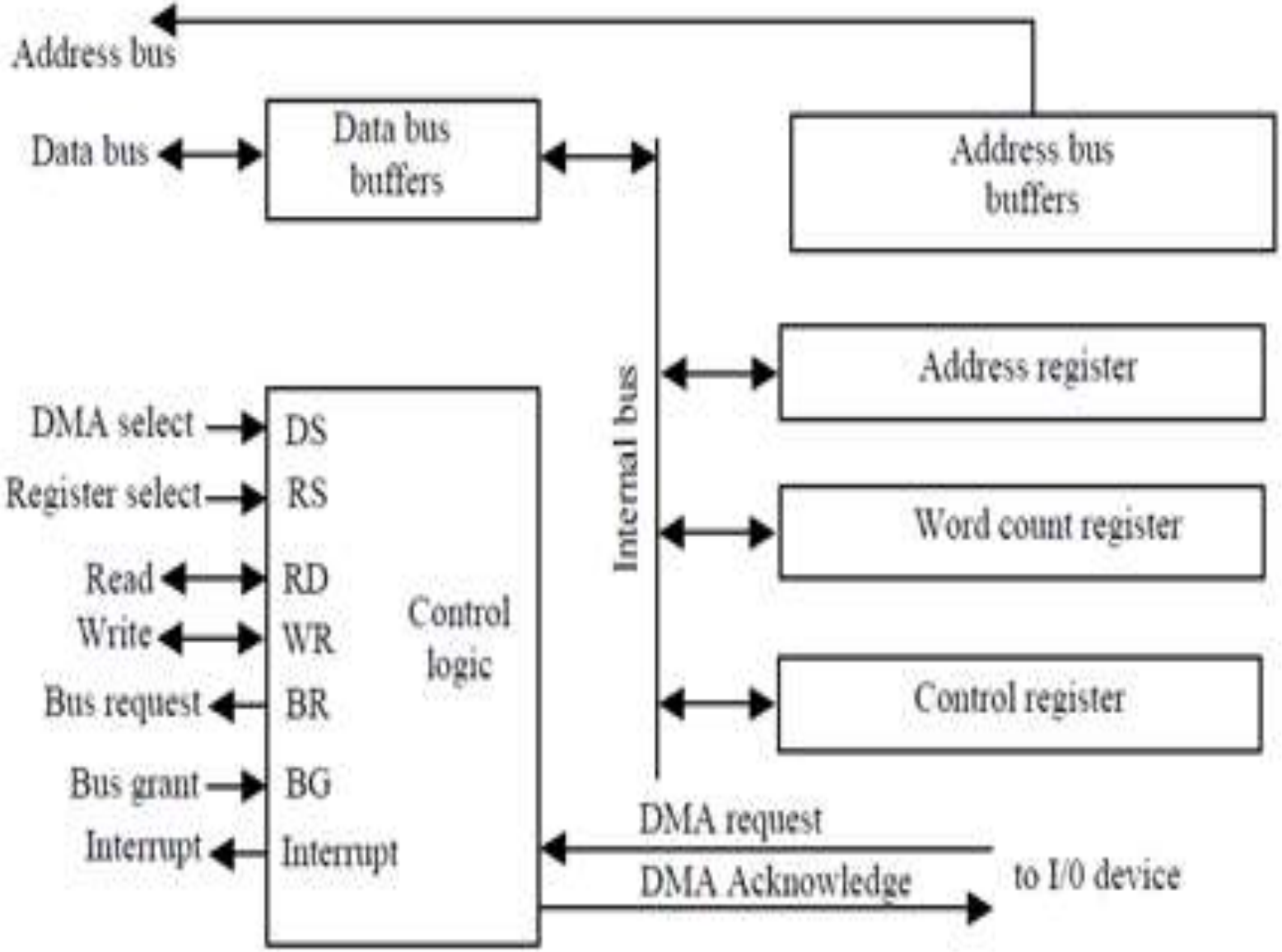


Figure - CPU Bus Signals for DMA Transfer

DMA CONTROLLER

- DMA controller is used to communicate with CPU and input output devices.
- The DMA controller that communicate with the data bus and control line within the memory the register in the DMA are selected by CPU through the address bus by enabling DS and RS
- The read and write are bidirectional.

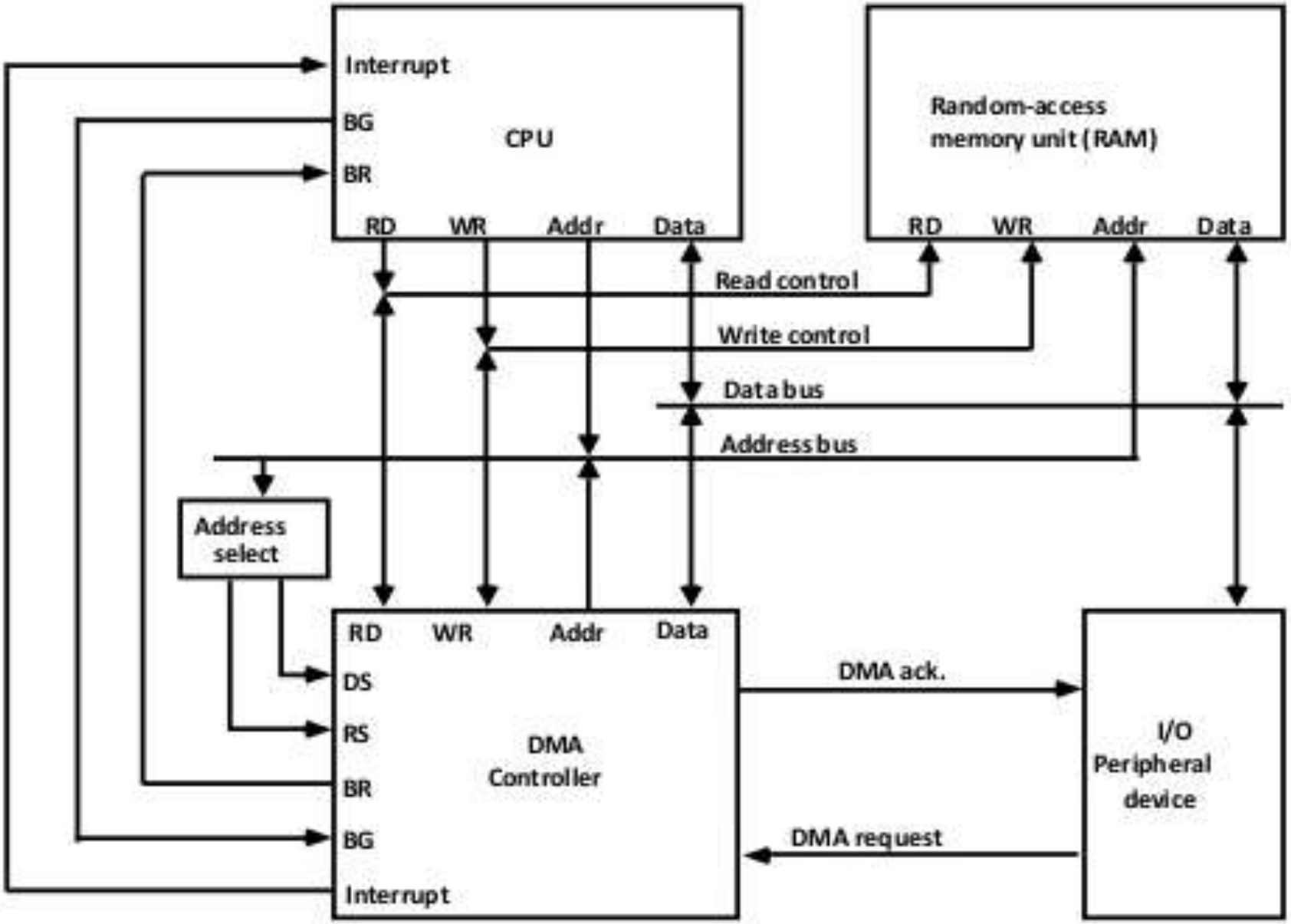
- When bus grant is 0 the cpu can communicate with DMA register
- When BG=1 the cpu can relinquish the DMA which communicate directly with the memory.
- The control register specifies the mode of transfer.
- The CPU initializes the DMA by sending the following information through the data bus:
- The starting address of the memory block where data are available or where data are to be stored .
- The word count which is the number of words in the memory block
- Control to specify the mode of transfer such as read or write.
- A control to start the DMA transfer


Address bus
Data bus
Data bus buffers
Address bus buffers
Internal bus
Address register
Word count register
Control register
DMA select
Register select
Read
Write
Bus request
Bus grant
Interrupt
DS
RS
RD
WR
BR
BG
Interrupt
Control logic
DMA request
DMA Acknowledge
to I/0 device

DMA TRANSFER

- When the peripheral device sends a DMA request , the DMA controller activate the BR line , information the CPU to relinquish the buses.
- The CPU resposds with the BG line, informing the DMA that uits buses are disabled.
-
- The DMA then puts the current value of its address registerebinto the address register into the address bus, initiated the RD or WR signal, and sends a DMA acknowledge to the peripheral device.
- When the peripheral device receives a DMA acknowledge , it puts a words in data bus or receives a word from the data bus.

- Thus the DMA control the read or write operations and supplies the address for the memory.
- The peripheral unit can then communicate with memory through the data.
- The DMA controller may have more than one channel.
- It is used for fast transfer of information between magnetic disk and memory.
- It is also used for updating the display.


Interrupt
BG
BR
CPU
RD
WR
Addr
Data
Random-access
memory unit (RAM)
RD
WR
Addr
Data
Read control
Write control
Data bus
Address bus
Address
select
RD
WR
Addr
Data
DS
RS
BR
BG
Interrupt
DMA
Controller
DMA ack.
DMA request
I/O
Peripheral
device

INPUT – OUTPUT PROCESSOR

- Interface communicate with the CPU , a computer may incorporate one or more external processor and assign them the task of communicating directly with all I/O devices.
- The memory unit occupies a central position and can communicate with each processor by means of direct memory access.
- The CPU is responsible for processing for processing data needed in the solution of computationa task.
- The IOP provide a path for transferring of data between various peripheral devices and the program.
- The communication between the IOP and the device attached to its similar to the program control method of transfer.

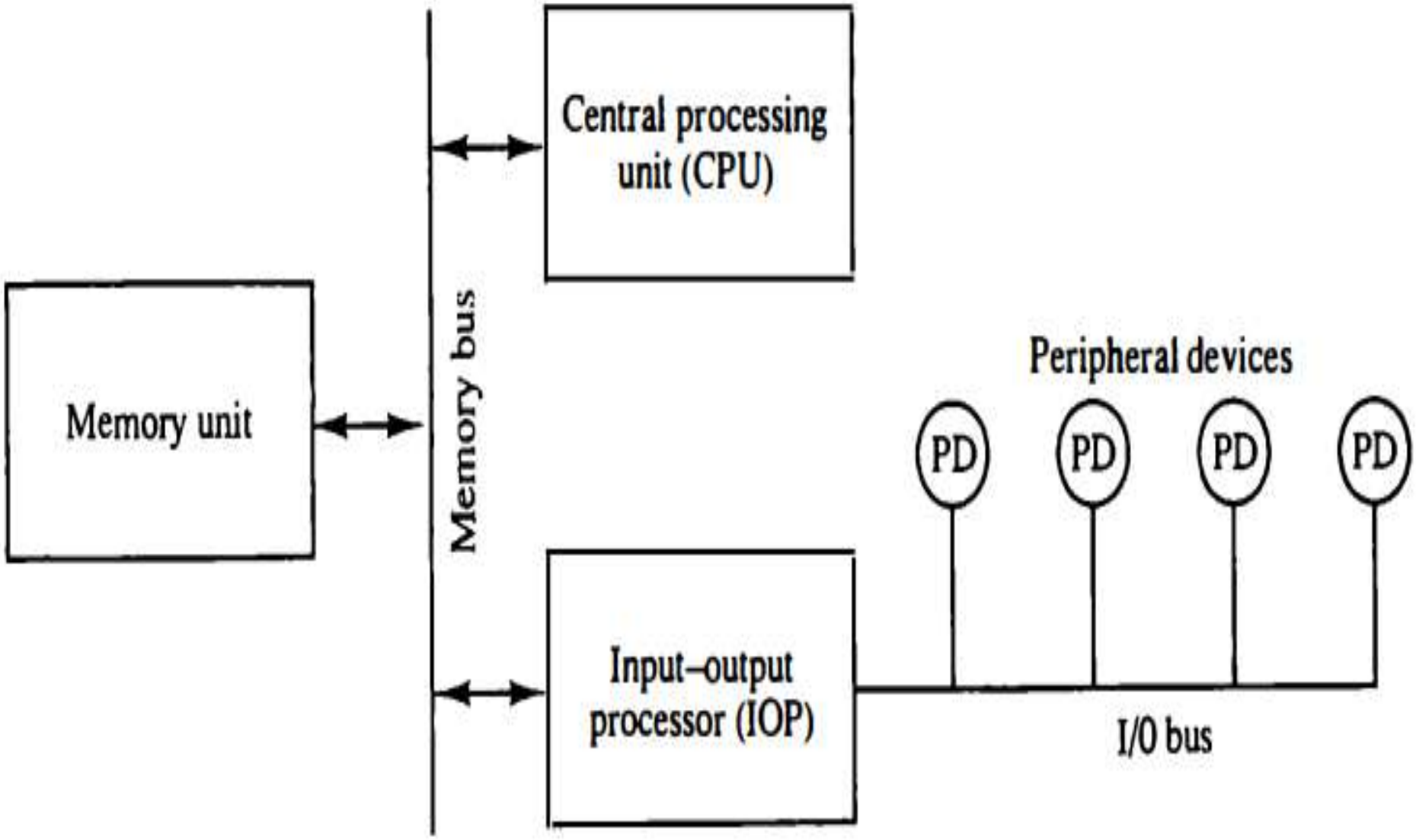


Figure 19 Block diagram of a computer with I/O processor.

CPU- IOP COMMUNICATION

- The communication between the CPU and the IOP may take in different forms.
- In most cases the memory unit act as a message center where each process leaves the information to other
- The IOP takes care of all the data transfer between several I//O unit and the memory while the cpu is processing the another program.

- The IOP and the processor compete for the use of memory..
- The IOP takes care of all data transfers between several I/O units and the memory while the CPU is processing another program.
- The IOP and CPU are competing for the use of memory, so the number of devices that can be in operation is limited by the access time of the memory.

Figure 20 CPU-IOP communication.