

**AN-FT8006S-AA**

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Release date	2019/06/21
Owner	Alan Lin

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# APPLICATION NOTE

**FocalTech**

## **FT8006S-AA**

### **Application Note for Instruction**

**Preliminary**

JUN. 21, 2019

Version 0.1

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## 1. PIN DESCRIPTIONS

### 1.1. Pin Definition

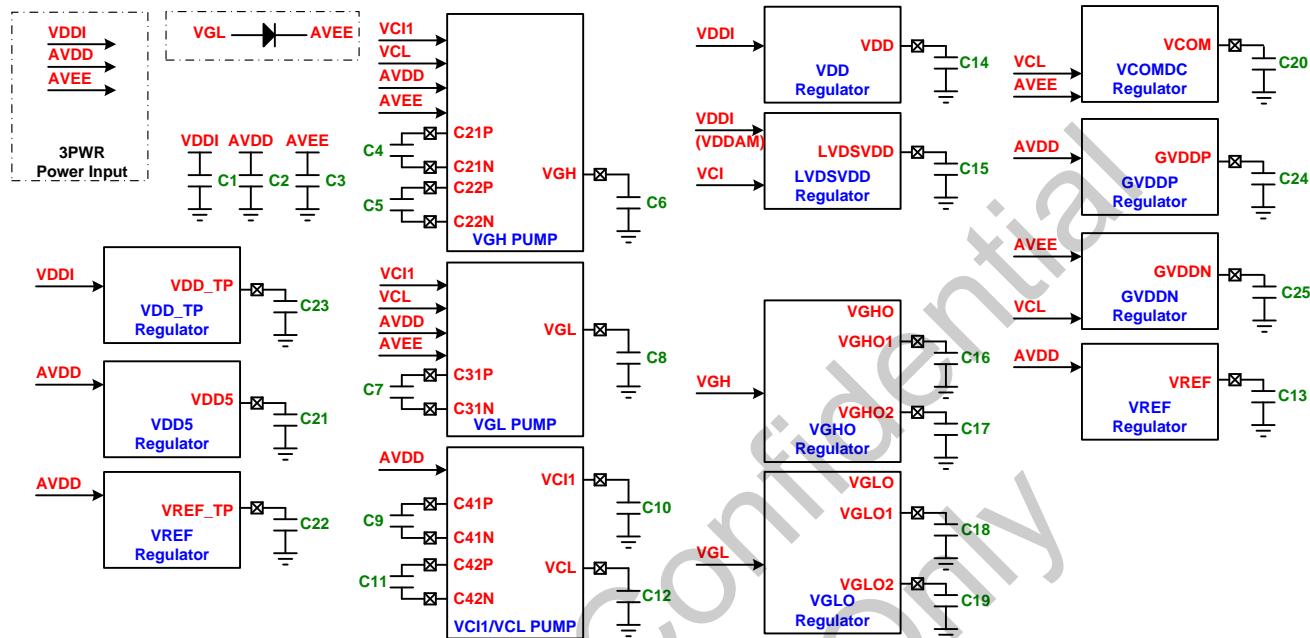
Signal	I/O	PAD Type (Voltage Level)	Function
<b>Power Supply Pad</b>			
AVDD	P	Analog Power	4.5V~6.5V. Connect a capacitor for stabilization
AVEE	P	Analog Power	-4.5V~-6.5V. Connect a capacitor for stabilization
VDDI	P	Digital Power	Power Supply for IO, 1.65V~1.95V.
VDDAM	P	Digital Power	Power Supply for MIPI LDO, 1.65V~1.95V
VDDI_TP	P	Digital Power	Power Supply for VDD_TP Regulator and TP Communication IO. 1.65V~1.95V.
AVSS	P	Analog Ground	Ground for source, AFE and <b>Analog circuit</b> .
VSS	P	Digital Ground	Ground for Digital Circuits
LVDSVSS	P	Digital Ground	Ground for <b>MIPI</b> Circuits
VSSR	P	Analog Ground	Ground for Reference & Regulator Blocks
OTP_PWR	P	I/O Power	Used for external power input for OTP program
<b>DC-DC Convereter Pad</b>			
VGH	O	Internal Power	Positive Charge Pump Power. Connect a capacitor for stabilization.
VGL	O	Internal Power	Negative Charge Pump Power. Connect a capacitor for stabilization.
VCI1	O	Internal Power	Positive Charge Pump Power. Connect a capacitor for stabilization.
VCL	O	Internal Power	Negative Charge Pump Power. Connect a capacitor for stabilization.
C21P/C21N C22P/C22N	O	Step-up capacitor	Flying cap for VGH Charge Pump. Connected to a capacitor as requirement.
C31P/C31N	O	Step-up capacitor	Flying cap for VGL Charge Pump. Connected to a capacitor as requirement.
C41P/C41N	O	Step-up capacitor	Flying cap for VCI1 Charge Pump. Connected to a capacitor as requirement.
C42P/C42N	O	Step-up capacitor	Flying cap for VCL Charge Pump. Connected to a capacitor as requirement.
<b>Regulator Pad</b>			
VGHO	O	Internal Power	Switch output voltage generated from VGHO1/VGHO2 <b>FPC Connect together</b>
VGHO1	O	Internal Power	Regulator output voltage generated from VGH. Connect a capacitor for stabilization.
VGHO2	O	Internal Power	Regulator output voltage generated from VGH. Connect a capacitor for stabilization.

Signal	I/O	PAD Type (Voltage Level)	Function																																																																																																						
VGLO	O	Internal Power	Switch output voltage generated from VGLO1/VGLO2 <b>FPC Connect together</b>																																																																																																						
VGLO1	O	Internal Power	Regulator output voltage generated from VGL. Connect a capacitor for stabilization.																																																																																																						
VGLO2	O	Internal Power	Regulator output voltage generated from VGL. Connect a capacitor for stabilization.																																																																																																						
VDD	O	Internal Power	Regulator output voltage, <b>FPC Connect together</b> Connect a capacitor for stabilization.																																																																																																						
LVDSVDD	O	Internal Power	Regulator output voltage generate, <b>FPC Connect together</b> Connect a capacitor for stabilization.																																																																																																						
VDD_TP	O	Internal Power	Regulator output voltage. <b>FPC Connect together</b> Connect a capacitor for stabilization.																																																																																																						
VREF	O	Internal Power	Regulator output voltage. Connect a capacitor for stabilization. [Optional Capacitor for stabilization]																																																																																																						
VREF_TP	O	Internal Power	Regulator output voltage. <b>FPC Connect together.</b> Connect a capacitor for stabilization.																																																																																																						
VDD5	O	Internal Power	Regulator output voltage. <b>FPC Connect together.</b> Connect a capacitor for stabilization.																																																																																																						
VCOM	O	Internal Power	Regulator output voltage. <b>FPC Connect together.</b> Connect a capacitor for stabilization. <b>Capacitor must be in the middle of FPC.</b>																																																																																																						
VCOM_OPT	O	Internal Power	VCOM Optional Buffer Output.																																																																																																						
VCOMPASS_L VCOMPASS_R	--	--	Pass line for VCOM from ILB to OLB																																																																																																						
GVDD	O	Internal Power	Regulator output voltage (for positive gamma high voltage generator).																																																																																																						
NGVDD	O	Internal Power	Regulator output voltage (for negative gamma high voltage generator).																																																																																																						
<b>LCD Interface Logic Pad</b>																																																																																																									
RESX	I	Digital (VDDI)	Global Reset Signal. Active Low. <b>IC Internal pull High</b>																																																																																																						
PSWAP DSWAP[1:0]	I	Digital (VDDI)	MIPI Lane Swap & Polarity control . MIPI Data Lane swap and polarity swap table <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>PSWAP</th> <th>DSWAP[1:0]</th> <th>DSI-D2+</th> <th>DSI-D2-</th> <th>DSI-D1+</th> <th>DSI-D1-</th> <th>DSI-CLK+</th> <th>DSI-CLK-</th> <th>DSI-D0+</th> <th>DSI-D0-</th> <th>DSI-D3+</th> <th>DSI-D3-</th> </tr> </thead> <tbody> <tr> <td rowspan="4">0</td> <td>00</td> <td>D3-</td> <td>D3+</td> <td>D2-</td> <td>D2+</td> <td>CLK-</td> <td>CLK+</td> <td>D1-</td> <td>D1+</td> <td>D0-</td> <td>D0+</td> </tr> <tr> <td>01</td> <td>D3-</td> <td>D3+</td> <td>D0-</td> <td>D0+</td> <td>CLK-</td> <td>CLK+</td> <td>D1-</td> <td>D1+</td> <td>D2-</td> <td>D2+</td> </tr> <tr> <td>10</td> <td>D0-</td> <td>D0+</td> <td>D1-</td> <td>D1+</td> <td>CLK-</td> <td>CLK+</td> <td>D2-</td> <td>D2+</td> <td>D3-</td> <td>D3+</td> </tr> <tr> <td>11</td> <td>D2-</td> <td>D2+</td> <td>D1-</td> <td>D1+</td> <td>CLK-</td> <td>CLK+</td> <td>D0-</td> <td>D0+</td> <td>D3-</td> <td>D3+</td> </tr> <tr> <td rowspan="4">1</td> <td>00</td> <td>D3+</td> <td>D3-</td> <td>D2+</td> <td>D2-</td> <td>CLK+</td> <td>CLK-</td> <td>D1+</td> <td>D1-</td> <td>D0+</td> <td>D0-</td> </tr> <tr> <td>01</td> <td>D3+</td> <td>D3-</td> <td>D0+</td> <td>D0-</td> <td>CLK+</td> <td>CLK-</td> <td>D1+</td> <td>D1-</td> <td>D2+</td> <td>D2-</td> </tr> <tr> <td>10</td> <td>D0+</td> <td>D0-</td> <td>D1+</td> <td>D1-</td> <td>CLK+</td> <td>CLK-</td> <td>D2+</td> <td>D2-</td> <td>D3+</td> <td>D3-</td> </tr> <tr> <td>11</td> <td>D2+</td> <td>D2-</td> <td>D1+</td> <td>D1-</td> <td>CLK+</td> <td>CLK-</td> <td>D0+</td> <td>D0-</td> <td>D3+</td> <td>D3-</td> </tr> </tbody> </table> <b>IC Internal pull high</b>	PSWAP	DSWAP[1:0]	DSI-D2+	DSI-D2-	DSI-D1+	DSI-D1-	DSI-CLK+	DSI-CLK-	DSI-D0+	DSI-D0-	DSI-D3+	DSI-D3-	0	00	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+	01	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+	10	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+	11	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+	1	00	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-	01	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-	10	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-	11	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-
PSWAP	DSWAP[1:0]	DSI-D2+	DSI-D2-	DSI-D1+	DSI-D1-	DSI-CLK+	DSI-CLK-	DSI-D0+	DSI-D0-	DSI-D3+	DSI-D3-																																																																																														
0	00	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+																																																																																														
	01	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+																																																																																														
	10	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+																																																																																														
	11	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+																																																																																														
1	00	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-																																																																																														
	01	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-																																																																																														
	10	D0+	D0-	D1+	D1-	CLK+	CLK-	D2+	D2-	D3+	D3-																																																																																														
	11	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-																																																																																														

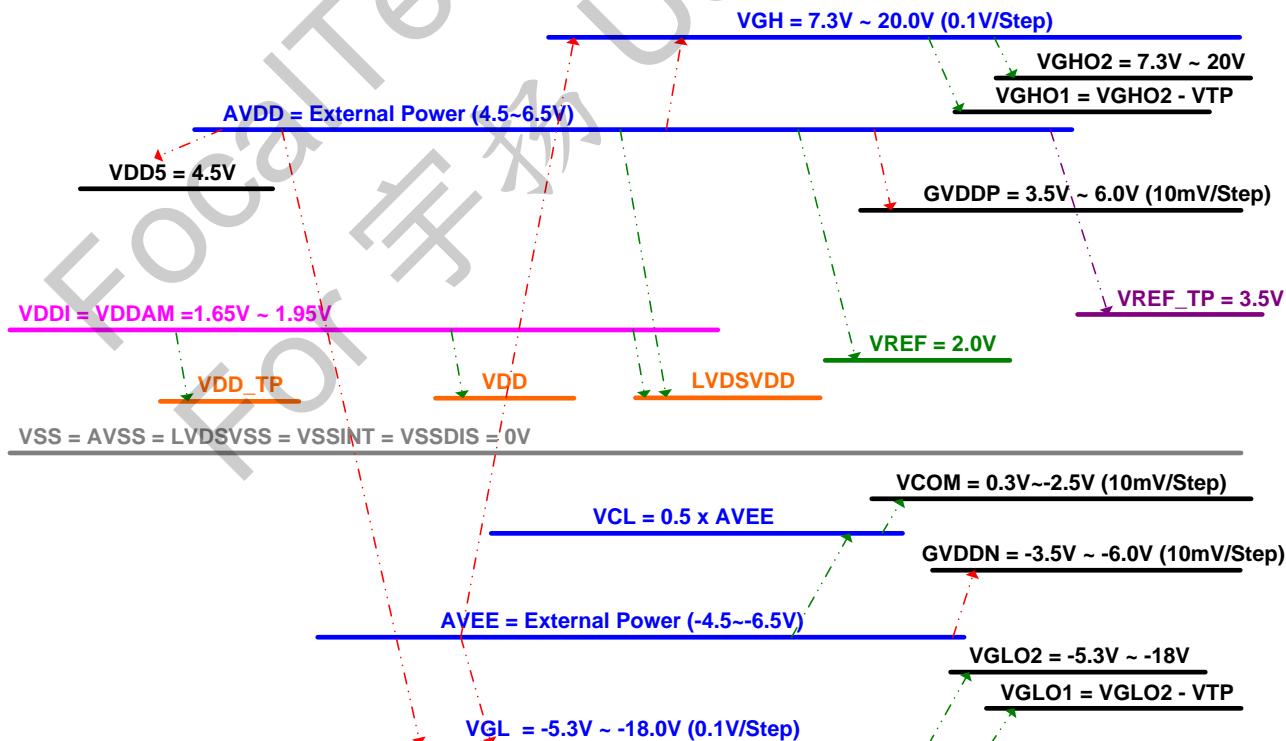
Signal	I/O	PAD Type (Voltage Level)	Function										
LANSEL[1:0]	I	Digital (VDDI)	<p>Interface Selection</p> <table border="1"> <thead> <tr> <th>LANSEL[1:0]</th><th>Interface Selection</th></tr> </thead> <tbody> <tr> <td>00</td><td>Reserved</td></tr> <tr> <td>01</td><td>MIPI-2 Lane</td></tr> <tr> <td>10</td><td>MIPI-3 Lane</td></tr> <tr> <td>11</td><td>MIPI-4 Lane</td></tr> </tbody> </table> <p><b>IC Internal pull high</b></p>	LANSEL[1:0]	Interface Selection	00	Reserved	01	MIPI-2 Lane	10	MIPI-3 Lane	11	MIPI-4 Lane
LANSEL[1:0]	Interface Selection												
00	Reserved												
01	MIPI-2 Lane												
10	MIPI-3 Lane												
11	MIPI-4 Lane												
BIST_EN	I	Digital (VDDI)	<p>BIST mode enable, High Active</p> <p><b>IC Internal pull Low</b></p>										
LCD_GPIO[7:0]	I/O	Digital (VDDI)	<p>LCD_GPIO can be set as TP_SYNC, LEDPWM,...etc</p> <p><b>IC Internal pull Low</b></p>										
<b>MIPI-DSI Interface input Signals</b>													
HISI_CLK_P/N	I	MIPI (LVDSVDD)	<p>MIPI-DSI CLOCK differential signal input pins.</p> <p>If not used, Please connect to LVDSVSS.</p>										
HISI_D0_P/N	I/O	MIPI (LVDSVDD)	<p>MIPI-DSI Data differential signal input pins. (Data lane 0)</p> <p>if not used , Please connect to LVDSVSS.</p>										
HISI_D1_P/N	I/O	MIPI (LVDSVDD)	<p>MIPI-DSI Data differential signal input pins. (Data lane 1)</p> <p>if not used , Please connect to LVDSVSS.</p>										
HISI_D2_P/N	I/O	MIPI (LVDSVDD)	<p>MIPI-DSI Data differential signal input pins. (Data lane 2)</p> <p>if not used , Please connect to LVDSVSS.</p>										
HISI_D3_P/N	I/O	MIPI (LVDSVDD)	<p>MIPI-DSI Data differential signal input pins. (Data lane 3)</p> <p>if not used , Please connect to LVDSVSS.</p>										
<b>TP Interface Logic Pad</b>													
BOOT_DEVICE	I	Digital (VDDI_TP)	<p>Interface select . <b>IC Internal pull Low</b>.</p> <p>0: I2C (boot with flash) ; 1: SPI (boot without flash)</p>										
TP_GPIO[4:0]	I/O	Digital (VDDI_TP)	<p>GPIO[0]: I2C_SCL / SPI_SCL clock pin</p> <p>GPIO[1]: I2C_SDA / SPI_MOSI pin</p> <p>GPIO[2]: SPI_MISO pin</p> <p>GPIO[3]: SPI_SS (Chip Select) pin</p> <p>GPIO[4]: INT/Wake pin</p> <p><b>GPIO[4:0] : IC Internal pull high.</b></p>										
CS	O	Digital (VDDI_TP)	SPI Chip select signal to Flash										
SCLK	O	Digital (VDDI_TP)	SPI serial clock to Flash, MAX = 6MHz										
MOSI	O	Digital (VDDI_TP)	SPI data output to Flash										
MISO	I	Digital (VDDI_TP)	SPI data input from Flash. <b>IC Internal pull low.</b>										
HOLD	O	Digital (VDDI_TP)	HOLD signal to Flash, active LOW										
WP	O	Digital (VDDI_TP)	write protect signal to Flash, active LOW										
<b>Test Pad</b>													
POR12_T	O	Digital (VDDI_TP)	POR PAD, for test only, leave it open.										
POR18_T	O	Digital (VDDI_TP)	POR PAD, for test only, leave it open.										
AFE_TEST[4:0]	O	Analog (AVDD)	Analog Test Pin, not accessible to user. Must be left open.										

Signal	I/O	PAD Type (Voltage Level)	Function
VGH1 VGH2	I	Power Input	This pin is used to discharge function. If not used, please let this pin short to VGOH.
DCHG1_L/ DCHG1_R	O	Analog output	For gate signal(Group1) slope control usage. If user wants to use, please connect a resister. If not used, please tie it to VSS or open.
DCHG2_L/ DCHG2_R	O	Analog output	For gate signal(Group2) slope control usage. If user wants to use, please connect a resister. If not used, please tie it to VSS or open.
LCD_EXT_OSC	I	Digital (VDDI)	LCD testmode, external clock input <b>IC Internal pull low</b>
LCD_TSPO[15:0]	O	Digital (VDDI)	LCD testmode output measurement for digital circuit
LCD_TSPI_DEN[19:0]	I	Digital (VDDI)	LCD testmode selection for digital circuit <b>IC Internal pull low.</b>
LCD_TSPI_AEN[3:0]	I	Digital (VDDI)	LCD testmode selection for analog circuit <b>IC Internal pull low.</b>
LCD_TEST[3:0]	O	Analog output	LCD testmode output measurement for analog circuit
SYNC_DAT_L[6:0] SYNC_DAT_R[6:0]	I	Digital (VDDI)	LCD testmode selection for digital circuit <b>IC Internal pull low.</b>
<b>Driving Pad</b>			
S[2160:1]	O	Analog (AVDD/AVEE)	Source Output
SDUM[3:0]	O	Analog (AVDD/AVEE)	Source Dummy Pin ( For ZigZag Panel)
SX[576:1]	O	Analog (AVDD)	Separate COM Electrode (TP Sensor Pins)
SXDUM1/ SXDUM2	O	Analog (AVDD)	TP Dummy Pin
GOUT_L[22:1] / GOUT_R[22:1]	O	Analog (VGH/VGL)	GOA Output. Please use GOUT[13:6] for CLK application.
<b>Cascade Pad</b>			
EXT_VCOM_EN	I	Digital (VDDI)	External VCOM Enable, "H"=Using external VCOM, 'L'=Using internal VCOM <b>IC Internal pull Low</b>

## 1.2. Power Block Diagram

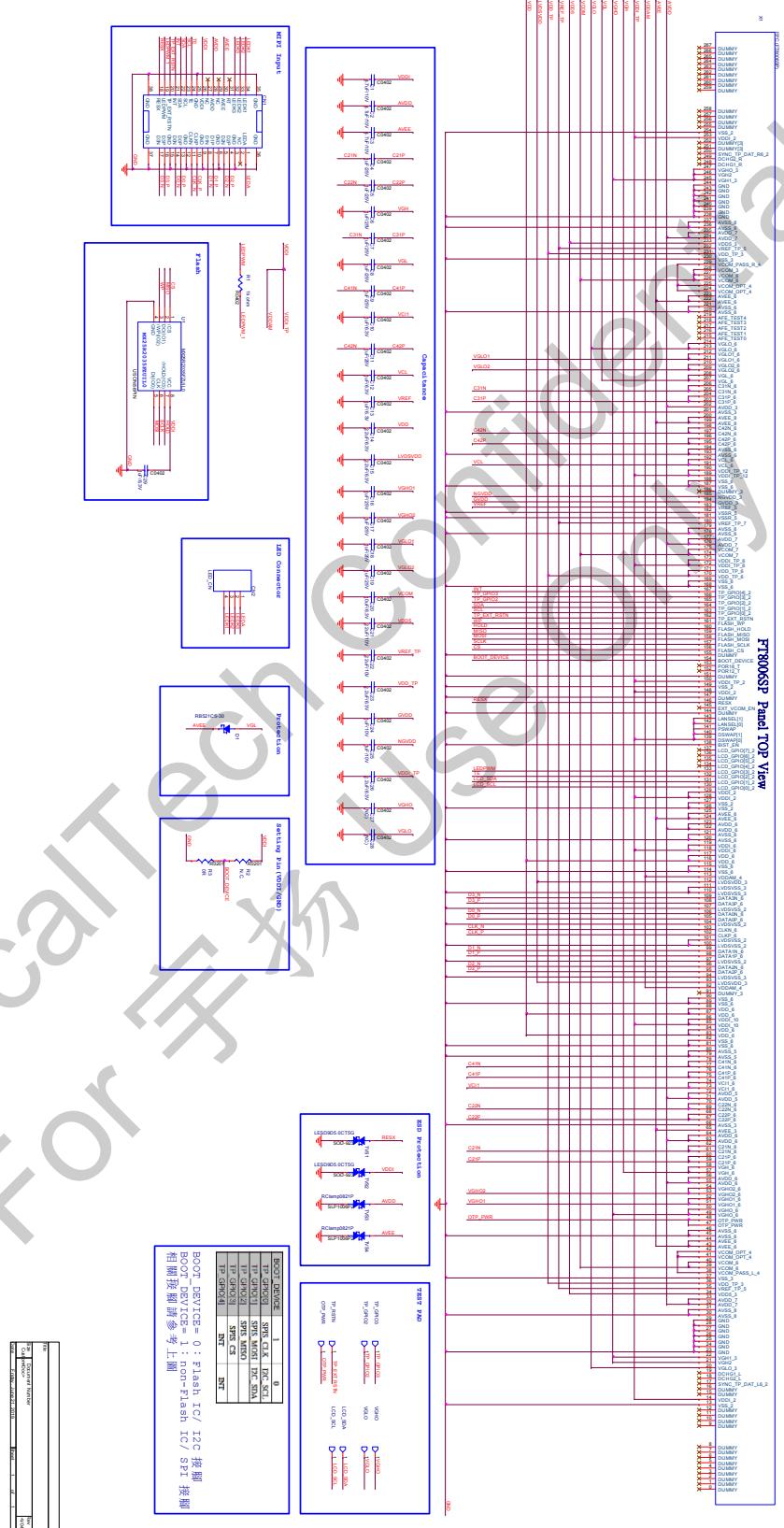


## 1.3. Power Supply Configuration



#### **1.4. Application Circuit**

Note: It's for design reference only! User should contact our sales or FAE for suitable circuit design in actual case.

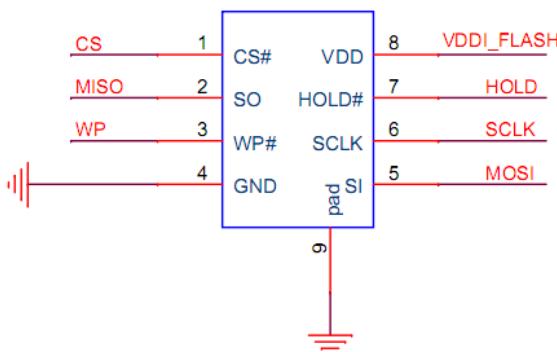


**1.5. BOM List**

NO.	Reference	Part	PCB Footprint	Quantity
1	C1,C2,C3	4.7uF/10V	C0402	3
2	C4,C5,C6,C7,C8,C9,C11,C16,C17,C18,C19	1uF/25V	C0402	11
3	C10,C12,C13,C29	1uF/6.3V	C0402	4
4	C14,C15,C23,C26	2.2uF/6.3V	C0402	4
5	C20	10uF/6.3V	C0402	1
6	C21,C22	2.2uF/10V	C0402	2
7	C24,C25	1uF/10V	C0402	2
8	D1	RB521CS-30	rb521CS-30	1
9	R3	0R	R0201	1
10	R1	1k ohm	R0402	1
11	TVS1,TVS2	LESD9D5.0CT5G	SOD-923	2
12	TVS3,TVS4	RClamp0821P	SLP1006P2	2
13	U1	MX25R2035FZUIL0	USON8-8PIN	1

## 1.6. Flash Select

- I. Flash Work Voltage : 1.8V~2.8V (FTXXXX VDDI\_Flash=1.8V)。
- II. Flash size : Greater than 512Bit(64KByte) ; Suggestion 1Mbit(128KBtje)。
- III. Flash Interface : Serial SPI , Support SPI Frequency: 3M/6M , Support SPI Phase :00 mode。
- IV. Flash Pin Description :



- V. Flash need Compatible Command:

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Write Enable	06h					
Write Enable for Volatile Status Register	50h					
Write Disable	04h					
Read Status Register-1	05h	(S7-S0) <sup>(2)</sup>				
Read Status Register-2	35h	(S15-S8) <sup>(2)</sup>				
Write Status Register	01h	S7-S0	S15-S8			
Page Program	02h	A23-A16	A15-A8	A7-A0	D7-D0	
Quad Page Program	32h	A23-A16	A15-A8	A7-A0	D7-D0, ... <sup>(3)</sup>	
Sector Erase (4KB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32KB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64KB)	D8h	A23-A16	A15-A8	A7-A0		
Chip Erase	C7h/60h					
Erase / Program Suspend	75h					
Erase / Program Resume	7Ah					
Power-down	B9h					
Continuous Read Mode Reset <sup>(4)</sup>	FFh	FFh				

INSTRUCTION NAME	BYTE 1 (CODE)	BYTE 2	BYTE 3	BYTE 4	BYTE 5	BYTE 6
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) <sup>(1)</sup>
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0, ...) <sup>(3)</sup>
Fast Read Dual I/O	BBh	A23-A8 <sup>(2)</sup>	A7-A0, M7-M0 <sup>(2)</sup>	(D7-D0, ...) <sup>(1)</sup>		
Fast Read Quad I/O	EBh	A23-A0, M7-M0 <sup>(4)</sup>	(x,x,x,x, D7-D0,...) <sup>(5)</sup>	(D7-D0, ...) <sup>(3)</sup>		
Word Read Quad I/O <sup>(7)</sup>	E7h	A23-A0, M7-M0 <sup>(4)</sup>	(x,x, D7-D0, ...) <sup>(6)</sup>	(D7-D0, ...) <sup>(3)</sup>		
Octal Word Read Quad I/O <sup>(8)</sup>	E3h	A23-A0, M7-M0 <sup>(4)</sup>	(D7-D0, ...) <sup>(3)</sup>			
Set Burst with Wrap	77h	xxxxxx, W6-W4 <sup>(4)</sup>				

#### VI. Flash Page Program

The Page Program instruction need allows from one byte to 256 bytes (a page) of data to be programmed at previously erased (FFh) memory locations, not recommend to choose the Flash only support 32 Byte.

The Page Program (PP) instruction is for programming the memory to be “0”. A Write Enable (WREN) instruction must execute to set the Write Enable Latch (WEL) bit before sending the Page Program (PP). After the instruction and address input, data to be programmed is input sequentially. The internal sequence controller will sequentially program the data from the initial address. If the transmitted data goes beyond the page boundary, the internal sequence controller may not function properly and the content of the device will not be guaranteed. Therefore, if the initial A4-A0 (The five least significant address bits) are set to all 0, maximum 32 bytes of data can be input sequentially. If the initial address A4-A0 (The five least significant address bits) are not set to all 0, maximum bytes of data input will be the subtraction of the initial address A4-A0 from 32bytes. The data exceeding 32bytes data is not sent to device. In this case, data is not guaranteed.

#### VII. Currently Focal has been tested Flash type:

Winbond : W25Q20BW

## 2.INSTRUCTIONS

### 2.1. Outline

FT8006S-AA supports high speed serial interface, MIPI, to configure system via accessing command register. When the command register is executed, sending the command information to specify which index register would be accessed and following the data to that control register. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.2 and D-PHY Version 1.1.

FT8006S-AA has the following major categories of instructions:

- (1). System function instructions (User Command Set).
- (2). Customer Command List and Description (Manufacturer Command Set / Command 2).

These instructions are asynchronous to the FT8006S-AA internal clock, requiring no wait cycles. Because the writing of instruction data does not interfere with the host controller processing, instructions can be handled smoothly and efficiently. The following describes details of instruction settings.

#### 2.1.1 System function command list and description

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register becomes default state (Refer “RESET TABLE” section). Commands 28h and 29h are updated during V-Blanking to avoid abnormal visual effects. By the way, all commands in master and slave side can be updated concurrently during V-Blanking via MIPI DSI v1.2 FSC function.

System function command access flow is described as following example.

##### Example 1: Sleep Out

Address 0x11

##### Example 2: Display On

Address 0x29

##### Example 3: BIST Mode

Address 0x02

DATWR 0x5A

**2.2. System function Command-1 Description**

Command	BankSel [5:0]	(Hex)	Write/Read /Command	Function	Parameter Number	MIPI Transmission
SWRESET	-	01h	C	Software reset	0	LPDT/HSDT
BIST_MODE	-	02h	W/R	Enter BIST Mode	1	LPDT/HSDT
RDDPM	-	0Ah	R	Read Display Power Mode	1	LPDT/HSDT
SLPIN	-	10h	C	Sleep-In	0	LPDT/HSDT
SLPOUT	-	11h	C	Sleep-Out	0	LPDT/HSDT
DEEP_STBY	-	17h	W/R	Enter Deep Standby Mode	1	LPDT/HSDT
BYPASS_MODE	-	19h	W/R	BYPASS mode enable	1	LPDT/HSDT
TERMR_EN	-	1Eh	W/R	MIPI TermR Enable	1	LPDT/HSDT
DISP_OFF	-	28h	C	Display off	0	LPDT/HSDT
DISP_ON	-	29h	C	Display on	0	LPDT/HSDT
OTP_STOP_RELOAD_MIPI	-	41h	W/R	OTP Stop Reload MIPI Enable	1	LPDT/HSDT
EXT_ADR	-	42h	W/R	Extended Address of Command Interface	1	LPDT/HSDT
Internal Used	-	47h	-	Internal Used	-	-
OTP_CTRL_STATUS	-	48h	W/R	OTP Control & Status	1	LPDT/HSDT
Internal Used	-	49h	-	Internal Used	-	-
FSC_CTRL	-	4Ah	W	MIPI FSC Function Control	1	LPDT/HSDT
Internal Used	-	4Ch	-	Internal Used	-	-
Internal Used	-	4Dh	-	Internal Used	-	-
OTP_STOP_RELOAD MCU	-	4Eh	W/R	OTP Stop Reload MCU Enable	1	LPDT/HSDT
DISBV_SET	-	51h	W	Display Brightness Value Setting	1	LPDT/HSDT
DISBV_RD	-	52h	W/R	Read Display Brightness Value	1	LPDT/HSDT
DISBV_CTRL	-	53h	W/R	Display Brightness Value Control	1	LPDT/HSDT
RDDISBV_CTRL	-	54h	R	Read Display Brightness Value Control	1	LPDT/HSDT
WRFCC_CABC	-	55h	W	Write Content Adaptive Brightness Control	1	LPDT/HSDT
RDFCC_CABC	-	56h	R	Read Content Adaptive Brightness Control	1	LPDT/HSDT
OTP_PROG	-	58h	W/R	OTP Program	1	LPDT/HSDT
Internal Used	-	5Bh	-	Internal Used	-	-
WRCABC_MDISBV	-	5Eh	W	Write CABC Minimum Brightness	1	LPDT/HSDT
RDCABC_MDISBV	-	5Fh	W/R	Read CABC Minimum Brightness	1	LPDT/HSDT
Internal Used	-	69h	-	Internal Used	-	-
Internal Used	-	6Ch	-	Internal Used	-	-
Internal Used	-	6Dh	-	Internal Used	-	-
Internal Used	-	6Eh	-	Internal Used	-	-
Internal Used	2Fh	87h	-	Internal Used	-	-
Internal Used	2Fh	8Ah	-	Internal Used	-	-
FCC_CE	2Fh	90h	W/R	Focal CleverColor – Color Enhancement	1	LPDT/HSDT
FCC_SHARPN	2Fh	92h	W/R	Focal CleverColor – Sharpness	1	LPDT/HSDT
FCC_CNTRST	2Fh	94h	W/R	Focal CleverColor – Contrast Enhancement	1	LPDT/HSDT
FCC_AIE	2Fh	97h	W/R	Focal CleverColor – AIE	1	LPDT/HSDT

Command	BankSel [5:0]	(Hex)	Write/Read /Command	Function	Parameter Number	MIPI Transmission
FCC_WA	2Fh	98h	W/R	Focal CleverColor – White Balance Adjustment	1	LPDT/HSDT
RDDDBS	2Fh	A1h	R	Read DDB Start	13 *Note2	LPDT/HSDT
RDDDBC	2Fh	A8h	R	Read DDB Continuous	*Note2	LPDT/HSDT
Internal Used	2Fh	B0h	-	Internal Used	-	-
Internal Used	2Fh	B1h	-	Internal Used	-	-
Internal Used	2Fh	B2h	-	Internal Used	-	-
Internal Used	2Fh	B3h	-	Internal Used	-	-
Internal Used	2Fh	B4h	-	Internal Used	-	-
Internal Used	2Fh	B5h	-	Internal Used	-	-
Internal Used	2Fh	B6h	-	Internal Used	-	-
RDID_DA	2Fh	DAh	R	Read ID_DA in OTP	1	LPDT/HSDT
RDID_DB	2Fh	DBh	R	Read ID_DB in OTP	1	LPDT/HSDT
RDID_DC	2Fh	DCh	R	Read ID_DC in OTP	1	LPDT/HSDT

Note: LPDT (Low Power Mode), HSDT (High Speed Mode)

Note 2: The maximum number for the sum of RDDDBS's and RDDDBC's parameter length is 5. For example, RDDDBS's parameter length is 2, and RDDDBC's parameter length is 3.

## 2.2.1. SWRESET (01h): Software Reset

Bank -									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
01H (SWRST)	No Parameter								

Description
SWRST : Software Reset
Address = '01H'
- When the Software Reset command is written, it causes a software reset to display only.
- It resets the commands and parameters to their reset default values and all source & gate outputs are set to VSS (display off).
(See default tables in each command description)
Restriction :
- It will be necessary to wait 100msec before sending new command following software reset.
- The display module loads all display supplier's factory default values to the registers during 100msec.
- Software Reset command cannot be work during Deep Standby State.

**2.2.2. BIST\_MODE (02H): Enter BIST mode**

Parameter Address	Bank-									Default
	D7	D6	D5	D4	D3	D2	D1	D0		
02H	reg_bist_en[7:0]									A5h

Description
reg_bist_en[7:0] :
- This command is used to set BIST Mode function
'5Ah' = Enter BIST Mode.
'Others' = Exit BIST Mode.
Restriction :
- Both register software setting and I/O hardware pin can enter BIST Mode function. (Control ORed)

**2.2.3. RDDPM (0AH): Read Display Power Mode**

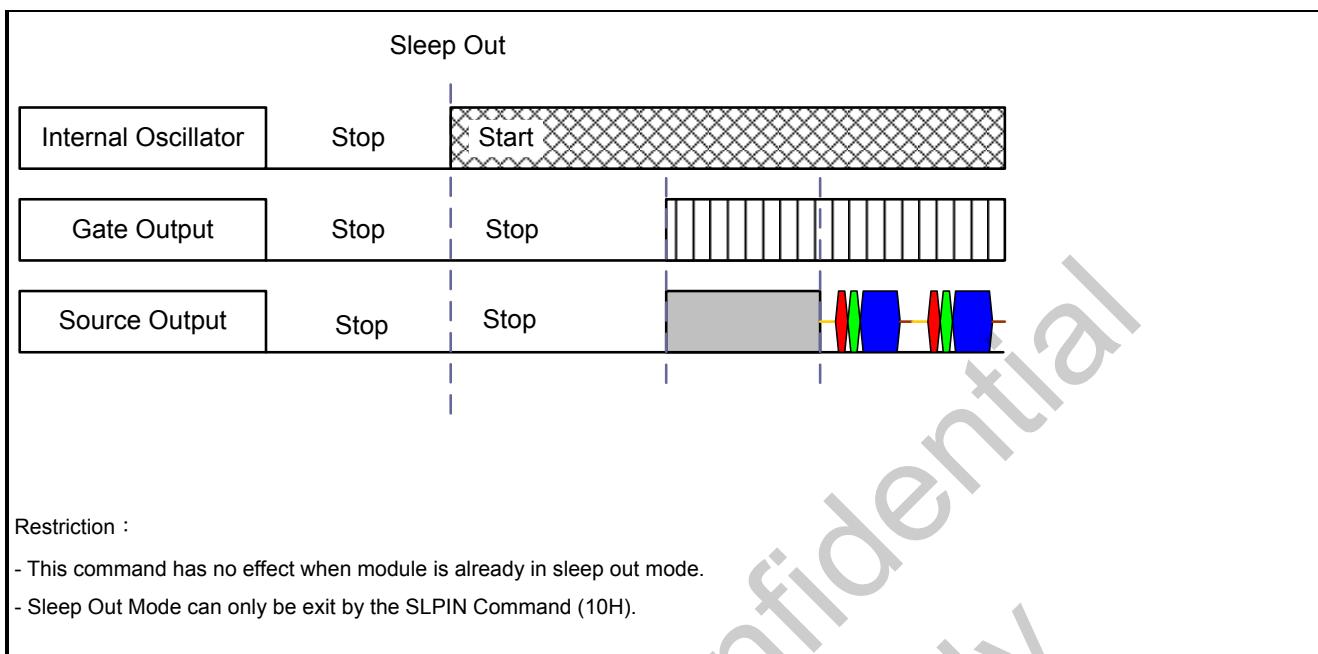
Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
0AH	BSTON	0	0	SLPOUT	1	DISON	0	0	08h

Description		
This command indicates the current status of the display as described in the table below:		
Bit	Description	Value
BSTON	Booster Voltage Status	“1”=Booster On “0”=Booster Off
D6	Not Used	0
D5	Not Used	0
SLPOUT	Sleep In/Out	“1” = Sleep Out, “0” = Sleep In
D3	Not Used	1
DISON	Display On/Off	“1” = Display On, “0” = Display Off
D1	Not Used	0
D0	Not Used	0

#### 2.2.4. SLPIN (10H) & SLPOUT (11H) : Sleep-In & Sleep-Out

Parameter Address	Bank-								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
10H (SLPIN)	No Parameter								-
11H (SLPOUT)	No Parameter								-

Description									
SLPIN : Sleep-In (Enter Standby Mode)									
Address = '10H'									
<ul style="list-style-type: none"> <li>- This command causes the LCD module to enter the power consumption reduced mode.</li> <li>- In this mode, internal display oscillator is stopped, and panel scanning is stopped.</li> <li>- Only the command path are still working to support the exit from Standby Mode.</li> </ul>									
<p style="text-align: center;">Sleep In</p>									
Restriction :									
<ul style="list-style-type: none"> <li>- This command has no effect when module is already in sleep in mode. Standby Mode can only be exit by the SLPOUT Command (11H).</li> </ul>									
SLPOUT : Sleep-Out (Exit Standby Mode)									
Address = '11H'									
<ul style="list-style-type: none"> <li>- This command causes the LCD module to exit the power consumption reduced mode.</li> <li>- In this mode, internal display oscillator is started, and panel scanning is started.</li> </ul>									



**2.2.5. DEEP\_STBY (17H/18H) : Enter Deep Standby Mode**

Parameter Address	Bank-								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
17H	DEEP_STBY0[7:0]								00h
18H	DEEP_STBY1[7:0]								00h

Description
- These two command are used to set Deep Standby Mode function.
- There are 2 methods that can enter Deep Standby State :
Method 1 : Set DEEP_STBY0[7:0] = 5Ah and DEEP_STBY1[7:0] = 5Ah in any state.
Method 2 : Set DEEP_STBY0[7:0] = A5h and DEEP_STBY1[7:0] = A5h when Sleep In Mode.
Restriction :
- Only Hardware Reset can exit Deep Standby Mode, and it will be necessary to wait 100msec before sending new command following hardware reset.
- The display module loads all display supplier's factory default values to the registers during 100msec.

**2.2.6. BYPASS\_MODE (19H): BYPASS mode enable**

Parameter Address	Bank-								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
19H					Reserved			BYPASS_M ODE_EN	00h

Description
BYPASS_MODE_EN :
- This command is used to set BYPASS Mode function that supports TP 60Hz sensing rate. If this function is disable (default), TP will work in 120Hz sensing rate.
'1' = BYPASS Mode enable. '0' = BYPASS Mode disable.(Default)

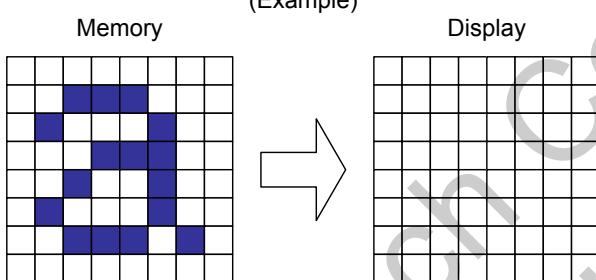
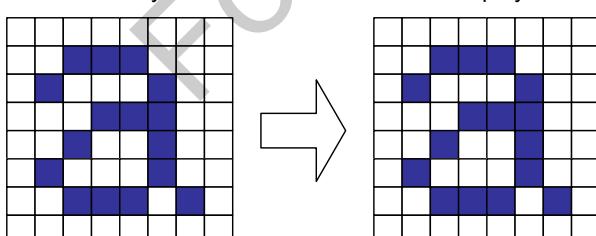
**2.2.7. TERMR\_EN (1EH): MIPI TermR Enable**

Parameter Address	Bank-								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
1EH	TERMR_EN								FFh

Description
TERMR_EN : MIPI TermR Enable
- This command is used to set MIPI TermR enable, disable or normal operation.
'5Ah' = Force to enable MIPI TermR
'A5h' = Force to disable MIPI TermR
'Others' = Normal operation that depends on MIPI High Speed Mode

## 2.2.8. DISPLAY\_CTRL (28H~29H) : Display Control

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
28H (DISPOFF)									No Parameter
29H (DISPON)									No Parameter

Description	
DISPOFF : Display Off	
Address = '28H'	
<ul style="list-style-type: none"> <li>- This command is used to enter into DISPLAY OFF mode. In this mode, the output from the Memory is disabled and blank page is inserted.</li> <li>- This command does not change any other status.</li> <li>- There will be no abnormal visible effect on the display.</li> <li>- Exit from this command by Display On (29H)</li> </ul>	
<p style="text-align: center;">(Example)</p> 	
Restriction :	
<ul style="list-style-type: none"> <li>-This command has no effect when module is already in Display Off mode.</li> </ul>	
DISPON : Display On	
Address = '29H'	
<ul style="list-style-type: none"> <li>- This command is used to recover from DISPLAY OFF mode. Output from the Memory is enabled.</li> <li>- This command does not change any other status.</li> </ul>	
<p style="text-align: center;">(Example)</p> 	
Restriction :	
<ul style="list-style-type: none"> <li>- This command has no effect when module is already in Display On mode.</li> </ul>	

**2.2.9. OTP\_STOP\_RELOAD (41H/4EH): OTP Stop Reload Enable**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
41H	OTP_STOP_RELOAD_MIPI[7:0]								00h
4EH	OTP_STOP_RELOAD MCU[7:0]								00h

Description
OTP_STOP_RELOAD_MIPI : OTP Stop Reload Enable for MIPI used.
- This command is used to enable OTP stop reload function
'5Ah' : Stop OTP reload and switch bus to external interface.
'Others' : Enable OTP reload and switch bus to reload controller.
OTP_STOP_RELOAD MCU : OTP Stop Reload Enable for MCU used.
- This command is used to enable OTP stop reload function
'5Ah' : Stop OTP reload and switch bus to external interface.
'Others' : Enable OTP reload and switch bus to reload controller.

**2.2.10. EXT\_ADR (42H): Extended Address of Command Interface**

Parameter Address	Bank-								Default
	D7	D6	D5	D4	D3	D2	D1	D0	
42H	0	0			Bank_Sel[5:0]				2Fh

**Description**

Bank\_Sel[5:0] : Bank Selection of following command groups for I2C, MIPI and SYSTEM interface.

- This command is used to set extended address of I2C, MIPI and SYSTEM interface.

Description	
Bank_Sel[5:0] : Bank Selection of following command groups for I2C, MIPI and SYSTEM interface.	- This command is used to set extended address of I2C, MIPI and SYSTEM interface.

**2.2.11. OTP\_CTRL\_STATUS (48H): OTP Control & Status**

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
48H	Reserved	OTP_LOAD_FINISH	OTP_RELO_FINISH	SPI_LOAD_FINISH	Reserved	OTP_OP_MODE[2:0]			00h

Description
OTP_LOAD_FINISH (Read-Only) : OTP Initial Load Finish Flag '1' = OTP initial load finish
OTP_RELOAD_FINISH (Read-Only) : OTP Reload Finish Flag '1' = OTP reload finish
SPI_LOAD_FINISH (Read-Only) : SPI Flash Load Finish Flag '1' = SPI flash load finish
OTP_OP_MODE : OTP Operation Mode '000' = Normal Mode '001' = Room Temp. Initial Margin Read '010' = Program Mode '011' = High Temp. Initial Margin Read '100' = Room Temp. PGM Margin Read '110' = High Temp. PGM Margin Read

**2.2.12. FSC\_CTRL (4AH~4BH) : MIPI FSC Function Control**

Parameter Address	Bank-									Default
	D7	D6	D5	D4	D3	D2	D1	D0		
4AH	FSC_IN_EN[7:0]									00h
4BH	FSC_STOP_LOAD[7:0]									00h

Description
FSC_IN_EN : MIPI FSC Input Duration Enable - This command is used to enable MIPI FSC input duration. - When this function is enable, the following MIPI commands will be placed in internal FIFO queue until receiving an Execute Queue Command. '5Ah' = Enable MIPI FSC input duration. 'Others' = Disable MIPI FSC input duration.
FSC_STOP_LOAD : Stop load MIPI FSC from FIFO - This command is used to stop load MIPI FSC from internal FIFO queue. '5Ah' = Stop load MIPI FSC from FIFO. 'Others' = Normal operation that follow MIPI DSI v1.2 FSC definition.

## 2.2.13. DISBV\_SET (51H/52H): Display Brightness Value Setting

Parameter Address	Bank-									Default
	D7	D6	D5	D4	D3	D2	D1	D0		
51H	DBV[11:4]									FFh
52H	Reserved					DBV[3:0]			FFh	

Description
- This command is used to adjust the brightness value of the display.
- It should be checked what is the relationship between this written value and output brightness of the display.
This relationship is defined on the display module specification.
- In principle relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.
Note: Focal CleverCover can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL" It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.2.14. DISBV\_RD (52H/53H): Read Display Brightness Value**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
52H					DBV[11:4]				FFh
53H		Reserved			DBV[3:0]				FFh

Description
<ul style="list-style-type: none"><li>- This command returns the brightness value of the display.</li><li>- This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode.</li><li>- It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</li><li>- In principle the relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.</li><li>- DBV[11:0] is reset when display is in sleep-in mode.</li><li>- DBV[11:0] is '0' when bit BCTRL of "Display Brightness Value Control (53H)" command is '0'.</li><li>- DBV[11:0] is manual set brightness specified with "Display Brightness Value Control (53H)" command when bit BCTRL is '1'.</li><li>- See command "Display Brightness Value Setting (51H)".</li></ul> <p>Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.</p>

**2.2.15. DISBV\_CTRL (53H): Display Brightness Value Control**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
53H	Reserved	BCTRL	Reserved	DD	BL	Reserved	Reserved	00h	

Description
- This command is used to control ambient light, brightness and gamma settings.
BCTRL : Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard.
'0' = Off (Brightness registers are 00h)
'1' = On (Brightness registers are active, according to the other parameters.)
DD : Display Dimming
- Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at DD=1, e.g. BCTRL: 0 -> 1 or 1-> 0.
'0' = Display Dimming is off
'1' = Display Dimming is on
BL : Backlight On/Off
- When BL bit change from "On" to "Off", backlight is turned off
'0' = Off (Completely turn off backlight circuit. Control lines must be low. )
'1' = On
Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL" It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.2.16. RDDISBV\_CTRL (54H): Read Display Brightness Value Control**

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
54H	Reserved	BCTRL	Reserved	DD	BL	Reserved	Reserved	00h	

Description
- This command returns ambient light and brightness control values, see command "Display Brightness Value Control (53H) ".
BCTRL: Brightness Control Block On/Off. This bit is always used to switch brightness for display.
'0' = Off
'1' = On
DD: Display Dimming
'0' = Display Dimming is off
'1' = Display Dimming is on
BL: Backlight On/Off, This bit is always controlled by the user
'0' = Off (completely turn off backlight circuit)
'1' = On
Note: Focal CleverCover can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

## 2.2.17. WRFCC\_CABC (55H): Write Focal CleverColor – Content Adaptive Brightness Control

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
55H					Reserved		CABC_MODE[1:0]	00h	

Description																	
- This command is used to set parameters for power functionality.																	
- There is possible to use 3 different modes for content adaptive image functionality, which are defined on a table below.																	
<table border="1"><thead><tr><th>CABC_MODE</th><th>Function</th><th>Note</th></tr></thead><tbody><tr><td>0h</td><td>Power Save Off</td><td>CABC Off</td></tr><tr><td>1h</td><td>Power Save Low</td><td>User Interface Image(UI)</td></tr><tr><td>2h</td><td>Power Save Medium</td><td>Still Picture(ST)</td></tr><tr><td>3h</td><td>Power Save High</td><td>Moving Image(MV)</td></tr></tbody></table>			CABC_MODE	Function	Note	0h	Power Save Off	CABC Off	1h	Power Save Low	User Interface Image(UI)	2h	Power Save Medium	Still Picture(ST)	3h	Power Save High	Moving Image(MV)
CABC_MODE	Function	Note															
0h	Power Save Off	CABC Off															
1h	Power Save Low	User Interface Image(UI)															
2h	Power Save Medium	Still Picture(ST)															
3h	Power Save High	Moving Image(MV)															
CABC = Content Adaptive Brightness Control																	
Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.																	

## 2.2.18. RDFCC\_CABC (56H): Read Focal CleverColor – Content Adaptive Brightness Control

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
56H					Reserved		CABC_MODE[1:0]	00h	

**Description**

- This command returns for power functionality see command “Write Focal CleverColor – Content Adaptive Brightness Control (55H) ”.

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command “BANK23H 99H~9AH, FCC\_CMD\_SEL” It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

2.2.19. **OTP\_PROG (58H/5AH/70H/71H/72H/73H) : OTP Program**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
58H	OTP_PROG_START[7:0]								00h
5AH	OTP_PROG_UNLOCK[7:0]								00h
70H	OTP_PROG_BANK[7:0]								00h
71H	OTP_PROG_BANK[15:8]								00h
72H	OTP_PROG_BANK[23:16]								00h
73H	OTP_PROG_BANK[31:24]								00h

Description
OTP_PROG_UNLOCK : OTP Programming Function Unlock - This command is used to set OTP programming function unlock. '96h' = Unlock OTP programming function. 'Others' = Lock OTP programming function.
OTP_PROG_START : OTP Bank Programming Start - This command is used to set OTP bank programming start. - When OTP bank programming is done, register value will be set to EDh. 'AAh' = Start OTP bank programming. 'Others' = Not programming.
OTP_PROG_BANK : OTP Programming Bank Set - This command is used to set OTP programming bank from Register/SRAM into OTP. Bit[0]: Bank 0 Bit[1]: Bank 1 ..... Bit[31]: Bank 31

**2.2.20. WRCABC\_MDISBV (5EH/5FH) : Focal CleverColor – Write CABC Minimum Display Brightness Value**

Bank-									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
5EH	CMB[11:4]							00h	
5FH	Reserved					CMB[3:0]			00h

**Description**

- This command is used to set the minimum brightness value of the display for CABC function.
- In principle relationship is that 000h value means the lowest brightness for CABC and FFFh value means the highest brightness for CABC.

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.2.21. RDCABC\_MDISBV (5FH/60H) : Focal CleverColor – Read CABC Minimum Display Brightness Value**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
5FH					CMB[11:4]				00h
60H		Reserved				CMB[3:0]			00h

Description
- This command returns the minimum brightness value of CABC function.
- In principle the relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.
- See command "Write CABC Minimum Brightness (5EH)".

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

## 2.2.22. FCC\_CE (90H~91H) : Focal CleverColor – Color Enhancement

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
90H					CE_SEL[6:0]			CE_EN	00h
91H		Reserved			CE_SKIN[3:0]				00h

Description
- This command is used to set Focal CleverColor Color Enhancement function - CE_EN : Color Enhancement function enable - CE_SEL[6:0] : Select Color Enhancement function gamma curve - CE_SKIN[3:0] : Adjust skin tone function
Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL" It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.2.23. FCC\_SHARPN (92H~93H) : Focal CleverColor – Sharpness**

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
92H	SHP_GAIN_MINUS[3:0]					SHP_SLOPE[2:0]		SHP_EN	00h
93H	Reserved					SHP_GAIN_PLUS[3:0]		00h	

Description																																							
This command is used to set Focal CleverColor Sharpness function																																							
- SHP_EN : Sharpness function enable.																																							
- SHP_SLOPE : Sharpness Slope Setting																																							
- SHP_GAIN_PLUS[3:0]/SHP_GAIN_MINUS[3:0] : Set Sharpness function gain ratio.																																							
<table border="1"> <thead> <tr> <th>GAIN_P[3:0]/GAIN_M[3:0]</th> <th>Gain Ratio</th> <th>GAIN_P[3:0]/GAIN_M[3:0]</th> <th>Gain Ratio</th> </tr> </thead> <tbody> <tr> <td>0h</td> <td>0</td> <td>8h</td> <td>0.8</td> </tr> <tr> <td>1h</td> <td>0.1</td> <td>9h</td> <td>0.9</td> </tr> <tr> <td>2h</td> <td>0.2</td> <td>Ah</td> <td>1.0</td> </tr> <tr> <td>3</td> <td>0.3</td> <td>Bh</td> <td>1.1</td> </tr> <tr> <td>4h</td> <td>0.4</td> <td>Ch</td> <td>1.2</td> </tr> <tr> <td>5h</td> <td>0.5</td> <td>Dh</td> <td>1.3</td> </tr> <tr> <td>6h</td> <td>0.6</td> <td>Eh</td> <td>1.4</td> </tr> <tr> <td>7h</td> <td>0.7</td> <td>Fh</td> <td>1.5</td> </tr> </tbody> </table>				GAIN_P[3:0]/GAIN_M[3:0]	Gain Ratio	GAIN_P[3:0]/GAIN_M[3:0]	Gain Ratio	0h	0	8h	0.8	1h	0.1	9h	0.9	2h	0.2	Ah	1.0	3	0.3	Bh	1.1	4h	0.4	Ch	1.2	5h	0.5	Dh	1.3	6h	0.6	Eh	1.4	7h	0.7	Fh	1.5
GAIN_P[3:0]/GAIN_M[3:0]	Gain Ratio	GAIN_P[3:0]/GAIN_M[3:0]	Gain Ratio																																				
0h	0	8h	0.8																																				
1h	0.1	9h	0.9																																				
2h	0.2	Ah	1.0																																				
3	0.3	Bh	1.1																																				
4h	0.4	Ch	1.2																																				
5h	0.5	Dh	1.3																																				
6h	0.6	Eh	1.4																																				
7h	0.7	Fh	1.5																																				
Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL"																																							
It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.																																							

## 2.2.24. FCC\_CNTRST (94H~96H) : Focal CleverColor – Contrast Enhancement

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
94H	CNTRST_LEVEL[5:0]					ADJ_MODE		CNT_EN	00h
95H	CNTRST_SHIFT[6:0]					CNT_LV[6]		00h	
96H	CNTRST_HISY_HB[3:0]			CNTRST_HISY_LB[3:0]				00h	

Description
<ul style="list-style-type: none"><li>- This command is used to set Focal CleverColor Contrast function</li><li>- CNT_EN : Contrast function enable.</li><li>- ADJ_MODE : Contrast function adjustment mode enable.</li><li>- CNTRST_LEVEL[6:0] : Select Contrast level.</li><li>- CNTRST_SHIFT [6:0] : Set Contrast shift.</li><li>- CNTRST_HISY_HB[3:0] : Set the Higher bound for contrast hisY.</li><li>- CNTRST_HISY_LB[3:0] : Set the Lower bound for contrast hisY.</li></ul> <p>Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.</p>

## 2.2.25. FCC\_AIE (97H) : Focal CleverColor – AIE

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
97H					AIE_LEVEL[6:0]			AIE_EN	00h

Description	
- This command is used to set Focal CleverColor AIE function	
- AIE_EN : Set AIE function enable.	
- AIE_Level[6:0] : Set AIE function level.	

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL" It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

## 2.2.26. FCC\_WA (98H) : Focal CleverColor – White Balance Adjustment

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
98H					WA_SEL[6:0]			WA_EN	00h

Description																	
- This command is used to set Focal CleverColor White Balance Adjustment function																	
- WA_EN : White Balance Adjustment function enable																	
- WA_SEL[6:0] : Set White Balance Adjustment parameter																	
<table border="1"><thead><tr><th>WA_SEL[6:0]</th><th>White Point Setting</th></tr></thead><tbody><tr><td>0h</td><td>Default White Point</td></tr><tr><td>1h ~ 64h</td><td>Cooler White Point</td></tr><tr><td>65h ~ 27 h</td><td>Warmer White Point</td></tr></tbody></table>										WA_SEL[6:0]	White Point Setting	0h	Default White Point	1h ~ 64h	Cooler White Point	65h ~ 27 h	Warmer White Point
WA_SEL[6:0]	White Point Setting																
0h	Default White Point																
1h ~ 64h	Cooler White Point																
65h ~ 27 h	Warmer White Point																
Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.																	

## 2.2.27. RDDDB (A1H/A8H) : Read DDB Start &amp; Read DDB Continue

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
A1H (RDDDBSTR)	No Parameter								-
A8H (RDDDBCNT)	No Parameter								-

Description
RDDDBSTR : Read DDB Start Address = 'A1H' - The RDDDBSTR command reads identifying and descriptive information from the peripheral. This information is organized in the Device Descriptor Block (DDB) stored on the peripheral.
RDDDBCNT : Read DDB Continue Address = 'A8H' - This RDDDBCNT command returns supplier's identification and display module model/revision information from the point where RDDDBSTR command was interrupted by another command.
RDDDBSTR & RDDDBCNT should cooperate with MIPI short packet : Set Maximum Return Packet Size. Before these two commands, the Set Maximum Return Packet Size packet should be sent in advance to set the numbers of returned reading data.
- The content of returned data is as follows: Parameter 1: ID0 in OTP. Parameter 2: ID1 in OTP. Parameter 3: ID2 in OTP. Parameter 4: ID3 in OTP. Parameter 5: ID4 in OTP. Parameter 6: ID5 in OTP. Parameter 7: ID6 in OTP. Parameter 8: ID7 in OTP. Parameter 9: ID8 in OTP. Parameter 10: ID9 in OTP. Parameter 11: ID_DA in OTP. Parameter 12: ID_DB in OTP. Parameter 13: ID_DC in OTP.
Restriction : - RDDDBSTR & RDDDBCNT commands are supported through MIPI interface only. - A RDDDBSTR command should be executed at least once before a RDDDBCNT command to define the read location. Otherwise, data read with a RDDDBCNT command is undefined.

## 2.2.28. RDID\_DA (DAH) : Read ID\_DA in OTP

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DAH					ID_DA[7:0]				00h

Description
- This read byte identifies the display module's manufacturer.

## 2.2.29. RDID\_DB (DBH) : Read ID\_DB in OTP

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DBH					ID_DB[7:0]				00h

**Description**

- This read byte is used to track the display module/driver version. It is defined by display supplier (with agreement) and changes each time a revision is made to the display, material or construction specifications.

## 2.2.30. RDID\_DC (DCH) : Read ID\_DC in OTP

Bank2F (Default Bank)									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DCH					ID_DC[7:0]				00h

Description	
- This read byte is used to track the display module/driver version. It is defined by display supplier (with agreement) and changes each time a revision is made to the display, material or construction specifications.	

### 2.3. System Function Command-2 Description

Command	BankSel [5:0]	(Hex)	Write/Read /Command	Function	MIPI Transmission
OTP_BANK1_PRG_FLG	00h	91h	W/R	OTP Program Status of Bank1	LPDT/HSDT
OTP_BANK2_PRG_FLG	00h	92h	W/R	OTP Program Status of Bank2	LPDT/HSDT
OTP_BANK3_PRG_FLG	00h	93h	W/R	OTP Program Status of Bank3	LPDT/HSDT
OTP_BANK4_PRG_FLG	00h	94h	W/R	OTP Program Status of Bank4	LPDT/HSDT
OTP_BANK10_PRG_FLG	00h	95h	W/R	OTP Program Status of Bank10	LPDT/HSDT
OTP_BANK23_PRG_FLG	00h	96h	W/R	OTP Program Status of Bank23	LPDT/HSDT
ID_SET	02h	80h	W/R	ID Setting	LPDT/HSDT
VCOM_SET	03h	80h	W/R	VCOM Setting	LPDT/HSDT
Temp_Sensor	04h	90h	W/R	Temperature sensor trim code and current sense code	LPDT/HSDT
PLL_SET	09h	84h	W/R	Pixel clock setting	LPDT/HSDT
LVD_SET	09h	89h	W/R	LVD Setting	LPDT/HSDT
Pump_CK_SET	09h	95h	W/R	VGH/VGL/VCL/VCI Pump Clock Rate Setting	LPDT/HSDT
Pump_Voltage_SET	09h	96h	W/R	VGH/VGL Voltage Setting	LPDT/HSDT
Clamp_Voltage_SET	09h	97h	W/R	VGH/VGL Clamp Voltage Setting	LPDT/HSDT
VGH0VGLO_SET	09h	99h	W/R	VGH02/VGH01/VGLO2/VGLO1 Voltage Setting	LPDT/HSDT
GVDDSET	0Ah	81h	W/R	GVDD/NGVDD Setting	LPDT/HSDT
AGMMA	0Ah	84h	W/R	Gamma Correction Characteristics Setting	LPDT/HSDT
MIPI_Set	0Bh	80h	W/R	MIPI Parameter Setting	LPDT/HSDT
LCD_System_Set	0Ch	80h	W/R	LCD System parameter setting	LPDT/HSDT
Resolution_Set	0Ch	81h	W/R	Resolution setting and blanking setting	LPDT/HSDT
PWIC_Set	0Eh	82h	W/R	PWIC parameter setting	LPDT/HSDT
GPIO_Set	0Eh	84h	W/R	GPIO output setting	LPDT/HSDT
Temp_Compensation	12h	80h	W/R	Temperature Compensation	LPDT/HSDT
Polarity_Set	13h	8Ch	W/R	Polarity parameter setting	LPDT/HSDT
GOA_OPT_SET1	14h	80h	W/R	GOA Other Setting 1	LPDT/HSDT
GOA_STV_SET	14h	8Ah	W/R	GOA STVx Setting	LPDT/HSDT
GOA_TPOFF_SWAP_SET	14h	A8h	W/R	GOA TPOFF Swap Setting	LPDT/HSDT
GOA_TPOFF_VBLANK_SET	14h	A8h	W/R	GOA TPOFF at V-blanking Setting	LPDT/HSDT
GOA_STV_CHOKE_SET	14h	B4h	W/R	GOA STV CHOKE Setting	LPDT/HSDT
GOA_CLK_SET	14h	B6h	W/R	GOA CLKx Setting	LPDT/HSDT
COG_TPSYNC_SET	14h	F6h	W/R	COG TPSYNC Setting	LPDT/HSDT
COG_GPMODE_SET	14h	FAh	W/R	COG GPMODE Setting	LPDT/HSDT
GOA_CLK_VBKH_SET	15h	81h	W/R	GOA CLK at V-blanking Setting	LPDT/HSDT
GOA_UD_SET	15h	91h	W/R	GOA UDx Setting	LPDT/HSDT
GOA_UD_SWAP_SET	15h	AEh	W/R	GOA UD Swap Setting	LPDT/HSDT
GOA_VDD_SET	15h	AEh	W/R	GOA VDDx Setting	LPDT/HSDT
GOA_LC_SET	15h	B7h	W/R	GOA LC Setting	LPDT/HSDT
GOA_INV_SET	15h	BCh	W/R	GOA INVERT Setting	LPDT/HSDT
PAN_U2D_GOUT_L_SET	15h	BCh	W/R	PANEL U2D Left GOUT Setting	LPDT/HSDT
PAN_D2U_GOUT_L_SET	15h	CDh	W/R	PANEL D2U Left GOUT Setting	LPDT/HSDT
PAN_U2D_GOUT_R_SET	15h	DDh	W/R	PANEL U2D Right GOUT Setting	LPDT/HSDT
PAN_D2U_GOUT_R_SET	15h	EEh	W/R	PANEL D2U Right GOUT Setting	LPDT/HSDT

Command	BankSel [5:0]	(Hex)	Write/Read /Command	Function	MIPI Transmission
GOA_EQ_SET	15h	FEh	<b>W/R</b>	GOA EQ Setting	LPDT/HSDT
CE_SET1	18h	80h	<b>W/R</b>	Focal CleverColor – Color Enhancement Parameter Setting 1	LPDT/HSDT
CE_SET2	18h	87h	<b>W/R</b>	Focal CleverColor – Color Enhancement Parameter Setting 2	LPDT/HSDT
CE_SET3	18h	93h	<b>W/R</b>	Focal CleverColor – Color Enhancement Parameter Setting 3	LPDT/HSDT
CE_SET4	18h	9Fh	<b>W/R</b>	Focal CleverColor – Color Enhancement Parameter Setting 4	LPDT/HSDT
SHARPN_SET	18h	ACh	<b>W/R</b>	Focal CleverColor – Sharpness Setting	LPDT/HSDT
HIS_SET	18h	AFh	<b>W/R</b>	Focal CleverColor – Histogram Analysis Setting	LPDT/HSDT
WA_SET	18h	B1h	<b>W/R</b>	Focal CleverColor – White Adjustment Parameter Setting	LPDT/HSDT
CABC_GAINSET	19h	80h	<b>W/R</b>	Focal CleverColor – CABC GAIN Setting	LPDT/HSDT
CABC_PWMSET	19h	8Ch	<b>W/R</b>	Focal CleverColor – CABC PWM Setting	LPDT/HSDT
AIE_PWMSET	19h	97h	<b>W/R</b>	Focal CleverColor – AIE PWM Setting	LPDT/HSDT
AIE_GAINSET	19h	98h	<b>W/R</b>	Focal CleverColor – AIE Gain Setting	LPDT/HSDT
PWM_CTRL	19h	A0h	<b>W/R</b>	PWM Pulse Control	LPDT/HSDT
DGAM_R	1Ah	80h	<b>W/R</b>	Focal CleverColor – Digital Gamma R Setting	LPDT/HSDT
DGAM_G	1Ah	B1h	<b>W/R</b>	Focal CleverColor – Digital Gamma G Setting	LPDT/HSDT
DGAM_B	1Ah	E2h	<b>W/R</b>	Focal CleverColor – Digital Gamma B Setting	LPDT/HSDT
VCOM_GVDD_Set	22h	8Bh	<b>W/R</b>	VCOM and GVDD parameter setting	LPDT/HSDT
FSC_SET	23h	80h	<b>W/R</b>	MIPI FSC Setting	LPDT/HSDT
PWM_EN	23h	83h	<b>W/R</b>	PWM Enable	LPDT/HSDT
FCC_CE	23h	86h	<b>W/R</b>	Focal CleverColor – Color Enhancement	LPDT/HSDT
FCC_SHARPN	23h	88h	<b>W/R</b>	Focal CleverColor – Sharpness	LPDT/HSDT
FCC_CNTRST	23h	8Ah	<b>W/R</b>	Focal CleverColor – Contrast Enhancement	LPDT/HSDT
FCC_AIE	23h	8Dh	<b>W/R</b>	Focal CleverColor – AIE	LPDT/HSDT
FCC_WA	23h	8Eh	<b>W/R</b>	Focal CleverColor – White Balance Adjustment	LPDT/HSDT
FCC_DGAMFRC	23h	8Fh	<b>W/R</b>	Focal CleverColor – Digital Gamma and Frame Rate Control	LPDT/HSDT
DISBV_SET	23h	90h	<b>W/R</b>	Display Brightness Value Setting	LPDT/HSDT
DISBV_RD	23h	92h	<b>R</b>	Read Display Brightness Value	LPDT/HSDT
DISBV_CTRL	23h	94h	<b>W/R</b>	Display Brightness Value Control	LPDT/HSDT
FCC_CABC	23h	95h	<b>W/R</b>	Focal CleverColor – Content Adaptive Brightness Control	LPDT/HSDT
CABC_MDISBV	23h	97h	<b>W/R</b>	Focal CleverColor – CABC Minimum Display Brightness Value	LPDT/HSDT
FCC_CMD_SEL	23h	99h	<b>W/R</b>	Focal CleverColor CMD1/CMD2 Selection	LPDT/HSDT
SPI_LOAD_FINISH	24h	90h	<b>W/R</b>	SPI Load Finish	LPDT/HSDT

**2.3.1 OTP\_BANK1\_PRG\_FLG (BANK00H 91H) : OTP Program Status of Bank1**

Bank00H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
91H		Reserved			SB1OverW rite	SB1Sel_st[2:0]			FFh

Description
- BANK00H 91H, D[3:0]
SB1Sel_st [2:0] is used to show program times of Bank1.
'111' = 0 times. (default)
'110' = 1 times.
'100' = 2 times.
'000' = 3 times.
SB1OverWrite is used to show over-programmed of Bank1 .
'0' = over programmed.
'1' = Non over-programmed(default)

**2.3.2 OTP\_BANK2\_PRG\_FLG (BANK00H 92H) : OTP Program Status of Bank2**

Bank00H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
92H			Reserved			SB2OverWr ite		SB2Sel_st[1:0]	FFh

Description
- BANK00H 92H, D[2:0]
SB2Sel_st [1:0] is used to show program times of Bank2.
'11' = 0 times. (default)
'10' = 1 times.
'00' = 2 times.
SB2OverWrite is used to show over-programmed of Bank2 .
'0' = over programmed.
'1' = Non over-programmed(default)

**2.3.3 OTP\_BANK3\_PRG\_FLG (BANK00H 93H) : OTP Program Status of Bank3**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
93H					SB3Sel_st[7:0]				FFh

Description
- BANK00H 93H, D[7:0] SB3Sel_st [7:0] is used to show program times of Bank3. '11111111' = 0 times. (default) '11111110' = 1 times. '11111100' = 2 times. '11111000' = 3 times. '11110000' = 4 times. '11100000' = 5 times. '11000000' = 6 times. '10000000' = 7 times. '00000000' = 8 times.

**2.3.4 OTP\_BANK4\_PRG\_FLG (BANK00H 94H) : OTP Program Status of Bank4**

Bank00H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
94H			Reserved			SB4OverWr ite		SB4Sel_st[1:0]	FFh

Description
- BANK00H 94H, D[2:0]
SB4Sel_st [1:0] is used to show program times of Bank4.
'11' = 0 times. (default)
'10' = 1 times.
'00' = 2 times.
SB4OverWrite is used to show over-programmed of Bank4 .
'0' = over programmed.
'1' = Non over-programmed(default)

**2.3.5 OTP\_BANK10\_PRG\_FLG (BANK00H 95H) : OTP Program Status of Bank10**

Bank00H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
95H			Reserved			SB10Over Write		SB10Sel_st[1:0]	FFh

Description
- BANK00H 95H, D[2:0]
SB10Sel_st [1:0] is used to show program times of Bank10.
'11' = 0 times. (default)
'10' = 1 times.
'00' = 2 times.
SB10OverWrite is used to show over-programmed of Bank10 .
'0' = over programmed.
'1' = Non over-programmed(default)

**2.3.6 OTP\_BANK23\_PRG\_FLG (BANK00H 96H) : OTP Program Status of Bank23**

Bank00H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
96H			Reserved			SB23Over Write		SB23Sel_st[1:0]	FFh

Description	
- BANK00H 96H, D[2:0]	
SB23Sel_st [1:0] is used to show program times of Bank23.	
'11' = 0 times. (default)	
'10' = 1 times.	
'00' = 2 times.	
SB23OverWrite is used to show over-programmed of Bank23 .	
'0' = over programmed.	
'1' = Non over-programmed(default)	

**2.3.7 ID\_SET (BANK02H 80H ~ 8CH) : ID Setting**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
80H					ID0				00h
81H					ID1				00h
82H					ID2				00h
83H					ID3				00h
84H					ID4				00h
85H					ID5				00h
86H					ID6				00h
87H					ID7				00h
88H					ID8				00h
89H					ID9				00h
8AH					ID_DA				00h
8BH					ID_DB				00h
8CH					ID_DC				00h

Description
- BANK02H 80H, D[7:0] ~ 8CH, D[7:0]
ID0[7:0] ~ ID_DC[7:0] is used to set ID0 ~ ID_DC respectively.
ID_DA/ID_DB/ID_DC also can be read via Command-1 DAh/DBh/DCh command.

**2.3.8 VCOM\_SET (BANK03H 80H~82H BANK08H 80H~82H) : VCOM Setting**

Bank03H													
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default				
80H	VCOM OTP[7:0]												
81H	VCOM OFF OTP[6:0]												
82H	Reserved					VCOM OFF OTP[8:7]							
Bank08H													
80H	VCOM MCU[7:0]												
81H	VCOM OFF MCU[6:0]												
82H	Reserved			VCOM_OF_F_TRIM_SEL	VCOM_TRI_M_SEL	VCOM OFF MCU[8:7]							

Description									
- BANK03H 80H, D[7:0]~82H, D[1:0] BANK08H 80H, D[7:0]~82H, D[3:0]									
VCOM OTP[8:0] : VCOM Trim Code in OTP									
- This VCOM code is programmed into OTP.									
VCOM MCU[8:0] : VCOM Trim Code in MCU									
- This VCOM code is written into register and can be updated by MCU if need be.									
VCOM TRIM SEL : VCOM Trim Code Selection									
'0' = Select VCOM code from VCOM OTP (default)									
'1' = Select VCOM code from VCOM MCU									
VCOM OFF Trim Code will apply to set a different VCOM value in Power-Off stage for special application if need be. Please refer to Power_Off_VCOM_Set section to enable VCOM_OFF_LEVEL function.									
VCOM OFF OTP[8:0] : VCOM OFF Trim Code in OTP									
- This VCOM OFF code is programmed into OTP .									
VCOM OFF MCU[8:0] : VCOM OFF Trim Code in MCU									
- This VCOM OFF code is written into register and can be updated by MCU if need be.									
VCOM OFF TRIM SEL : VCOM _OFF Trim Code Selection in Power-Off Stage.									
'0' : VCOM OFF OTP (default)									
'1' : VCOM OFF MCU									

COD_E	VCOM_V	COD_D	VCOM_V	COD_E	VCOM_V	COD_E	VCOM_V	COD_E	VCOM_V								
0	1	64	0.36	128	-0.28	192	-0.92	256	-1.56	320	-2.2	384	-2.84	448	-3.49		
1	0.99	65	0.35	129	-0.29	193	-0.93	257	-1.57	321	-2.21	385	-2.85	449	-3.5		
2	0.98	66	0.34	130	-0.3	194	-0.94	258	-1.58	322	-2.22	386	-2.86	450	-3.51		
3	0.97	67	0.33	131	-0.31	195	-0.95	259	-1.59	323	-2.23	387	-2.87	451	-3.52		
4	0.96	68	0.32	132	-0.32	196	-0.96	260	-1.6	324	-2.24	388	-2.88	452	-3.53		
5	0.95	69	0.31	133	-0.33	197	-0.97	261	-1.61	325	-2.25	389	-2.89	453	-3.54		
6	0.94	70	0.3	134	-0.34	198	-0.98	262	-1.62	326	-2.26	390	-2.9	454	-3.55		
7	0.93	71	0.29	135	-0.35	199	-0.99	263	-1.63	327	-2.27	391	-2.91	455	-3.56		
8	0.92	72	0.28	136	-0.36	200	-1	264	-1.64	328	-2.28	392	-2.92	456	-3.57		
9	0.91	73	0.27	137	-0.37	201	-1.01	265	-1.65	329	-2.29	393	NA	457	NA		
10	0.9	74	0.26	138	-0.38	202	-1.02	266	-1.66	330	-2.3	394	NA	458	NA		
11	0.89	75	0.25	139	-0.39	203	-1.03	267	-1.67	331	-2.31	395	NA	459	NA		
12	0.88	76	0.24	140	-0.4	204	-1.04	268	-1.68	332	-2.32	396	NA	460	NA		
13	0.87	77	0.23	141	-0.41	205	-1.05	269	-1.69	333	-2.33	397	NA	461	NA		
14	0.86	78	0.22	142	-0.42	206	-1.06	270	-1.7	334	-2.34	398	NA	462	NA		
15	0.85	79	0.21	143	-0.43	207	-1.07	271	-1.71	335	-2.35	399	NA	463	NA		
16	0.84	80	0.2	144	-0.44	208	-1.08	272	-1.72	336	-2.36	400	NA	464	NA		
17	0.83	81	0.19	145	-0.45	209	-1.09	273	-1.73	337	-2.37	401	NA	465	NA		
18	0.82	82	0.18	146	-0.46	210	-1.1	274	-1.74	338	-2.38	402	NA	466	NA		
19	0.81	83	0.17	147	-0.47	211	-1.11	275	-1.75	339	-2.39	403	NA	467	NA		
20	0.8	84	0.16	148	-0.48	212	-1.12	276	-1.76	340	-2.4	404	NA	468	NA		
21	0.79	85	0.15	149	-0.49	213	-1.13	277	-1.77	341	-2.41	405	NA	469	NA		
22	0.78	86	0.14	150	-0.5	214	-1.14	278	-1.78	342	-2.42	406	NA	470	NA		
23	0.77	87	0.13	151	-0.51	215	-1.15	279	-1.79	343	-2.43	407	NA	471	NA		
24	0.76	88	0.12	152	-0.52	216	-1.16	280	-1.8	344	-2.44	408	NA	472	NA		
25	0.75	89	0.11	153	-0.53	217	-1.17	281	-1.81	345	-2.45	409	NA	473	NA		
26	0.74	90	0.1	154	-0.54	218	-1.18	282	-1.82	346	-2.46	410	NA	474	NA		
27	0.73	91	0.09	155	-0.55	219	-1.19	283	-1.83	347	-2.47	411	NA	475	NA		
28	0.72	92	0.08	156	-0.56	220	-1.2	284	-1.84	348	-2.48	412	NA	476	NA		
29	0.71	93	0.07	157	-0.57	221	-1.21	285	-1.85	349	-2.49	413	NA	477	NA		
30	0.7	94	0.06	158	-0.58	222	-1.22	286	-1.86	350	-2.5	414	NA	478	NA		
31	0.69	95	0.05	159	-0.59	223	-1.23	287	-1.87	351	NA	415	NA	479	NA		
32	0.68	96	0.04	160	-0.6	224	-1.24	288	-1.88	352	NA	416	NA	480	NA		
33	0.67	97	0.03	161	-0.61	225	-1.25	289	-1.89	353	NA	417	NA	481	NA		
34	0.66	98	0.02	162	-0.62	226	-1.26	290	-1.9	354	NA	418	NA	482	NA		
35	0.65	99	0.01	163	-0.63	227	-1.27	291	-1.91	355	NA	419	NA	483	NA		
36	0.64	100	0	164	-0.64	228	-1.28	292	-1.92	356	NA	420	NA	484	NA		
37	0.63	101	-0.01	165	-0.65	229	-1.29	293	-1.93	357	NA	421	NA	485	NA		

38	0.62	102	-0.02	166	-0.66	230	-1.3	294	-1.94	358	NA	422	NA	486	NA
39	0.61	103	-0.03	167	-0.67	231	-1.31	295	-1.95	359	NA	423	NA	487	NA
40	0.6	104	-0.04	168	-0.68	232	-1.32	296	-1.96	360	NA	424	NA	488	NA
41	0.59	105	-0.05	169	-0.69	233	-1.33	297	-1.97	361	NA	425	NA	489	NA
42	0.58	106	-0.06	170	-0.7	234	-1.34	298	-1.98	362	NA	426	NA	490	NA
43	0.57	107	-0.07	171	-0.71	235	-1.35	299	-1.99	363	NA	427	NA	491	NA
44	0.56	108	-0.08	172	-0.72	236	-1.36	300	-2	364	NA	428	NA	492	NA
45	0.55	109	-0.09	173	-0.73	237	-1.37	301	-2.01	365	NA	429	NA	493	NA
46	0.54	110	-0.1	174	-0.74	238	-1.38	302	-2.02	366	NA	430	NA	494	NA
47	0.53	111	-0.11	175	-0.75	239	-1.39	303	-2.03	367	NA	431	NA	495	NA
48	0.52	112	-0.12	176	-0.76	240	-1.4	304	-2.04	368	NA	432	NA	496	NA
49	0.51	113	-0.13	177	-0.77	241	-1.41	305	-2.05	369	NA	433	NA	497	NA
50	0.5	114	-0.14	178	-0.78	242	-1.42	306	-2.06	370	NA	434	NA	498	NA
51	0.49	115	-0.15	179	-0.79	243	-1.43	307	-2.07	371	NA	435	NA	499	NA
52	0.48	116	-0.16	180	-0.8	244	-1.44	308	-2.08	372	NA	436	NA	500	NA
53	0.47	117	-0.17	181	-0.81	245	-1.45	309	-2.09	373	NA	437	NA	501	NA
54	0.46	118	-0.18	182	-0.82	246	-1.46	310	-2.1	374	NA	438	NA	502	NA
55	0.45	119	-0.19	183	-0.83	247	-1.47	311	-2.11	375	NA	439	NA	503	NA
56	0.44	120	-0.2	184	-0.84	248	-1.48	312	-2.12	376	NA	440	NA	504	NA
57	0.43	121	-0.21	185	-0.85	249	-1.49	313	-2.13	377	NA	441	NA	505	NA
58	0.42	122	-0.22	186	-0.86	250	-1.5	314	-2.14	378	NA	442	NA	506	NA
59	0.41	123	-0.23	187	-0.87	251	-1.51	315	-2.15	379	NA	443	NA	507	NA
60	0.4	124	-0.24	188	-0.88	252	-1.52	316	-2.16	380	NA	444	NA	508	NA
61	0.39	125	-0.25	189	-0.89	253	-1.53	317	-2.17	381	NA	445	NA	509	NA
62	0.38	126	-0.26	190	-0.9	254	-1.54	318	-2.18	382	NA	446	NA	510	NA
63	0.37	127	-0.27	191	-0.91	255	-1.55	319	-2.19	383	NA	447	NA	511	NA

Note: VCOM >= VCL + 0.5V ; VCL = 1/2 \* AVEE

**2.3.9 Temp\_Sensor (BANK04H 90H~92H BANK12H A7H~A8H) : Temperature sensor trim code and current sense code**

Bank04H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
90H	TEMP_TRIM_HI[5:0]						Internal Used		00H
91H	TEMP_TRIM_LO[5:0]						TEMP_TRIM_HI[7:6]		00H
92H	Reserved						TEMP_TRIM_LO[7:6]		00H

Bank12H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
A7H	Temperature_Code_AD[7:0]						00H		
A8H	Temperature_Code_AVG[7:0]						00H		

Description
TEMP_TRIM_HI[7:0] : Temperature Sensor T_HI Code
TEMP_TRIM_LO[7:0] : Temperature Sensor T_LO Code
Temperature_Code_AD[7:0] : Temperature Code from analog macro
Temperature_Code_Avg[7:0] : Temperature Code Hysteresis –
Temperature_Code_AVG = 15/16Temperature_Code_AVG + 1/16 Temperature_Code_AD

**2.3.10 PLL\_SET (BANK09H 85H~86H) : Pixel clock setting**

Bank09H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
85H	PLL135M_DIV[3:0]				Internal Used				D5h
86H	Internal Used					PLL135M_DIV[4]		4Ah	

Description
- BANK09H 85H, D[7:4] ~ 86H, D[0]
PLL135M_DIV : Set PLL Frequency (Valid range 11 ~ 31)
PLL_OUT(Mhz) = PLL135M_DIV * 4.375Mhz

**2.3.11 LVD\_SET (BANK09H 89H~8AH) : LVD Setting**

Bank09H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
89H	LVD_VDDI_SEL[1:0]						Internal Used		62h
8AH		Internal Used						LVD_AVDD_SEL[1:0]	0Dh

Description	
- BANK09H 89H, D[7:6]	
LVD_VDDI_SEL[1:0] : VDDI LVD Trigger Level Setting	
LVD_VDDI_SEL[1:0]	Voltage (V)
2'bX1	1.4V
- BANK0AH 8AH, D[1:0]	
LVD_AVDD_SEL[1:0] : AVDD LVD Trigger Level Selection	
LVD_AVDD_SEL[1:0]	Voltage (V)
2'b00	3.6V
2'b01 (Default)	4.0V
2'b10	4.4V
2'b11	4.8V

**2.3.12 Pump\_CK\_SET (BANK09H 95H~96H) : VGH/VGL/VCL/VCI Pump Clock Rate Setting**

Bank09H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
95H	PUMP_VGL_CK_RATE[2:0]			PUMP_VGH_CK_RATE[2:0]			Internal Used		91h
96H	PUMP4_SEL_NORM[1:0] 1		PUMP_VCI_CK_RATE[2:0]			PUMP_VCL_CK_RATE[2:0]			A4h

Description
- BANK09H 95H, D[7:2] ~ 96H, D[5:0]
PUMP_VGH_CK_RATE : VGH Pump Ctrl - Clock Rate
000 : 8X Line Rate (period = 1/8 * Line width)
001 : 4X Line Rate (period = 1/4 * Line width)
010 : 2X Line Rate (period = 1/2 * Line width)
011 : 1X Line Rate (period = 1 * Line width)
100 : 1/2X Line Rate (period = 2 * Line width) (Default)
101 : 1/4X Line Rate (period = 4 * Line width)
110 : 1/8X Line Rate (period = 8 * Line width)
111 : 1/16X Line Rate (period = 16 * Line width)
PUMP_VGL_CK_RATE : VGL Pump Ctrl - Clock Rate
000 : 8X Line Rate (period = 1/8 * Line width)
001 : 4X Line Rate (period = 1/4 * Line width)
010 : 2X Line Rate (period = 1/2 * Line width)
011 : 1X Line Rate (period = 1 * Line width)
100 : 1/2X Line Rate (period = 2 * Line width) (Default)
101 : 1/4X Line Rate (period = 4 * Line width)
110 : 1/8X Line Rate (period = 8 * Line width)
111 : 1/16X Line Rate (period = 16 * Line width)
PUMP_VCL_CK_RATE : VCL Pump Ctrl - Clock Rate
000 : 8X Line Rate (period = 1/8 * Line width)
001 : 4X Line Rate (period = 1/4 * Line width)
010 : 2X Line Rate (period = 1/2 * Line width)
011 : 1X Line Rate (period = 1 * Line width)
100 : 1/2X Line Rate (period = 2 * Line width) (Default)
101 : 1/4X Line Rate (period = 4 * Line width)
110 : 1/8X Line Rate (period = 8 * Line width)
111 : 1/16X Line Rate (period = 16 * Line width)
PUMP_VCI_CK_RATE : VCI Pump Ctrl - Clock Rate
000 : 8X Line Rate (period = 1/8 * Line width)
001 : 4X Line Rate (period = 1/4 * Line width)
010 : 2X Line Rate (period = 1/2 * Line width)

011 : 1X Line Rate (period = 1 \* Line width)  
100 : 1/2X Line Rate (period = 2 \* Line width) (Default)  
101 : 1/4X Line Rate (period = 4 \* Line width)  
110 : 1/8X Line Rate (period = 8 \* Line width)  
111 : 1/16X Line Rate (period = 16 \* Line width)

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**2.3.13 Pump\_Voltage\_SET (BANK09H 96H~A0H) : VGH/VGL Voltage Setting**

Bank09H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
96H	PUMP4_SEL_NORM[1:0]		PUMP_VCI_CK_RATE[2:0]			PUMP_VCL_CK_RATE[2:0]			A4h
97H	PUMP_PU_MP5_SEL[0]	PUMP_EN_AMP	PUMP_EN_PUMP4_CL2	PUMP_EN_PUMP4_CL2	PUMP_PUMP4_SEL_STBN[2:0]			PUMP_PUM_P4_SEL_NORM[2]	F0h
98H	PUMP_PUMP4_CLAMP[6:0]				PUMP_PUM_P5_SEL[1]			A5h	
9FH	PUMP_VCLS_R[1:0]		PUMP_EN_PUMP31_SH	Reserved					00h
A0H	Reserved					PUMP_VCL_S_R[2]	51h		

Description	
- BANK09H 96H, D[7:6] ~ A0H, D[0]	
PUMP_PUMP4_SEL(NORM/STBN) : VGH Pump Voltage in Normal Mode/Standby Mode	
PUMP_PUMP4_SEL[2:0]	Mode
3'd0	X4 (AVDD-AVEE)
3'd1	X5 (VCI1+AVDD-AVEE)
3'd2	X6 (2AVDD-AVEE)
3'd3	X7 (VCI1+AVDD-2AVEE)
3'd4	X8 (2AVDD-2AVEE)
3'd5	NONE
3'd6	NONE
3'd7	NONE
PUMP_PUMP5_SEL : VGL Pump Voltage	
PUMP_PUMP5_SEL[1:0]	Mode
2'b00	X3 (VCL+AVEE)
2'b01	X4 (2AVEE)
2'b10	X5 (VCL+AVEE-AVDD)
2'b11	X6 (2AVEE-AVDD)

PUMP\_VCLS\_R : VCL Pump Voltage

PUMP_VCLS_R[2:0]	Voltage(V)
3'd0	-2
3'd1	-2.25
3'd2	-2.5
3'd3	-2.75
3'd4	-3
3'd5	-3.5
3'd6	-4
3'd7	-4.5

**2.3.14 Clamp\_Voltage\_SET (BANK09H 97H~99H) : VGH/VGL Clamp Voltage Setting**

Bank09H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
97H	PUMP_PU_MP5_SEL[0]	PUMP_EN_PUMP5_CLAMP	PUMP_EN_PUMP4_C22	PUMP_EN_PUMP4_CLAMP_NORM	PUMP_PUMP4_SEL_STBN[2:0]			PUMP_PUM_P4_SEL_NORM[2]	F0h
98H	PUMP_PUMP4_CLAMP[6:0]						PUMP_PUM_P5_SEL[1]		A5h
99H	HVREG_V_GHO2_SEL[0]	PUMP_PUMP5_CLAMP[6:0]							C3h

Description							
- BANK09H 97H, D[4] ~ 99H, D[6:0]							
PUMP_EN_PUMP4_CLAMP_NORM : VGH Clamp Enable Signal @ NORM_ST							
PUMP_EN_PUMP5_CLAMP : VGL Clamp Enable Signal							
PUMP_PUMP4_CLAMP[6:0] : VGH Clamp Voltage							
PUMP_PUMP4_CLAMP[6:0]	Voltage(V)	PUMP_PUMP4_CLAMP[6:0]	Voltage(V)	PUMP_PUMP4_CLAMP[6:0]	Voltage(V)	PUMP_PUMP4_CLAMP[6:0]	Voltage(V)
7'd0	7.3	7'd32	10.5	7'd64	13.7	7'd96	16.9
7'd1	7.4	7'd33	10.6	7'd65	13.8	7'd97	17
7'd2	7.5	7'd34	10.7	7'd66	13.9	7'd98	17.1
7'd3	7.6	7'd35	10.8	7'd67	14	7'd99	17.2
7'd4	7.7	7'd36	10.9	7'd68	14.1	7'd100	17.3
7'd5	7.8	7'd37	11	7'd69	14.2	7'd101	17.4
7'd6	7.9	7'd38	11.1	7'd70	14.3	7'd102	17.5
7'd7	8	7'd39	11.2	7'd71	14.4	7'd103	17.6
7'd8	8.1	7'd40	11.3	7'd72	14.5	7'd104	17.7
7'd9	8.2	7'd41	11.4	7'd73	14.6	7'd105	17.8
7'd10	8.3	7'd42	11.5	7'd74	14.7	7'd106	17.9
7'd11	8.4	7'd43	11.6	7'd75	14.8	7'd107	18
7'd12	8.5	7'd44	11.7	7'd76	14.9	7'd108	18.1
7'd13	8.6	7'd45	11.8	7'd77	15	7'd109	18.2
7'd14	8.7	7'd46	11.9	7'd78	15.1	7'd110	18.3
7'd15	8.8	7'd47	12	7'd79	15.2	7'd111	18.4
7'd16	8.9	7'd48	12.1	7'd80	15.3	7'd112	18.5
7'd17	9	7'd49	12.2	7'd81	15.4	7'd113	18.6
7'd18	9.1	7'd50	12.3	7'd82	15.5	7'd114	18.7
7'd19	9.2	7'd51	12.4	7'd83	15.6	7'd115	18.8
7'd20	9.3	7'd52	12.5	7'd84	15.7	7'd116	18.9
7'd21	9.4	7'd53	12.6	7'd85	15.8	7'd117	19

7'd22	9.5	7'd54	12.7	7'd86	15.9	7'd118	19.1
7'd23	9.6	7'd55	12.8	7'd87	16	7'd119	19.2
7'd24	9.7	7'd56	12.9	7'd88	16.1	7'd120	19.3
7'd25	9.8	7'd57	13	7'd89	16.2	7'd121	19.4
7'd26	9.9	7'd58	13.1	7'd90	16.3	7'd122	19.5
7'd27	10	7'd59	13.2	7'd91	16.4	7'd123	19.6
7'd28	10.1	7'd60	13.3	7'd92	16.5	7'd124	19.7
7'd29	10.2	7'd61	13.4	7'd93	16.6	7'd125	19.8
7'd30	10.3	7'd62	13.5	7'd94	16.7	7'd126	19.9
7'd31	10.4	7'd63	13.6	7'd95	16.8	7'd127	20

PUMP\_PUMP5\_CLAMP[6:0] : VGL Clamp Voltage

PUMP_PUMP5_CLAMP[6:0]	Voltage(V)	PUMP_PUMP5_CLAMP[6:0]	Voltage(V)	PUMP_PUMP5_CLAMP[6:0]	Voltage(V)	PUMP_PUMP5_CLAMP[6:0]	Voltage(V)
7'd0	-5.3	7'd32	-8.5	7'd64	-11.7	7'd96	-14.9
7'd1	-5.4	7'd33	-8.6	7'd65	-11.8	7'd97	-15
7'd2	-5.5	7'd34	-8.7	7'd66	-11.9	7'd98	-15.1
7'd3	-5.6	7'd35	-8.8	7'd67	-12	7'd99	-15.2
7'd4	-5.7	7'd36	-8.9	7'd68	-12.1	7'd100	-15.3
7'd5	-5.8	7'd37	-9	7'd69	-12.2	7'd101	-15.4
7'd6	-5.9	7'd38	-9.1	7'd70	-12.3	7'd102	-15.5
7'd7	-6	7'd39	-9.2	7'd71	-12.4	7'd103	-15.6
7'd8	-6.1	7'd40	-9.3	7'd72	-12.5	7'd104	-15.7
7'd9	-6.2	7'd41	-9.4	7'd73	-12.6	7'd105	-15.8
7'd10	-6.3	7'd42	-9.5	7'd74	-12.7	7'd106	-15.9
7'd11	-6.4	7'd43	-9.6	7'd75	-12.8	7'd107	-16
7'd12	-6.5	7'd44	-9.7	7'd76	-12.9	7'd108	-16.1
7'd13	-6.6	7'd45	-9.8	7'd77	-13	7'd109	-16.2
7'd14	-6.7	7'd46	-9.9	7'd78	-13.1	7'd110	-16.3
7'd15	-6.8	7'd47	-10	7'd79	-13.2	7'd111	-16.4
7'd16	-6.9	7'd48	-10.1	7'd80	-13.3	7'd112	-16.5
7'd17	-7	7'd49	-10.2	7'd81	-13.4	7'd113	-16.6
7'd18	-7.1	7'd50	-10.3	7'd82	-13.5	7'd114	-16.7
7'd19	-7.2	7'd51	-10.4	7'd83	-13.6	7'd115	-16.8
7'd20	-7.3	7'd52	-10.5	7'd84	-13.7	7'd116	-16.9
7'd21	-7.4	7'd53	-10.6	7'd85	-13.8	7'd117	-17
7'd22	-7.5	7'd54	-10.7	7'd86	-13.9	7'd118	-17.1
7'd23	-7.6	7'd55	-10.8	7'd87	-14	7'd119	-17.2
7'd24	-7.7	7'd56	-10.9	7'd88	-14.1	7'd120	-17.3
7'd25	-7.8	7'd57	-11	7'd89	-14.2	7'd121	-17.4
7'd26	-7.9	7'd58	-11.1	7'd90	-14.3	7'd122	-17.5
7'd27	-8	7'd59	-11.2	7'd91	-14.4	7'd123	-17.6
7'd28	-8.1	7'd60	-11.3	7'd92	-14.5	7'd124	-17.7

7'd29	-8.2	7'd61	-11.4	7'd93	-14.6	7'd125	-17.8
7'd30	-8.3	7'd62	-11.5	7'd94	-14.7	7'd126	-17.9
7'd31	-8.4	7'd63	-11.6	7'd95	-14.8	7'd127	-18

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**2.3.15 VGHOVGLO\_SET (BANK09H 99H~9DH) : VGHO2/VGHO1/VGLO2/VGLO1 Voltage Setting**

Bank09H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
99H	HVREG_V GHO2_SEL [0]	PUMP_PUMP5_CLAMP[6:0]							C3h
9AH	HVREG_V GHO2_OFF _SET[0]	HVREG_V GHO2_ON _SET	HVREG_VGHO2_SEL[6:1]						
9BH	HVREG_TP_SEL_R[1:0]		HVREG_TP_SEL[2:0]			Internal Used		HVREG_VG HO2_OFF_ SET[1]	02h
9CH	HVREG_VGLO2_SEL[6:0]								HVREG_TP SEL_R[2]
9DH	Reserved	VGLO_SE L	VGHO_S EL	Internal Used		HVREG_VGLO2_OFF_S ET[1:0]	HVREG_VG LO2_ON_S ET		8Bh

Description							
- BANK09H 99H, D[7] ~ 9DH, D[2:0]							
HVREG_VGHO2_SEL : VGHO2 voltage setting							
HVREG_VGHO2_SEL[6:0]							
CODE(DEC)	Voltage(V)	CODE(DEC)	Voltage(V)	CODE(DEC)	Voltage(V)	CODE(DEC)	Voltage(V)
0	7.3	20	10.5	40	13.7	60	16.9
1	7.4	21	10.6	41	13.8	61	17
2	7.5	22	10.7	42	13.9	62	17.1
3	7.6	23	10.8	43	14	63	17.2
4	7.7	24	10.9	44	14.1	64	17.3
5	7.8	25	11	45	14.2	65	17.4
6	7.9	26	11.1	46	14.3	66	17.5
7	8	27	11.2	47	14.4	67	17.6
8	8.1	28	11.3	48	14.5	68	17.7
9	8.2	29	11.4	49	14.6	69	17.8
0A	8.3	2A	11.5	4A	14.7	6A	17.9
0B	8.4	2B	11.6	4B	14.8	6B	18
0C	8.5	2C	11.7	4C	14.9	6C	18.1
0D	8.6	2D	11.8	4D	15	6D	18.2
0E	8.7	2E	11.9	4E	15.1	6E	18.3
0F	8.8	2F	12	4F	15.2	6F	18.4
10	8.9	30	12.1	50	15.3	70	18.5

11	9	31	12.2	51	15.4	71	18.6
12	9.1	32	12.3	52	15.5	72	18.7
13	9.2	33	12.4	53	15.6	73	18.8
14	9.3	34	12.5	54	15.7	74	18.9
15	9.4	35	12.6	55	15.8	75	19
16	9.5	36	12.7	56	15.9	76	19.1
17	9.6	37	12.8	57	16	77	19.2
18	9.7	38	12.9	58	16.1	78	19.3
19	9.8	39	13	59	16.2	79	19.4
1A	9.9	3A	13.1	5A	16.3	7A	19.5
1B	10	3B	13.2	5B	16.4	7B	19.6
1C	10.1	3C	13.3	5C	16.5	7C	19.7
1D	10.2	3D	13.4	5D	16.6	7D	19.8
1E	10.3	3E	13.5	5E	16.7	7E	19.9
1F	10.4	3F	13.6	5F	16.8	7F	20

HVREG\_VGHO2\_ON\_SET : VGHO2 Enable voltage setting

0 : VGHO2 = VGH

1: VGHO2 = VGHO2

HVREG\_VGHO2\_OFF\_SET : VGHO2 Disable voltage setting

00 : VGHO2 = GND

01 : VGHO2 = Hi-Z

10 : VGHO2 = VGH

11 : VGHO2 = VGH

HVREG\_TP\_SEL : VGHO Delta voltage setting

HVREG_VGHO_TP_SEL[2:0]	VGHO2-VGHO1
000	1.5V
001	2V
010	2.5V
011	3V
100	3.5V
101	4V
110	4.5V
111	5V

HVREG\_TP\_SEL\_R : VGLO Delta voltage setting

HVREG_VGHL_TP_SEL[2:0]	VGLO2-VGLO1
000	1.5V
001	2V
010	2.5V
011	3V
100	3.5V
101	4V
110	4.5V
111	5V

HVREG\_VGLO2\_SEL : VGLO2 voltage setting

HVREG_VGLO2_SEL[6:0]							
CODE(DEC)	Voltage(V)	CODE(DEC)	Voltage(V)	CODE(DEC)	Voltage(V)	CODE(DEC)	Voltage(V)
0	-5.3	20	-8.5	40	-11.7	60	-14.9
1	-5.4	21	-8.6	41	-11.8	61	-15
2	-5.5	22	-8.7	42	-11.9	62	-15.1
3	-5.6	23	-8.8	43	-12	63	-15.2
4	-5.7	24	-8.9	44	-12.1	64	-15.3
5	-5.8	25	-9	45	-12.2	65	-15.4
6	-5.9	26	-9.1	46	-12.3	66	-15.5
7	-6	27	-9.2	47	-12.4	67	-15.6
8	-6.1	28	-9.3	48	-12.5	68	-15.7
9	-6.2	29	-9.4	49	-12.6	69	-15.8
0A	-6.3	2A	-9.5	4A	-12.7	6A	-15.9
0B	-6.4	2B	-9.6	4B	-12.8	6B	-16
0C	-6.5	2C	-9.7	4C	-12.9	6C	-16.1
0D	-6.6	2D	-9.8	4D	-13	6D	-16.2
0E	-6.7	2E	-9.9	4E	-13.1	6E	-16.3
0F	-6.8	2F	-10	4F	-13.2	6F	-16.4
10	-6.9	30	-10.1	50	-13.3	70	-16.5
11	-7	31	-10.2	51	-13.4	71	-16.6
12	-7.1	32	-10.3	52	-13.5	72	-16.7
13	-7.2	33	-10.4	53	-13.6	73	-16.8
14	-7.3	34	-10.5	54	-13.7	74	-16.9
15	-7.4	35	-10.6	55	-13.8	75	-17
16	-7.5	36	-10.7	56	-13.9	76	-17.1
17	-7.6	37	-10.8	57	-14	77	-17.2
18	-7.7	38	-10.9	58	-14.1	78	-17.3
19	-7.8	39	-11	59	-14.2	79	-17.4
1A	-7.9	3A	-11.1	5A	-14.3	7A	-17.5
1B	-8	3B	-11.2	5B	-14.4	7B	-17.6

1C	-8.1	3C	-11.3	5C	-14.5	7C	-17.7
1D	-8.2	3D	-11.4	5D	-14.6	7D	-17.8
1E	-8.3	3E	-11.5	5E	-14.7	7E	-17.9
1F	-8.4	3F	-11.6	5F	-14.8	7F	-18

HVREG\_VGLO2\_ON\_SET : VGLO2 Enable voltage setting

0 : VGLO2 = VGL

1: VGLO2 = VGLO2

HVREG\_VGLO2\_OFF\_SET : VGLO2 Disable voltage setting

00 : VGLO2 = GND

01 : VGLO2 = Hi-Z

10 : VGLO2 = VGL

11 : VGLO2 = VGL

VGHO\_SEL : VGHO selector ,

0--> VGHO=VGHO1

1-->VGHO=VGHO2

VGLO\_SEL : VGLO selector

0--> VGLO=VGLO1

1-->VGHO=VGLO2

**2.3.16 GVDDSET (BANK0AH 81H~83H) : GVDD/NGVDD Setting**

Bank0AH									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
81H	GVDD_VG[7:0]								FDh
82H	GVDD_NVG [6:0]								FAh
83H	Internal Used			Reserved		GVDD_NVG [8:7]		01h	

Description																	
- BANK0AH 81H, D[7:0] ~ 82H, D[0]																	
GVDD_VG[8:0] is used to set GVDD voltage																	
COD E	GVDD level	COD E	GVDD level	COD E	GVDD level	COD E	GVDD level	COD E	GVDD level	COD E	GVDD level	COD E	GVDD level	COD E	GVDD level	COD E	GVDD level
0	2.99	64	3.372	128	3.753	192	4.135	256	4.517	320	4.899	384	5.281	448	5.663		
1	2.996	65	3.377	129	3.759	193	4.141	257	4.523	321	4.905	385	5.287	449	5.669		
2	3.002	66	3.383	130	3.765	194	4.147	258	4.529	322	4.911	386	5.293	450	5.675		
3	3.008	67	3.389	131	3.771	195	4.153	259	4.535	323	4.917	387	5.299	451	5.681		
4	3.013	68	3.395	132	3.777	196	4.159	260	4.541	324	4.923	388	5.305	452	5.687		
5	3.019	69	3.401	133	3.783	197	4.165	261	4.547	325	4.929	389	5.311	453	5.693		
6	3.025	70	3.407	134	3.789	198	4.171	262	4.553	326	4.935	390	5.317	454	5.699		
7	3.031	71	3.413	135	3.795	199	4.177	263	4.559	327	4.941	391	5.323	455	5.705		
8	3.037	72	3.419	136	3.801	200	4.183	264	4.565	328	4.947	392	5.329	456	5.711		
9	3.043	73	3.425	137	3.807	201	4.189	265	4.571	329	4.953	393	5.335	457	5.717		
10	3.049	74	3.431	138	3.813	202	4.195	266	4.577	330	4.959	394	5.341	458	5.723		
11	3.055	75	3.437	139	3.819	203	4.201	267	4.583	331	4.965	395	5.347	459	5.729		
12	3.061	76	3.443	140	3.825	204	4.207	268	4.589	332	4.971	396	5.353	460	5.735		
13	3.067	77	3.449	141	3.831	205	4.213	269	4.595	333	4.977	397	5.359	461	5.741		
14	3.073	78	3.455	142	3.837	206	4.219	270	4.601	334	4.983	398	5.365	462	5.746		
15	3.079	79	3.461	143	3.843	207	4.225	271	4.607	335	4.989	399	5.371	463	5.752		
16	3.085	80	3.467	144	3.849	208	4.231	272	4.613	336	4.995	400	5.377	464	5.758		
17	3.091	81	3.473	145	3.855	209	4.237	273	4.619	337	5.001	401	5.382	465	5.764		
18	3.097	82	3.479	146	3.861	210	4.243	274	4.625	338	5.007	402	5.388	466	5.77		
19	3.103	83	3.485	147	3.867	211	4.249	275	4.631	339	5.013	403	5.394	467	5.776		
20	3.109	84	3.491	148	3.873	212	4.255	276	4.637	340	5.018	404	5.4	468	5.782		
21	3.115	85	3.497	149	3.879	213	4.261	277	4.643	341	5.024	405	5.406	469	5.788		
22	3.121	86	3.503	150	3.885	214	4.267	278	4.649	342	5.03	406	5.412	470	5.794		
23	3.127	87	3.509	151	3.891	215	4.273	279	4.654	343	5.036	407	5.418	471	5.8		
24	3.133	88	3.515	152	3.897	216	4.279	280	4.66	344	5.042	408	5.424	472	5.806		
25	3.139	89	3.521	153	3.903	217	4.285	281	4.666	345	5.048	409	5.43	473	5.812		
26	3.145	90	3.527	154	3.909	218	4.29	282	4.672	346	5.054	410	5.436	474	5.818		

27	3.151	91	3.533	155	3.915	219	4.296	283	4.678	347	5.06	411	5.442	475	5.824
28	3.157	92	3.539	156	3.921	220	4.302	284	4.684	348	5.066	412	5.448	476	5.83
29	3.163	93	3.545	157	3.926	221	4.308	285	4.69	349	5.072	413	5.454	477	5.836
30	3.169	94	3.551	158	3.932	222	4.314	286	4.696	350	5.078	414	5.46	478	5.842
31	3.175	95	3.556	159	3.938	223	4.32	287	4.702	351	5.084	415	5.466	479	5.848
32	3.181	96	3.562	160	3.944	224	4.326	288	4.708	352	5.09	416	5.472	480	5.854
33	3.187	97	3.568	161	3.95	225	4.332	289	4.714	353	5.096	417	5.478	481	5.86
34	3.192	98	3.574	162	3.956	226	4.338	290	4.72	354	5.102	418	5.484	482	5.866
35	3.198	99	3.58	163	3.962	227	4.344	291	4.726	355	5.108	419	5.49	483	5.872
36	3.204	100	3.586	164	3.968	228	4.35	292	4.732	356	5.114	420	5.496	484	5.878
37	3.21	101	3.592	165	3.974	229	4.356	293	4.738	357	5.12	421	5.502	485	5.884
38	3.216	102	3.598	166	3.98	230	4.362	294	4.744	358	5.126	422	5.508	486	5.89
39	3.222	103	3.604	167	3.986	231	4.368	295	4.75	359	5.132	423	5.514	487	5.896
40	3.228	104	3.61	168	3.992	232	4.374	296	4.756	360	5.138	424	5.52	488	5.902
41	3.234	105	3.616	169	3.998	233	4.38	297	4.762	361	5.144	425	5.526	489	5.908
42	3.24	106	3.622	170	4.004	234	4.386	298	4.768	362	5.15	426	5.532	490	5.914
43	3.246	107	3.628	171	4.01	235	4.392	299	4.774	363	5.156	427	5.538	491	5.92
44	3.252	108	3.634	172	4.016	236	4.398	300	4.78	364	5.162	428	5.544	492	5.926
45	3.258	109	3.64	173	4.022	237	4.404	301	4.786	365	5.168	429	5.55	493	5.931
46	3.264	110	3.646	174	4.028	238	4.41	302	4.792	366	5.174	430	5.556	494	5.937
47	3.27	111	3.652	175	4.034	239	4.416	303	4.798	367	5.18	431	5.562	495	5.943
48	3.276	112	3.658	176	4.04	240	4.422	304	4.804	368	5.186	432	5.567	496	5.949
49	3.282	113	3.664	177	4.046	241	4.428	305	4.81	369	5.192	433	5.573	497	5.955
50	3.288	114	3.67	178	4.052	242	4.434	306	4.816	370	5.198	434	5.579	498	5.961
51	3.294	115	3.676	179	4.058	243	4.44	307	4.822	371	5.203	435	5.585	499	5.967
52	3.3	116	3.682	180	4.064	244	4.446	308	4.828	372	5.209	436	5.591	500	5.973
53	3.306	117	3.688	181	4.07	245	4.452	309	4.833	373	5.215	437	5.597	501	5.979
54	3.312	118	3.694	182	4.076	246	4.458	310	4.839	374	5.221	438	5.603	502	5.985
55	3.318	119	3.7	183	4.082	247	4.464	311	4.845	375	5.227	439	5.609	503	5.991
56	3.324	120	3.706	184	4.088	248	4.469	312	4.851	376	5.233	440	5.615	504	5.997
57	3.33	121	3.712	185	4.094	249	4.475	313	4.857	377	5.239	441	5.621	505	6.003
58	3.336	122	3.718	186	4.1	250	4.481	314	4.863	378	5.245	442	5.627	506	6.009
59	3.342	123	3.724	187	4.105	251	4.487	315	4.869	379	5.251	443	5.633	507	6.015
60	3.348	124	3.73	188	4.111	252	4.493	316	4.875	380	5.257	444	5.639	508	6.021
61	3.354	125	3.736	189	4.117	253	4.499	317	4.881	381	5.263	445	5.645	509	6.027
62	3.36	126	3.741	190	4.123	254	4.505	318	4.887	382	5.269	446	5.651	510	6.033
63	3.366	127	3.747	191	4.129	255	4.511	319	4.893	383	5.275	447	5.657	511	6.039

- BANK0AH 82H, D[7:1] ~ 83H, D[1:0]

GVDD\_NVG[8:0] is used to set NGVDD voltage

COD E	NGVDD level																
0	-2.99	64	-3.372	128	-3.753	192	-4.135	256	-4.517	320	-4.899	384	-5.281	448	-5.663		
1	-2.996	65	-3.377	129	-3.759	193	-4.141	257	-4.523	321	-4.905	385	-5.287	449	-5.669		
2	-3.002	66	-3.383	130	-3.765	194	-4.147	258	-4.529	322	-4.911	386	-5.293	450	-5.675		
3	-3.008	67	-3.389	131	-3.771	195	-4.153	259	-4.535	323	-4.917	387	-5.299	451	-5.681		
4	-3.013	68	-3.395	132	-3.777	196	-4.159	260	-4.541	324	-4.923	388	-5.305	452	-5.687		
5	-3.019	69	-3.401	133	-3.783	197	-4.165	261	-4.547	325	-4.929	389	-5.311	453	-5.693		
6	-3.025	70	-3.407	134	-3.789	198	-4.171	262	-4.553	326	-4.935	390	-5.317	454	-5.699		
7	-3.031	71	-3.413	135	-3.795	199	-4.177	263	-4.559	327	-4.941	391	-5.323	455	-5.705		
8	-3.037	72	-3.419	136	-3.801	200	-4.183	264	-4.565	328	-4.947	392	-5.329	456	-5.711		
9	-3.043	73	-3.425	137	-3.807	201	-4.189	265	-4.571	329	-4.953	393	-5.335	457	-5.717		
10	-3.049	74	-3.431	138	-3.813	202	-4.195	266	-4.577	330	-4.959	394	-5.341	458	-5.723		
11	-3.055	75	-3.437	139	-3.819	203	-4.201	267	-4.583	331	-4.965	395	-5.347	459	-5.729		
12	-3.061	76	-3.443	140	-3.825	204	-4.207	268	-4.589	332	-4.971	396	-5.353	460	-5.735		
13	-3.067	77	-3.449	141	-3.831	205	-4.213	269	-4.595	333	-4.977	397	-5.359	461	-5.741		
14	-3.073	78	-3.455	142	-3.837	206	-4.219	270	-4.601	334	-4.983	398	-5.365	462	-5.746		
15	-3.079	79	-3.461	143	-3.843	207	-4.225	271	-4.607	335	-4.989	399	-5.371	463	-5.752		
16	-3.085	80	-3.467	144	-3.849	208	-4.231	272	-4.613	336	-4.995	400	-5.377	464	-5.758		
17	-3.091	81	-3.473	145	-3.855	209	-4.237	273	-4.619	337	-5.001	401	-5.382	465	-5.764		
18	-3.097	82	-3.479	146	-3.861	210	-4.243	274	-4.625	338	-5.007	402	-5.388	466	-5.77		
19	-3.103	83	-3.485	147	-3.867	211	-4.249	275	-4.631	339	-5.013	403	-5.394	467	-5.776		
20	-3.109	84	-3.491	148	-3.873	212	-4.255	276	-4.637	340	-5.018	404	-5.4	468	-5.782		
21	-3.115	85	-3.497	149	-3.879	213	-4.261	277	-4.643	341	-5.024	405	-5.406	469	-5.788		
22	-3.121	86	-3.503	150	-3.885	214	-4.267	278	-4.649	342	-5.03	406	-5.412	470	-5.794		
23	-3.127	87	-3.509	151	-3.891	215	-4.273	279	-4.654	343	-5.036	407	-5.418	471	-5.8		
24	-3.133	88	-3.515	152	-3.897	216	-4.279	280	-4.66	344	-5.042	408	-5.424	472	-5.806		
25	-3.139	89	-3.521	153	-3.903	217	-4.285	281	-4.666	345	-5.048	409	-5.43	473	-5.812		
26	-3.145	90	-3.527	154	-3.909	218	-4.29	282	-4.672	346	-5.054	410	-5.436	474	-5.818		
27	-3.151	91	-3.533	155	-3.915	219	-4.296	283	-4.678	347	-5.06	411	-5.442	475	-5.824		
28	-3.157	92	-3.539	156	-3.921	220	-4.302	284	-4.684	348	-5.066	412	-5.448	476	-5.83		
29	-3.163	93	-3.545	157	-3.926	221	-4.308	285	-4.69	349	-5.072	413	-5.454	477	-5.836		
30	-3.169	94	-3.551	158	-3.932	222	-4.314	286	-4.696	350	-5.078	414	-5.46	478	-5.842		
31	-3.175	95	-3.556	159	-3.938	223	-4.32	287	-4.702	351	-5.084	415	-5.466	479	-5.848		
32	-3.181	96	-3.562	160	-3.944	224	-4.326	288	-4.708	352	-5.09	416	-5.472	480	-5.854		
33	-3.187	97	-3.568	161	-3.95	225	-4.332	289	-4.714	353	-5.096	417	-5.478	481	-5.86		
34	-3.192	98	-3.574	162	-3.956	226	-4.338	290	-4.72	354	-5.102	418	-5.484	482	-5.866		

35	-3.198	99	-3.58	163	-3.962	227	-4.344	291	-4.726	355	-5.108	419	-5.49	483	-5.872
36	-3.204	100	-3.586	164	-3.968	228	-4.35	292	-4.732	356	-5.114	420	-5.496	484	-5.878
37	-3.21	101	-3.592	165	-3.974	229	-4.356	293	-4.738	357	-5.12	421	-5.502	485	-5.884
38	-3.216	102	-3.598	166	-3.98	230	-4.362	294	-4.744	358	-5.126	422	-5.508	486	-5.89
39	-3.222	103	-3.604	167	-3.986	231	-4.368	295	-4.75	359	-5.132	423	-5.514	487	-5.896
40	-3.228	104	-3.61	168	-3.992	232	-4.374	296	-4.756	360	-5.138	424	-5.52	488	-5.902
41	-3.234	105	-3.616	169	-3.998	233	-4.38	297	-4.762	361	-5.144	425	-5.526	489	-5.908
42	-3.24	106	-3.622	170	-4.004	234	-4.386	298	-4.768	362	-5.15	426	-5.532	490	-5.914
43	-3.246	107	-3.628	171	-4.01	235	-4.392	299	-4.774	363	-5.156	427	-5.538	491	-5.92
44	-3.252	108	-3.634	172	-4.016	236	-4.398	300	-4.78	364	-5.162	428	-5.544	492	-5.926
45	-3.258	109	-3.64	173	-4.022	237	-4.404	301	-4.786	365	-5.168	429	-5.55	493	-5.931
46	-3.264	110	-3.646	174	-4.028	238	-4.41	302	-4.792	366	-5.174	430	-5.556	494	-5.937
47	-3.27	111	-3.652	175	-4.034	239	-4.416	303	-4.798	367	-5.18	431	-5.562	495	-5.943
48	-3.276	112	-3.658	176	-4.04	240	-4.422	304	-4.804	368	-5.186	432	-5.567	496	-5.949
49	-3.282	113	-3.664	177	-4.046	241	-4.428	305	-4.81	369	-5.192	433	-5.573	497	-5.955
50	-3.288	114	-3.67	178	-4.052	242	-4.434	306	-4.816	370	-5.198	434	-5.579	498	-5.961
51	-3.294	115	-3.676	179	-4.058	243	-4.44	307	-4.822	371	-5.203	435	-5.585	499	-5.967
52	-3.3	116	-3.682	180	-4.064	244	-4.446	308	-4.828	372	-5.209	436	-5.591	500	-5.973
53	-3.306	117	-3.688	181	-4.07	245	-4.452	309	-4.833	373	-5.215	437	-5.597	501	-5.979
54	-3.312	118	-3.694	182	-4.076	246	-4.458	310	-4.839	374	-5.221	438	-5.603	502	-5.985
55	-3.318	119	-3.7	183	-4.082	247	-4.464	311	-4.845	375	-5.227	439	-5.609	503	-5.991
56	-3.324	120	-3.706	184	-4.088	248	-4.469	312	-4.851	376	-5.233	440	-5.615	504	-5.997
57	-3.33	121	-3.712	185	-4.094	249	-4.475	313	-4.857	377	-5.239	441	-5.621	505	-6.003
58	-3.336	122	-3.718	186	-4.1	250	-4.481	314	-4.863	378	-5.245	442	-5.627	506	-6.009
59	-3.342	123	-3.724	187	-4.105	251	-4.487	315	-4.869	379	-5.251	443	-5.633	507	-6.015
60	-3.348	124	-3.73	188	-4.111	252	-4.493	316	-4.875	380	-5.257	444	-5.639	508	-6.021
61	-3.354	125	-3.736	189	-4.117	253	-4.499	317	-4.881	381	-5.263	445	-5.645	509	-6.027
62	-3.36	126	-3.741	190	-4.123	254	-4.505	318	-4.887	382	-5.269	446	-5.651	510	-6.033
63	-3.366	127	-3.747	191	-4.129	255	-4.511	319	-4.893	383	-5.275	447	-5.657	511	-6.039

**2.3.17 AGMMA (BANK0AH 84H~ABH) : Gamma Correction Characteristics Setting**

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
84H					GAMMA_VR1V0P [7:0]				1Dh
85H					GAMMA_VR1V2P [7:0]				22h
86H					GAMMA_VR1V4P [7:0]				28h
87H					GAMMA_VR1V7P [7:0]				36h
88H					GAMMA_VR1V11P [7:0]				47h
89H					GAMMA_VR1V16P [7:0]				58h
8AH					GAMMA_VR1V24P [7:0]				5Eh
8BH					GAMMA_VR1V52P [7:0]				8Fh
8CH					GAMMA_VR1V80P [7:0]				71h
8DH					GAMMA_VR1V112P [7:0]				AFh
8EH					GAMMA_VR1V143P [7:0]				86h
8FH					GAMMA_VR1V175P [7:0]				53h
90H					GAMMA_VR1V203P [7:0]				85h
91H					GAMMA_VR1V231P [7:0]				56h
92H					GAMMA_VR1V239P [7:0]				54h
93H					GAMMA_VR1V244P [7:0]				45h
94H					GAMMA_VR1V248P [7:0]				36h
95H					GAMMA_VR1V251P [7:0]				28h
96H					GAMMA_VR1V253P [7:0]				1Bh
97H					GAMMA_VR1V255P [7:0]				0Bh
98H					GAMMA_VR1V0N [7:0]				1Dh
99H					GAMMA_VR1V2N [7:0]				22h
9AH					GAMMA_VR1V4N [7:0]				28h
9BH					GAMMA_VR1V7N [7:0]				36h
9CH					GAMMA_VR1V11N [7:0]				47h
9DH					GAMMA_VR1V16N [7:0]				58h
9EH					GAMMA_VR1V24N [7:0]				5Eh
9FH					GAMMA_VR1V52N [7:0]				8Fh
A0H					GAMMA_VR1V80N [7:0]				71h
A1H					GAMMA_VR1V112N [7:0]				AFh
A2H					GAMMA_VR1V143N [7:0]				86h
A3H					GAMMA_VR1V175N [7:0]				53h
A4H					GAMMA_VR1V203N [7:0]				85h
A5H					GAMMA_VR1V231N [7:0]				56h
A6H					GAMMA_VR1V239N [7:0]				54h
A7H					GAMMA_VR1V244N [7:0]				45h
A8H					GAMMA_VR1V248N [7:0]				36h
A9H					GAMMA_VR1V251N [7:0]				28h
AAH					GAMMA_VR1V253N [7:0]				1Bh
ABH					GAMMA_VR1V255N [7:0]				0Bh

Description
- BANK0AH 84H, D[7:0] GAMMA_VR1V0P [7:0] is used to adjust V0P.
- BANK0AH 85H, D[7:0] GAMMA_VR1V2P [7:0] is used to adjust V2P.
- BANK0AH 86H, D[7:0] GAMMA_VR1V4P [7:0] is used to adjust V4P.
- BANK0AH 87H, D[7:0] GAMMA_VR1V7P [7:0] is used to adjust V7P.
- BANK0AH 88H, D[7:0] GAMMA_VR1V11P [7:0] is used to adjust V11P.
- BANK0AH 89H, D[7:0] GAMMA_VR1V16P [7:0] is used to adjust V16P.
- BANK0AH 8AH, D[7:0] GAMMA_VR1V24P [7:0] is used to adjust V24P.
- BANK0AH 8BH, D[7:0] GAMMA_VR1V52P [7:0] is used to adjust V52P.
- BANK0AH 8CH, D[7:0] GAMMA_VR1V80P [7:0] is used to adjust V80P.
- BANK0AH 8DH, D[7:0] GAMMA_VR1V112P [7:0] is used to adjust V112P.
- BANK0AH 8EH, D[7:0] GAMMA_VR1V143P [7:0] is used to adjust V143P.
- BANK0AH 8FH, D[7:0] GAMMA_VR1V175P [7:0] is used to adjust V175P.
- BANK0AH 90H, D[7:0] GAMMA_VR1V203P [7:0] is used to adjust V203P.
- BANK0AH 91H, D[7:0] GAMMA_VR1V231P [7:0] is used to adjust V231P.
- BANK0AH 92H, D[7:0] GAMMA_VR1V239P [7:0] is used to adjust V239P.
- BANK0AH 93H, D[7:0] GAMMA_VR1V244P [7:0] is used to adjust V244P.
- BANK0AH 94H, D[7:0] GAMMA_VR1V248P [7:0] is used to adjust V248P.
- BANK0AH 95H, D[7:0] GAMMA_VR1V251P [7:0] is used to adjust V251P.
- BANK0AH 96H, D[7:0] GAMMA_VR1V253P [7:0] is used to adjust V253P.
- BANK0AH 97H, D[7:0] GAMMA_VR1V255P [7:0] is used to adjust V255P.
- BANK0AH 98H, D[7:0] GAMMA_VR1V0N [7:0] is used to adjust V0N.
- BANK0AH 99H, D[7:0] GAMMA_VR1V2N [7:0] is used to adjust V2N.
- BANK0AH 9AH, D[7:0] GAMMA_VR1V4N [7:0] is used to adjust V4N.

- BANK0AH 9BH, D[7:0]  
GAMMA\_VR1V7N [7:0] is used to adjust V7N.

- BANK0AH 9CH, D[7:0]  
GAMMA\_VR1V11N [7:0] is used to adjust V11N.

- BANK0AH 9DH, D[7:0]  
GAMMA\_VR1V16N [7:0] is used to adjust V16N.

- BANK0AH 9EH, D[7:0]  
GAMMA\_VR1V24N [7:0] is used to adjust V24N.

- BANK0AH 9FH, D[7:0]  
GAMMA\_VR1V52N [7:0] is used to adjust V52N.

- BANK0AH A0H, D[7:0]  
GAMMA\_VR1V80N [7:0] is used to adjust V80N.

- BANK0AH A1H, D[7:0]  
GAMMA\_VR1V112N [7:0] is used to adjust V112N.

- BANK0AH A2H, D[7:0]  
GAMMA\_VR1V143N [7:0] is used to adjust V143N.

- BANK0AH A3H, D[7:0]  
GAMMA\_VR1V175N [7:0] is used to adjust V175N.

- BANK0AH A4H, D[7:0]  
GAMMA\_VR1V203N [7:0] is used to adjust V203N.

- BANK0AH A5H, D[7:0]  
GAMMA\_VR1V231N [7:0] is used to adjust V231N.

- BANK0AH A6H, D[7:0]  
GAMMA\_VR1V239N [7:0] is used to adjust V239N.

- BANK0AH A7H, D[7:0]  
GAMMA\_VR1V244N [7:0] is used to adjust V244N.

- BANK0AH A8H, D[7:0]  
GAMMA\_VR1V248N [7:0] is used to adjust V248N.

- BANK0AH A9H, D[7:0]  
GAMMA\_VR1V251N [7:0] is used to adjust V251N.

- BANK0AH AAH, D[7:0]  
GAMMA\_VR1V253N [7:0] is used to adjust V253N.

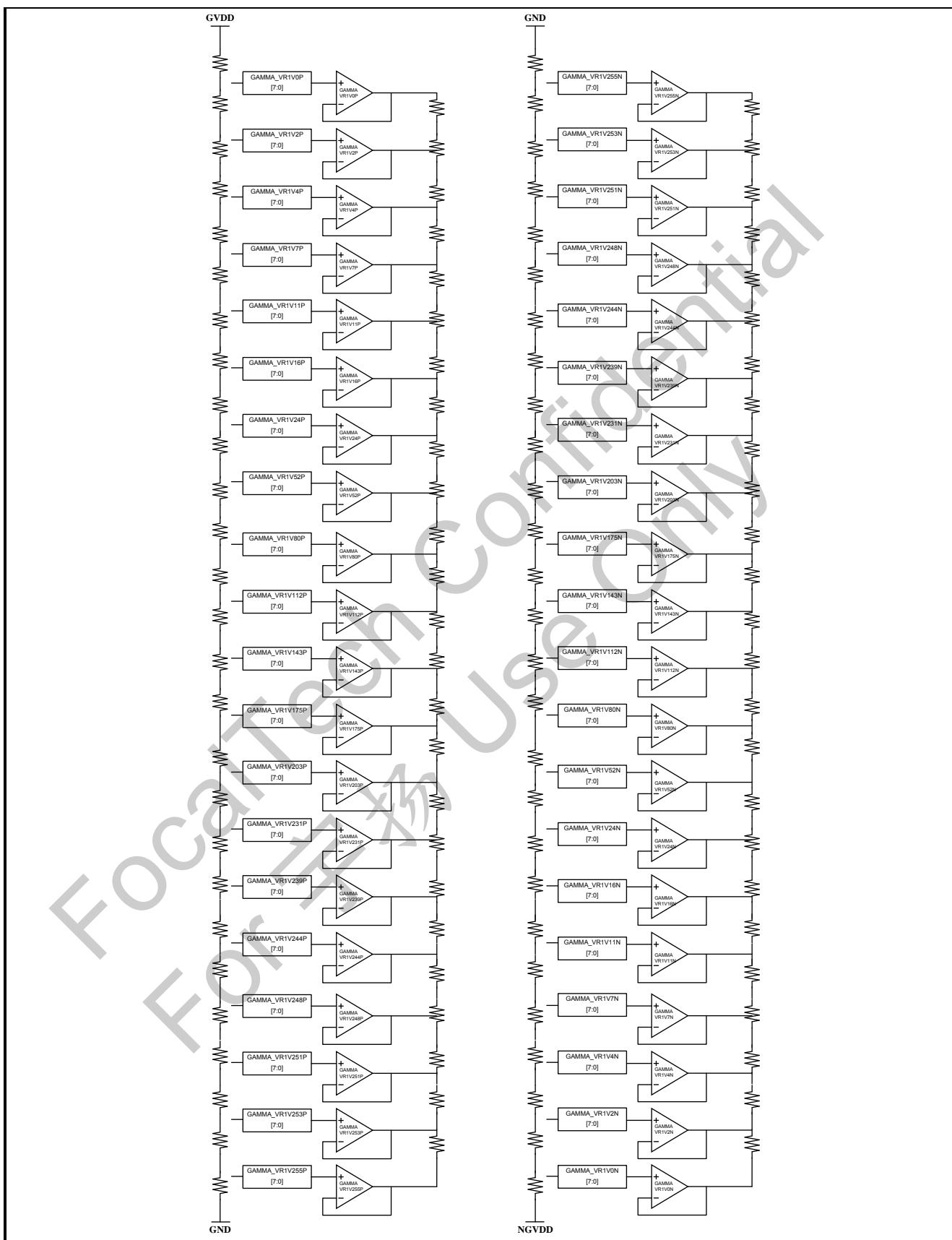
- BANK0AH ABH, D[7:0]  
GAMMA\_VR1V255N [7:0] is used to adjust V255N.

The following table is the example of default setting when GVDD = 5.20V, NGVDD = -5.20V,

Note: Please contact with Focal-tech for the Analog GAMMA table requirement.

GAMMA Point	Adjust Voltage	GAMMA Point	Adjust Voltage
GAMMA_VR1V0P	4.864V	GAMMA_VR1V0N	-4.921V
GAMMA_VR1V2P	4.649V	GAMMA_VR1V2N	-4.604V
GAMMA_VR1V4P	4.446V	GAMMA_VR1V4N	-4.446V
GAMMA_VR1V7P	4.323V	GAMMA_VR1V7N	-4.323V

GAMMA_VR1V11P	4.129V	GAMMA_VR1V11N	-4.129V
GAMMA_VR1V16P	3.970V	GAMMA_VR1V16N	-3.970V
GAMMA_VR1V24P	3.744V	GAMMA_VR1V24N	-3.744V
GAMMA_VR1V52P	3.213V	GAMMA_VR1V52N	-3.213V
GAMMA_VR1V80P	2.896V	GAMMA_VR1V80N	-2.896V
GAMMA_VR1V112P	2.602V	GAMMA_VR1V112N	-2.602V
GAMMA_VR1V143P	2.370V	GAMMA_VR1V143P	-2.370V
GAMMA_VR1V175P	2.110V	GAMMA_VR1V175P	-2.110V
GAMMA_VR1V203P	1.833V	GAMMA_VR1V203P	-1.833V
GAMMA_VR1V231P	1.357V	GAMMA_VR1V231P	-1.357V
GAMMA_VR1V239P	1.154V	GAMMA_VR1V239P	-1.154V
GAMMA_VR1V244P	0.939V	GAMMA_VR1V244P	-0.939V
GAMMA_VR1V248P	0.747V	GAMMA_VR1V248P	-0.747V
GAMMA_VR1V251P	0.543V	GAMMA_VR1V251P	-0.543V
GAMMA_VR1V253P	0.396V	GAMMA_VR1V253P	-0.396V
GAMMA_VR1V255P	0.215V	GAMMA_VR1V255P	-0.215V



**2.3.18 MIPI\_Set (BANK0BH 87H, BANK0DH 80H) : MIPI Parameters Setting**

Bank0BH									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
87H	Reserved	Internal Used	MIPI_POL	MIPI_LAN_SWAP[1:0]		Internal Used			47h
Bank0DH									
80H		Internal Used		Reserved		MIPI_LAN_SEL[1:0]			F0h

Description																																																																																																																	
- BANK 0BH 87H, D[4:3]																																																																																																																	
MIPI_LAN_SWAP[1:0] : MIPI Lane Swap Setting																																																																																																																	
- BANK 0BH 87H, D[5]																																																																																																																	
MIPI_POL[1:0] : MIPI Polarity Setting																																																																																																																	
<table border="1"> <thead> <tr> <th>PSWAP</th> <th>DSWAP[1:0]</th> <th>DSI-D2+</th> <th>DSI-D2-</th> <th>DSI-D1+</th> <th>DSI-D1-</th> <th>DSI-CLK+</th> <th>DSI-CLK-</th> <th>DSI-D0+</th> <th>DSI-D0-</th> <th>DSI-D3+</th> <th>DSI-D3-</th> </tr> </thead> <tbody> <tr> <td rowspan="4">0</td> <td>00</td> <td>D3-</td> <td>D3+</td> <td>D2-</td> <td>D2+</td> <td>CLK-</td> <td>CLK+</td> <td>D1-</td> <td>D1+</td> <td>D0-</td> <td>D0+</td> </tr> <tr> <td>01</td> <td>D3-</td> <td>D3+</td> <td>D0-</td> <td>D0+</td> <td>CLK-</td> <td>CLK+</td> <td>D1-</td> <td>D1+</td> <td>D2-</td> <td>D2+</td> </tr> <tr> <td>10</td> <td>D0-</td> <td>D0+</td> <td>D1-</td> <td>D1+</td> <td>CLK-</td> <td>CLK+</td> <td>D2-</td> <td>D2+</td> <td>D3-</td> <td>D3+</td> </tr> <tr> <td>11</td> <td>D2-</td> <td>D2+</td> <td>D1-</td> <td>D1+</td> <td>CLK-</td> <td>CLK+</td> <td>D0-</td> <td>D0+</td> <td>D3-</td> <td>D3+</td> </tr> <tr> <td rowspan="4">1</td> <td>00</td> <td>D3+</td> <td>D3-</td> <td>D2+</td> <td>D2-</td> <td>CLK+</td> <td>CLK-</td> <td>D1+</td> <td>D1-</td> <td>D0+</td> <td>D0-</td> </tr> <tr> <td>01</td> <td>D3+</td> <td>D3-</td> <td>D0+</td> <td>D0-</td> <td>CLK+</td> <td>CLK-</td> <td>D1+</td> <td>D1-</td> <td>D2+</td> <td>D2-</td> </tr> <tr> <td>10</td> <td>D0+</td> <td>D0-</td> <td>D1+</td> <td>D1-</td> <td>CLK+</td> <td>CLK-</td> <td>D2-</td> <td>D2+</td> <td>D3+</td> <td>D3-</td> </tr> <tr> <td>11</td> <td>D2+</td> <td>D2-</td> <td>D1+</td> <td>D1-</td> <td>CLK+</td> <td>CLK-</td> <td>D0+</td> <td>D0-</td> <td>D3+</td> <td>D3-</td> </tr> </tbody> </table>												PSWAP	DSWAP[1:0]	DSI-D2+	DSI-D2-	DSI-D1+	DSI-D1-	DSI-CLK+	DSI-CLK-	DSI-D0+	DSI-D0-	DSI-D3+	DSI-D3-	0	00	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+	01	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+	10	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+	11	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+	1	00	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-	01	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-	10	D0+	D0-	D1+	D1-	CLK+	CLK-	D2-	D2+	D3+	D3-	11	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-
PSWAP	DSWAP[1:0]	DSI-D2+	DSI-D2-	DSI-D1+	DSI-D1-	DSI-CLK+	DSI-CLK-	DSI-D0+	DSI-D0-	DSI-D3+	DSI-D3-																																																																																																						
0	00	D3-	D3+	D2-	D2+	CLK-	CLK+	D1-	D1+	D0-	D0+																																																																																																						
	01	D3-	D3+	D0-	D0+	CLK-	CLK+	D1-	D1+	D2-	D2+																																																																																																						
	10	D0-	D0+	D1-	D1+	CLK-	CLK+	D2-	D2+	D3-	D3+																																																																																																						
	11	D2-	D2+	D1-	D1+	CLK-	CLK+	D0-	D0+	D3-	D3+																																																																																																						
1	00	D3+	D3-	D2+	D2-	CLK+	CLK-	D1+	D1-	D0+	D0-																																																																																																						
	01	D3+	D3-	D0+	D0-	CLK+	CLK-	D1+	D1-	D2+	D2-																																																																																																						
	10	D0+	D0-	D1+	D1-	CLK+	CLK-	D2-	D2+	D3+	D3-																																																																																																						
	11	D2+	D2-	D1+	D1-	CLK+	CLK-	D0+	D0-	D3+	D3-																																																																																																						

Note:

MIPI polarity and lane swap selection can be set via IO PAD and register parameter. The finally result is decided by the "XOR" logic operation of both.

EX:

$$\begin{aligned} \text{PSWAP} &= \text{reg\_MIPI\_POL} \quad (\text{XOR}) \quad \text{io\_PSWAP} \\ \text{DSWAP}[1:0] &= \text{reg\_MIPI\_LAN\_SWAP}[1:0] \quad (\text{XOR}) \quad \text{io\_DSWAP}[1:0] \end{aligned}$$

- BANK 0DH 80H, D[1:0]

MIPI\_LAN\_SEL[1:0] : MIPI Lane Number Selection

LANSEL[1:0]	Interface Selection
00	Reserved
01	MIPI-2 Lane
10	MIPI-3 Lane
11	MIPI-4 Lane

Note:

MIPI lane selection can be set via IO PAD and register parameter. The finally result is decided by the "XOR" logic operation of both.

EX: LANSEL[1:0] = reg\_MIPI\_LAN\_SEL[1:0] (XOR) io\_LANSEL[1:0]

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**2.3.19 LCD\_System\_Set (BANK0CH 80H) : LCD System parameter setting**

Bank0CH									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
80H	Internal Used					Reserved	UPDN	CRL	FAh

Description
- BANK CH 80H, D[1:0]
CRL:
1'b0: IC on bottom side ( left to right )
1'b1: IC on top side ( right to left )
UPDN:
1'b1: Screen Up to down
1'b0: Screen Down to up

### 2.3.20 Resolution\_Set (BANK0CH 81H~87H) : Resolution setting and blanking setting

Bank0CH										
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default	
81H	Hact[0]	Internal Used								68h
82H	Hact[8:1]								68h	
83H	Vact[4:0]					Hact[11:9]				01h
84H	Hblk[0]	Vact[11:5]								28h
85H	Hblk[8:1]								A0h	
86H	Vblk[4:0]					Hblk[11:9]				A0h
87H	Reserved	Vblk[11:5]								03h

Description	
- BANK CH 81H, D[7] ~ 87H ,D[6:0]	
Hact [11:0] use to set horizontal resolution	
Vact [11:0] use to set vertical resolution	
Support following resolution 720RGB x 1280, 720RGB x 1440, 720RGB x 1520, 720RGB x 1600	
Hblk [11:0] use to set H Blanking	
Vblk [11:0] use to set V Blanking	

**2.3.21 PWIC\_Set (BANK0EH 82H ~ 83h 87H) : PWIC parameter setting**

Bank0EH									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
82H	GPIO6_force_PWIC_Disable[7:0]								55h
83H	GPIO7_force_PWIC_Disable[7:0]								55h
87H	PWIC_Period[7:0]								1Ch

Description
GPIO6_force_PWIC_Disable[7:0] :
8'hAA: Disable force GPIO6 to output PWIC_P Other : Enable force GPIO6 to output PWIC_P
GPIO7_force_PWIC_Disable[7:0] :
8'hAA: Disable force GPIO7 to output PWIC_N Other : Enable force GPIO7 to output PWIC_N
PWIC_Period[7:0] :
PWIC_P / PWIC_N Period = 8.75Mhz / (PWIC_Period +1) Default 301KHz

**2.3.22 GPIO\_Set (BANK0EH 84H~86H) : GPIO output setting**

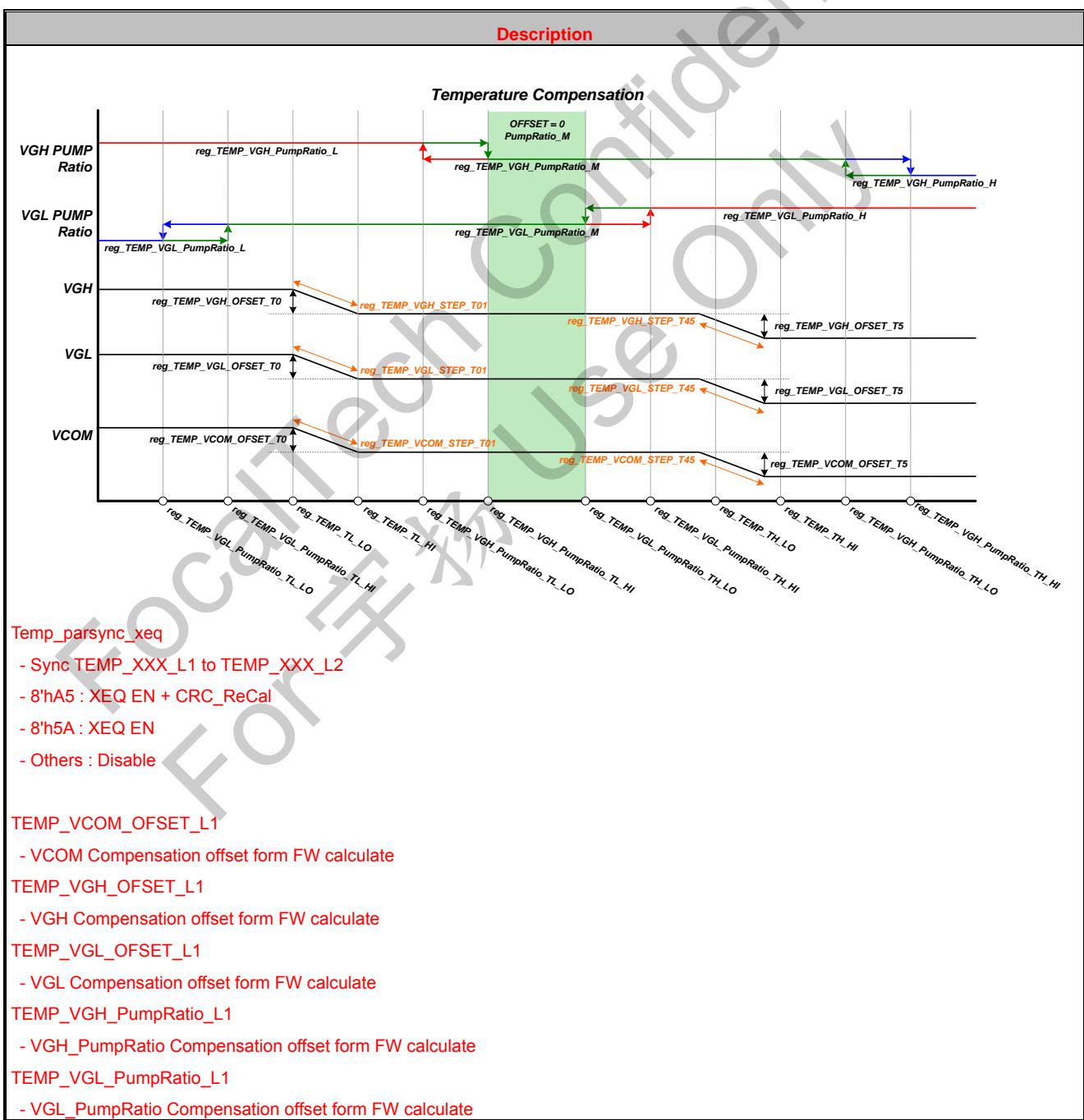
Bank0EH									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
84H								GPIO2_SEL[3:0]	21h
85H								GPIO4_SEL[3:0]	98h
86H								GPIO6_SEL[3:0]	76h

Description	
GPIO2_SEL[3:0] : GPIO2 signal selection	
GPIO3_SEL[3:0] : GPIO3 signal selection	
GPIO4_SEL[3:0] : GPIO4 signal selection	
GPIO5_SEL[3:0] : GPIO5 signal selection	
GPIO6_SEL[3:0] : GPIO6 signal selection	
GPIO7_SEL[3:0] : GPIO7 signal selection	
GPIO*_SEL[3:0]	
4'd1	
4'd2	
4'd3	
4'd4	
4'd6	
4'd7	
4'd8	
4'd9	
Others	

## 2.3.23 Temp\_Compensation (BANK12H 80H~A6H) : Temperature Compensation

BANK12H													
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default				
80H	Temp_parsync_xeq[7:0]								00h				
81H	TEMP_VCOM_OFSET_L1[7:0]								00h				
82H	Reserved								TEMP_VCOM_OFSET_L1[8]				
83H	Reserved	TEMP_VGH_OFSET_L1[6:0]											
84H	Reserved	TEMP_VGL_OFSET_L1[6:0]											
85H	Reserved								TEMP_VGH_PumpRatio_L1[1:0]				
86H	Reserved								TEMP_VGL_PumpRatio_L1[1:0]				
87H	TEMP_VCOM_OFSET_L2[7:0]								00h				
88H	Reserved								TEMP_VCOM_OFSET_L2[8]				
89H	Reserved	TEMP_VGH_OFSET_L2[6:0]											
8AH	Reserved	TEMP_VGL_OFSET_L2[6:0]											
8BH	Reserved								TEMP_VGH_PumpRatio_L2[1:0]				
8CH	Reserved								TEMP_VGL_PumpRatio_L2[1:0]				
8DH	Reserved					Internal Used	TEMP_CO_MP_EN	TEMP_SEN_SOR_EN	00h				
8EH	TEMP_TH_HI												
8FH	TEMP_TH_LO												
90H	TEMP_TL_HI												
91H	TEMP_TL_LO												
92H	TEMP_VCOM_OFSET_TH[7:0]												
93H	Reserved								TEMP_VCOM_OFSET_TH[8]				
94H	TEMP_VCOM_OFSET_TL[7:0]												
95H	Reserved								TEMP_VCOM_OFSET_TL[8]				
96H	TEMP_VCOM_STEP_TL[3:0]					TEMP_VCOM_STEP_TH[3:0]							
97H	Reserved	TEMP_VGH_OFSET_TH[6:0]											
98H	Reserved	TEMP_VGH_OFSET_TL[6:0]											
99H	TEMP_VGH_STEP_TL[3:0]					TEMP_VGH_STEP_TH[3:0]							
9AH	Reserved	TEMP_VGL_OFSET_TH[6:0]											
9BH	Reserved	TEMP_VGL_OFSET_TL[6:0]											
9CH	TEMP_VGL_STEP_TL[3:0]					TEMP_VGL_STEP_TH[3:0]							
9DH	TEMP_VGH_PumpRatio THI_H[7:0]												
9EH	TEMP_VGH_PumpRatio THI_L[7:0]												

9FH	TEMP_VGH_PumpRatio_TLO_H[7:0]			05H
A0H	TEMP_VGH_PumpRatio_TLO_L[7:0]			FBh
A1H	Reserved	TEMP_VGH_PumpRatio_L[1:0]	TEMP_VGH_PumpRatio_M[1:0]	TEMP_VGH_PumpRatio_H[1:0]
A2H	TEMP_VGL_PumpRatio THI_H[7:0]			2Dh
A3H	TEMP_VGL_PumpRatio THI_L[7:0]			23H
A4H	TEMP_VGL_PumpRatio TLO_H[7:0]			05H
A5H	TEMP_VGL_PumpRatio TLO_L[7:0]			FBh
A6H	Reserved	TEMP_VGL_PumpRatio_L[1:0]	TEMP_VGL_PumpRatio_M[1:0]	TEMP_VGL_PumpRatio_H[1:0]



TEMP\_VCOM\_OFSET\_L2

- Current VCOM Compensation offset

TEMP\_VGH\_OFSET\_L2

- Current VGH Compensation offset

TEMP\_VGL\_OFSET\_L2

- Current VGL Compensation offset

TEMP\_VGH\_PumpRatio\_L2

- Current VGH\_PumpRatio Compensation offset

TEMP\_VGL\_PumpRatio\_L2

- Current VGL\_PumpRatio Compensation offset

TEMP\_SENSOR\_EN

-Temperature Sensor enable

TEMP\_COMP\_EN

-Temperature Compensation enable

TEMP\_TH\_HI

-Temperature Compensation Stage TH\_HI°C (default 65)

TEMP\_TH\_LO

-Temperature Compensation Stage TH\_LO°C (default 55)

TEMP\_TL\_HI

-Temperature Compensation Stage TL\_HI°C (default -15)

TEMP\_TL\_LO

-Temperature Compensation Stage TL\_LO°C (default -25)

TEMP\_VCOM\_OFSET\_TH

-VCOM Compensation offset (&gt; TH\_HI°C) (Signed 2's complement)

VCOM = VCOM\_Code[8:0] + TEMP\_VCOM\_OFSET\_TH[8:0]

TEMP\_VCOM\_OFSET\_TL

-VCOM Compensation offset (&lt; TL\_LO°C) (Signed 2's complement)

VCOM = VCOM\_Code[8:0] + TEMP\_VCOM\_OFSET\_TL[8:0]

TEMP\_VCOM\_STEP\_TH

-VCOM Compensation diming offset (TH\_LO°C~TH\_HI°C) (Signed 2's complement)

UP : VCOM = VCOM\_Code[8:0] + TEMP\_VCOM\_STEP\_TH[3:0]\*N

DW : VCOM = VCOM\_Code[8:0] + TEMP\_VCOM\_OFSET\_TH[8:0] - TEMP\_VCOM\_STEP\_TH[3:0]\*N

TEMP\_VCOM\_STEP\_TL

-VCOM Compensation diming offset (TL\_LO°C~TL\_HI°C) (Signed 2's complement)

UP : VCOM = VCOM\_Code[8:0] + TEMP\_VCOM\_STEP\_TL[3:0]

DW : VCOM = VCOM\_Code[8:0] + TEMP\_VCOM\_OFSET\_TL[8:0] + TEMP\_VCOM\_STEP\_TL[3:0]

TEMP\_VGH\_OFSET\_TH

-VGH Compensation offset (&gt; TH\_HI°C) (Signed 2's complement)

VGH = VGH\_Code[6:0] + TEMP\_VGH\_OFSET\_TH[6:0]

TEMP\_VGH\_OFSET\_TL

-VGH Compensation offset (&lt; TL\_LO°C) (Signed 2's complement)

VGH = VGH\_Code[6:0] + TEMP\_VGH\_OFSET\_TL[6:0]

## TEMP\_VGH\_STEP\_TH

-VGH Compensation diming offset ( TH\_LO°C~TH\_HI°C ) (Signed 2's complement)

UP : VGH = VGH\_Code[6:0] + TEMP\_VGH\_STEP\_TH[3:0]\*N

DW : VGH = VGH\_Code[6:0] + TEMP\_VGH\_OFSET\_TH[6:0] + TEMP\_VGH\_STEP\_TH[3:0]\*N

## TEMP\_VGH\_STEP\_TL

-VGH Compensation diming offset ( TL\_LO°C~TL\_HI°C ) (Signed 2's complement)

UP : VGH = VGH\_Code[6:0] + TEMP\_VGH\_STEP\_TL[3:0]\*N

DW : VGH = VGH\_Code[6:0] + TEMP\_VGH\_OFSET\_TL[6:0] + TEMP\_VGH\_STEP\_TL[3:0]\*N

## TEMP\_VGL\_OFSET\_TH

-VGL Compensation offset (> TH\_HI°C) (Signed 2's complement)

VGL = VGL\_Code[6:0] + TEMP\_VGL\_OFSET\_TH[6:0]

## TEMP\_VGL\_OFSET\_TL

-VGL Compensation offset (< TL\_LO°C) (Signed 2's complement)

VGL = VGL\_Code[6:0] + TEMP\_VGL\_OFSET\_TL[6:0]

## TEMP\_VGL\_STEP\_TH

-VGL Compensation diming offset ( TH\_LO°C~TH\_HI°C ) (Signed 2's complement)

UP : VGL = VGL\_Code[6:0] + TEMP\_VGL\_STEP\_TH[3:0]\*N

DW : VGL = VGL\_Code[6:0] + TEMP\_VGL\_OFSET\_TH[6:0] + TEMP\_VGL\_STEP\_TH[3:0]\*N

## TEMP\_VGL\_STEP\_TL

-VGL Compensation diming offset ( TL\_LO°C~TL\_HI°C ) (Signed 2's complement)

UP : VGL = VGL\_Code[6:0] + TEMP\_VGL\_STEP\_TL[3:0]\*N

DW : VGL = VGL\_Code[6:0] + TEMP\_VGL\_OFSET\_TL[6:0] + TEMP\_VGL\_STEP\_TL[3:0]\*N

## TEMP\_VGH\_PumpRatio THI\_H

-When Temperature > VGH\_PUMP\_Ratio THI\_H, set Pump\_Ratio = H

## TEMP\_VGH\_PumpRatio THI\_L

-When Temperature < VGH\_PUMP\_Ratio THI\_L, set Pump\_Ratio = M

## TEMP\_VGH\_PumpRatio TLO\_H

-When Temperature > VGH\_PUMP\_Ratio TLO\_H, set Pump\_Ratio = M

## TEMP\_VGH\_PumpRatio TLO\_L

-When Temperature < VGH\_PUMP\_Ratio TLO\_L, set Pump\_Ratio = L

## TEMP\_VGH\_PumpRatio\_H

-VGH Pump Ratio Temp\_HI Setting

## TEMP\_VGH\_PumpRatio\_M

-VGH Pump Ratio Temp\_Norm Setting

## TEMP\_VGH\_PumpRatio\_L

-VGH Pump Ratio Temp\_LO Setting

## TEMP\_VGL\_PumpRatio THI\_H

-When Temperature > VGL\_PUMP\_Ratio THI\_H, set Pump\_Ratio = H

## TEMP\_VGL\_PumpRatio THI\_L

-When Temperature < VGL\_PUMP\_Ratio THI\_L, set Pump\_Ratio = M

## TEMP\_VGL\_PumpRatio TLO\_H

-When Temperature > VGL\_PUMP\_Ratio TLO\_H, set Pump\_Ratio = M

## TEMP\_VGL\_PumpRatio TLO\_L

-When Temperature < VGL\_PUMP\_Ratio TLO\_L, set Pump\_Ratio = L

TEMP\_VGL\_PumpRatio\_H  
-VGL Pump Ratio Temp\_HI Setting  
TEMP\_VGL\_PumpRatio\_M  
-VGL Pump Ratio Temp\_Norm Setting  
TEMP\_VGL\_PumpRatio\_L  
-VGL Pump Ratio Temp\_LO Setting

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**2.3.24 Polarity\_Set (BANK13H 8CH ~ 8DH) : Polarity parameter setting**

Bank13H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
8CH	POLBlankEn[0]	Internal Used							44h
8DH	Internal Used	POLInv[1:0]		POLInit[2:0]			Reserved		0CH

Description
- BANK 13H 8CH, D[7] ~ 8DH, D[1:0]
POLBlankEn[0] : 1'b1 = enable polarity toggle in V blanking
POLInit[2:0] : Polarity initial value, [1:0]: 2'b11 = 1 frame inversion, [1:0]: 2'b10 = 2 frame inversion, [1:0]: 2'b01 = always low, [1:0]: 2'b00 = always high [2]: 1'b1 = Invert polarity initial value, [2]: 1'b0 = not invert.
POLInv[1:0] : Polarity inversion type. 2'b11 = 1+2 line inversion. 2'b10 = 2 line inversion. 2'b01 = 1 line inversion. 2'b00 = column inversion.

**2.3.25 GOA\_OPT\_SET1 (BANK14H 80H~84H) : GOA Other Setting 1**

Bank14H											
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default		
80H	frm_gt_tg_ln[2:0]			LTPS_RST_	IGZO_direct	tcon_clk1_id	frm_gt_odd	tmgen_type	41h		
81H	clk_gt_sel[1:0]		stv_gt_sel[1:0]	frm_gt_tg_ln[6:3]					01h		
82H	sdrss_rtn[0]	h128_th[1:0]		clk_sdrss_mode[1:0]		sdrss_mode[1:0]	ch_goa_ma_sk		40h		
83H	sdrss_rtn[8:1]										
84H	tp_fixed_predmy_r[1:0]		vlen_pre_set[1:0]	vsync_mod_e	sdrss_rtn[11:9]				E9h		

Description									
Please follow the sequence below.									
Use GPIO4/GPIO5 ( tcon_LinePre / tcon_Linidx ) internal reference signal for GIP verification									
Step :									
REG41h = 0x5A									
REG42h = 0x0E									
REG94h = 0xA5									
REG95h = 0xA5									
REG9Ah = 0xFE									
Result :									
LCD_GPIO[4] = tcon_LinePre									
LCD_GPIO[5] = tcon_Linidx									
Note: Reference point 1 <sup>st</sup> DE is defined below. (DE = tcon_LinePre & tcon_Linidx)									

- These parameters are used to adjust additional GOA signal setting.

- BANK14H 80H, D[7:0] ~ 84H, D[5:0]

tmgen\_type : Tmgen type selection, 0:cog, 1:goa

frm\_gt\_odd\_inv : Frame gating inversion, 0: no inversion (odd frame gating) 1: inversion (even frame gating)

tcon\_clk1\_idx\_inv : CLK2,CLK2\_s bypass mode inversion, 0:clk1\_1\_IDX[1:0]=clk1\_IDX[1:0], 1:clk1\_1\_IDX[1:0]=~clk1\_IDX[1:0]

IGZO\_direct\_mode : 0: Change to power off sequence during clear region 0: Change to power off sequence directly

LTPS\_RST\_cont\_en : 0: RST signal pull low when status from bist to normal 1: RST signal keep value when status from bist to normal

frm\_gt\_tg\_ln[6:0] : Frame gating toggle line selection before reference point

stv\_gt\_sel[1:0] : STV gating selection, 0:disable, 1:half gating, 2:~half gating, 3:frame gating

clk\_gt\_sel[1:0] : CLK gating selection, 0:disable, 1:half gating, 2:quarter gating, 3:frame gating

ch\_goa\_mask : Mask 1 frame goa clk signals when mode switching (norm -> bist), 0:disable, 1:enable

sdrss\_mode[1:0] : Others SDRRS mode enable Bit[1]: Rising Edge Bit[0]: Falling Edge , 0:disable, 1: enable

clk\_sdrss\_mode[1:0] : CLK SDRRS mode enable Bit[1]: Rising Edge Bit[0]: Falling Edge , 0:disable, 1: enable

h128\_th[1:0] : OSC clock number setting of each 1/128 step in SDRRS mode, Multiplier 0:1, 1:2, 2:4, 3:8

sdrss\_rtn[11:0] : SDRRS mode max falling position

vsync\_mode : MIPI learning methodology 0: DE Mode 1:Vsync Mode

vlen\_pre\_set[1:0] : Pre-start vtotal cover vtotal loss (max:3 lines)

Illustrations of Quantification and SDRRS mode settings below.



**2.3.26 GOA\_STV\_SET1 (BANK14H 8AH~92H) : GOA STVx Setting 1**

Bank14H											
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default		
8AH	stv_2side_rtune[6:0]					stv_2side_en		00h			
8BH	stv_2side_d mytune[0]	stv_2side_ftune[6:0]					00h				
8CH	rst_vbkl_set[1:0]		stv_2side_dmystune[6:1]					00h			
8DH	rst_vbkl_set[9:2]								40h		
8EH	stv1_fb_set	stv1_f_set	rst1_sel	stv1_sel[1:0]		stv1_en	rst_vbkl_set[11:10]		C5h		
8FH	stv1_r[1:0]		stv1_shift[5:0]						C7h		
90H	stv1_f[2:0]			stv1_r[6:2]							
91H	stv1_width[3:0]				stv1_f[6:3]						
92H	stv2_sel[1:0]		stv2_en	stv1s_vbkh sel	stv1s_vbkh en	stv1_vbkh sel	stv1_vbkh en	stv1_inv	20h		

Description
- These parameters set a single-pulse type of gate signal with adjustable width, and location.
- Please reference to BANK 11H BAH, D[7:0] ~ ECH, D[7:0] for Power sequence of GIP.
- Please reference to GOA_OPT_SET1 for SDRRS mode.
- BANK14H 8AH, D[7:0] ~ 92H, D[4:0]
stv_2side_en : Generate delay STV 1H(adjustable) signal, 1'b0: disable 1'b1: enable
stv_2side_rtune[6:0] : 2side STV rising edge fine-tune(normal region) (unit is $\frac{1}{128}$ H)
stv_2side_ftune[6:0] : 2side STV falling edge fine-tune(normal region) (unit is $\frac{1}{128}$ H)
stv_2side_dmystune[6:0]:2side STV both edge fine-tune(dummy region) (unit is $\frac{1}{128}$ H)
rst_vbkl_set[11:0] : RST number setting of reference point
stv1_en : STV1 enable
stv1_sel[1:0] : STV1 type selection, 2'd0:STV, 2'd1:RST, 2'd 2:TPOFF, 2'd 3:TPOFF (cross TP_TERM)
Corresponding power sequence type ,2'd0:VST, 2'd1:VEND or RST, 2'd 2: TPOff, 2'd 3: TPOff
rst1_sel : RST1 power sequence type selection, 1'b0: VEND 1'b1: RST
stv1_f_set : STV1 falling edge selection, 1'b0: stv_r(quan)/stv_f (sdrss) 1'b1: stv_f(quan) / rtn - stv_f (sdrss)
stv1_fb_set : Set STV1 rising edge location, 1'b0: Rising edge after reference point 1'b1: Rising edge before reference point
stv1_shift[5:0] : Set starting position of the STV1 pulse with respect to the reference point(unit is line)
stv1_r[6:0] : Fine tune rising edge of STV1 signal. In quantification mode, the line is cut into 128 units.
stv1_f[6:0] : Fine tune falling edge of STV1 signal. In quantification mode, the line is cut into 128 units.
stv1_width[3:0] : Set STV1 pulse width(unit is line)
stv1_inv : STV1 inversion
stv1_vbkh_en : STV1 pull high at V-blanking region , 1'b0:disable 1'b1:enable
stv1_vbkh_sel : STV1 pull high selection, 1'b0:stv_vbkh_1 1'b1:stv_vbkh_2
stv1s_vbkh_en : STV1s pull high at V-blanking region, 1'b0:disable 1'b1:enable
stv1s_vbkh_sel : STV1s pull high selection, 1'b0:stv_vbkh_1 1'b1:stv_vbkh_2

Illustration of STV settings below.

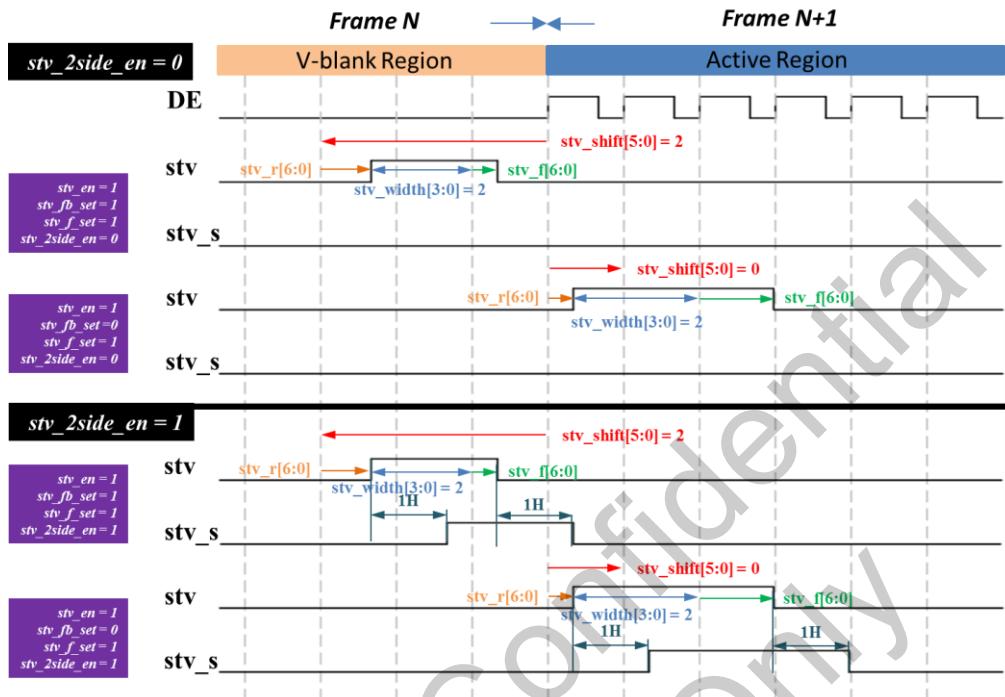
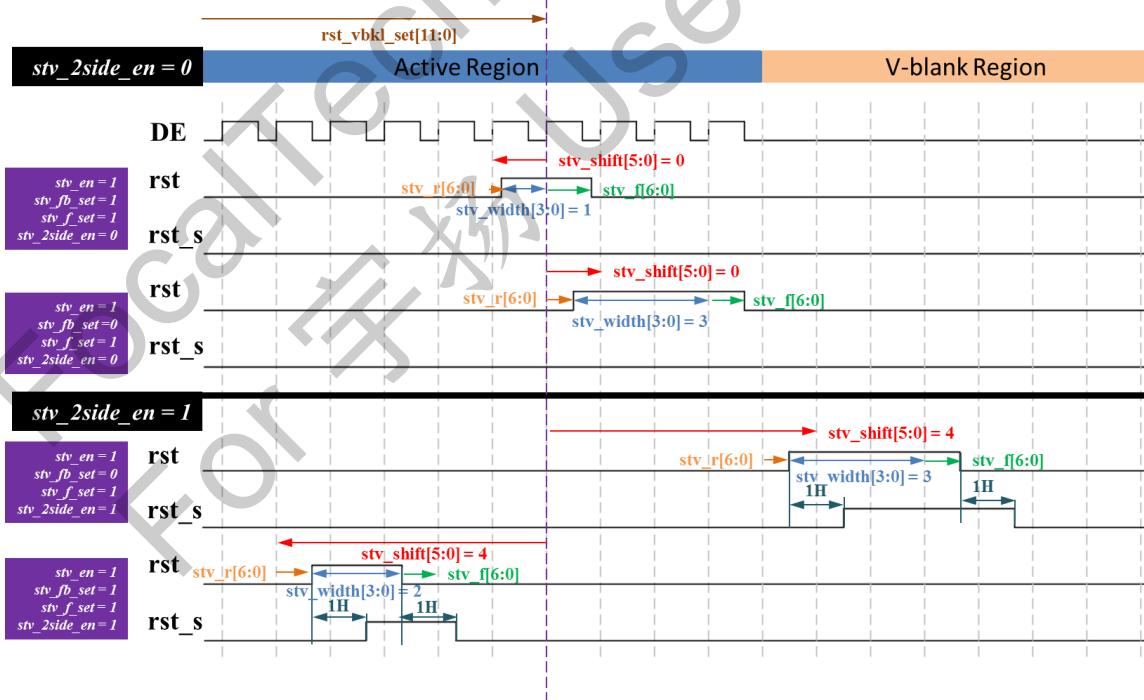
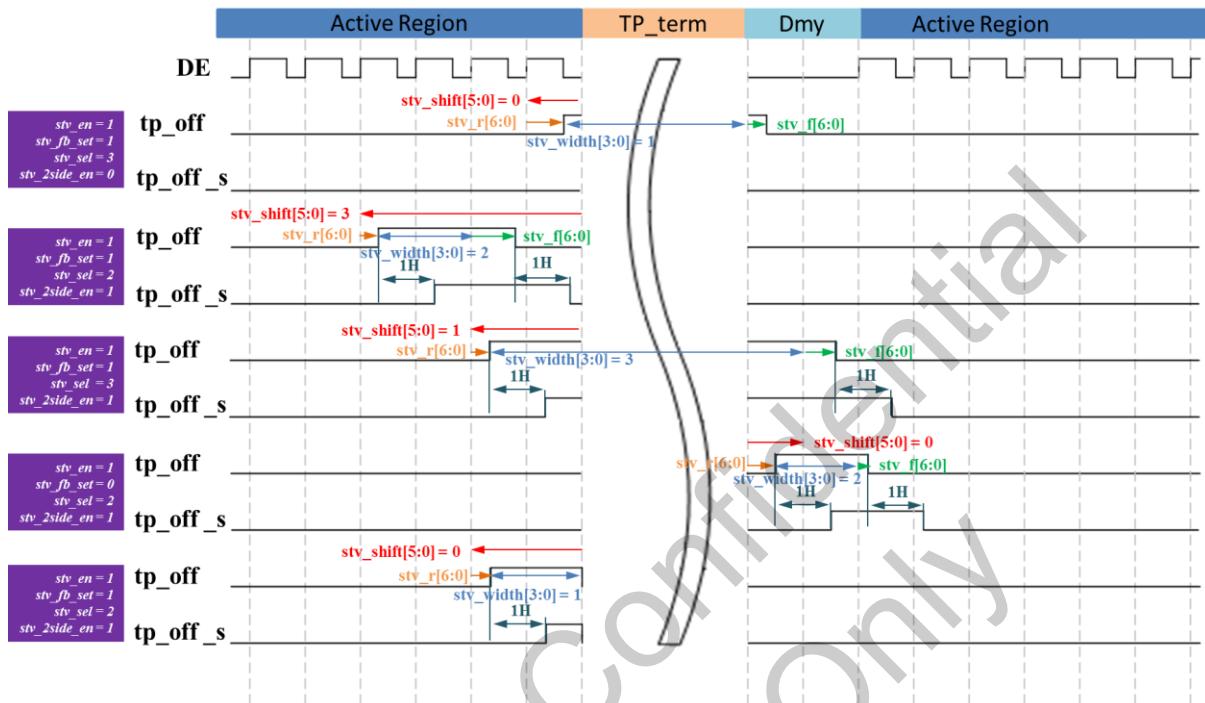


Illustration of RST settings below.

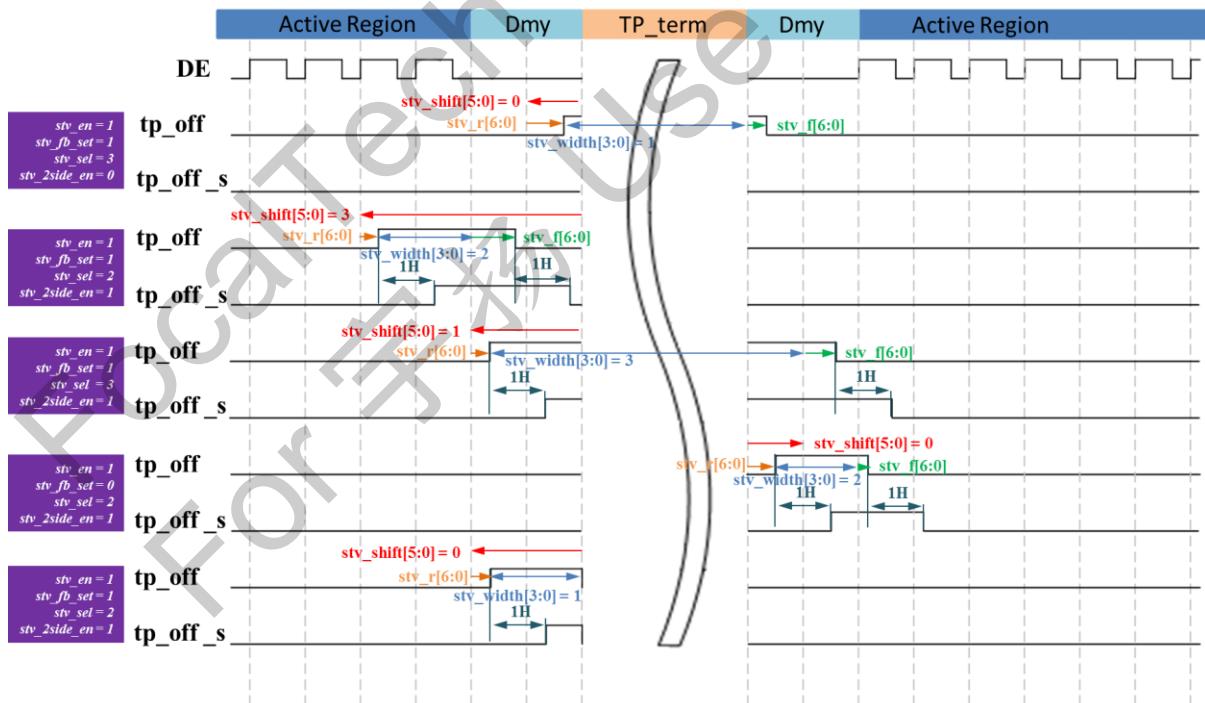


Illustrations of different TPOFF settings below.

Case1 :



Case2 :



Note1) Case1 illustrates the TPOFF setting parameters without pre\_dummy settings.

Note2) Case2 illustrates the TPOFF setting parameters with pre\_dummy settings.

**2.3.27 GOA\_STV\_SET2 (BANK14H 92H~9FH) : GOA STVx Setting 2**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
92H	stv2_sel[1:0]	stv2_en	stv1s_vbkh_sel	stv1s_vbkh_en	stv1_vbkh_sel	stv1_vbkh_en	stv1_inv	20h	
93H	stv2_shift[4:0]				stv2_fb_set	stv2_f_set	rst2_sel	36h	
94H	stv2_r[6:0]							stv2_shift[5]	46h
95H	stv2_width[0]	stv2_f[6:0]							F0h
96H	stv2s_vbkh_sel	stv2s_vbkh_en	stv2_vbkh_sel	stv2_vbkh_en	stv2_inv	stv2_width[3:1]			01h
97H	stv3_shift[1:0]	stv3_fb_set	stv3_f_set	rst3_sel	stv3_sel[1:0]	stv3_en	stv3_inv	71h	
98H	stv3_r[3:0]			stv3_shift[5:0]			stv3_fb_set	31h	
99H	stv3_f[4:0]				stv3_r[6:4]				82h
9AH	stv3_vbkh_en	stv3_inv	stv3_width[3:0]				stv3_f[6:5]	0Fh	
9BH	stv4_f_set	rst4_sel	stv4_sel[1:0]	stv4_en	stv3s_vbkh_sel	stv3s_vbkh_en	stv3_vbkh_sel	stv3_inv	88h
9CH	stv4_r[0]	stv4_shift[5:0]					stv4_fb_set	89h	
9DH	stv4_f[1:0]		stv4_r[6:1]						11h
9EH	stv4_width[2:0]			stv4_f[6:2]			stv4_inv	stv4_width[3]	7Ch
9FH	stv5_sel[0]	stv5_en	stv4s_vbkh_sel	stv4s_vbkh_en	stv4_vbkh_sel	stv4_vbkh_en	stv4_inv	00h	

Description									
- Please reference to GOA_STV_SET1 for further information.									

**2.3.28 GOA\_STV\_SET3 (BANK14H 9FH~A8H) : GOA STVx Setting 3**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
9FH	stv5_sel[0]	stv5_en	stv4s_vbkh_sel	stv4s_vbkh_en	stv4_vbkh_sel	stv4_vbkh_en	stv4_inv	stv4_width[3]	00h
A0H	stv5_shift[3:0]				stv5_fb_set	stv5_f_set	rst5_sel	stv5_sel[1]	00h
A1H	stv5_r[5:0]							stv5_shift[5:4]	FCh
A2H	stv5_ff[6:0]							stv5_r[6]	7Eh
A3H	stv5s_vbkh_en	stv5_vbkh_sel	stv5_vbkh_en	stv5_inv	stv5_width[3:0]				00h
A4H	stv6_shift[0]	stv6_fb_set	stv6_f_set	rst6_sel	stv6_sel[1:0]		stv6_en	stv5s_vbkh_sel	00h
A5H	stv6_r[2:0]			stv6_shift[5:1]					
A6H	stv6_f[3:0]				stv6_r[6:3]				F7h
A7H	stv6_inv	stv6_width[3:0]				stv6_ff[6:4]			
A8H	stv_vbkl_se_t[0]	tpoff_swap_order	tpoff_swap_mode[1:0]		stv6s_vbkh_sel	stv6s_vbkh_en	stv6_vbkh_sel	stv6_vbkh_en	00h

Description									
- Please reference to GOA_STV_SET1 for further information.									

**2.3.29 GOA\_TPOFF\_SWAP\_SET (BANK14H A8H) : GOA TPOFF Swap Setting**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
A8H	stv_vbkl_se t[0]	tpoff_swap_order	tpoff_swap_mode[1:0]	stv6s_vbkh sel	stv6s_vbkh en	stv6_vbkh sel	stv6_vbkh en	00h	

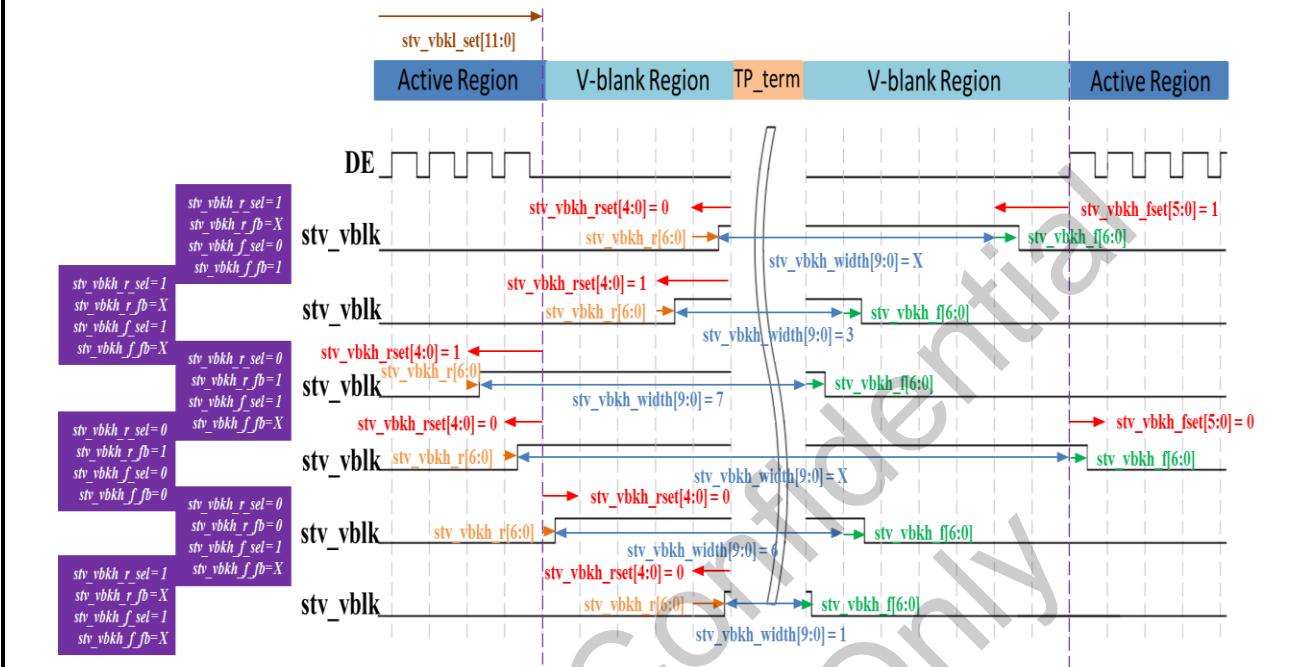
Description
- BANK14H A8H, D[6:4] tpoff_swap_mode[1:0] : Swap region selection 0 : disable 1 : display stop at odd gate 2 : display stop at even gate 3 : Reserved tpoff_swap_order : 0 : TPOFF 2sides signal swap 1: TPOFF even and odd signals swap

**2.3.30 GOA\_TPOFF\_VBLANK\_SET (BANK14H A8H~B4H) : GOA TPOFF at V-blanking Setting**

Bank14H													
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default				
A8H	stv_vbkl_se_t[0]	tpoff_swap_order	tpoff_swap_mode[1:0]		stv6s_vbkh_sel	stv6s_vbkh_en	stv6_vbkh_sel	stv6_vbkh_en	00h				
A9H	stv_vbkl_set[8:1]												
AAH	stv_vbkh_1_rset[0]	stv_vbkh_1_rf_fb	stv_vbkh_1_r_sel	stv_vbkh_1_rf_sel	stv_vbkh_1_en	stv_vbkl_set[11:9]							
ABH	stv_vbkh_1_fset[1:0]		stv_vbkh_1_rf_fb	stv_vbkh_1_rf_sel	stv_vbkh_1_rset[4:1]								
ACH	stv_vbkh_1_r[2:0]			stv_vbkh_1_rf_sel	stv_vbkh_1_fset[5:2]								
ADH	stv_vbkh_1_ff[3:0]				stv_vbkh_1_r[6:3]								
AEH	stv_vbkh_1_width[4:0]					stv_vbkh_1_ff[6:4]							
AFH	stv_vbkh_2_r_sel	stv_vbkh_2_sel	stv_vbkh_2_en	stv_vbkh_1_width[9:5]									
B0H	stv_vbkh_2_rf_fb	stv_vbkh_2_rf_sel	stv_vbkh_2_rset[4:0]					stv_vbkh_2_rf_fb	00h				
B1H	stv_vbkh_2_r[0]	stv_vbkh_2_rf_sel	stv_vbkh_2_fset[5:0]						00h				
B2H	stv_vbkh_2_ff[1:0]		stv_vbkh_2_r[6:1]										
B3H	stv_vbkh_2_width[2:0]			stv_vbkh_2_ff[6:2]									
B4H	stv_choked_en	stv_vbkh_2_width[9:3]							00h				

Description
- These parameters set the extra single-pulse at V-blanking region for TPOFF signal.
- BANK14H A8H, D[7] ~ AFH, D[4:0]
stv_vbkl_set[11:0] : STV_VBKH reference point number setting.
stv_vbkh_1_en: STV_VBKH_1 pull high at V-blanking.
stv_vbkh_1_sel : STV_VBKH_1 0: pull high in all frames during V-blanking 1: pull high only in fifo mode during V-blanking
stv_vbkh_1_r_sel : STV_VBKH_1 rising edge reference point selection 0: stv_vbkl_set 1: vblk_tp_term
stv_vbkh_1_r_fb : 0: STV_VBKH_1 falling edge locates after reference point 1: STV_VBKH_1 falling edge locates before reference point
stv_vbkh_1_rset[4:0] : Set rising edge of STV_VBKH_1, (stv_vbkl_set[11:0] +/- stv_vbkh_1_rset[4:0])H or stv_vbkh_1_rset[4:0]H
stv_vbkh_1_f_sel : STV_VBKH_1 falling edge selection 0: vbkh_fset 1:rising edge + stv_vbkh_1_width
stv_vbkh_1_f_fb : 0: STV_VBKH_1 falling edge locates after reference point 1: STV_VBKH_1 falling edge locates before reference point
stv_vbkh_1_fset[5:0] : Specifies falling edge of STV_VBKH_1 between reference point(unit is line)
stv_vbkh_1_rf_sel : STV_VBKH_1 falling edge selection,
1'b0: stv_vbkh_1_r(quan)/stv_vbkh_1_f(srdr) 1'b1:stv_vbkh_1_f(quan) / rtn - stv_vbkh_1_f(srdr)
stv_vbkh_1_r[6:0] : Fine tune rising edge of STV_VBKH_1 signal. In quantification mode, the line is cut into 128 units.
stv_vbkh_1_f[6:0] : Fine tune falling edge of STV_VBKH_1 signal. In quantification mode, the line is cut into 128 units
stv_vbkh_1_width[9:0] : Specifies falling edge of STV_VBKH_1 between rising edge(unit is line)
- BANK14H AFH, D[7:5] ~ B4H, D[6:0]
See stv_vbkh_1 above for reference

Illustration of TPOFF at V-BLANK region settings below.



#### 2.3.31 GOA\_STV\_CHOKE\_SET (BANK14H B4H~B6H) : GOA STV CHOKE Setting

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
B4H	stv_choked_en	stv_vbkh_2_width[9:3]							00h
B5H	stv_choked_width[3:0]				stv_bypass_width[3:0]				00h
B6H	clk_2side_rtune[2:0]			clk_2side_en	stv_choked_width[7:4]				00h

Description									
- BANK14H B4H, D[7] ~ B6H, D[3:0]									
stv_choked_en : stv_choked_en enable									
stv_bypass_width[3:0] : stv bypass region : stv_bypass_width[3:0] * 4 H									
stv_choked_width[7:0] : stv choked region : stv_choked_width[7:0] * 16 H									
Illustration of stv_choke settings below.									
<p>Frame N      Frame N+1      Frame N+2      Frame N+3</p> <p>stv_choked_en = 0</p> <p>Vactive</p> <p>stv_1</p> <p>stv_2</p> <p>stv_3</p> <p>stv_4</p> <p>stv_bypass_width = X stv_choked_width = X</p> <p>stv_choked_en = 1</p> <p>stv_1</p> <p>stv_2</p> <p>stv_3</p> <p>stv_4</p> <p>stv_bypass_width = 4 stv_choked_width = 15</p> <p>stv_choked_region = stv_choked_width * 16      stv_choked_region = stv_choked_width * 16</p> <p>stv_bypass_region = stv_bypass_width * 4      stv_bypass_region = stv_bypass_width * 4</p>									

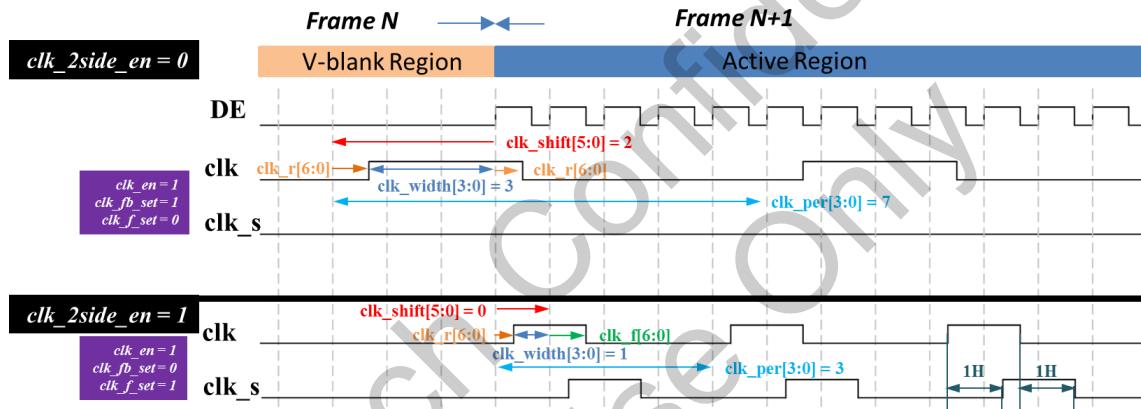
**2.3.32 GOA\_CLK\_SET1 (BANK14H B6H~C7H) : GOA CLKx Setting 1**

Bank14H																	
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default								
B6H	clk_2side_rtune[2:0]			clk_2side_en	stv_choked_width[7:4]												
B7H	clk_2side_ftune[3:0]			clk_2side_rtune[6:3]					00h								
B8H	clk_2side_dmtytune[4:0]					clk_2side_ftune [6:4]											
B9H	clk_vbkl_1_set[4:0]					clk_vbkl_en	clk_2side_dmtytune[6:5]										
BAH	clk_vbkl_2_set[0]	clk_vbkl_1_set[11:5]															
BBH	clk_vbkl_2_set[8:1]																
BCH	clk_r_fixyoe_adj[1:0]	clk_pulse_clip[1:0]		clk_width_clip_en	clk_vbkl_2_set[11:9]												
BDH	clk_f_fixyoe_adj[1:0]	clk_r_fixyoe_adj[7:2]															
BEH	clk_gt_tg_ln[1:0]	clk_f_fixyoe_adj[7:2]															
BFH	clk_b2f_gt_tg_ln[2:0]			clk_gt_tg_ln[6:2]													
C0H	clk_f2b_gt_tg_ln[3:0]				clk_b2f_gt_tg_ln[6:3]												
C1H	clk1_per[3:0]			clk1_en	clk_f2b_gt_tg_ln[6:4]												
C2H	clk1_shift[5:0]					clk1_fb_set	clk1_f_set	07h									
C3H	clk1_f[0]	clk1_r[6:0]															
C4H	clk1_width[1:0]		clk1_f[6:1]														
C5H	Internal Used						clk1_width[3:2]										
C7H	clk1_vbkl_sel	clk1_disp_cnt_en	Internal Used														

Description									
- These parameters set the gate clock type signals CLK1 to CLK8 during sleep out and normal display.									
- Please reference to BANK 11H BAH, D[7:0] ~ ECH, D[7:0] for Power sequence of GIP.									
- Please reference to GOA_OPT_SET1 for CLK SDRRS mode.									
- BANK14H B6H, D[7:4] ~ C7H, D[7:0]									
clk_2side_en : Generate delay CLK 1H(adjustable) signal enable, 1'b0: disable 1'b1: enable									
clk_2side_rtune[6:0] : 2side CLK rising edge fine-tune in normal region									
clk_2side_ftune[6:0] : 2side CLK falling edge fine-tune in normal region									
clk_2side_dmtytune[6:0] : 2side CLK both edge fine-tune in dummy region									
clk_vbkl_en : CLK pull low at V-blanking enable, 1'b0: CLK keep toggle at V-blanking 1'b1: CLK pull low at V-blanking									
clk_vbkl_1_set[11:0] : CLK number setting of V-blanking as low									
clk_vbkl_2_set[11:0] : CLK number setting of V-blanking as low									
clk_width_clip_en : CLK width clip to period length enable									
clk_pulse_clip[1:0] : End of CLK stop at 2'd0: Continue 2'd1:greater than period length between CLK start 2'd2: clk_gt_tg_ln 2'd3: reserved									
clk_r_fixyoe_adj[7:0] : CLK rising edge compensation in external mode BIT[7] 0: minus 1: plus									
clk_f_fixyoe_adj[7:0] : CLK falling edge compensation in external mode BIT[7] 0: minus 1: plus									
clk_gt_tg_ln[6:0] : CLK clear region setting (lead 1st_DE) when status fixed									
clk_b2f_gt_tg_ln[6:0] : CLK clear region setting (lead 1st_DE) when status from external to internal									
clk_f2b_gt_tg_ln[6:0] : CLK clear region setting (lead 1st_DE) when status from internal to external									

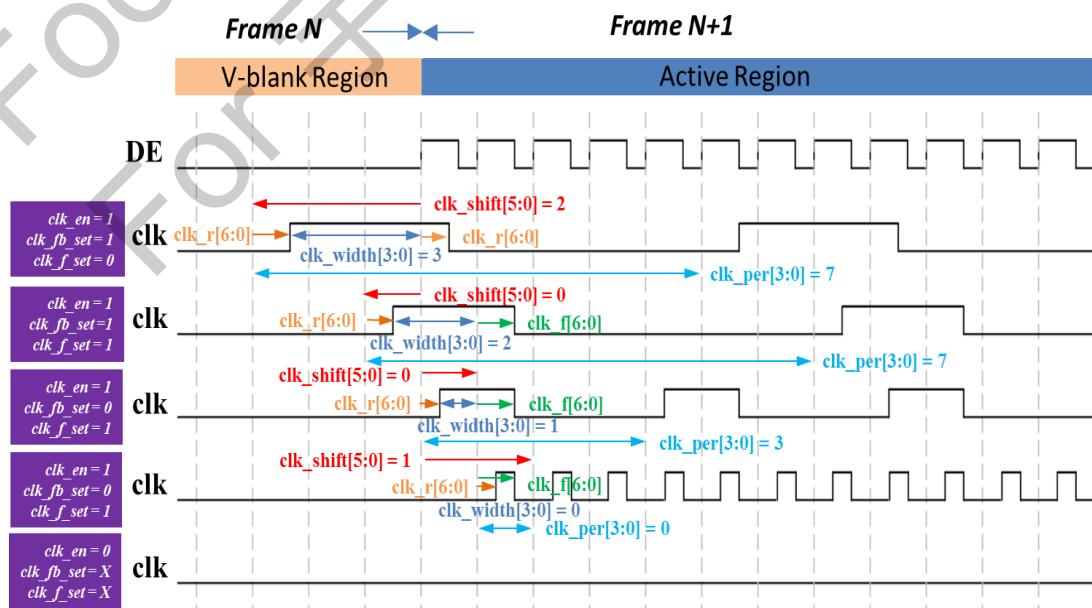
clk1\_en : CLK1 enable  
 clk1\_per[3:0] : Period of CLK1  
 clk1\_f\_set : CLK1 falling edge selection, 1'b0: clk\_r(quan)/clk\_f (sdrrs)    1'b1: clk\_f(quan) / rtn - clk\_f (sdrrs)  
 clk1\_fb\_set : Set CLK1 rising edge location, 1'b0: Rising edge after reference point(1<sup>st</sup> DE) 1'b1: Rising edge before reference point(1<sup>st</sup> DE)  
 clk1\_shift[5:0] : Specifies start point(1<sup>st</sup> rising edge) of CLK1 where the clock starts to toggle(unit is line)  
 clk1\_r[6:0] : Fine tune rising edge of CLK1 signal. In quantification mode, the line is cut into 128 units.  
 clk1\_f[6:0] : Fine tune falling edge of CLK1 signal. In quantification mode, the line is cut into 128 units.  
 clk1\_width[3:0] : Set high pulse period of CLK1 signal(unit is line)  
 clk1\_disp\_cont\_en : CLK1 ignore pre-dummy line number in post region  
 clk1\_vblk1\_sel : CLK1 V-blanking low selection, 0:clk\_vblk1\_1\_set, 1:clk\_vblk1\_2\_set

Illustration of CLK 2sides settings below.

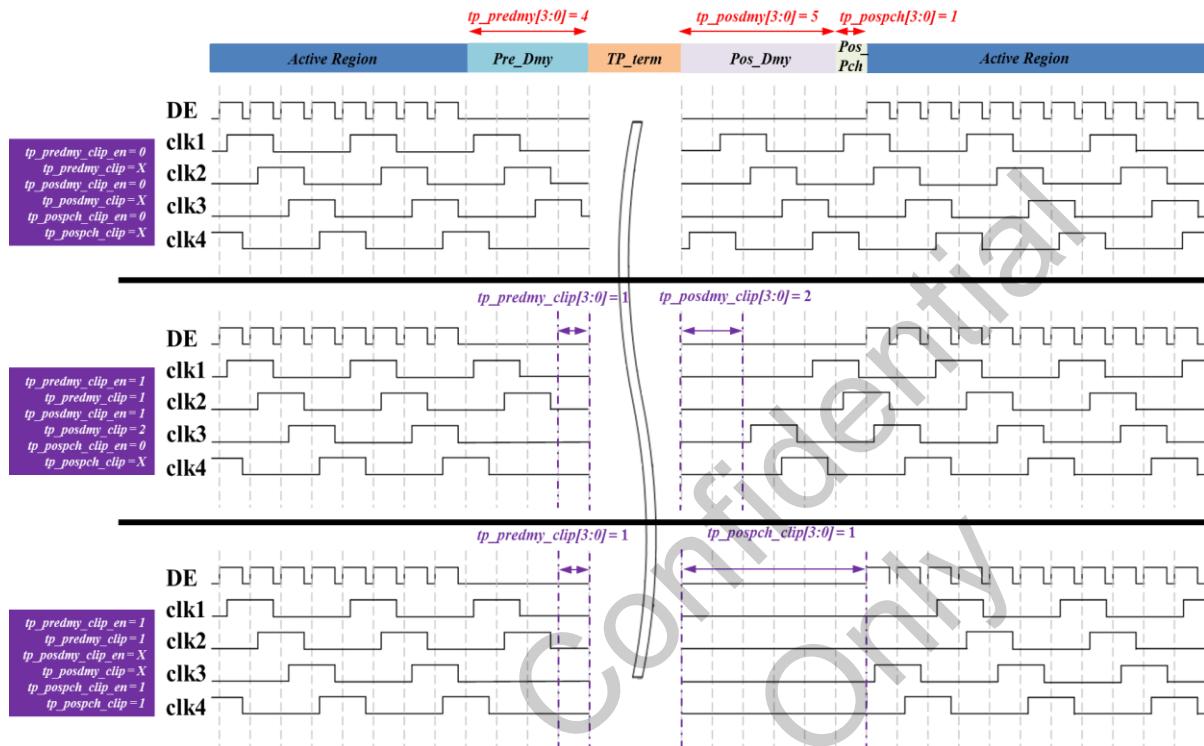


Illustrations of different CLK settings below.

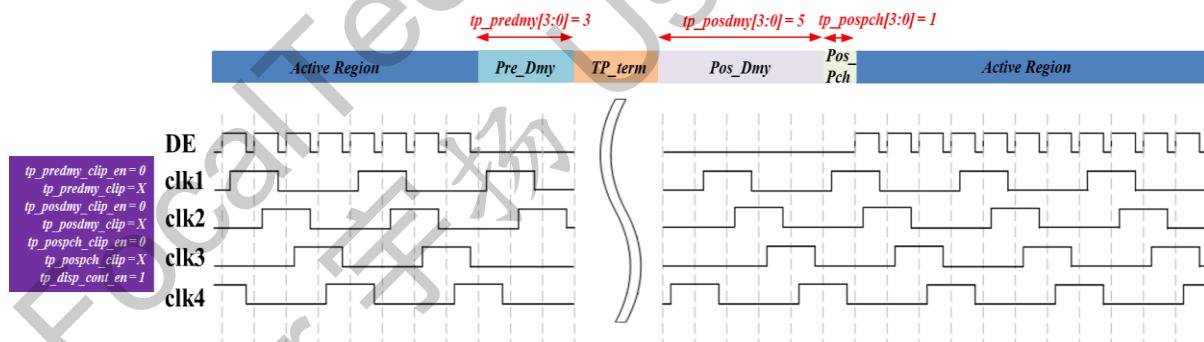
Case1



## Case2



## Case3



Note1) Case1 illustrates the CLK normal display settings.

Note2) Case2 illustrates the CLK with TP\_TERM settings.

Note2) Case3 illustrates the CLK with TP\_TERM and parameter tp\_disp\_cont\_en enable settings.

**2.3.33 GOA\_CLK\_SET2 (BANK14H C8H~D5H) : GOA CLKx Setting 2**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
C8H	clk2_shift[0]	clk2_fb_set	clk2_f_set	clk2_per[3:0]				clk2_en	6Fh
C9H	clk2_r[2:0]			clk2_shift[5:1]					60h
CAH	clk2_f[3:0]				clk2_r[6:3]				
CBH	Internal Used	clk2_width[3:0]				clk2_f[6:4]			
CEH	clk3_per[1:0]		clk3_en	clk2_vbkl_s el	clk2_disp_c ont_en	Internal Used			
CFH	clk3_shift[3:0]				clk3_fb_set	clk3_f_set	clk3_per[3:2]		05h
D0H	clk3_r[5:0]					clk3_shift[5:4]			
D1H	clk3_f[6:0]						clk3_r[6]		E0h
D2H	Internal Used				clk3_width[3:0]				
D5H	clk4_f_set	clk4_per[3:0]				clk4_en	clk3_vbkl_s el	clk3_disp_c ont_en	BCh

Description									
- Please reference to GOA_CLK_SET1 for further information.									

**2.3.34 GOA\_CLK\_SET3 (BANK14H D5H~E2H) : GOA CLKx Setting 3**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
D5H	clk4_f_set	clk4_per[3:0]				clk4_en	clk3_vbkl_s el	clk3_disp_c ont_en	BCh
D6H	clk4_r[0]	clk4_shift[5:0]						clk4_fb_set	82h
D7H	clk4_f[1:0]		clk4_r[6:1]						
D8H	clk4_width[2:0]			clk4_ff[6:2]				7Ch	
D9H	Internal Used								clk4_width[3] 1 C0h
DBH	clk5_en	clk4_vbkl_s el	clk4_disp_c ont_en	Internal Used					
DCH	clk5_shift[1:0]		clk5_fb_set	clk5_f_set	clk5_per[3:0]				
DDH	clk5_r[3:0]				clk5_shift[5:2]				
DEH	clk5_ff[4:0]				clk5_r[6:4]				
DFH	Internal Used		clk5_width[3:0]			clk5_f[6:5]			0Fh
E2H	clk6_per[2:0]			clk6_en	clk5_vbkl_s el	clk5_disp_c ont_en	Internal Used		F0h

Description
- Please reference to GOA_CLK_SET1 for further information.

**2.3.35 GOA\_CLK\_SET4 (BANK14H E2H~EFH) : GOA CLKx Setting 4**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
E2H	clk6_per[2:0]			clk6_en	clk5_vbkl_s el	clk5_disp_c ont_en	Internal Used		F0h
E3H	clk6_shift[4:0]				clk6_fb_set	clk6_f_set	clk6_per[3]		26h
E4H	clk6_r[6:0]						clk6_shift[5]		46h
E5H	clk6_width[0] ]	clk6_f[6:0]							F0h
E6H	Internal Used			clk6_pospch _clip_en	clk6_width[3:1]				01h
E8H	clk6_disp cont_en	FOCAL TECH internal Configuration only							00h
E9H	clk7_fb_set	clk7_f_set	clk7_per[3:0]			clk7_en	clk6_vbkl_s el		DEh
EAH	clk7_r[1:0]		clk7_shift[5:0]						C3h
EBH	clk7_f[2:0]			clk7_r[6:2]					08h
ECH	clk7_width[3:0]			clk7_f[6:3]					3Eh
EFH	clk8_per[0]	clk8_en	clk7_vbkl_s el	clk7_disp_c ont_en	Internal Used				C0h

Description	
- Please reference to GOA_CLK_SET1 for further information.	

**2.3.36 GOA\_CLK\_SET5 (BANK14H EFH~F6H) : GOA CLKx Setting 5**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
EFH	clk8_per[0]	clk8_en	clk7_vbkl_s el	clk7_disp_c ont_en	Internal Used				C0h
F0H	clk8_shift[2:0]			clk8_fb_set	clk8_f_set	clk8_per[3:1]			5Bh
F1H	clk8_rf[4:0]				clk8_shift[5:3]				18h
F2H	clk8_ff[5:0]					clk8_rf[6:5]			C1h
F3H	Internal Used			clk8_width[3:0]			clk8_ff[6]	07h	
F6H	tpsync_per[3:0]				tpsync_en	clk8_vbkl_s el	clk8_disp_c ont_en	Internal Used	00h

Description
- Please reference to GOA_CLK_SET1 for further information.

**2.3.37 COG\_TPSYNC\_SET (BANK14H F6H~FAH) : COG TPSYNC Setting**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
F6H	tpsync_per[3:0]				tpsync_en	clk8_vbkl_s el	clk8_disp_c ont_en	Internal Used	00h
F7H	tpsync_shift[5:0]						tpsync_fb_s et	tpsync_f_se t	00h
F8H	tpsync_f[0]	tpsync_r[6:0]							
F9H	tpsync_width[1:0]		tpsync_f[6:1]						00h
FAH	gpmode_per[1:0]	gpmode_en	tpsync_mod e	tpsync_vbkl en	tpsync_vbkl sel	tpsync_width[3:2]			00h

Description
- BANK14H FAH, D[4]
tpsync_mode : TPSYNC selection 0: Vsync 1: Hsync + Vsync (Vsync can disable)
- please reference to GOA_CLK_SET1 for further information.

**2.3.38 COG\_GPMODE\_SET (BANK14H FAH ~ BANK15H 81H) : COG GPMODE Setting**

Bank14H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
FAH	gpmode_per[1:0]	gpmode_en	tpsync_mod_e	tpsync_vbkl_en	tpsync_vbkl_sel	tpsync_width[3:2]		00h	
FBH	gpmode_shift[3:0]			gpmode_fb_set	gpmode_f_s et	gpmode_per[3:2]		00h	
FCH	gpmode_r[5:0]					gpmode_shift[5:4]		00h	
FDH	gpmode_f[6:0]						gpmode_r[6]	1	00h
FEH	gpmode_pospch_clip[2:0]			gpmode_pospch_clip_en	gpmode_width[3:0]				00h
FFH	gpmode_preadmy_clip[0]	gpmode_preadmy_clip_en	gpmode_posdmy_clip[3:0]				gpmode_posdmy_clip_en	gpmode_posdmy_clip[3]	00h
Bank15H									
80H	gpmode_posdmy_mask[3:0]				gpmode_posdmy_mask_en	gpmode_predmy_clip[3:1]			00h
81H	clk_vbkh_rf	clk_vbkh_f_sel	clk_vbkh_en	clk_vbkh_tp_sel	gpmode_vk_en	gpmode_vk_sel	gpmode_dis_p_cont_en		00h

**Description**

- Please reference to GOA\_CLK\_SET1 for further information.

### 2.3.39 GOA\_CLK\_VBKH\_SET (BANK15H 81H~8CH) : GOA CLK at V-blanking Setting

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
81H	clk_vbkh_r_fb	clk_vbkh_f_sel	clk_vbkh_e_n		clk_vbkh_tp_sel	gpmode_vb_kl_en	gpmode_vb_kl_sel	gpmode_dis_p_cont_en	00h
82H	clk_vbkh_fset[1:0]	clk_vbkh_f_fb			clk_vbkh_rset[4:0]				00h
83H	clk_vbkh_r[3:0]				clk_vbkh_fset[5:2]				00h
84H	clk_vbkh_f[4:0]				clk_vbkh_r[6:4]				00h
85H	clk_vbkh_width[1:0]	clks_vbkh_sel[1:0]		clk_vbkh_sel[1:0]	clk_vbkh_f[6:5]				00h
86H	clk_vbkh_width[9:2]								00h
87H	clk_mask_rset[4:0]			clk_mask_r_fb	clk_mask_mode	clk_mask_en			00h
88H	clk_mask_fset[5:0]			clk_mask_f_fb	clk_mask_f_sel				00h
89H	clk_mask_f[0]	clk_mask_r[6:0]							00h
8AH	clk_mask_w_idth[0]	clk_mask_f_en		clk_mask_f[6:1]					00h
8BH	clk_mask_width[8:1]								00h
8CH	tpsync_vbkh_rset[5:0]			tpsync_vbkh_h_en	clk_mask_w_idth[9]				00h

Description
- These parameters set the extra cycles at V-blanking region for each gate driver clock signal CLKx.
- BANK15H 81H, D[7:3] ~ 86H, D[7:0]
clk_vbkh_tp_sel[1:0] : CLK_VBKH and CLK_MASK 0: Pull high 1: Pull low 2:Keep status 3:Invert status during TP_TERM clk_vbkh_en : CLK pull high at V-blanking (CLK_VBKH) enable clk_vbkh_f_sel : CLK_VBKH falling edge selection 0: vbkh_fset 1:rising edge + clk_vbkh_width clk_vbkh_r_fb : 0: CLK_VBKH rising edge locates after reference point 1: CLK_VBKH rising edge locates before reference point clk_vbkh_rset[4:0] : Set rising edge of CLK_VBKH(unit is line) clk_vbkh_f_fb : 0: CLK_VBKH falling edge locates after reference point 1: CLK_VBKH falling edge locates before reference point clk_vbkh_fset[5:0] : Specifies falling edge of CLK_VBKH between reference point(unit is line) clk_vbkh_r[6:0] : Fine tune rising edge of CLK_VBKH signal. In quantification mode, the line is cut into 128 units. clk_vbkh_f[6:0] : Fine tune falling edge of CLK_VBKH signal. In quantification mode, the line is cut into 128 units. clk_vbkh_sel[1:0] : CLKx signal VBKH select, 0:CLK_VBKH, 1:CLK_MASK, 2: O:CLK_VBKH、E:CLK_MASK, 3: O:CLK_MASK、E:CLK_VBKH clks_vbkh_sel[1:0] : CLKSx signal VBKH select, 0:CLK_VBKH, 1:CLK_MASK, 2: O:CLK_VBKH、E:CLK_MASK, 3: O:CLK_MASK、E:CLK_VBKH clk_vbkh_width[9:0] : Set high pulse period of CLK_VBKH signal(unit is line)
- BANK15H 87H, D[7:0] ~ 8CH, D[0] clk_mask_mode : CLK_MASL 0: High active 1: Low active during V-blank
The others see CLK_VBKH above for reference

Illustration of CLK\_VBKH settings below.

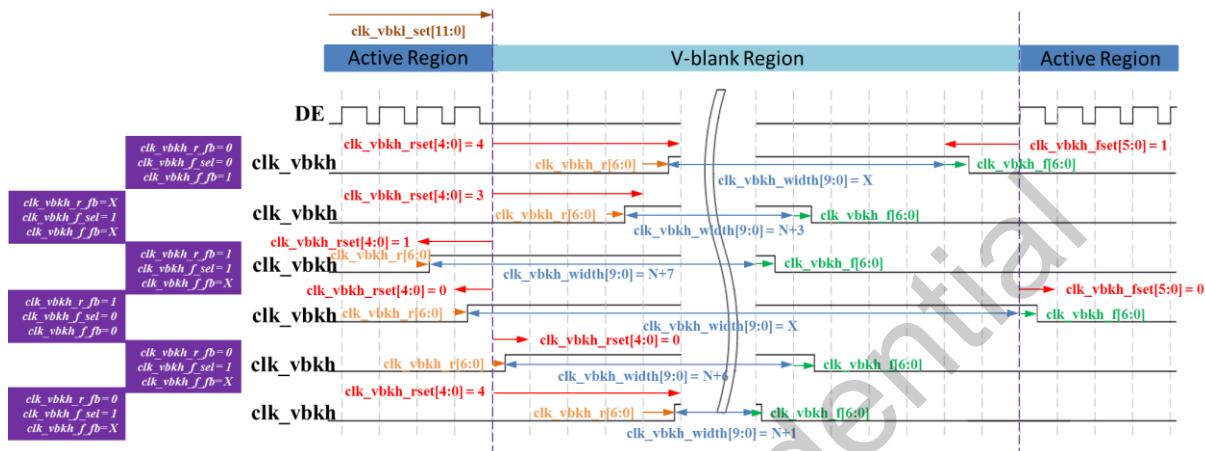
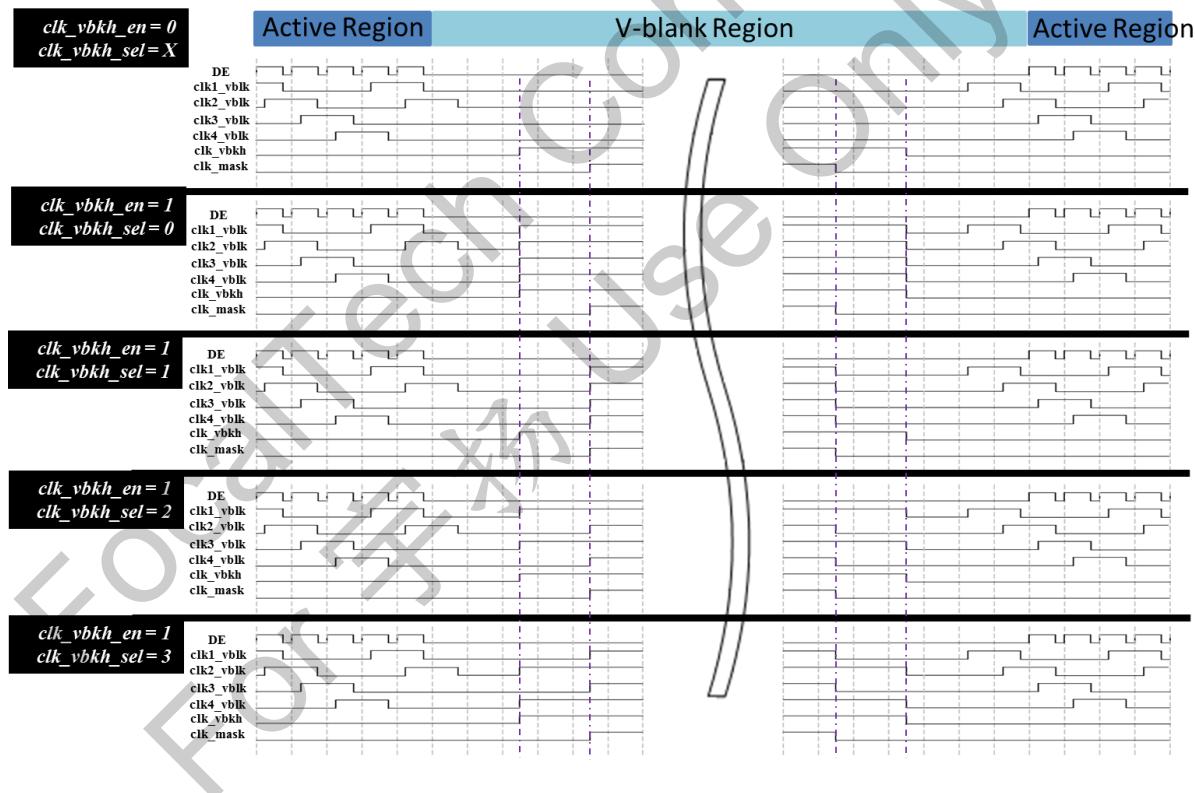


Illustration of different clk\_vbkhsel settings below.



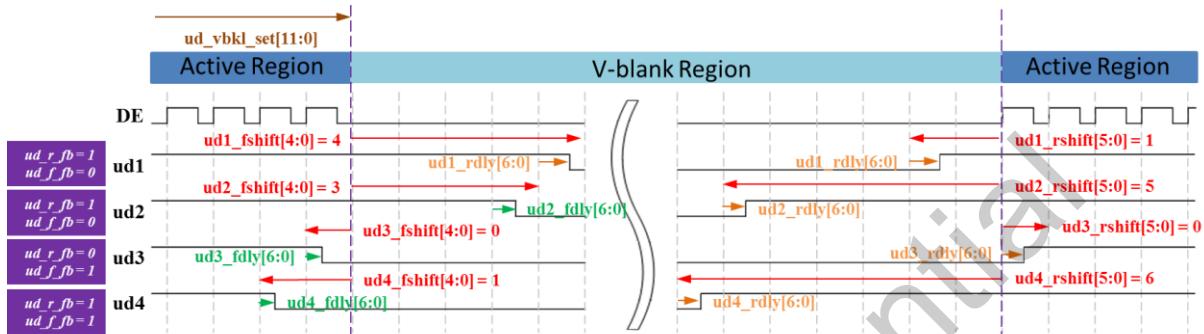
**2.3.40 GOA\_UD\_SET1 (BANK15H 91H~9AH) : GOA UDx Setting 1**

Bank15H												
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default			
91H	ud_vbkl_set[0]	cog_oe1_continual	cog_ckv_continual	tpsync_vbkh_width[9:5]								
92H	ud_vbkl_set[8:1]								81h			
93H	ud1_rshift[0]	ud1_r_fb	ud1_mode	ud1_inv	ud1_en	ud_vbkl_set[11:9]			6Ah			
94H	ud1_fshift[1:0]		ud1_f_fb	ud1_rshift[5:0]								
95H	ud1_rdly[3:0]			ud1_f_set	ud1_fshift[4:2]				A8h			
96H	ud1_fdly[4:0]				ud1_rdly[6:4]							
97H	ud1_tp_width[0]	ud1_tp_shift[3:0]			ud1_tp_fb_set	ud1_fdly[6:5]			86h			
98H	ud1_tp_rdly[4:0]				ud1_tp_width[3:1]							
99H	ud1_tp_fdly[5:0]					ud1_tp_rdly[6:5]			6Ah			
9AH	ud2_rshift[2:0]		ud2_r_fb	ud2_mode	ud2_inv	ud2_en	ud1_tp_fdly[6]	1Fh				

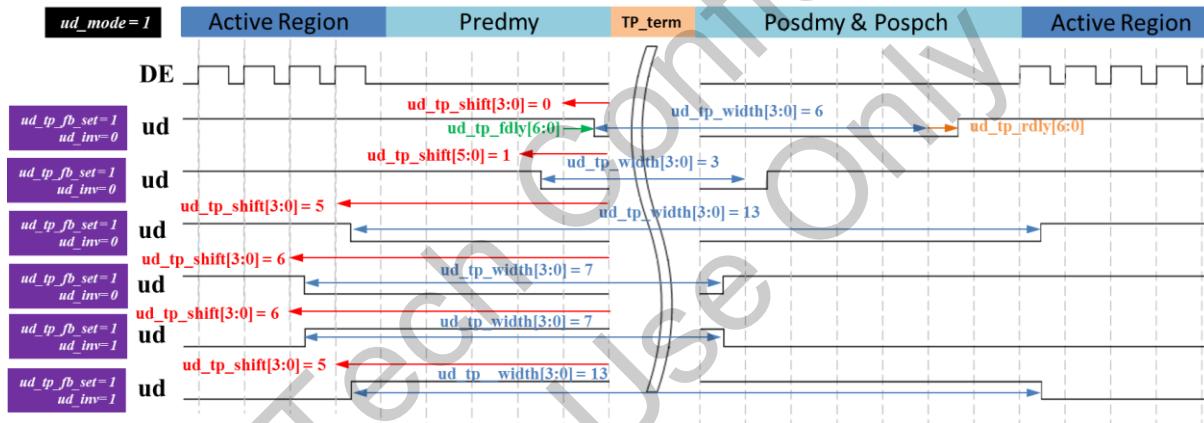
Description
- Please reference to BANK 11H BAH, D[7:0] ~ ECH, D[7:0] for Power sequence of GIP.
- BANK15H 91H, D[7] ~ 9AH, D[0]
ud_vbkl_set[11:0] : UD number setting of reference point (0~4095 lines)
ud1_en : UD1 enable
ud1_inv : UD1 inversion
ud1_mode : UD1 TP_TERM parameters enable
ud1_r_fb : 0: UD1 rising edge locates after reference point 1: UD1 rising edge locates before reference point
ud1_rshift[5:0] : Set rising edge of UD1(unit is line)
ud1_f_fb : 0: UD1 falling edge locates after ud_vbkl_set 1: UD1 falling edge locates before ud_vbkl_set
ud1_fshift[4:0] : Set falling edge of UD1(unit is line)
ud1_f_set : UD1 falling edge selection, 0: ud1_r(quan)/ud1_f (sdrss)      1: ud1_f(quan) / rtn - ud1_f (sdrss)
ud1_rdly[6:0] : Fine tune rising edge of UD1 signal. In quantification mode, the line is cut into 128 units.
ud1_fdly[6:0] : Fine tune falling edge of UD1 signal. In quantification mode, the line is cut into 128 units.
ud1_tp_fb_set : 0: UD1 falling edge locates after TP_TERM      1:UD1 rising edge locates before TP_TERM
ud1_tp_shift[3:0] : Set TP_TERM falling edge of UD1(unit is line)
ud1_tp_width[3:0] : Set pull low region of UD1 signal during TP_TERM(unit is line)
ud1_tp_rdly[6:0] : Set pull low region of UD1 signal during TP_TERM. In quantification mode, the line is cut into 128 units.
ud1_tp_fdly[6:0] : Delay falling edge of UD1 during TP_TERM. In quantification mode, the line is cut into 128 units.

Illustrations of different UD settings below.

Case1 :



Case2 :



Note1) Case1 illustrates the UD parameters settings.

Note2) Case2 illustrates the UD setting parameters with TP\_TERM settings.

**2.3.41 GOA\_UD\_SET2 (BANK15H 9AH~AEH) : GOA UDx Setting 2**

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
9AH	ud2_rshift[2:0]			ud2_r_fb	ud2_mode	ud2_inv	ud2_en	ud1_tp_fdl[y[6]]	1FH
9BH	ud2_fshift[3:0]			ud2_f_fb		ud2_rshift[5:3]			31h
9CH		ud2_rdl[y[5:0]]				ud2_f_set	ud2_fshift[4]		6Ah
9DH		ud2_fdl[y[6:0]]					ud2_rdl[y[6]]		B5h
9EH	ud2_tp_width[2:0]			ud2_tp_shift[3:0]			ud2_tp_fb_set		21h
9FH		ud2_tp_rdl[y[6:0]]					ud2_tp_width[3]		B4h
A0H	ud3_en			ud2_tp_fdl[y[6:0]]					5Ah
A1H		ud3_rshift[4:0]			ud3_r_fb	ud3_mode	ud3_inv		00h
A2H	ud3_f_set		ud3_fshift[4:0]		ud3_f_fb	ud3_rshift[5]			00h
A3H	ud3_fdl[y[0]]			ud3_rdl[y[6:0]]					00h
A4H	ud3_tp_shif[t[0]]	ud3_tp_fb_set			ud3_fdl[y[6:1]]				00h
A5H	ud3_tp_rdl[y[0]]		ud3_tp_width[3:0]		ud3_tp_shift[3:1]				00h
A6H	ud3_tp_fdl[y[1:0]]			ud3_tp_rdl[y[6:1]]					00h
A7H	ud4_mode	ud4_inv	ud4_en		ud3_tp_fdl[y[6:2]]				00h
A8H	ud4_f_fb			ud4_rshift[5:0]		ud4_r_fb			00h
A9H	ud4_rdl[y[1:0]]	ud4_f_set		ud4_fshift[4:0]					00h
AAH	ud4_fdl[y[2:0]]			ud4_rdl[y[6:2]]					00h
ABH	ud4_tp_shift[2:0]		ud4_tp_fb_set		ud4_fdl[y[6:3]]				00h
ACH	ud4_tp_rdl[y[2:0]]			ud4_tp_width[3:0]		ud4_tp_shift[3]			00h
ADH	ud4_tp_fdl[y[3:0]]			ud4_tp_rdl[y[6:3]]					00h
AEH	vdd_vbkl_set[1:0]	ud_swap_order		ud_swap_mode[1:0]		ud4_tp_fdl[y[6:4]]			00h

**Description**

- Please reference to GOA\_UD\_SET1 for further information.

**2.3.42 GOA\_UD\_SWAP\_SET (BANK15H AEH) : GOA UD Swap Setting**

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
AEH	vdd_vbkl_set[1:0]		ud_swap_order	ud_swap_mode[1:0]		ud4_tp_fdl[6:4]			00h

Description
- BANK15H AEH, D[5:3] ud_swap_mode[1:0] : Swap region selection 0 : disable 1 : display stop at odd gate 2 : display stop at even gate 3 : Reserved ud_swap_order : 0 : UD even and odd signals swap (UD1<->UD2, UD3<->UD4) 1: UD signals swap(UD1<->UD3, UD2<->UD4)

### 2.3.43 GOA\_VDD\_SET (BANK15H AEH~B7H) : GOA VDDx Setting

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
AEH	vdd_vbkl_set[1:0]	ud_swap_order	ud_swap_mode[1:0]	ud4_tp_fdl[y6:4]					00h
AFH	vdd_vbkl_set[9:2]								
B0H	vdd1_rshift[2:0]	vdd1_r_fb	vdd1_inv	vdd1_en	vdd_vbkl_set[11:10]				
B1H	vdd1_fshift[3:0]			vdd1_f_fb	vdd1_rshift[5:3]				
B2H	vdd1_rdl[y5:0]					vdd1_f_set	vdd1_fshift[4]		
B3H	vdd1_fdl[y6:0]					vdd1_rdl[y6]	00h		
B4H	vdd2_rshift[4:0]				vdd2_r_fb	vdd2_inv	vdd2_en		
B5H	vdd2_f_set	vdd2_fshift[4:0]				vdd2_f_fb	vdd2_rshift[5]	00h	
B6H	vdd2_fdl[y0]	vdd2_rdl[y6:0]					00h		
B7H	lc1_sel	lc_en	vdd2_fdl[y6:1]						00h

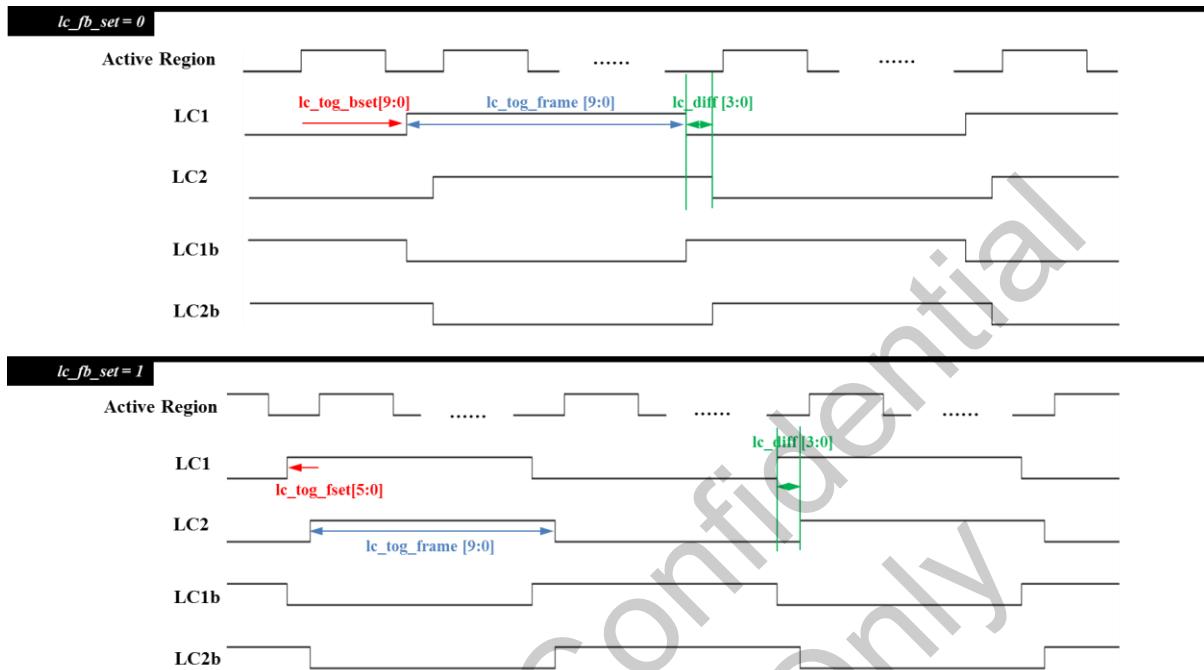
Description
- Please reference to BANK 11H BAH, D[7:0] ~ ECH, D[7:0] for Power sequence of GIP.
- BANK15H AEH, D[7:6] ~ B3H, D[7:0]
vdd_vbkl_set[11:0] : VDD number setting of reference point
vdd1_en : VDD1 enable
vdd1_inv : VDD1 inversion
vdd1_r_fb : 0: VDD1 rising edge locates after reference point    1:VDD1 rising edge locates before reference point
vdd1_rshift[5:0] : Set rising edge of VDD1(unit is line)
vdd1_f_fb : 0:VDD1 falling edge locates after vdd_vbkl_set    1:VDD1 falling edge locates before vdd_vbkl_set
vdd1_fshift[4:0] : Set falling edge of VDD1(unit is line)
vdd1_f_set : VDD1 falling edge selection, 0: vdd1_r(quan)/vdd1_f (sdrss)    1: vdd1_f(quan) / rtn - vdd1_f (sdrss)
vdd1_rdl[y6:0] : Fine tune rising edge of VDD1 signal. In quantification mode, the line is cut into 128 units.
vdd1_fdl[y6:0] : Fine tune falling edge of VDD1 signal. In quantification mode, the line is cut into 128 units.
- BANK15H B4H, D[7:0] ~ B7H, D[5:0]
See VDD1 above for reference
Illustration of VDD settings below.
<p>The diagram illustrates the timing and sequencing of VDD signals across three regions: Active Region, V-blank Region, and Active Region. The signals shown are:</p> <ul style="list-style-type: none"> <li><b>vdd1_rshift[5:0]</b>: A step function indicating the quantization of the rising edge position. It has values 1, 5, 6, and 0 at different points.</li> <li><b>vdd1_fshift[4:0]</b>: A signal indicating the quantization of the falling edge position. It has values 4, 3, 0, and 1 at different points.</li> <li><b>vdd1_fdl[y6:0]</b>: A signal indicating the fine-tuning of the falling edge. It has values 0, 1, 0, and 1 at different points.</li> <li><b>vdd1_rfb</b>: A signal indicating the reference point for the rising edge. It has values 1 and 0 at different points.</li> <li><b>vdd1_ffb</b>: A signal indicating the reference point for the falling edge. It has values 1 and 0 at different points.</li> <li><b>DE</b>: A digital enable signal.</li> </ul>

### 2.3.44 GOA\_LC\_SET (BANK15H B7H~BCH) : GOA LC Setting

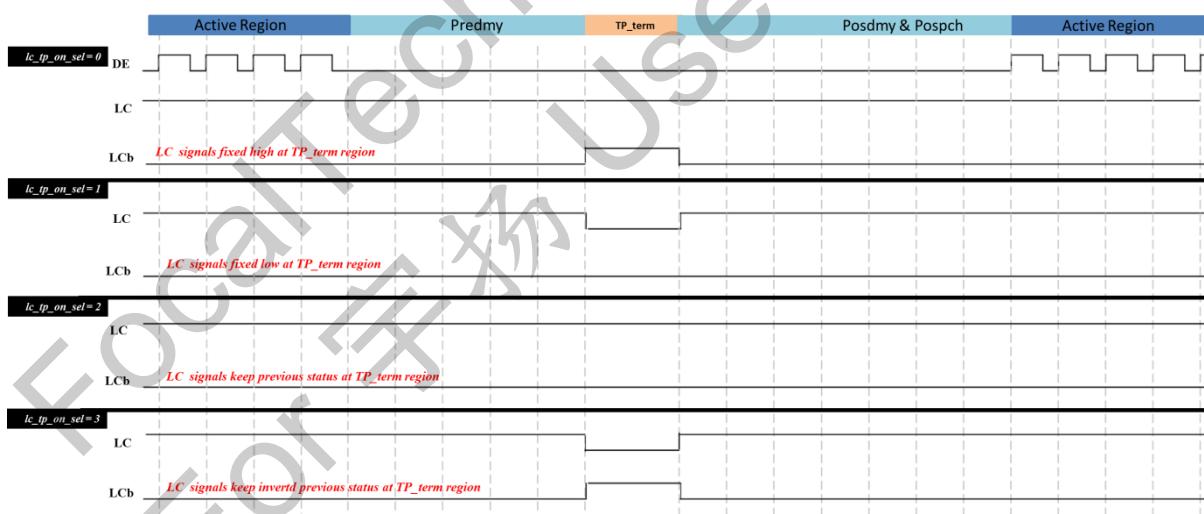
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
B7H	lc1_sel	lc_en			vdd2_fdl[6:1]				00h
B8H			lc1_tog_fset[5:0]			lc_fb_set	lc2_sel		13h
B9H				lc1_tog_bset[7:0]					00h
BAH			lc_tog_frm[5:0]			lc1_tog_bset[9:8]			F0h
BBH		lc2_diff[3:0]			lc_tog_frm[9:6]				00h
BCH	goa_u2d_l_0_sel[0]	gout_inv	topen_inv	lc_vblk_sel	lc_tp_on_sel[1:0]	jdc_mode	lc_mode_se		94h

Description	
<ul style="list-style-type: none"> <li>- These parameters set the LC and LCb signals and LCb is always the inverse of LC. The LC is mainly designed to flip or toggle by frames. Other than that it could toggle every 1 to 1024 frames.</li> </ul>	
<ul style="list-style-type: none"> <li>- Please reference to BANK 11H BAH, D[7:0] ~ ECH, D[7:0] for Power sequence of GIP.</li> </ul>	
<ul style="list-style-type: none"> <li>- BANK15H B7H, D[7:6] ~ BCH, D[4:0]</li> </ul>	
<p>lc_en : LC enable</p> <p>lc1_sel : LC1 power sequence selection 0: LCB power_on sequence 1: LC power_on sequence</p> <p>lc2_sel : LC2 power sequence selection 0: LCB power_on sequence 1: LC power_on sequence</p> <p>lc_fb_set : LC toggle point at 0:end of vactive region interval 1: LC toggle between DE 1st(Lead)</p> <p>lc1_tog_fset[5:0] : LC1 toggle between DE 1st(Lead) and lc1_tog_fset. (unit is line)</p> <p>lc1_tog_bset[9:0] : LC1 toggle point at vact[11:0] + lc1_tog_bset. (unit is line)</p> <p>lc_tog_frm[9:0] : LC1 toggle period [1-1024 frames]</p> <p>lc2_diff[3:0] : difference between lc1 and lc2. (unit is line)</p> <p>lc_mode_sel : LC mode, 0: LC1 lead LC2 1: LC1 overlap LC2</p> <p>jdc_mode : JDC function enable</p> <p>lc_tp_on_sel[1:0] : LC at TP_TERM region 0 : LC fixed high 1 : LC fixed low 2 : LC keep previous status 3 : LC inverted previous status</p> <p>lc_vblk_sel : LC at V-blanking TP_TERM region 0:keep previous status 1:lc_tp_on_sel[1:0]</p>	
<p>Illustrations of different LC settings below.</p> <p>Case1 :</p>	

Case2 :



Case3 :



Note1) Case1 illustrates the LC setting parameters with mode1 ( $lc\_mode\_sel = 2'd0$ ).

Note2) Case2 illustrates the LC setting parameters with mode2 ( $lc\_mode\_sel = 2'd1$ ).

Note3) Case3 illustrates the LC with TP\_TERM setting parameters with mode2 ( $lc\_mode\_sel = 2'd1$ ).

**2.3.45 GOA\_INV\_SET (BANK15H BCH) : GOA INVERT Setting**

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
BCH	goa_u2d_l_0_sel[0]	gout_inv	topen_inv	lc_vblk_sel	lc_tp_on_sel[1:0]	jdc_mode	lc_mode_se_1		94h

Description
- BANK15H BCH, D[6:5]
topen_inv : TP_EN signal inversion
gout_inv : Gout pin signals inversion

**2.3.46 PAN\_U2D\_GOUT\_L\_SET (BANK15H BCH~CDH) : PANEL U2D Left GOUT Setting**

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
BCH	goa_u2d_l_0_sel[0]	gout_inv	topen_inv	lc_vblk_sel	lc_tp_on_sel	jdc_mode	lc_mode_se1	94h	
BDH	goa_u2d_l_1_sel[2:0]				goa_u2d_l_0_sel[5:1]				36h
BEH		goa_u2d_l_2_sel[4:0]			goa_u2d_l_1_sel[5:3]				E4h
BFH	goa_u2d_l_4_sel[0]			goa_u2d_l_3_sel[5:0]			goa_u2d_l_2_sel[5]		04h
C0H	goa_u2d_l_5_sel[2:0]			goa_u2d_l_4_sel[5:1]					43h
C1H		goa_u2d_l_6_sel[4:0]		goa_u2d_l_5_sel[5:3]					71h
C2H	goa_u2d_l_8_sel[0]			goa_u2d_l_7_sel[5:0]			goa_u2d_l_6_sel[5]		38h
C3H	goa_u2d_l_9_sel[2:0]			goa_u2d_l_8_sel[5:1]					50h
C4H		goa_u2d_l_10_sel[4:0]		goa_u2d_l_9_sel[5:3]					95h
C5H	goa_u2d_l_12_sel[0]			goa_u2d_l_11_sel[5:0]			goa_u2d_l_10_sel[5]		ACh
C6H	goa_u2d_l_13_sel[2:0]			goa_u2d_l_12_sel[5:1]					B6h
C7H		goa_u2d_l_14_sel[4:0]		goa_u2d_l_13_sel[5:3]					6Dh
C8H	goa_u2d_l_16_sel[0]			goa_u2d_l_15_sel[5:0]			goa_u2d_l_14_sel[5]		DBh
C9H	goa_u2d_l_17_sel[2:0]			goa_u2d_l_16_sel[5:1]					B6h
CAH		goa_u2d_l_18_sel[4:0]		goa_u2d_l_17_sel[5:3]					6Dh
CBH	goa_u2d_l_20_sel[0]			goa_u2d_l_19_sel[5:0]			goa_u2d_l_18_sel[5]		DBh
CCH	goa_u2d_l_21_sel[2:0]			goa_u2d_l_20_sel[5:1]					B6h
CDH		goa_d2u_l_0_sel[4:0]		goa_u2d_l_21_sel[5:3]					6Dh

Description
-These parameters are used to map internal GOA signals to left side GOA output pad for normal scan (U2D).
- BANK15H BCH, D[7] ~ CDH, D[2:0]
goa_u2d_l_0_sel[5:0] ~ goa_u2d_l_21_sel [5:0] : Forward Left GIP signal selection: 0-45.
Example:
To assign clk_1 to GOA Output PAD GOUT1 during normal scan : set goa_u2d_l_0_sel[5:0] = 6'd0
To assign stv1 to GOA Output PAD GOUT2 during normal scan : set goa_u2d_l_1_sel[5:0] = 6'd16
Note1) The parameters goa_u2d_l_0_sel[5:0] ~ goa_u2d_l_21_sel [5:0] is mapping to GOA Output PAD GOUT1 ~ GOUT22

The illustration below is a GOA PAD mapping table.

Sel[5:0]	Tmgen_signal								
0	clk_1	10	clk_6	20	stv_3	30	lc_2	40	vex
1	clk_1s	11	clk_6s	21	stv_3s	31	lc_2b	41	vds
2	clk_2	12	clk_7	22	stv_4	32	ud_1	42	vgh
3	clk_2s	13	clk_7s	23	stv_4s	33	ud_2	43	vgl
4	clk_3	14	clk_8	24	stv_5	34	ud_3	44	gnd
5	clk_3s	15	clk_8s	25	stv_5s	35	ud_4	45	hi-z
6	clk_4	16	stv_1	26	stv_6	36	vdd_1		
7	clk_4s	17	stv_1s	27	stv_6s	37	vdd_2		
8	clk_5	18	stv_2	28	lc_1	38	vss		
9	clk_5s	19	stv_2s	29	lc_1b	39	tp_term		

**2.3.47 PAN\_D2U\_GOUT\_L\_SET (BANK15H CDH~DDH) : PANEL D2U Left GOUT Setting**

Bank15H											
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default		
CDH	goa_d2u_l_0_sel[4:0]					goa_u2d_l_21_sel[5:3]			6Dh		
CEH	goa_d2u_l_2_sel[0]	goa_d2u_l_1_sel[5:0]					goa_d2u_l_0_sel[5]		43h		
CFH	goa_d2u_l_3_sel[2:0]			goa_d2u_l_2_sel[5:1]					95h		
D0H	goa_d2u_l_4_sel[4:0]					goa_d2u_l_3_sel[5:3]			41h		
D1H	goa_d2u_l_6_sel[0]	goa_d2u_l_5_sel[5:0]					goa_d2u_l_4_sel[5]		08h		
D2H	goa_d2u_l_7_sel[2:0]			goa_d2u_l_6_sel[5:1]					80h		
D3H	goa_d2u_l_8_sel[4:0]					goa_d2u_l_7_sel[5:3]			03h		
D4H	goa_d2u_l_10_sel[0]	goa_d2u_l_9_sel[5:0]					goa_d2u_l_8_sel[5]		39h		
D5H	goa_d2u_l_11_sel[2:0]			goa_d2u_l_10_sel[5:1]					0Ah		
D6H	goa_d2u_l_12_sel[4:0]					goa_d2u_l_11_sel[5:3]			6Ah		
D7H	goa_d2u_l_14_sel[0]	goa_d2u_l_13_sel[5:0]					goa_d2u_l_12_sel[5]		DBh		
D8H	goa_d2u_l_15_sel[2:0]			goa_d2u_l_14_sel[5:1]					B6h		
D9H	goa_d2u_l_16_sel[4:0]					goa_d2u_l_15_sel[5:3]			6Dh		
DAH	goa_d2u_l_18_sel[0]	goa_d2u_l_17_sel[5:0]					goa_d2u_l_16_sel[5]		DBh		
DBH	goa_d2u_l_19_sel[2:0]			goa_d2u_l_18_sel[5:1]					B6h		
DCH	goa_d2u_l_20_sel[4:0]					goa_d2u_l_19_sel[5:3]			6Dh		
DDH	goa_u2d_r_0_sel[0]	goa_d2u_l_21_sel[5:0]					goa_d2u_l_20_sel[5]		DBh		

Description									
-These parameters are used to map internal GOA signals to left side GOA output pad for reverse scan (D2U).									
- BANK15H CDH, D[7:3] ~ DDH, D[6:0]									
goa_d2u_l_0_sel [5:0] ~ goa_d2u_l_21_sel [5:0] : Backward Left GIP signal selection: 0-45.									
- Please reference to PAN_U2D_GOUT_L_SET for further information.									

**2.3.48 PAN\_U2D\_GOUT\_R\_SET (BANK15H DDH~EEH) : PANEL U2D Right GOUT Setting**

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
DDH	goa_u2d_r_0_sel[0]	goa_d2u_l_21_sel[5:0]					goa_d2u_l_20_sel[5]	DBh	
DEH	goa_u2d_r_1_sel[2:0]			goa_u2d_r_0_sel[5:1]				36h	
DFH	goa_u2d_r_2_sel[4:0]				goa_u2d_r_1_sel[5:3]			E4h	
E0H	goa_u2d_r_4_sel[0]	goa_u2d_r_3_sel[5:0]					goa_u2d_r_2_sel[5]	00h	
E1H	goa_u2d_r_5_sel[2:0]			goa_u2d_r_4_sel[5:1]				02h	
E2H	goa_u2d_r_6_sel[4:0]				goa_u2d_r_5_sel[5:3]			61h	
E3H	goa_u2d_r_8_sel[0]	goa_u2d_r_7_sel[5:0]					goa_u2d_r_6_sel[5]	38h	
E4H	goa_u2d_r_9_sel[2:0]			goa_u2d_r_8_sel[5:1]				50h	
E5H	goa_u2d_r_10_sel[4:0]				goa_u2d_r_9_sel[5:3]			85h	
E6H	goa_u2d_r_12_sel[0]	goa_u2d_r_11_sel[5:0]					goa_u2d_r_10_sel[5]	A8h	
E7H	goa_u2d_r_13_sel[2:0]			goa_u2d_r_12_sel[5:1]				B6h	
E8H	goa_u2d_r_14_sel[4:0]				goa_u2d_r_13_sel[5:3]			6Dh	
E9H	goa_u2d_r_16_sel[0]	goa_u2d_r_15_sel[5:0]					goa_u2d_r_14_sel[5]	DBh	
EAH	goa_u2d_r_17_sel[2:0]			goa_u2d_r_16_sel[5:1]				B6h	
EBH	goa_u2d_r_18_sel[4:0]				goa_u2d_r_17_sel[5:3]			6Dh	
ECH	goa_u2d_r_20_sel[0]	goa_u2d_r_19_sel[5:0]					goa_u2d_r_18_sel[5]	DBh	
EDH	goa_u2d_r_21_sel[2:0]			goa_u2d_r_20_sel[5:1]				B6h	
EEH	goa_d2u_r_0_sel[4:0]				goa_u2d_r_21_sel[5:3]			6Dh	

Description
-These parameters are used to map internal GOA signals to right side GOA output pad for normal scan (U2D).
- BANK15H DDH, D[7] ~ EEH, D[2:0]
goa_u2d_r_0_sel [5:0] ~ goa_u2d_r_21_sel [5:0] : Forward Right GIP signal selection: 0-45.
- Please reference to PAN_U2D_GOUT_L_SET for further information.

**2.3.49 PAN\_D2U\_GOUT\_R\_SET (BANK15H EEH~FEH) : PANEL D2U Right GOUT Setting**

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
EEH	goa_d2u_r_0_sel[4:0]					goa_d2u_r_21_sel[5:3]			6Dh
EFH	goa_d2u_r_2_sel[0]	goa_d2u_r_1_sel[5:0]					goa_d2u_r_0_sel[5]	43h	
F0H	goa_d2u_r_3_sel[2:0]			goa_d2u_r_2_sel[5:1]					D5h
F1H	goa_d2u_r_4_sel[4:0]					goa_d2u_r_3_sel[5:3]			51h
F2H	goa_d2u_r_6_sel[0]	goa_d2u_r_5_sel[5:0]					goa_d2u_r_4_sel[5]	0Ch	
F3H	goa_d2u_r_7_sel[2:0]			goa_d2u_r_6_sel[5:1]					81h
F4H	goa_d2u_r_8_sel[4:0]					goa_d2u_r_7_sel[5:3]			03h
F5H	goa_d2u_r_10_sel[0]	goa_d2u_r_9_sel[5:0]					goa_d2u_r_8_sel[5]	39h	
F6H	goa_d2u_r_11_sel[2:0]			goa_d2u_r_10_sel[5:1]					4Bh
F7H	goa_d2u_r_12_sel[4:0]					goa_d2u_r_11_sel[5:3]			6Ah
F8H	goa_d2u_r_14_sel[0]	goa_d2u_r_13_sel[5:0]					goa_d2u_r_12_sel[5]	DBh	
F9H	goa_d2u_r_15_sel[2:0]			goa_d2u_r_14_sel[5:1]					B6h
FAH	goa_d2u_r_16_sel[4:0]					goa_d2u_r_15_sel[5:3]			6Dh
FBH	goa_d2u_r_18_sel[0]	goa_d2u_r_17_sel[5:0]					goa_d2u_r_16_sel[5]	DBh	
FCH	goa_d2u_r_19_sel[2:0]			goa_d2u_r_18_sel[5:1]					B6h
FDH	goa_d2u_r_20_sel[4:0]					goa_d2u_r_19_sel[5:3]			6Dh
FEH	bypass_gpc_h_en	goa_d2u_r_21_sel[5:0]					goa_d2u_r_20_sel[5]	5Bh	

Description	
-These parameters are used to map internal GOA signals to right side GOA output pad for reverse scan (D2U).	
- BANK15H EEH, D[7:3] ~ FEH, D[6:0]	
goa_d2u_r_0_sel [5:0] ~ goa_d2u_r_21_sel [5:0] : Backward Right GIP signal selection: 0-45.	
- Please reference to PAN_U2D_GOUT_L_SET for further information.	

**2.3.50 GOA\_EQ\_SET (BANK15H FEH ~ BANK16H 91H) : GOA EQ Setting**

Bank15H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
FEH	bypass_gpc_h_en		goa_d2u_r_21_sel[5:0]						goa_d2u_r_20_sel[5]
FFH	clk_group1_gpch_r_width[1:0]	other_gpch_fen	clk_gpch_fe	stv_gpch_fe	other_gpch_ren	clk_gpch_re	stv_gpch_re		00h
Bank16H									
80H	clk_group2_gpch_r_width[1:0]		clk_group1_gpch_r_width[7:2]						00h
81H	clk_group1_gpch_f_width[1:0]		clk_group2_gpch_r_width[7:2]						00h
82H	clk_group2_gpch_f_width[1:0]		clk_group1_gpch_f_width [7:2]						00h
83H	stv_group1_gpch_r_width[1:0]		clk_group2_gpch_f_width [7:2]						00h
84H	stv_group2_gpch_r_width[1:0]		stv_group1_gpch_r_width [7:2]						00h
85H	stv_group3_gpch_r_width[1:0]		stv_group2_gpch_r_width [7:2]						00h
86H	stv_group4_gpch_r_width[1:0]		stv_group3_gpch_r_width [7:2]						00h
87H	stv_group1_gpch_f_width[1:0]		stv_group4_gpch_r_width [7:2]						00h
88H	stv_group2_gpch_f_width[1:0]		stv_group1_gpch_f_width [7:2]						00h
89H	stv_group3_gpch_f_width[1:0]		stv_group2_gpch_f_width [7:2]						00h
8AH	stv_group4_gpch_f_width[1:0]		stv_group3_gpch_f_width [7:2]						00h
8BH	avee_gpch_r_width[1:0]		stv_group4_gpch_f_width[7:2]						00h
8CH	gnd_gpch_r_width[1:0]		avee_gpch_r_width [7:2]						00h
8DH	avdd_gpch_r_width[1:0]		gnd_gpch_r_width [7:2]						00h
8EH	avee_gpch_f_width[1:0]		avdd_gpch_r_width [7:2]						00h
8FH	gnd_gpch_f_width[1:0]		avee_gpch_f_width [7:2]						00h
90H	avdd_gpch_f_width[1:0]		gnd_gpch_f_width [7:2]						00h
91H	cog_stv1_o_e_inv_o	cog_stv1_o_e	avdd_gpch_f_width [7:2]						00h

**Description**

- These parameters set gate pre-charge for STV type, CLK type, and the others. The rising and falling edge pre-charge each has an individual setting.

- BANK15H FEH, D[7:5] ~ BANK16H 91H, D[5:0]

bypass\_gpch\_en : All signals power on and power off sequence pre-charge mode enable

stv\_gpch\_ren : STV rising edge pre-charge mode enable

clk\_gpch\_ren : CLK rising edge pre-charge mode enable

other\_gpch\_ren : Others rising edge pre-charge mode enable

stv\_gpch\_fen : STV falling edge pre-charge mode enable

clk\_gpch\_fen : CLK falling edge pre-charge mode enable

other\_gpch\_fen : Others falling edge pre-charge mode enable

clk\_group1\_gpch\_r\_width[7:0] : CLK1-4s rising edge pre-charge to AVSS level width

clk\_group2\_gpch\_r\_width[7:0] : CLK5-8s rising edge pre-charge to AVSS level width

clk\_group1\_gpch\_f\_width[7:0] : CLK1-4s falling edge pre-charge to AVSS level width

clk\_group2\_gpch\_f\_width[7:0] : CLK5-8s falling edge pre-charge to AVSS level width

stv\_group1\_gpch\_r\_width[7:0] : STV1 rising edge pre-charge to AVSS level width

stv\_group2\_gpch\_r\_width[7:0] : STV2 rising edge pre-charge to AVSS level width

stv\_group3\_gpch\_r\_width[7:0] : STV3 rising edge pre-charge to AVSS level width

stv\_group4\_gpch\_r\_width[7:0] : STV4 rising edge pre-charge to AVSS level width

stv\_group1\_gpch\_f\_width[7:0] : STV1 falling edge pre-charge to AVSS level width

stv\_group2\_gpch\_f\_width[7:0] : STV2 falling edge pre-charge to AVSS level width

stv\_group3\_gpch\_f\_width[7:0] : STV3 falling edge pre-charge to AVSS level width

stv\_group4\_gpch\_f\_width[7:0] : STV4 falling edge pre-charge to AVSS level width

avee\_gpch\_r\_width[7:0] : All signals rising edge pre-charge to VPCHN level width

gnd\_gpch\_r\_width[7:0] : Other signals rising edge pre-charge to AVSS level width

avdd\_gpch\_r\_width[7:0] : All signals rising edge pre-charge to VPCHP level width

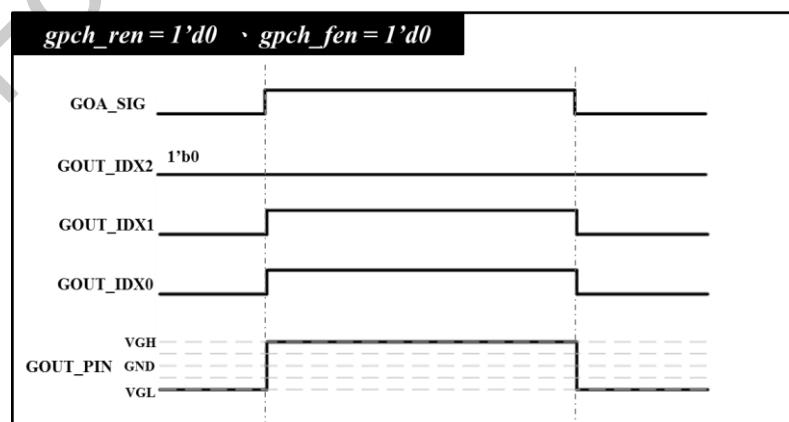
avee\_gpch\_f\_width[7:0] : All signals rising edge pre-charge to VPCHN level width

gnd\_gpch\_f\_width[7:0] : Other signals rising edge pre-charge to AVSS level width

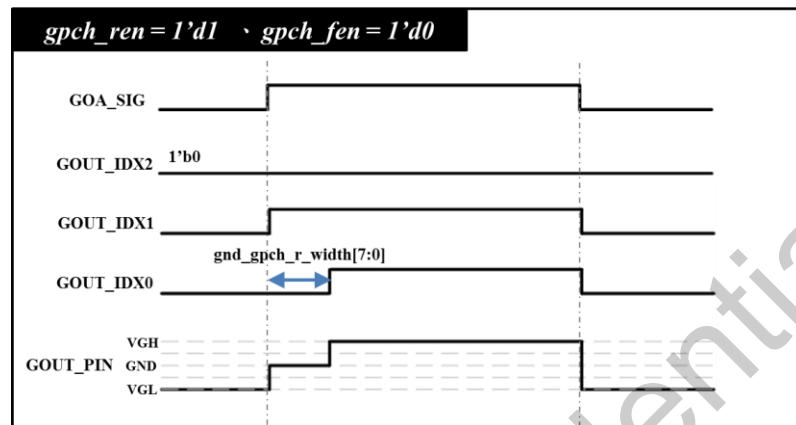
avdd\_gpch\_f\_width[7:0] : All signals rising edge pre-charge to VPCHP level width

Illustrations of 2bit Pre-charge Mode settings below.

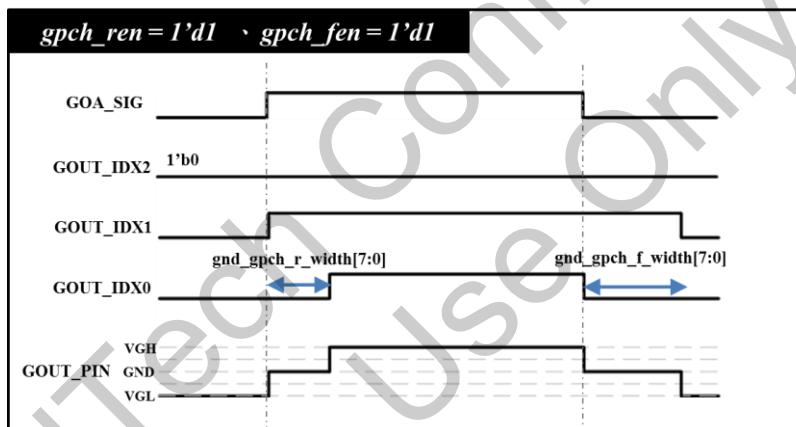
Case1



Case2



Case3



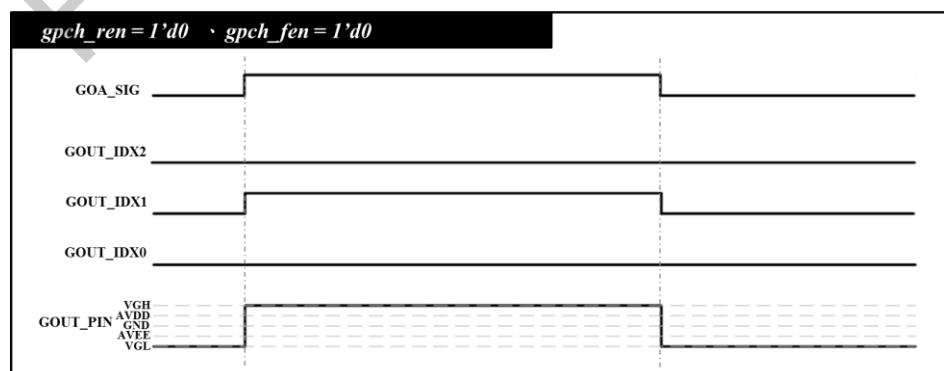
Note1) Case1 illustrates the pre-charge off settings.

Note2) Case2 illustrates the pre-charge falling off settings.

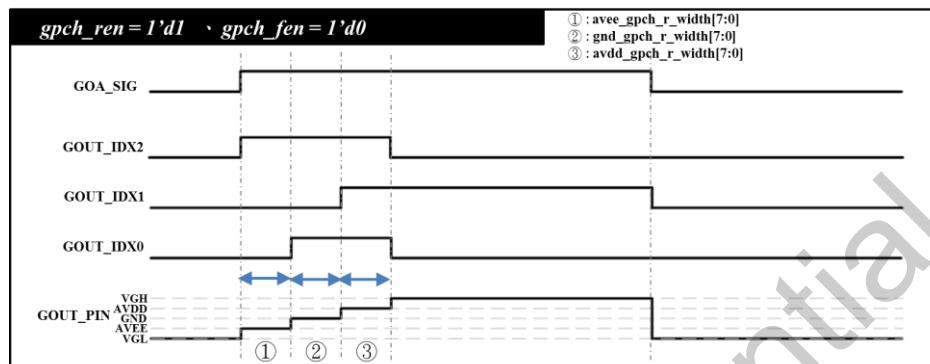
Note3) Case3 illustrates the pre-charge on settings.

Illustrations of 3bit Pre-charge Mode settings below.

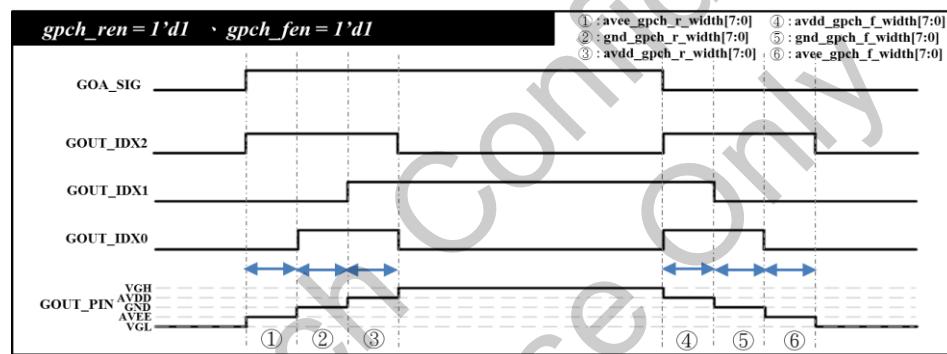
Case4



### Case5



### Case6



Note4) Case4 illustrates the pre-charge off settings.

Note5) Case5 illustrates the pre-charge falling off settings.

Note6) Case6 illustrates the pre-charge on settings.

Note7) Only left GOA Output PAD GOUT 6~13 and right GOA Output PAD GOUT 6~13 support 3bit Pre-charge Mode.

**2.3.51 CE\_SET1 (BANK18H 80H~87H) : Focal CleverColor – Color Enhancement Parameter Setting 1**

Bank18H											
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default		
80H	HUE02[3:0]			HUE01[4:0]					EFh		
81H	HUE04[0]	HUE03[4:0]					HUE02[4]		BDh		
82H	HUE05[3:0]				HUE04[4:1]				F7h		
83H	HUE07[1:0]		HUE06[4:0]				HUE05[4]		DEh		
84H	HUE08[4:0]					HUE07[4:2]			7Bh		
85H	HUE10[2:0]			HUE09[4:0]					EFh		
86H	HUE12[0]	HUE11[4:0]				HUE10[4:3]			BDh		
87H	P1_SAT01[3:0]				HUE12[4:1]				07h		

Description
- BANK18H 80H, D[7:0] ~ 87H, D[3:0] HUE01[4:0] ~ HUE12[4:0] are used for Focal color enhancement algorithm calculation.

**2.3.52 CE\_SET2 (BANK18 87H~93H) : Focal CleverColor – Color Enhancement Parameter Setting 2**

Bank18H										
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default	
87H	P1_SAT01[3:0]					HUE12[4:1]				07h
88H	P1_SAT02[3:0]					P1_SAT01[7:4]				08h
89H	P1_SAT03[3:0]					P1_SAT02[7:4]				08h
8AH	P1_SAT04[3:0]					P1_SAT03[7:4]				0Ah
8BH	P1_SAT05[3:0]					P1_SAT04[7:4]				0Ch
8CH	P1_SAT06[3:0]					P1_SAT05[7:4]				0Ch
8DH	P1_SAT07[3:0]					P1_SAT06[7:4]				0Ch
8EH	P1_SAT08[3:0]					P1_SAT07[7:4]				0Ch
8FH	P1_SAT09[3:0]					P1_SAT08[7:4]				0Ch
90H	P1_SAT10[3:0]					P1_SAT09[7:4]				0Ch
91H	P1_SAT11[3:0]					P1_SAT10[7:4]				0Ch
92H	P1_SAT12[3:0]					P1_SAT11[7:4]				0Ch
93H	P2_SAT01[3:0]					P1_SAT12[7:4]				5Ch

Description
- BANK18 87H, D[7:4] ~ 93H, D[3:0] P1_SAT01[7:0] ~ P1_SAT12[7:0] are used for Focal color enhancement algorithm calculation.

**2.3.53 CE\_SET3 (BANK18 93H~9FH) : Focal CleverColor – Color Enhancement Parameter Setting 3**

Bank18H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
93H				P2_SAT01[3:0]			P1_SAT12[7:4]		5Ch
94H				P2_SAT02[3:0]			P2_SAT01[7:4]		09h
95H				P2_SAT03[3:0]			P2_SAT02[7:4]		A8h
96H				P2_SAT04[3:0]			P2_SAT03[7:4]		AAh
97H				P2_SAT05[3:0]			P2_SAT04[7:4]		AAh
98H				P2_SAT06[3:0]			P2_SAT05[7:4]		AAh
99H				P2_SAT07[3:0]			P2_SAT06[7:4]		AAh
9AH				P2_SAT08[3:0]			P2_SAT07[7:4]		AAh
9BH				P2_SAT09[3:0]			P2_SAT08[7:4]		AAh
9CH				P2_SAT10[3:0]			P2_SAT09[7:4]		AAh
9DH				P2_SAT11[3:0]			P2_SAT10[7:4]		AAh
9EH				P2_SAT12[3:0]			P2_SAT11[7:4]		AAh
9FH				P3_SAT01[3:0]			P2_SAT12[7:4]		5Ah

Description
- BANK18 93H, D[7:4] ~ 9FH, D[3:0] P2_SAT01[7:0] ~ P2_SAT12[7:0] are used for Focal color enhancement algorithm calculation.

**2.3.54 CE\_SET4 (BANK18 9FH~ABH) : Focal CleverColor – Color Enhancement Parameter Setting 4**

Bank18H											
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default		
9FH	P3_SAT01[3:0]					P2_SAT12[7:4]					5Ah
A0H	P3_SAT02[3:0]					P3_SAT01[7:4]					59h
A1H	P3_SAT03[3:0]					P3_SAT02[7:4]					59h
A2H	P3_SAT04[3:0]					P3_SAT03[7:4]					59h
A3H	P3_SAT05[3:0]					P3_SAT04[7:4]					59h
A4H	P3_SAT06[3:0]					P3_SAT05[7:4]					59h
A5H	P3_SAT07[3:0]					P3_SAT06[7:4]					59h
A6H	P3_SAT08[3:0]					P3_SAT07[7:4]					59h
A7H	P3_SAT09[3:0]					P3_SAT08[7:4]					59h
A8H	P3_SAT10[3:0]					P3_SAT09[7:4]					59h
A9H	P3_SAT11[3:0]					P3_SAT10[7:4]					59h
AAH	P3_SAT12[3:0]					P3_SAT11[7:4]					59h
ABH	Reserved					P3_SAT12[7:4]					09h

Description
- BANK18H 9FH, D[7:4] ~ ABH, D[3:0] P3_SAT01[7:0] ~ P3_SAT12[7:0] are used for Focal color enhancement algorithm calculation.

**2.3.55 SHARPN\_SET (BANK18H ACH~ADH) : Focal CleverColor – Sharpness Setting**

Bank18H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
ACH	SHP_YDIFF_L[7:0]								04h
ADH	SHP_YDIFF_H[7:0]								FFh

Description
- BANK18H ACH, D[7:0] ~ ADH, D[7:0]
SHP_YDIFF_L [7:0]: Lower bound limit of Sharpness function. If gray value of the pixel smaller than this Lower bound limit, the pixel will not be operated by Sharpness function.
SHP_YDIFF_H [7:0]: Upper bound limit of Sharpness function. If gray value of the pixel larger than this upper bound limit, the pixel will not be operated by Sharpness function.

**2.3.56 HIS\_SET (BANK18H AFH~B0H) : Focal CleverColor – Histogram Analysis Setting**

Bank18H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
AFH	HIS_RATIO[1:0]		HIS_GAIN[1:0]		CABC_MODE[1:0]		CNTRST_MODE[1:0]		80h
B0H			MANUAL_HISY[7:0]						80h

Description
- BANK18H AFH, D[7:0] ~ B0H, D[7:0]
CNTRST_MODE[1:0] : Set the histogram analysis mode for contrast enhancement.
CABC_MODE[1:0] : Set the histogram analysis mode for cabc.
HIS_GAIN[1:0] : Set the histogram analysis gain value.
HIS_RATIO[1:0] : Set the histogram analysis ratio.
MANUAL_HISY[7:0] : HisY value for manual mode.

**2.3.57 WA\_SET (BANK18H B1H~BDH) : Focal CleverColor – White Adjustment Parameter Setting**

Bank18H																			
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default										
B1H	WA_TYPICAL_R[7:0]								00h										
B2H	WA_TYPICAL_G[4:0]					WA_TYPICAL_R[10:8]			04h										
B3H	WA_TYPICAL_B[1:0]		WA_TYPICAL_G[10:5]					WA_TYPICAL_B[9:2]											
B4H	WA_COOL_R[6:0]								00h										
B5H	W_T_B[10]							WA_COOL_R[10:7]											
B6H	WA_COOL_G[3:0]				WA_COOL_G[10:4]														
B7H	W_C_B[0]	WA_COOL_G[10:4]																	
B8H	WA_COOL_B[8:1]																		
B9H	WA_WARM_R[5:0]						WA_COOL_B[10:9]												
BAH	WA_WARM_G[2:0]				WA_WARM_R[10:5]														
BBH	WA_WARM_G[10:3]																		
BCH	WA_WARM_B[7:0]																		
BDH	Reserved					WA_WARM_B [10:8]													

Description
- BANK19H B1H, D[7:0] ~ BDH, D[2:0]
WA_TYPICAL_R : Focal white adjustment algorithm calculation for TYPICAL mode.
WA_TYPICAL_G : Focal white adjustment algorithm calculation for TYPICAL mode.
WA_TYPICAL_B : Focal white adjustment algorithm calculation for TYPICAL mode.
WA_COOL_R : Focal white adjustment algorithm calculation for COOL mode.
WA_COOL_G : Focal white adjustment algorithm calculation for COOL mode.
WA_COOL_B : Focal white adjustment algorithm calculation for COOL mode.
WA_WARM_R : Focal white adjustment algorithm calculation for WARM mode.
WA_WARM_G : Focal white adjustment algorithm calculation for WARM mode.
WA_WARM_B : Focal white adjustment algorithm calculation for WARM mode.

**2.3.58 CABC\_GAINSET (BANK19H 80H~8BH) : Focal CleverColor – CABC GAIN Setting**

Bank19H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
80H	CABC_GAIN1[7:0]								F0h
81H	CABC_GAIN2[7:0]								D9h
82H	CABC_GAIN3[7:0]								C8h
83H	CABC_GAIN4[7:0]								BAh
84H	CABC_GAIN5[7:0]								AFh
85H	CABC_GAIN6[7:0]								A6h
86H	CABC_GAIN7[7:0]								9Eh
87H	CABC_GAIN8[7:0]								98h
88H	CABC_GAIN9[7:0]								92h
89H	CABC_GAIN10[7:0]								8Dh
8AH	CABC_GAIN11[7:0]								88h
8BH	CABC_GAIN12[7:0]								84h

Description	
- BANK19H 80H, D[7:0] ~ 8BH, D[7:0]	
CABC_GAIN1[7:0] ~ CABC_GAIN12[7:0] : CABC gamma curve gain value.	

**2.3.59 CABC\_PWMSET (BANK19H 8CH~96H) : Focal CleverColor – CABC PWM Setting**

Bank19H										
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default	
8CH	ST_DIMING_FRM[3:0]					MV_DIMING_FRM[3:0]				00h
8DH	UI_PWM_LB[3:0]					UI_DIMING_FRM[3:0]				60h
8EH	UI_PWM_HB[3:0]					UI_PWM_LB[7:4]				F6h
8FH	ST_PWM_LB[3:0]					UI_PWM_HB[7:4]				CFh
90H	ST_PWM_HB[3:0]					ST_PWM_LB[7:4]				FCh
91H	MV_PWM_LB[3:0]					ST_PWM_HB[7:4]				6Fh
92H	MV_PWM_HB[3:0]					MV_PWM_LB[7:4]				F6h
93H	UI_PWM_LB[11:8]					MV_PWM_HB[7:4]				EFh
94H	ST_PWM_LB[11:8]					UI_PWM_HB[11:8]				CFh
95H	MV_PWM_LB[11:8]					ST_PWM_HB[11:8]				AFh
96H	Reserved					MV_PWM_HB[11:8]				0Fh

Description
- BANK19H 8CH, D[7:0] ~ 96H, D[3:0]
MV_DIMING_FRM : CABC dimming frame number for MV mode.
UI_DIMING_FRM : CABC dimming frame number for UI mode.
ST_DIMING_FRM : CABC dimming frame number for ST mode.
MV_PWM_LB : CABC PWM lower bound for MV mode.
MV_PWM_HB : CABC PWM higher bound for MV mode.
UI_PWM_LB : CABC PWM lower bound for UI mode.
UI_PWM_HB : CABC PWM higher bound for UI mode.
ST_PWM_LB : CABC PWM lower bound for ST mode.
ST_PWM_HB : CABC PWM higher bound for ST mode.

**2.3.60 AIE\_PWMSET (BANK19H 97H~98H) : Focal CleverColor – AIE PWM Setting**

Bank19H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
97H	PWM_AIE_DBV[11:4]								FFh
98H	AIE_GAIN1[2:0]			HBM_DIS	PWM_AIE_DBV[3:0]			AFh	

Description
- BANK19H 97H, D[7:0] ~ 98H, D[4:0]
PWM_AIE_DBV[11:0] : PWM setting when AIE on.
HBM_DIS : Disable AIE PWM setting.

**2.3.61 AIE\_GAINSET (BANK19H 98H~9FH) : Focal CleverColor – AIE Gain Setting**

Bank19H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
98H	AIE_GAIN1[2:0]		HBM		PWM_AIE_DBV_LO[3:0]				AFh
99H	AIE_GAIN2[2:0]				AIE_GAIN1[7:3]				B5h
9AH	AIE_GAIN3[2:0]				AIE_GAIN2[7:3]				71h
9BH	AIE_GAIN4[2:0]				AIE_GAIN3[7:3]				0Eh
9CH	AIE_GAIN5[2:0]				AIE_GAIN4[7:3]				6Ch
9DH	AIE_GAIN6[2:0]				AIE_GAIN5[7:3]				4Ah
9EH	AIE_GAIN7[2:0]				AIE_GAIN6[7:3]				69h
9FH	Reserved				AIE_GAIN7[7:3]				08h

Description
- BANK19H 98H, D[7:5] ~ 9FH, D[4:0] AIE_GAIN1[7:0] ~ AIE_GAIN7[7:0] : AIE gamma curve gain value.

### 2.3.62 PWM\_CTRL (BANK19H A0H~A3H) : PWM Pulse Control

Bank19H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
A0H	PWM_DBF_IDLE[7:0]								0FH
A1H	PWM_DBF_NORM[7:0]								0FH
A2H	PWM_DIM_FRM[3:0]				PWM_FREQ_SEL[2:0]		PWM_INV	02h	
A3H	Reserved		DISBV_RD_option[1:0]		PWM_DIM_FRM[7:4]			00h	

Description	
- This command is used to set parameters for PWM pulse controller.	
PWM_INV : BC signal polarity	
PWM_DIM_FRM[3:0] : Set pwm diming frame number	
PWM_DIM_FRM[3:0]	diming frame number
0h	1
1h	2
2h	4
3h	8
4h	16
5h	32
6h	64
7h	128
8h	256
Others	Not Support

DISBV\_RD\_option : Command "Read Display Brightness Value" Option

00 : Display Brightness

01 : PWM Value

PWM\_DBF\_IDLE[7:0] : Adjust PWM pulse frequency in idle mode

PWM\_DBF\_NORM[7:0] : Adjust PWM pulse frequency in normal mode

PWM\_FREQ\_SEL[2:0] : Select PWM adjustment frequency

DBF	PWM_FREQ_SEL[2:0] (KHz)					DBF	PWM_FREQ_SEL[2:0] (KHz)					DBF	PWM_FREQ_SEL[2:0] (KHz)				
	000	001	010	011	100		000	001	010	011	100		000	001	010	011	100
0	68.36	136.7	34.18	17.09	8.545	86	0.786	1.571	0.393	0.196	0.098	172	0.395	0.79	0.198	0.099	0.049
1	34.18	68.36	17.09	8.545	4.272	87	0.777	1.554	0.388	0.194	0.097	173	0.393	0.786	0.196	0.098	0.049
2	22.79	45.57	11.39	5.697	2.848	88	0.768	1.536	0.384	0.192	0.096	174	0.391	0.781	0.195	0.098	0.049
3	17.09	34.18	8.545	4.272	2.136	89	0.76	1.519	0.38	0.19	0.095	175	0.388	0.777	0.194	0.097	0.049
4	13.67	27.34	6.836	3.418	1.709	90	0.751	1.502	0.376	0.188	0.094	176	0.386	0.772	0.193	0.097	0.048
5	11.39	22.79	5.697	2.848	1.424	91	0.743	1.486	0.372	0.186	0.093	177	0.384	0.768	0.192	0.096	0.048
6	9.766	19.53	4.883	2.441	1.221	92	0.735	1.47	0.368	0.184	0.092	178	0.382	0.764	0.191	0.095	0.048

7	8.545	17.09	4.272	2.136	1.068	93	0.727	1.454	0.364	0.182	0.091	179	0.38	0.76	0.19	0.095	0.047
8	7.595	15.19	3.798	1.899	0.949	94	0.72	1.439	0.36	0.18	0.09	180	0.378	0.755	0.189	0.094	0.047
9	6.836	13.67	3.418	1.709	0.854	95	0.712	1.424	0.356	0.178	0.089	181	0.376	0.751	0.188	0.094	0.047
10	6.214	12.43	3.107	1.554	0.777	96	0.705	1.409	0.352	0.176	0.088	182	0.374	0.747	0.187	0.093	0.047
11	5.697	11.39	2.848	1.424	0.712	97	0.698	1.395	0.349	0.174	0.087	183	0.372	0.743	0.186	0.093	0.046
12	5.258	10.52	2.629	1.315	0.657	98	0.69	1.381	0.345	0.173	0.086	184	0.37	0.739	0.185	0.092	0.046
13	4.883	9.766	2.441	1.221	0.61	99	0.684	1.367	0.342	0.171	0.085	185	0.368	0.735	0.184	0.092	0.046
14	4.557	9.115	2.279	1.139	0.57	100	0.677	1.354	0.338	0.169	0.085	186	0.366	0.731	0.183	0.091	0.046
15	4.272	8.545	2.136	1.068	0.534	101	0.67	1.34	0.335	0.168	0.084	187	0.364	0.727	0.182	0.091	0.045
16	4.021	8.042	2.011	1.005	0.503	102	0.664	1.327	0.332	0.166	0.083	188	0.362	0.723	0.181	0.09	0.045
17	3.798	7.595	1.899	0.949	0.475	103	0.657	1.315	0.329	0.164	0.082	189	0.36	0.72	0.18	0.09	0.045
18	3.598	7.196	1.799	0.899	0.45	104	0.651	1.302	0.326	0.163	0.081	190	0.358	0.716	0.179	0.089	0.045
19	3.418	6.836	1.709	0.854	0.427	105	0.645	1.29	0.322	0.161	0.081	191	0.356	0.712	0.178	0.089	0.045
20	3.255	6.51	1.628	0.814	0.407	106	0.639	1.278	0.319	0.16	0.08	192	0.354	0.708	0.177	0.089	0.044
21	3.107	6.214	1.554	0.777	0.388	107	0.633	1.266	0.316	0.158	0.079	193	0.352	0.705	0.176	0.088	0.044
22	2.972	5.944	1.486	0.743	0.372	108	0.627	1.254	0.314	0.157	0.078	194	0.351	0.701	0.175	0.088	0.044
23	2.848	5.697	1.424	0.712	0.356	109	0.621	1.243	0.311	0.155	0.078	195	0.349	0.698	0.174	0.087	0.044
24	2.734	5.469	1.367	0.684	0.342	110	0.616	1.232	0.308	0.154	0.077	196	0.347	0.694	0.174	0.087	0.043
25	2.629	5.258	1.315	0.657	0.329	111	0.61	1.221	0.305	0.153	0.076	197	0.345	0.69	0.173	0.086	0.043
26	2.532	5.064	1.266	0.633	0.316	112	0.605	1.21	0.302	0.151	0.076	198	0.344	0.687	0.172	0.086	0.043
27	2.441	4.883	1.221	0.61	0.305	113	0.6	1.199	0.3	0.15	0.075	199	0.342	0.684	0.171	0.085	0.043
28	2.357	4.714	1.179	0.589	0.295	114	0.594	1.189	0.297	0.149	0.074	200	0.34	0.68	0.17	0.085	0.043
29	2.279	4.557	1.139	0.57	0.285	115	0.589	1.179	0.295	0.147	0.074	201	0.338	0.677	0.169	0.085	0.042
30	2.205	4.41	1.103	0.551	0.276	116	0.584	1.169	0.292	0.146	0.073	202	0.337	0.673	0.168	0.084	0.042
31	2.136	4.272	1.068	0.534	0.267	117	0.579	1.159	0.29	0.145	0.072	203	0.335	0.67	0.168	0.084	0.042
32	2.071	4.143	1.036	0.518	0.259	118	0.574	1.149	0.287	0.144	0.072	204	0.333	0.667	0.167	0.083	0.042
33	2.011	4.021	1.005	0.503	0.251	119	0.57	1.139	0.285	0.142	0.071	205	0.332	0.664	0.166	0.083	0.041
34	1.953	3.906	0.977	0.488	0.244	120	0.565	1.13	0.282	0.141	0.071	206	0.33	0.66	0.165	0.083	0.041
35	1.899	3.798	0.949	0.475	0.237	121	0.56	1.121	0.28	0.14	0.07	207	0.329	0.657	0.164	0.082	0.041
36	1.848	3.695	0.924	0.462	0.231	122	0.556	1.112	0.278	0.139	0.069	208	0.327	0.654	0.164	0.082	0.041
37	1.799	3.598	0.899	0.45	0.225	123	0.551	1.103	0.276	0.138	0.069	209	0.326	0.651	0.163	0.081	0.041
38	1.753	3.506	0.876	0.438	0.219	124	0.547	1.094	0.273	0.137	0.068	210	0.324	0.648	0.162	0.081	0.04
39	1.709	3.418	0.854	0.427	0.214	125	0.543	1.085	0.271	0.136	0.068	211	0.322	0.645	0.161	0.081	0.04
40	1.667	3.335	0.834	0.417	0.208	126	0.538	1.077	0.269	0.135	0.067	212	0.321	0.642	0.16	0.08	0.04
41	1.628	3.255	0.814	0.407	0.203	127	0.534	1.068	0.267	0.134	0.067	213	0.319	0.639	0.16	0.08	0.04
42	1.59	3.18	0.795	0.397	0.199	128	0.53	1.06	0.265	0.132	0.066	214	0.318	0.636	0.159	0.079	0.04
43	1.554	3.107	0.777	0.388	0.194	129	0.526	1.052	0.263	0.131	0.066	215	0.316	0.633	0.158	0.079	0.04
44	1.519	3.038	0.76	0.38	0.19	130	0.522	1.044	0.261	0.13	0.065	216	0.315	0.63	0.158	0.079	0.039

45	1.486	2.972	0.743	0.372	0.186	131	0.518	1.036	0.259	0.129	0.065	217	0.314	0.627	0.157	0.078	0.039
46	1.454	2.909	0.727	0.364	0.182	132	0.514	1.028	0.257	0.128	0.064	218	0.312	0.624	0.156	0.078	0.039
47	1.424	2.848	0.712	0.356	0.178	133	0.51	1.02	0.255	0.128	0.064	219	0.311	0.621	0.155	0.078	0.039
48	1.395	2.79	0.698	0.349	0.174	134	0.506	1.013	0.253	0.127	0.063	220	0.309	0.619	0.155	0.077	0.039
49	1.367	2.734	0.684	0.342	0.171	135	0.503	1.005	0.251	0.126	0.063	221	0.308	0.616	0.154	0.077	0.038
50	1.34	2.681	0.67	0.335	0.168	136	0.499	0.998	0.249	0.125	0.062	222	0.307	0.613	0.153	0.077	0.038
51	1.315	2.629	0.657	0.329	0.164	137	0.495	0.991	0.248	0.124	0.062	223	0.305	0.61	0.153	0.076	0.038
52	1.29	2.58	0.645	0.322	0.161	138	0.492	0.984	0.246	0.123	0.061	224	0.304	0.608	0.152	0.076	0.038
53	1.266	2.532	0.633	0.316	0.158	139	0.488	0.977	0.244	0.122	0.061	225	0.302	0.605	0.151	0.076	0.038
54	1.243	2.486	0.621	0.311	0.155	140	0.485	0.97	0.242	0.121	0.061	226	0.301	0.602	0.151	0.075	0.038
55	1.221	2.441	0.61	0.305	0.153	141	0.481	0.963	0.241	0.12	0.06	227	0.3	0.6	0.15	0.075	0.037
56	1.199	2.399	0.6	0.3	0.15	142	0.478	0.956	0.239	0.12	0.06	228	0.299	0.597	0.149	0.075	0.037
57	1.179	2.357	0.589	0.295	0.147	143	0.475	0.949	0.237	0.119	0.059	229	0.297	0.594	0.149	0.074	0.037
58	1.159	2.317	0.579	0.29	0.145	144	0.471	0.943	0.236	0.118	0.059	230	0.296	0.592	0.148	0.074	0.037
59	1.139	2.279	0.57	0.285	0.142	145	0.468	0.936	0.234	0.117	0.059	231	0.295	0.589	0.147	0.074	0.037
60	1.121	2.241	0.56	0.28	0.14	146	0.465	0.93	0.233	0.116	0.058	232	0.293	0.587	0.147	0.073	0.037
61	1.103	2.205	0.551	0.276	0.138	147	0.462	0.924	0.231	0.115	0.058	233	0.292	0.584	0.146	0.073	0.037
62	1.085	2.17	0.543	0.271	0.136	148	0.459	0.918	0.229	0.115	0.057	234	0.291	0.582	0.145	0.073	0.036
63	1.068	2.136	0.534	0.267	0.134	149	0.456	0.911	0.228	0.114	0.057	235	0.29	0.579	0.145	0.072	0.036
64	1.052	2.103	0.526	0.263	0.131	150	0.453	0.905	0.226	0.113	0.057	236	0.288	0.577	0.144	0.072	0.036
65	1.036	2.071	0.518	0.259	0.129	151	0.45	0.899	0.225	0.112	0.056	237	0.287	0.574	0.144	0.072	0.036
66	1.02	2.041	0.51	0.255	0.128	152	0.447	0.894	0.223	0.112	0.056	238	0.286	0.572	0.143	0.072	0.036
67	1.005	2.011	0.503	0.251	0.126	153	0.444	0.888	0.222	0.111	0.055	239	0.285	0.57	0.142	0.071	0.036
68	0.991	1.981	0.495	0.248	0.124	154	0.441	0.882	0.221	0.11	0.055	240	0.284	0.567	0.142	0.071	0.035
69	0.977	1.953	0.488	0.244	0.122	155	0.438	0.876	0.219	0.11	0.055	241	0.282	0.565	0.141	0.071	0.035
70	0.963	1.926	0.481	0.241	0.12	156	0.435	0.871	0.218	0.109	0.054	242	0.281	0.563	0.141	0.07	0.035
71	0.949	1.899	0.475	0.237	0.119	157	0.433	0.865	0.216	0.108	0.054	243	0.28	0.56	0.14	0.07	0.035
72	0.936	1.873	0.468	0.234	0.117	158	0.43	0.86	0.215	0.107	0.054	244	0.279	0.558	0.14	0.07	0.035
73	0.924	1.848	0.462	0.231	0.115	159	0.427	0.854	0.214	0.107	0.053	245	0.278	0.556	0.139	0.069	0.035
74	0.911	1.823	0.456	0.228	0.114	160	0.425	0.849	0.212	0.106	0.053	246	0.277	0.554	0.138	0.069	0.035
75	0.899	1.799	0.45	0.225	0.112	161	0.422	0.844	0.211	0.105	0.053	247	0.276	0.551	0.138	0.069	0.034
76	0.888	1.776	0.444	0.222	0.111	162	0.419	0.839	0.21	0.105	0.052	248	0.275	0.549	0.137	0.069	0.034
77	0.876	1.753	0.438	0.219	0.11	163	0.417	0.834	0.208	0.104	0.052	249	0.273	0.547	0.137	0.068	0.034
78	0.865	1.731	0.433	0.216	0.108	164	0.414	0.829	0.207	0.104	0.052	250	0.272	0.545	0.136	0.068	0.034
79	0.854	1.709	0.427	0.214	0.107	165	0.412	0.824	0.206	0.103	0.051	251	0.271	0.543	0.136	0.068	0.034
80	0.844	1.688	0.422	0.211	0.105	166	0.409	0.819	0.205	0.102	0.051	252	0.27	0.54	0.135	0.068	0.034
81	0.834	1.667	0.417	0.208	0.104	167	0.407	0.814	0.203	0.102	0.051	253	0.269	0.538	0.135	0.067	0.034
82	0.824	1.647	0.412	0.206	0.103	168	0.404	0.809	0.202	0.101	0.051	254	0.268	0.536	0.134	0.067	0.034

83	0.814	1.628	0.407	0.203	0.102	169	0.402	0.804	0.201	0.101	0.05	255	0.267	0.534	0.134	0.067	0.033
84	0.804	1.608	0.402	0.201	0.101	170	0.4	0.8	0.2	0.1	0.05						
85	0.795	1.59	0.397	0.199	0.099	171	0.397	0.795	0.199	0.099	0.05						

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**2.3.63 DGAM\_R (BANK1AH 80H~B0H) : Focal CleverColor – Digital Gamma R Setting**

Bank1AH									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
80H					Integer_R0[7:0]				00h
81H					Integer_R4[7:0]				04h
82H					Integer_R8[7:0]				08h
83H					Integer_R12[7:0]				0Ch
84H	Decimal_R12[1:0]		Decimal_R8[1:0]		Decimal_R4[1:0]		Decimal_R0[1:0]		00h
85H					Integer_R16[7:0]				10h
86H					Integer_R20[7:0]				14h
87H					Integer_R24[7:0]				18h
88H					Integer_R28[7:0]				1Ch
89H	Decimal_R28[1:0]		Decimal_R24[1:0]		Decimal_R20[1:0]		Decimal_R16[1:0]		00h
8AH					Integer_R32[7:0]				20h
8BH					Integer_R40[7:0]				28h
8CH					Integer_R48[7:0]				30h
8DH					Integer_R56[7:0]				38h
8EH	Decimal_R56[1:0]		Decimal_R48[1:0]		Decimal_R40[1:0]		Decimal_R32[1:0]		00h
8FH					Integer_R64[7:0]				40h
90H					Integer_R72[7:0]				48h
91H					Integer_R80[7:0]				50h
92H					Integer_R88[7:0]				58h
93H	Decimal_R88[1:0]		Decimal_R80[1:0]		Decimal_72[1:0]		Decimal_R64[1:0]		00h
94H					Integer_R96[7:0]				60h
95H					Integer_R104[7:0]				68h
96H					Integer_R112[7:0]				70h
97H					Integer_R120[7:0]				78h
98H	Decimal_R120[1:0]		Decimal_R112[1:0]		Decimal_R104[1:0]		Decimal_R96[1:0]		00h
99H					Integer_R128[7:0]				80h
9AH					Integer_R136[7:0]				88h
9BH					Integer_R144[7:0]				90h
9CH					Integer_R152[7:0]				98h
9DH	Decimal_R152[1:0]		Decimal_R144[1:0]		Decimal_R136[1:0]		Decimal_R128[1:0]		00h
9EH					Integer_R160[7:0]				A0h
9FH					Integer_R168[7:0]				A8h
A0H					Integer_R176[7:0]				B0h
A1H					Integer_R184[7:0]				B8h
A2H	Decimal_R184[1:0]		Decimal_R176[1:0]		Decimal_R168[1:0]		Decimal_R160[1:0]		00h
A3H					Integer_R192[7:0]				C0h
A4H					Integer_R200[7:0]				C8h
A5H					Integer_R208[7:0]				D0h
A6H					Integer_R216[7:0]				D8h
A7H	Decimal_R216[1:0]		Decimal_R208[1:0]		Decimal_R200[1:0]		Decimal_R192[1:0]		00h

A8H	Integer_R224[7:0]				E0h
A9H	Integer_R232[7:0]				E8h
AAH	Integer_R240[7:0]				F0h
ABH	Integer_R248[7:0]				F8h
ACH	Decimal_R248[1:0]	Decimal_R240[1:0]	Decimal_R232[1:0]	Decimal_R224[1:0]	00h
ADH	Integer_R252[7:0]				FCh
AEH	Integer_R254[7:0]				FEh
AFH	Integer_R255[7:0]				FFh
B0H	0	0	Decimal_R255[1:0]	Decimal_R254[1:0]	Decimal_R252[1:0]
					00h

Description
<p>- BANK1AH 80H, D[7:0] ~ B0H, D[5:0]:</p> <p>Integer_R# : 0 ~ 255</p> <p>Decimal_R# :</p> <ul style="list-style-type: none"> <li>00 → .00</li> <li>01 → .25</li> <li>10 → .50</li> <li>11 → .75</li> </ul> <p>Example :</p> <p>R252 = 240.25  R254 = 248.5  R255 = 252.75</p> <p>Bank Select : (0x51, 0x1A)</p> <p>Write Command : (0xAD, 0xf0, 0xf8, 0xfc, 0x39)</p>

**2.3.64 DGAM\_G (BANK1AH B1H~E1H) : Focal CleverColor – Digital Gamma G Setting**

Bank1AH																
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default							
B1H					Integer_G0[7:0]							00h				
B2H					Integer_G4[7:0]							04h				
B3H					Integer_G8[7:0]							08h				
B4H					Integer_G12[7:0]							0Ch				
B5H	Decimal_G12[1:0]		Decimal_G8[1:0]		Decimal_G4[1:0]		Decimal_G0[1:0]		00h							
B6H					Integer_G16[7:0]							10h				
B7H					Integer_G20[7:0]							14h				
B8H					Integer_G24[7:0]							18h				
B9H					Integer_G28[7:0]							1Ch				
BAH	Decimal_G28[1:0]		Decimal_G24[1:0]		Decimal_G20[1:0]		Decimal_G16[1:0]		00h							
BBH					Integer_G32[7:0]							20h				
BCH					Integer_G40[7:0]							28h				
BDH					Integer_G48[7:0]							30h				
BEH					Integer_G56[7:0]							38h				
BFH	Decimal_G56[1:0]		Decimal_G48[1:0]		Decimal_G40[1:0]		Decimal_G32[1:0]		00h							
C0H					Integer_G64[7:0]							40h				
C1H					Integer_G72[7:0]							48h				
C2H					Integer_G80[7:0]							50h				
C3H					Integer_G88[7:0]							58h				
C4H	Decimal_G88[1:0]		Decimal_G80[1:0]		Decimal_72[1:0]		Decimal_G64[1:0]		00h							
C5H					Integer_G96[7:0]							60h				
C6H					Integer_G104[7:0]							68h				
C7H					Integer_G112[7:0]							70h				
C8H					Integer_G120[7:0]							78h				
C9H	Decimal_G120[1:0]		Decimal_G112[1:0]		Decimal_G104[1:0]		Decimal_G96[1:0]		00h							
CAH					Integer_G128[7:0]							80h				
CBH					Integer_G136[7:0]							88h				
CCH					Integer_G144[7:0]							90h				
CDH					Integer_G152[7:0]							98h				
CEH	Decimal_G152[1:0]		Decimal_G144[1:0]		Decimal_G136[1:0]		Decimal_G128[1:0]		00h							
CFH					Integer_G160[7:0]							A0h				
D0H					Integer_G168[7:0]							A8h				
D1H					Integer_G176[7:0]							B0h				
D2H					Integer_G184[7:0]							B8h				
D3H	Decimal_G184[1:0]		Decimal_G176[1:0]		Decimal_G168[1:0]		Decimal_G160[1:0]		00h							
D4H					Integer_G192[7:0]							C0h				
D5H					Integer_G200[7:0]							C8h				
D6H					Integer_G208[7:0]							D0h				
D7H					Integer_G216[7:0]							D8h				
D8H	Decimal_G216[1:0]		Decimal_G208[1:0]		Decimal_G200[1:0]		Decimal_G192[1:0]		00h							

D9H	Integer_G224[7:0]				E0h
DAH	Integer_G232[7:0]				E8h
DBH	Integer_G240[7:0]				F0h
DCH	Integer_G248[7:0]				F8h
DDH	Decimal_G248[1:0]	Decimal_G240[1:0]	Decimal_G232[1:0]	Decimal_G224[1:0]	00h
DEH	Integer_G252[7:0]				FCh
DFH	Integer_G254[7:0]				FEh
E0H	Integer_G255[7:0]				FFh
E1H	0	0	Decimal_G255[1:0]	Decimal_G254[1:0]	Decimal_G252[1:0]
					00h

Description
<p>- BANK1AH B1H, D[7:0] ~ E1H, D[5:0]:</p> <p>Integer_G# : 0 ~ 255</p> <p>Decimal_G# :</p> <ul style="list-style-type: none"> <li>00 → .00</li> <li>01 → .25</li> <li>10 → .50</li> <li>11 → .75</li> </ul> <p>Example :</p> <p>G252 = 240.25</p> <p>G254 = 248.5</p> <p>G255 = 252.75</p> <p>Bank Select : (0x51, 0x1A)</p> <p>Write Command : (0xDE, 0xf0, 0xf8, 0xfc, 0x39)</p>

**2.3.65 DGAM\_B (BANK1AH E2H ~ BANK1BH 12H) : Focal CleverColor – Digital Gamma B Setting**

Bank1AH									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
E2H					Integer_B0[7:0]				00h
E3H					Integer_B4[7:0]				04h
E4H					Integer_B8[7:0]				08h
E5H					Integer_B12[7:0]				0Ch
E6H	Decimal_B12[1:0]		Decimal_B8[1:0]		Decimal_B4[1:0]		Decimal_B0[1:0]		00h
E7H					Integer_B16[7:0]				10h
E8H					Integer_B20[7:0]				14h
E9H					Integer_B24[7:0]				18h
EAH					Integer_B28[7:0]				1Ch
EBH	Decimal_B28[1:0]		Decimal_B24[1:0]		Decimal_B20[1:0]		Decimal_B16[1:0]		00h
ECH					Integer_B32[7:0]				20h
EDH					Integer_B40[7:0]				28h
EEH					Integer_B48[7:0]				30h
EFH					Integer_B56[7:0]				38h
F0H	Decimal_B56[1:0]		Decimal_B48[1:0]		Decimal_B40[1:0]		Decimal_B32[1:0]		00h
F1H					Integer_B64[7:0]				40h
F2H					Integer_B72[7:0]				48h
F3H					Integer_B80[7:0]				50h
F4H					Integer_B88[7:0]				58h
F5H	Decimal_B88[1:0]		Decimal_B80[1:0]		Decimal_72[1:0]		Decimal_B64[1:0]		00h
F6H					Integer_B96[7:0]				60h
F7H					Integer_B104[7:0]				68h
F8H					Integer_B112[7:0]				70h
F9H					Integer_B120[7:0]				78h
FAH	Decimal_B120[1:0]		Decimal_B112[1:0]		Decimal_B104[1:0]		Decimal_B96[1:0]		00h
FBH					Integer_B128[7:0]				80h
FCH					Integer_B136[7:0]				88h
FDH					Integer_B144[7:0]				90h
FEH					Integer_B152[7:0]				98h
FFH	Decimal_B152[1:0]		Decimal_B144[1:0]		Decimal_B136[1:0]		Decimal_B128[1:0]		00h
Bank1BH									
80H					Integer_B160[7:0]				A0h
81H					Integer_B168[7:0]				A8h
82H					Integer_B176[7:0]				B0h
83H					Integer_B184[7:0]				B8h
84H	Decimal_B184[1:0]		Decimal_B176[1:0]		Decimal_B168[1:0]		Decimal_B160[1:0]		00h
85H					Integer_B192[7:0]				C0h
86H					Integer_B200[7:0]				C8h
87H					Integer_B208[7:0]				D0h
88H					Integer_B216[7:0]				D8h

89H	Decimal_B216[1:0]	Decimal_B208[1:0]	Decimal_B200[1:0]	Decimal_B192[1:0]	00h
8AH			Integer_B224[7:0]		E0h
8BH			Integer_B232[7:0]		E8h
8CH			Integer_B240[7:0]		F0h
8DH			Integer_B248[7:0]		F8h
8EH	Decimal_B248[1:0]	Decimal_B240[1:0]	Decimal_B232[1:0]	Decimal_B224[1:0]	00h
8FH			Integer_B252[7:0]		FCh
90H			Integer_B254[7:0]		FEh
91H			Integer_B255[7:0]		FFh
92H	0	0	Decimal_B255[1:0]	Decimal_B254[1:0]	Decimal_B252[1:0]
					00h

Description
- BANK1AH E2H, D[7:0] ~ BANK1BH 12H, D[5:0]:
Intger_B# : 0 ~ 255
Decimal_B# :
00 → .00
01 → .25
10 → .50
11 → .75
Example :
B252 = 240.25
B254 = 248.5
B255 = 252.75
Bank Select : (0x51, 0x1B)
Write Command : (0x8F, 0xf0, 0xf8, 0xfc, 0x39)

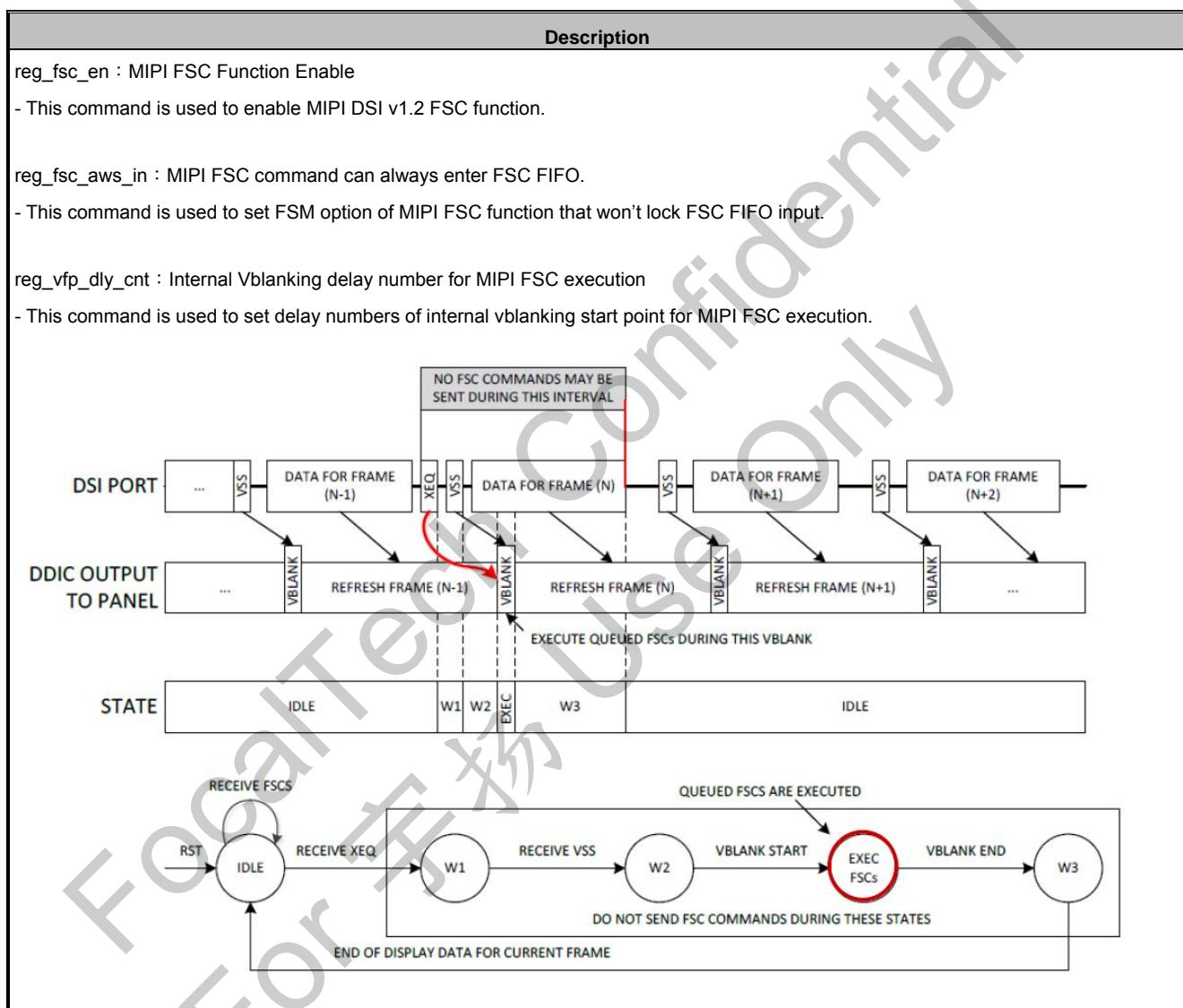
**2.3.66 VCOM\_GVDD\_Set (BANK22H 8BH) : VCOM and GVDD parameter setting**

Bank22H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
8BH	Internal Used	Reserved		vcom_gnd_ master_en[0]	vcom_mas ter_en[0]	Reserved	gvdd_master _en[0]	Internal Used	1Eh

Description
- BANK 22H 8BH, D[6:1]
gvdd_master_en[0] : 1'b1 = Enable Master GVDD. 1'b0 = Disable Master GVDD
vcom_master_en[0] : 1'b1 = Enable Master VCOM. 1'b0 = Disable Master VCOM
vcom_gnd_master_en[0] : If VCOM disable. 1'b1: VCOM pull low. 1'b0: VCOM floating
Note: if use external VCOM. Please setting vcom_master_en and vcom_gnd_master_en.
vcom_master_en[0] = 1'b0
vcom_gnd_master_en[0] = 1'b0

### 2.3.67 FSC\_SET (BANK23H 80H) : MIPI FSC Setting

Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
80H						reg_fsc_aw_s_in	Reserved	reg_fsc_en	01h



**2.3.68 PWM\_EN (BANK23H 83H) : PWM Enable**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
83H		Reserved			reg_PWM_en[3:0]				05h

Description
reg_PWM_en : PWM Enable
'Ah' = Disable
'Others' = Enable

**2.3.70 FCC\_CE (BANK23H 86H ~ 87H) : Focal CleverColor – Color Enhancement**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
86H	CE_SEL[6:0]						ENA	00h	
87H	Reserved				CE_SKIN[3:0]				00h

Description
- This command is used to set Focal CleverColor Color Enhancement function - ENA : Color Enhancement function enable - CE_SEL[6:0] : Select Color Enhancement function gamma curve - CE_SKIN[3:0] : Adjust skin tone function  Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL" It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.71 FCC\_SHARPN (BANK23H 88H~89H) : Focal CleverColor – Sharpness**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
88H	SHP_GAIN_PLUS[3:0]					SHP_SLOPE[2:0]		ENA	00h
89H	Reserved					SHP_GAIN_MINUS[3:0]			00h

Description				
This command is used to set Focal CleverColor Sharpness function				
- ENA : Sharpness function enable.				
- SHP_SLOPE : Sharpness Slope Setting				
- SHP_GAIN_PLUS[3:0]/SHP_GAIN_MINUS[3:0] : Set Sharpness function gain ratio.				
G IN_P[3:0]/GAIN_M[3:0]	Gain Ratio	GAIN_P[3:0]/GAIN_M[3:0]	Gain Ratio	
0h	0	8h	0.8	
1h	0.1	9h	0.9	
2h	0.2	Ah	1.0	
3h	0.3	Bh	1.1	
4h	0.4	Ch	1.2	
5h	0.5	Dh	1.3	
6h	0.6	Eh	1.4	
7h	0.7	Fh	1.5	

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL"  
It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.72 FCC\_CNTRST (BANK23H 8AH~8CH) : Focal CleverColor – Contrast Enhancement**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
8AH	CNTRST_LEVEL[5:0]					ADJ_MODE	ENA	00h	
8BH	CNTRST_SHIFT[6:0]					CNT_LV[6]	00h		
8CH	CNTRST_HISY_HB[3:0]			CNTRST_HISY_LB[3:0]				00h	

Description
<ul style="list-style-type: none"> <li>- This command is used to set Focal CleverColor Contrast function</li> <li>- ENA : Contrast function enable.</li> <li>- ADJ_MODE : Contrast function adjustment mode enable.</li> <li>- CNTRST_LEVEL[6:0] : Select Contrast level.</li> <li>- CNTRST_SHIFT [6:0] : Set Contrast shift.</li> <li>- CNTRST_HISY_HB[3:0] : Set the Higher bound for contrast hisY.</li> <li>- CNTRST_HISY_LB[3:0] : Set the Lower bound for contrast hisY.</li> </ul> <p>Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.</p>

**2.3.73 FCC\_AIE (BANK23H 8DH) : Focal CleverColor – AIE**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
8DH					AIE_LEVEL[6:0]			ENA	00h

Description	
- This command is used to set Focal CleverColor AIE function	
- ENA : Set AIE function enable.	
- AIE_Level[6:0] : Set AIE function level.	

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.74 FCC\_WA (BANK23H 8EH) : Focal CleverColor – White Balance Adjustment**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
8EH					WA_SEL[6:0]			ENA	00h

Description																	
- This command is used to set Focal CleverColor White Balance Adjustment function																	
- ENA : White Balance Adjustment function enable																	
- WA_SEL[6:0] : Set White Balance Adjustment parameter																	
<table border="1"><thead><tr><th>WA_SEL[6:0]</th><th>White Point Setting</th></tr></thead><tbody><tr><td>0h</td><td>Default White Point</td></tr><tr><td>1h ~ 64h</td><td>Cooler White Point</td></tr><tr><td>65h ~ 27 h</td><td>Warmer White Point</td></tr></tbody></table>										WA_SEL[6:0]	White Point Setting	0h	Default White Point	1h ~ 64h	Cooler White Point	65h ~ 27 h	Warmer White Point
WA_SEL[6:0]	White Point Setting																
0h	Default White Point																
1h ~ 64h	Cooler White Point																
65h ~ 27 h	Warmer White Point																
Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.																	

**2.3.75 FCC\_DGAMFRC (BANK23H 8FH) : Focal CleverColor – Digital Gamma and Frame Rate Control**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
8FH			Reserved			FRC_AUTO	FRC_EN	DGAM_EN	00h

Description
- This command is used to set parameters for digital gamma and Frame Rate Control. - DGAM_EN : Digital Gamma function enable. - FRC_EN : Frame Rate Control function enable. - FRC_AUTO : If any image function enable, FRC will turn on when this bit is '0'.

**2.3.76 DISBV\_SET (BANK23H 90H~91H) : Display Brightness Value Setting**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
90H	DBV[11:4]								FFh
91H	Reserved				DBV[3:0]				0Fh

Description
- This command is used to adjust the brightness value of the display.
- It should be checked what is the relationship between this written value and output brightness of the display. This relationship is defined on the display module specification.
- In principle relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.77 DISBV\_RD (BANK23H 92H ~ 93H) : Read Display Brightness Value**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
92H	DBV[11:4]							00h	
93H	Reserved				DBV[3:0]				00h

Description
<ul style="list-style-type: none"><li>- This command returns the brightness value of the display.</li><li>- This command can be used to read the brightness value of the display also when Display brightness control is in automatic mode.</li><li>- It should be checked what the relationship between this returned value and output brightness of the display. This relationship is defined on the display module specification.</li><li>- In principle the relationship is that 000h value means the lowest brightness and FFFh value means the highest brightness.</li><li>- DBV[11:0] is reset when display is in sleep-in mode.</li><li>- DBV[11:0] is '0' when bit BCTRL of "Write CTRL Display (BANK23H 94H)" command is '0'.</li><li>- DBV[11:0] is manual set brightness specified with "Write CTRL Display (BANK23H 94H)" command when bit BCTRL is '1'.</li><li>- See command "Write Display Brightness Value(BANK23H 90H ~ 91H)".</li></ul> <p>Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC_CMD_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.</p>

**2.3.78 DISBV\_CTRL (BANK23H 94H) : Display Brightness Value Control**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
94H	Reserved	BCTRL	Reserved	DD	BL	Reserved		00h	

**Description**

- This command is used to control ambient light, brightness and gamma settings.

BCTRL : Brightness Control Block On/Off. This bit is always used to switch brightness for display and keyboard.

'0' = Off (Brightness registers are 00h)

'1' = On (Brightness registers are active, according to the other parameters.)

DD : Display Dimming

- Dimming function is adapted to the brightness registers for display and keyboard when bit BCTRL is changed at DD=1,  
e.g. BCTRL: 0 -> 1 or 1-> 0.

'0' = Display Dimming is off

'1' = Display Dimming is on

BL : Backlight On/Off

- When BL bit change from "On" to "Off", backlight is turned off

'0' = Off (Completely turn off backlight circuit. Control lines must be low. )

'1' = On

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL"  
It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.79 FCC\_CABC (BANK23H 95H) : Focal CleverColor – Content Adaptive Brightness Control**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
95H					Reserved		CABC_MODE[1:0]	00h	

**Description**

- This command is used to set parameters for power functionality.
- There is possible to use 3 different modes for content adaptive image functionality, which are defined on a table below.

CABC_MODE	Function	Note
0h	Power Save Off	CABC Off
1h	Power Save Low	User Interface Image(UI)
2h	Power Save Medium	Still Picture(ST)
3h	Power Save High	Moving Image(MV)

CABC = Content Adaptive Brightness Control

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.80 CABC\_MDISBV (BANK23H 97H~98H) : Focal CleverColor – CABC Minimum Display Brightness Value**

Bank23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
97H	CMB[11:4]							00h	
98H	Reserved				CMB[3:0]				00h

**Description**

- This command is used to set the minimum brightness value of the display for CABC function.
- In principle relationship is that 000h value means the lowest brightness for CABC and FFFh value means the highest brightness for CABC.

Note: Focal CleverColver can be configured by either CMD1 or CMD2. Please refer to command "BANK23H 99H~9AH, FCC\_CMD\_SEL". It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.81 FCC\_CMD\_SEL (BANK23H 99H~9AH) : Focal CleverColor CMD1/CMD2 Selection**

BANK23H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
99H	CABC_SEL	DISBV_SEL	DBV_SEL	WA_SEL	AIE_SEL	CNT_SEL	SHP_SEL	CE_SEL	99h
9AH				Reserved			CMB_SEL	Reserved	07h

Description
CE_SEL : Select FCC_CE control from CMD1 or CMD2 0:CMD2 1:CMD1
SHP_SEL : Select FCC_SHARPN control from CMD1 or CMD2 0:CMD2 1:CMD1
CNT_SEL : Select FCC_CNTRST control from CMD1 or CMD2 0:CMD2 1:CMD1
AIE_SEL : Select FCC_AIE control from CMD1 or CMD2 0:CMD2 1:CMD1
WA_SEL : Select FCC_WA control from CMD1 or CMD2 0:CMD2 1:CMD1
DBV_SEL : Select DISBV_CTRL control from CMD1 or CMD2 0:CMD2 1:CMD1
DISBV_SEL : Select DISBV_CTRL control from CMD1 or CMD2 0:CMD2 1:CMD1
CABC_SEL : Select FCC_CABC control from CMD1 or CMD2 0:CMD2 1:CMD1
CMB_SEL : Select CABC_MDISBV control from CMD1 or CMD2 0:CMD2 1:CMD1
Note: Focal CleverColor can be configured by either CMD1 or CMD2. It is suggested to set up Focal CleverColor by CMD2 only if real-time turning on/off is not necessary.

**2.3.82 SPI\_LOAD\_FINISH (BANK24H 90H) : SPI Load Finish**

Bank24H									
Parameter Address	D7	D6	D5	D4	D3	D2	D1	D0	Default
90H	SPI_LOAD_FINISH								5Ah

Description
SPI_LOAD_FINISH : SPI Load Finish.
- This command is used to enter LCD normal display state when SPI load finished.
'5Ah' = SPI not Load Finish.
'Others' = SPI Load Finish

**3.FUNCTIONS****3.1 BIST Function**

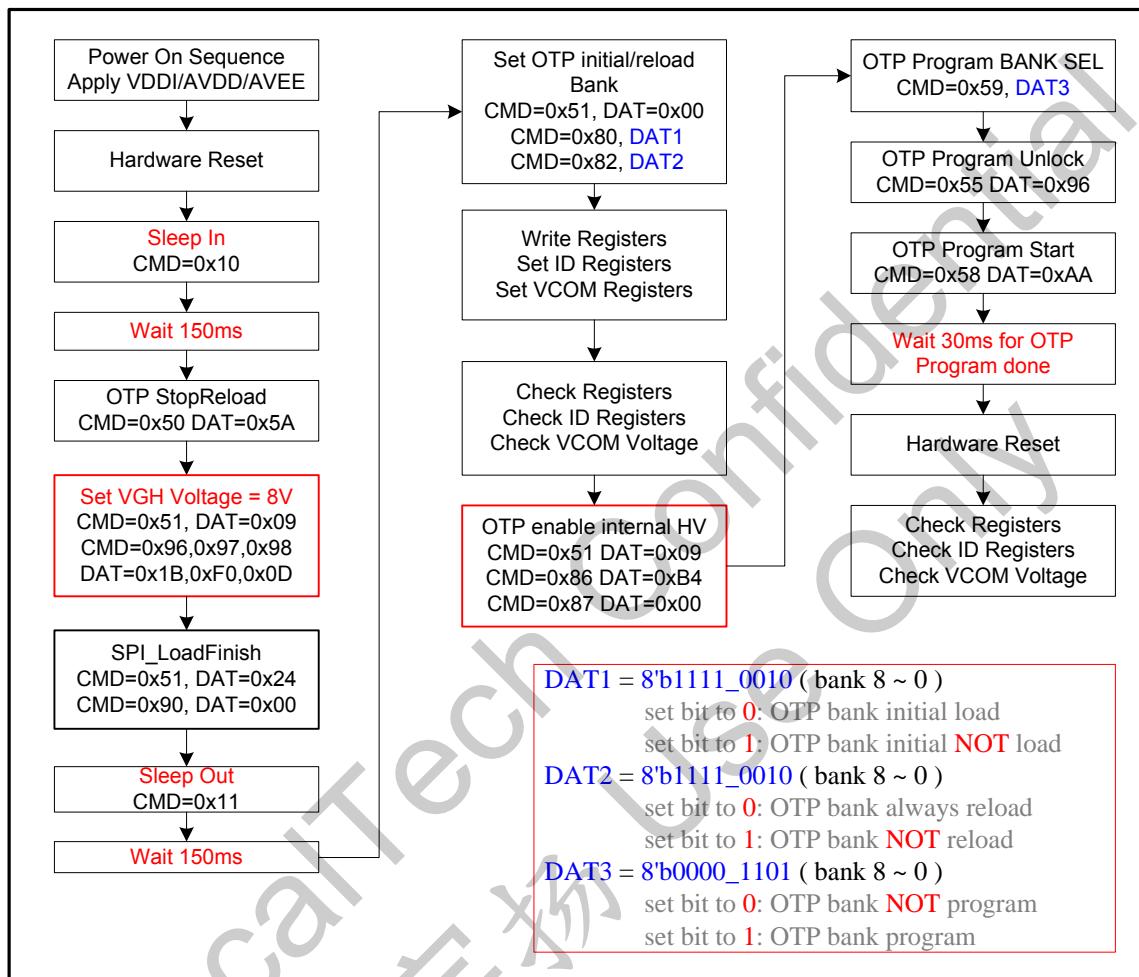
When either hardware pin "BIST\_EN" or Command-1 register "reg\_bist\_en" is enabled, internal BIST pattern generator will enable to generate specific patterns to display circularly according to the following sequence.

1	2	3	4	5	6	7	8
White	Black	Red	Green	Blue	Yellow	Magenta	Cyan
9	10	11	12	13	14	15	16
V8ColBar	H256Gray	V256Gray	CrossTalk	ChsBrd8x8	ChsBrd5x5	CL127	Flicker

### 3.2 NVM Programming Procedure

#### 3.3.1. NVM program flow chart with Internal Power

Here is an example of OTP program ID and VCOM with internal power:



**4.DISCLAIMER**

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**5.REVISION HISTORY**

Date	Revision #	Description	Page	Auditor
JUN.21, 2019	0.1	Original.	1~175	Alan Lin

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