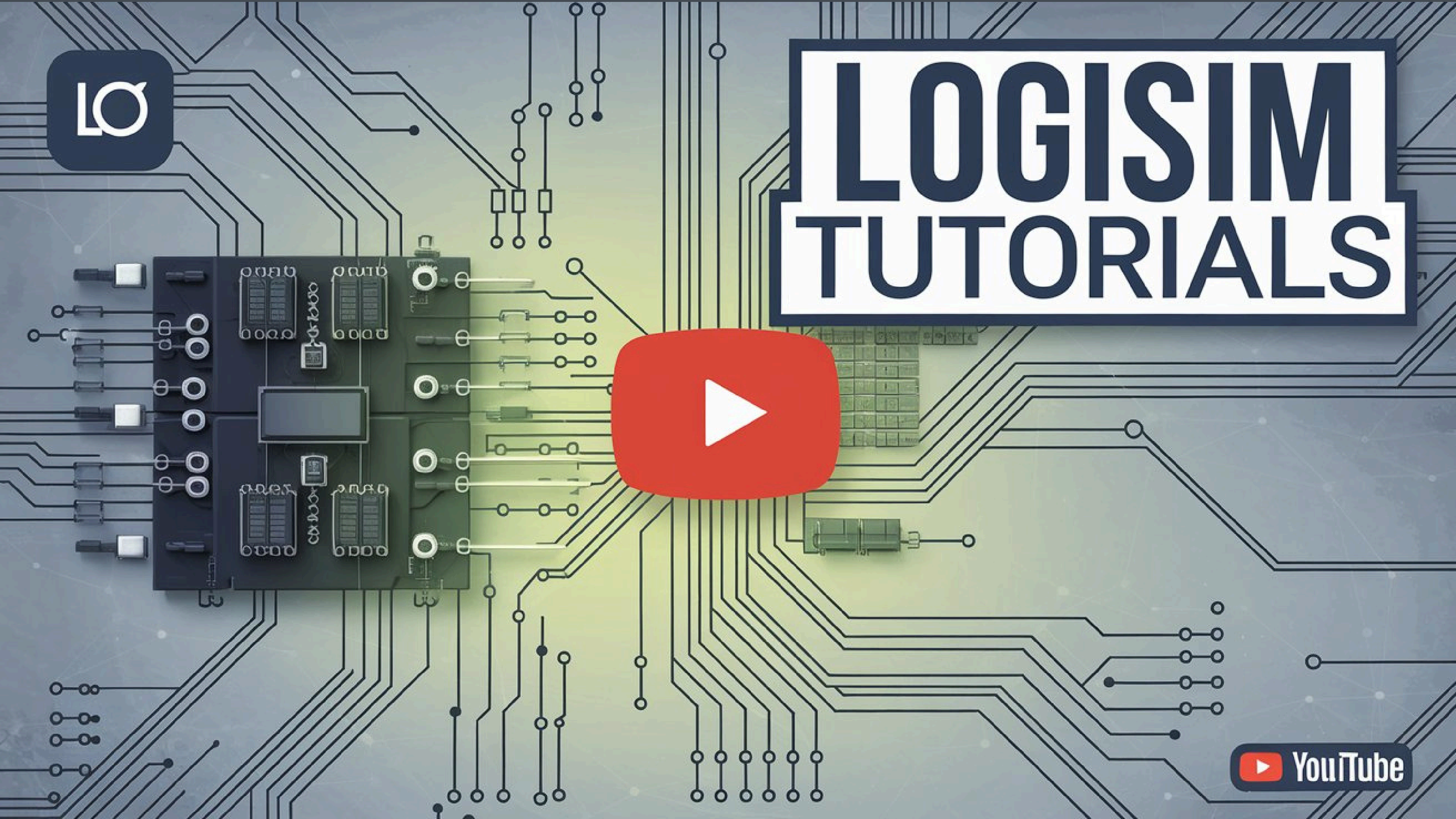
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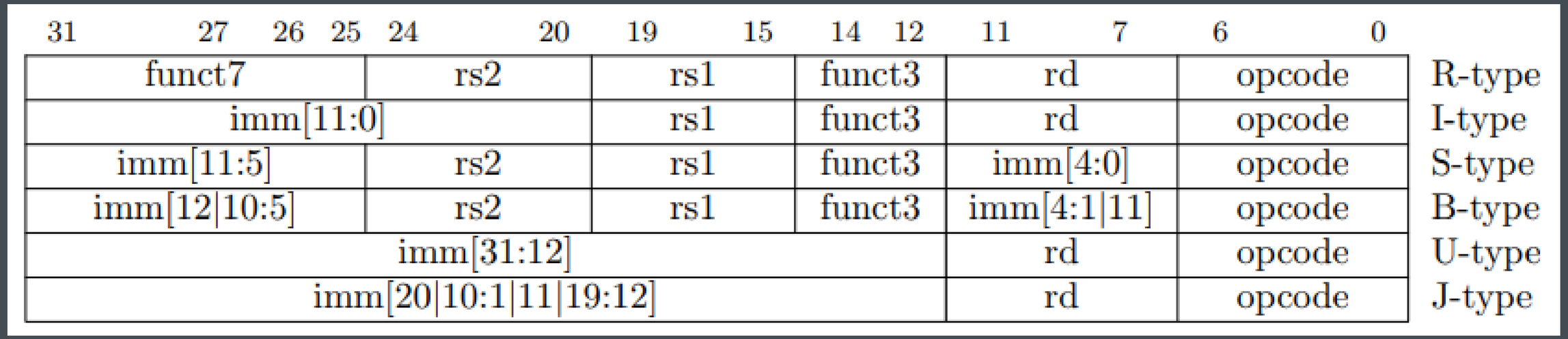
Introduction to Control Unit

The Control Unit is the brain of the CPU. It plays a critical role in instruction decoding and generating control signals to coordinate data movement and operations across the CPU. In a RISC-V single-cycle processor, the control unit manages the flow of execution by:

- Decoding the instruction from memory.
- Generating control signals for various parts of the CPU (ALU, register file, memory).
- Ensuring synchronous operation across all components in the single cycle.

Understanding the Structure of a RISC-V Instruction



31 27	26 25	24 20	19 15	14 12	11 7	6 0	
funct7		rs2	rs1	funct3	rd	opcode	R-type
imm[11:0]			rs1	funct3	rd	opcode	I-type
imm[11:5]		rs2	rs1	funct3	imm[4:0]	opcode	S-type
imm[12|10:5]		rs2	rs1	funct3	imm[4:1|11]	opcode	B-type
imm[31:12]					rd	opcode	U-type
imm[20|10:1|11|19:12]					rd	opcode	J-type

Example

add x1, x2, x3

Instruction Breakdown:

- Opcode (7 bits): 0110011 (Arithmetic operation)
- rd (5 bits): x1 (Destination register)
- funct3 (3 bits): 000 (Addition)
- rs1 (5 bits): x2 (First source register)
- rs2 (5 bits): x3 (Second source register)
- funct7 (7 bits): 0000000 (Specifies addition)

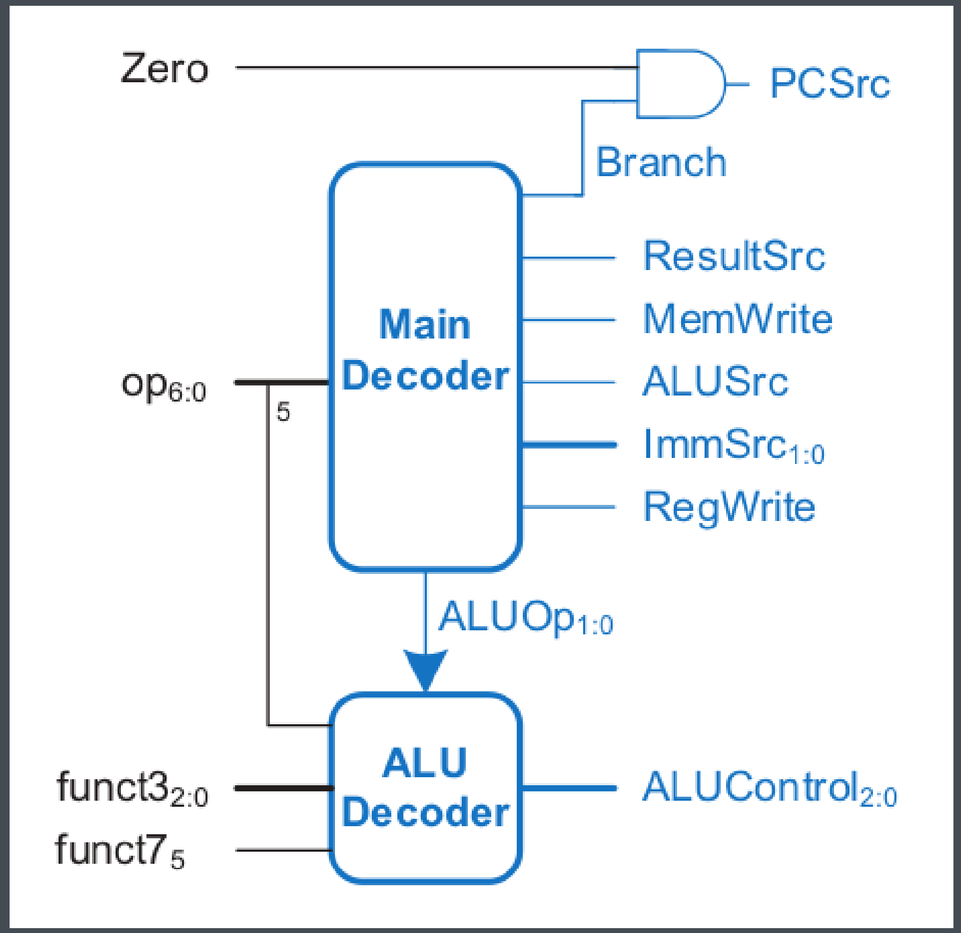
Main Components of the Control Unit

01 Main Control Unit

Responsible for high-level control signals based on the opcode.

02 ALU Control Unit

Generates specific ALU control signals based on the function code and ALUOp signals from the Main Control Unit



Main Control Unit Control Signals

Instruction	Op	RegWrite	ImmSrc	ALUSrc	MemWrite	ResultSrc	Branch	ALUOp
`lw`	0000011	1	00	1	0	1	0	00
`sw`	0100011	0	01	1	1	x	0	00
R-type	0110011	1	xx	0	0	0	0	10
`beq`	1100011	0	10	0	0	x	1	01

ALU Control Unit

ALUOp	funct3	$\{op_5, funct7_5\}$	ALUControl	Instruction
00	x	x	000 (add)	`lw, sw`
01	x	x	001 (subtract)	`beq`
10	000	00, 01, 10	000 (add)	`add`
	000	11	001 (subtract)	`sub`
	010	x	101 (set less than)	`slt`
	110	x	011 (or)	`or`
	111	x	010 (and)	`and`

Thank You