BLOCK RAM GENERATOR
USER-Guide
Version 2

Project by:

MERL Organization

Table of Contents

1: Cloning Block-RAM-Generator

Clone the Git repo from the given URL:

https://github.com/merledu/RAM-Generator.git

Command to clone the repo

```
git clone https://github.com/merledu/RAM-Generator.git
```

2: Requirements

Before using the generator make sure, you have the following, tools install on your computer/server.

1) PyQT 5
2) Python 3.5 or higher.
3) Icarus Verilog version 11
4) GTK Wave
5) Vivado 2018.2
6) Graphviz

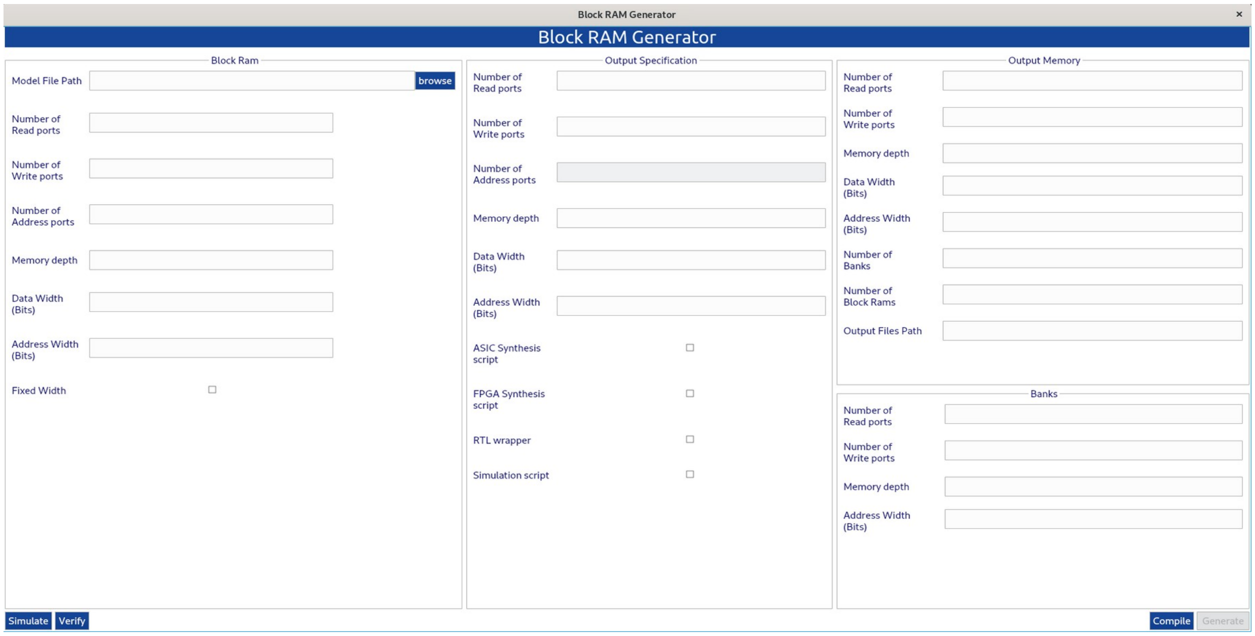
3: Getting Started with Block-RAM-Generator

3.1 Launch GUI

Run the BlockRAM.py script by executing the following command

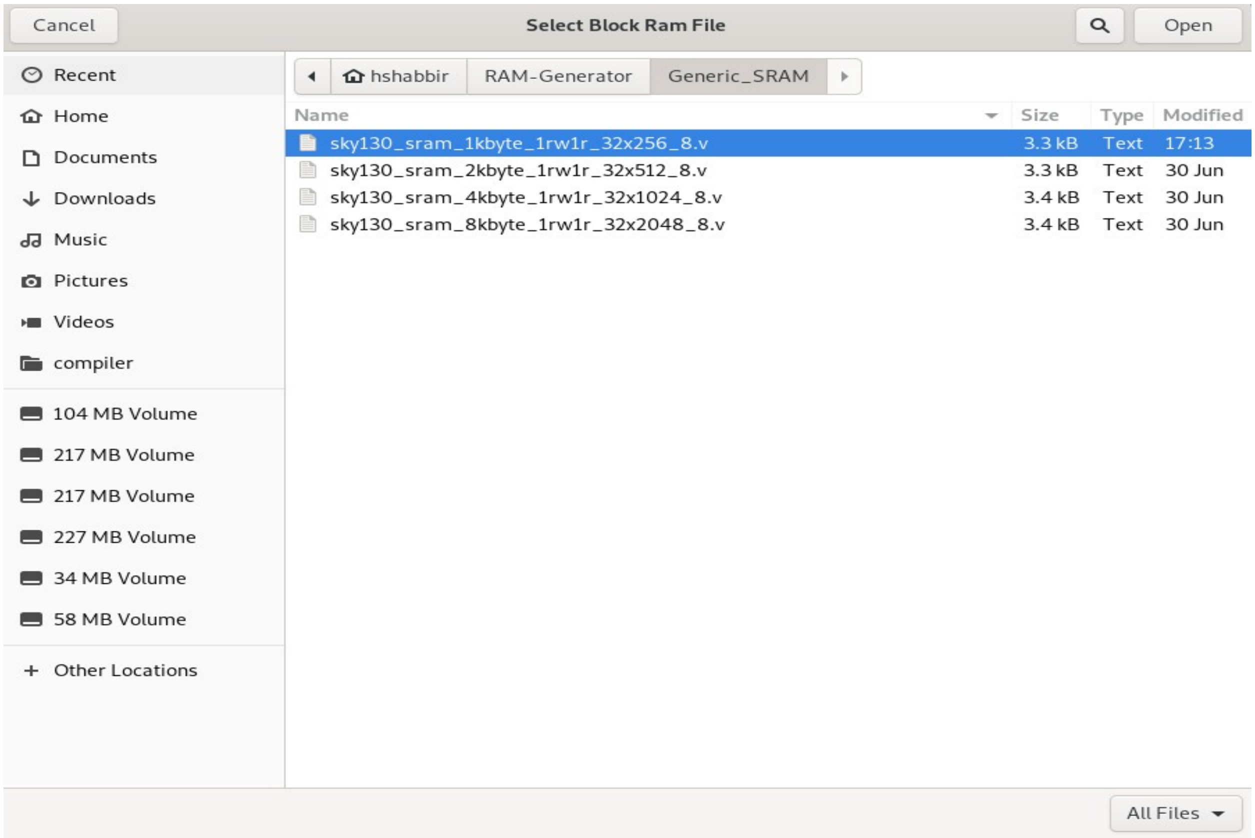
```
pyhton3 /Path/to/RAM-Generator/compiler/BlockRAM.py
```

The GUI interface window will appear.



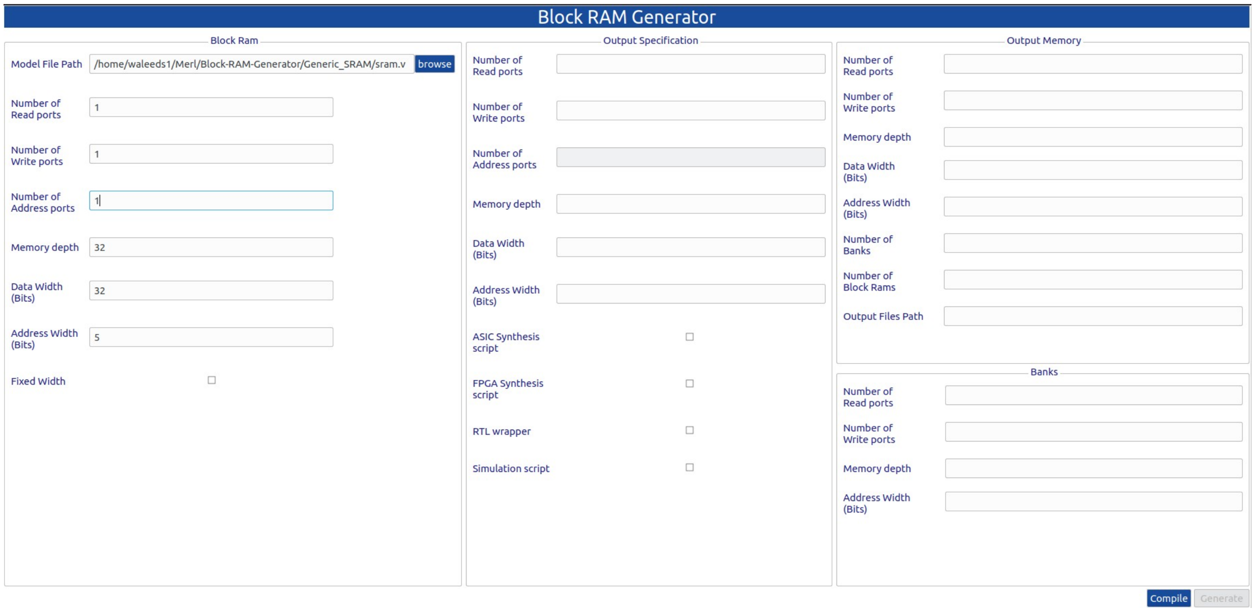
3.2 Block RAM Model

Select the SRAM base model as an input Block RAM provided in **RAM-Generator/Generic_SRAM**.



Name	Size	Type	Modified
sky130_sram_1kbyte_1rw1r_32x256_8.v	3.3 kB	Text	17:13
sky130_sram_2kbyte_1rw1r_32x512_8.v	3.3 kB	Text	30 Jun
sky130_sram_4kbyte_1rw1r_32x1024_8.v	3.4 kB	Text	30 Jun
sky130_sram_8kbyte_1rw1r_32x2048_8.v	3.4 kB	Text	30 Jun

After the selection of the input file for the Block RAM, provide the information for the remaining inputs. As we are using SRAM as a Block RAM, so the remaining inputs will be.

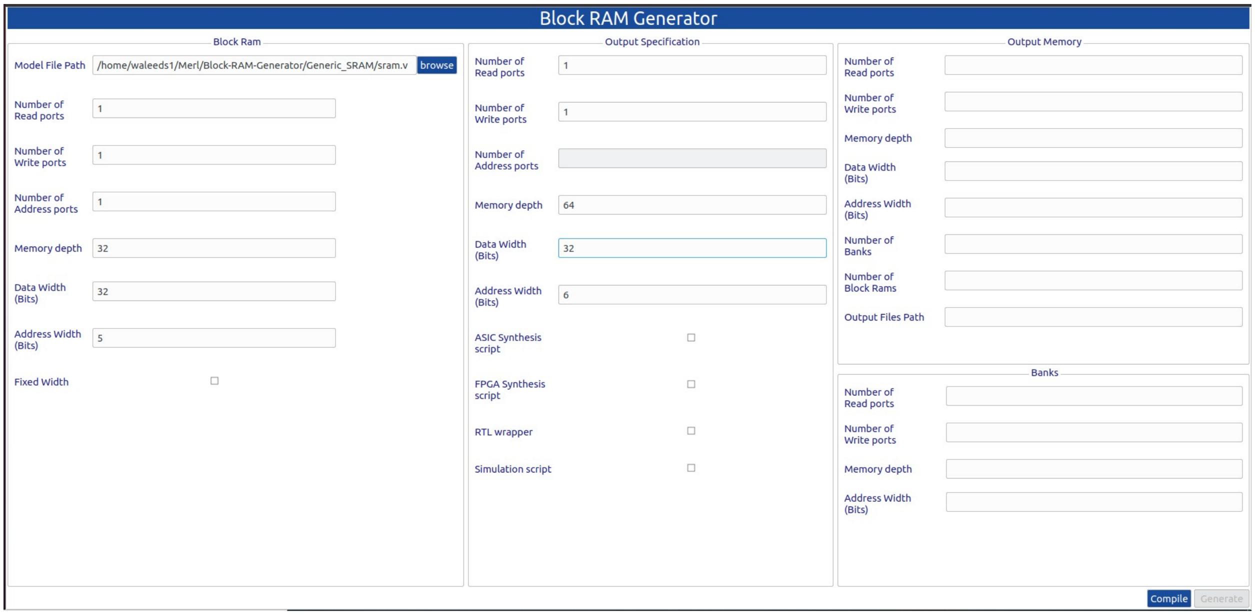


Model File Path	/home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports	1
Number of Write ports	1
Number of Address ports	1
Memory depth	32
Data Width (Bits)	32
Address Width (Bits)	5
Fixed Width	□

3.3 Output Specification

Input the information regarding the specification you want in **Output Specification** column.

Case 1: 1R1W



Block Ram

Model File Path	/home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports	1
Number of Write ports	1
Number of Address ports	1
Memory depth	32
Data Width (Bits)	32
Address Width (Bits)	5
Fixed Width	□

Output Specification

Number of Read ports	1
Number of Write ports	1
Number of Address ports	
Memory depth	64
Data Width (Bits)	32
Address Width (Bits)	6
ASIC Synthesis script	□
FPGA Synthesis script	□
RTL wrapper	□
Simulation script	□

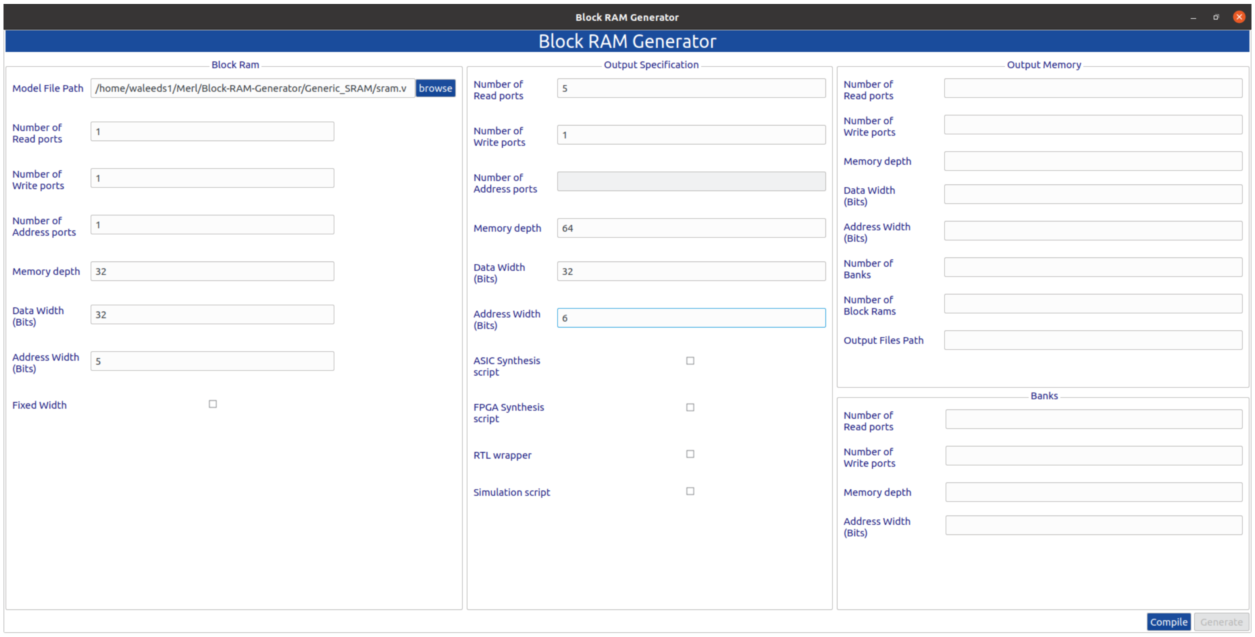
Output Memory

Number of Read ports	
Number of Write ports	
Memory depth	
Data Width (Bits)	
Address Width (Bits)	
Number of Banks	
Number of Block Rams	
Output Files Path	

Banks

Number of Read ports	
Number of Write ports	
Memory depth	
Address Width (Bits)	

Case 2: NR1W



Block Ram

Model File Path	/home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports	1
Number of Write ports	1
Number of Address ports	1
Memory depth	32
Data Width (Bits)	32
Address Width (Bits)	5
Fixed Width	□

Output Specification

Number of Read ports	5
Number of Write ports	1
Number of Address ports	
Memory depth	64
Data Width (Bits)	32
Address Width (Bits)	6
ASIC Synthesis script	□
FPGA Synthesis script	□
RTL wrapper	□
Simulation script	□

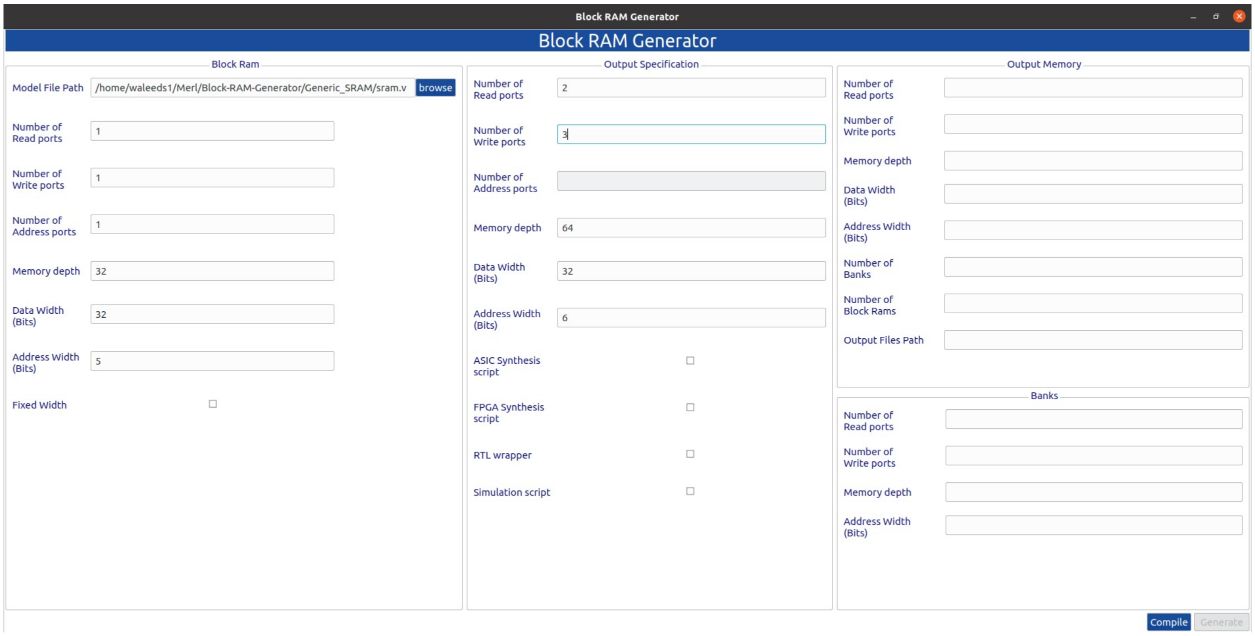
Output Memory

Number of Read ports	
Number of Write ports	
Memory depth	
Data Width (Bits)	
Address Width (Bits)	
Number of Banks	
Number of Block Rams	
Output Files Path	

Banks

Number of Read ports	
Number of Write ports	
Memory depth	
Address Width (Bits)	

Case 3: NRNW



Block Ram

Model File Path: /home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports: 1
Number of Write ports: 1
Number of Address ports: 1
Memory depth: 32
Data Width (Bits): 32
Address Width (Bits): 5
Fixed Width □

Output Specification

Number of Read ports: 2
Number of Write ports: 3
Number of Address ports:
Memory depth: 64
Data Width (Bits): 32
Address Width (Bits): 6
ASIC Synthesis script □
FPGA Synthesis script □
RTL wrapper □
Simulation script □

Output Memory

Number of Read ports:
Number of Write ports:
Memory depth:
Data Width (Bits):
Address Width (Bits):
Number of Banks:
Number of Block Rams:
Output Files Path:

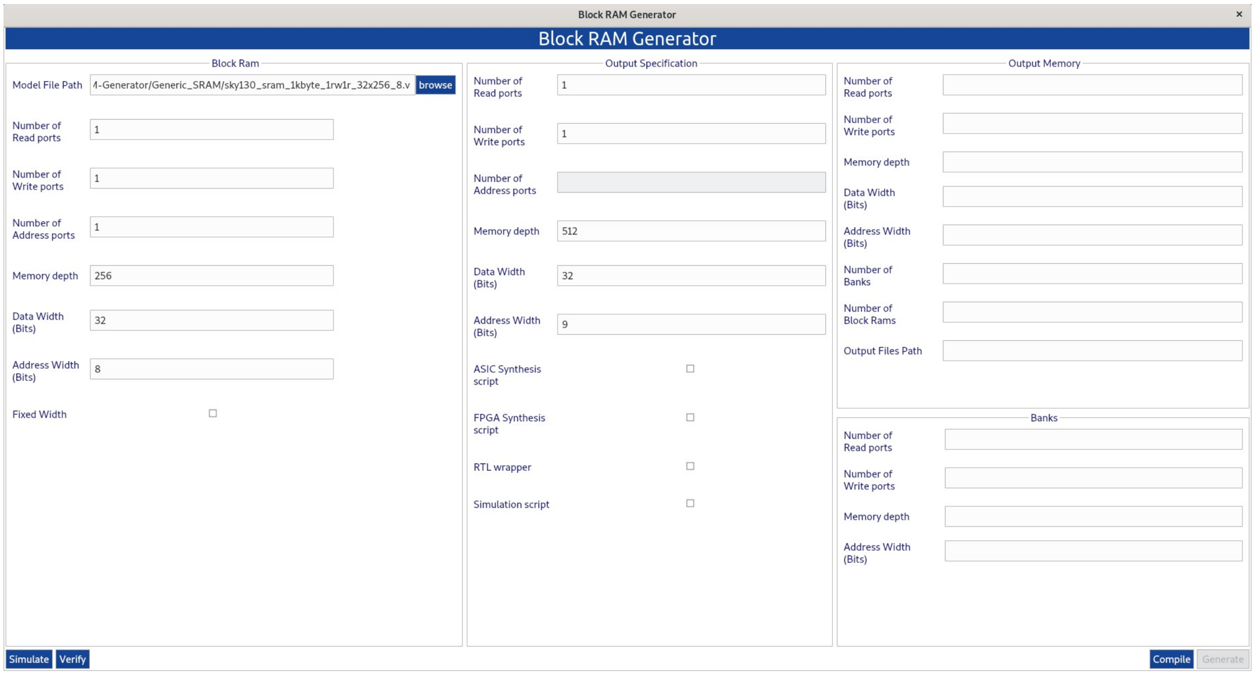
Banks

Number of Read ports:
Number of Write ports:
Memory depth:
Address Width (Bits):

3.4 Generating Files

3.4.1 Model Same as Base Width

To generate the model with same width as of the base model width do not check the **Fixed width** check box.



Block RAM Generator

Block Ram

Model File Path: /-Generator/Generic_SRAM/sky130_sram_1kbyte_1rw1r_32x256_8.v

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports: 1

Memory depth: 256

Data Width (Bits): 32

Address Width (Bits): 8

Fixed Width □

Output Specification

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports:

Memory depth: 512

Data Width (Bits): 32

Address Width (Bits): 9

ASIC Synthesis script □

FPGA Synthesis script □

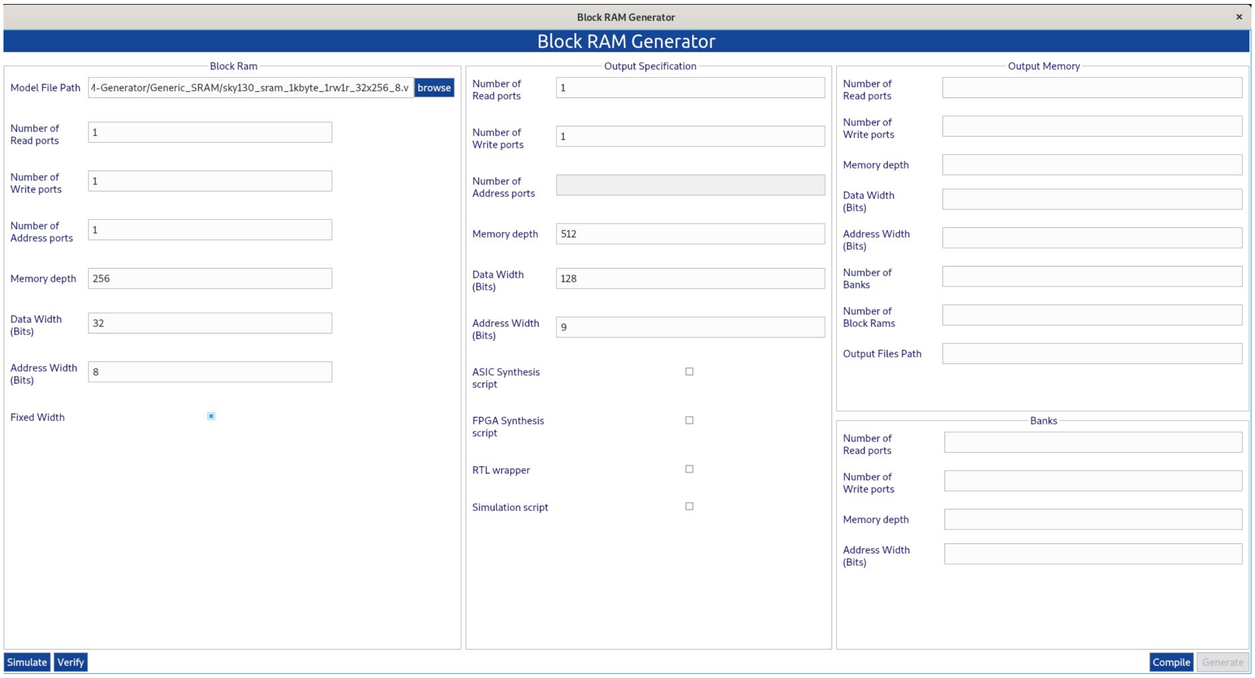
RTL wrapper □

Simulation script □

3.4.2 Model Greater than Base Width

If you want to generate the model with greater width than the base model select the **Fixed Width** check box.

Note: You can only generate the models with the greater width in the multiples of base model width.



Block RAM Generator

Block Ram

Model File Path: /-Generator/Generic_SRAM/sky130_sram_1kbyte_1rw1r_32x256_8.v

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports: 1

Memory depth: 256

Data Width (Bits): 32

Address Width (Bits): 8

Fixed Width ☑

Output Specification

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports:

Memory depth: 512

Data Width (Bits): 128

Address Width (Bits): 9

ASIC Synthesis script □

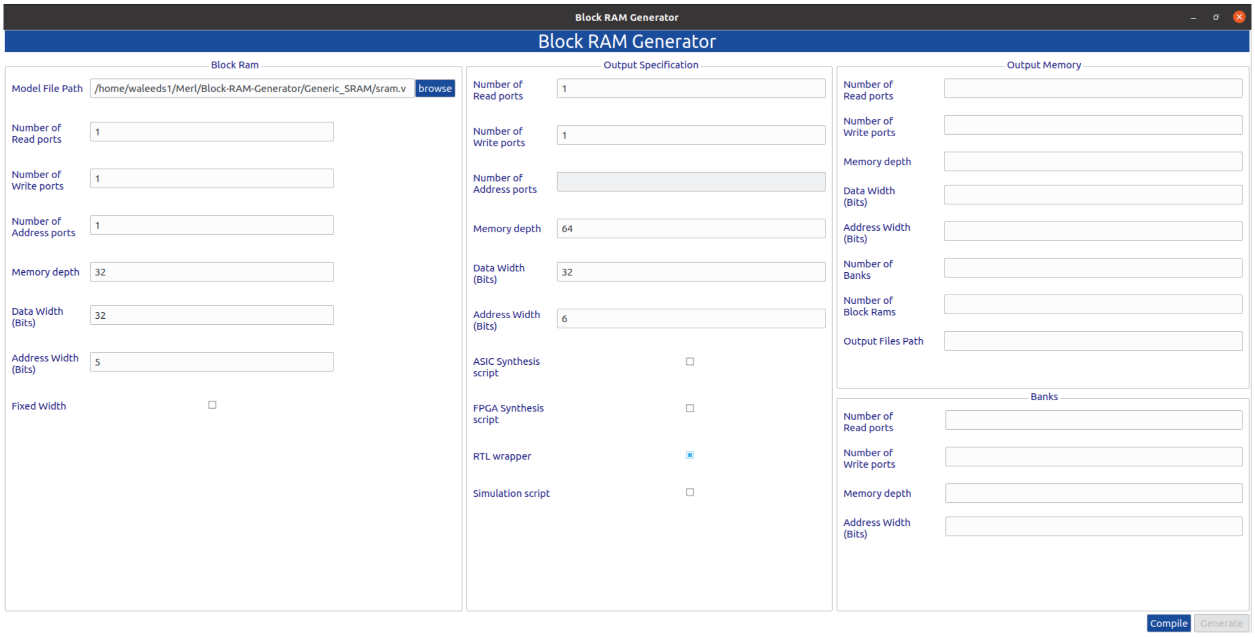
FPGA Synthesis script □

RTL wrapper □

Simulation script □

3.4.3 RTL Wrapper

To generate the RTL wrapper select the RTL wrapper check box. The generator will only generate the RTL file.



Block Ram

Model File Path	/home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports	1
Number of Write ports	1
Number of Address ports	1
Memory depth	32
Data Width (Bits)	32
Address Width (Bits)	5
Fixed Width	☐

Output Specification

Number of Read ports	1
Number of Write ports	1
Number of Address ports	
Memory depth	64
Data Width (Bits)	32
Address Width (Bits)	6
ASIC Synthesis script	☐
FPGA Synthesis script	☐
RTL wrapper	☑
Simulation script	☐

Output Memory

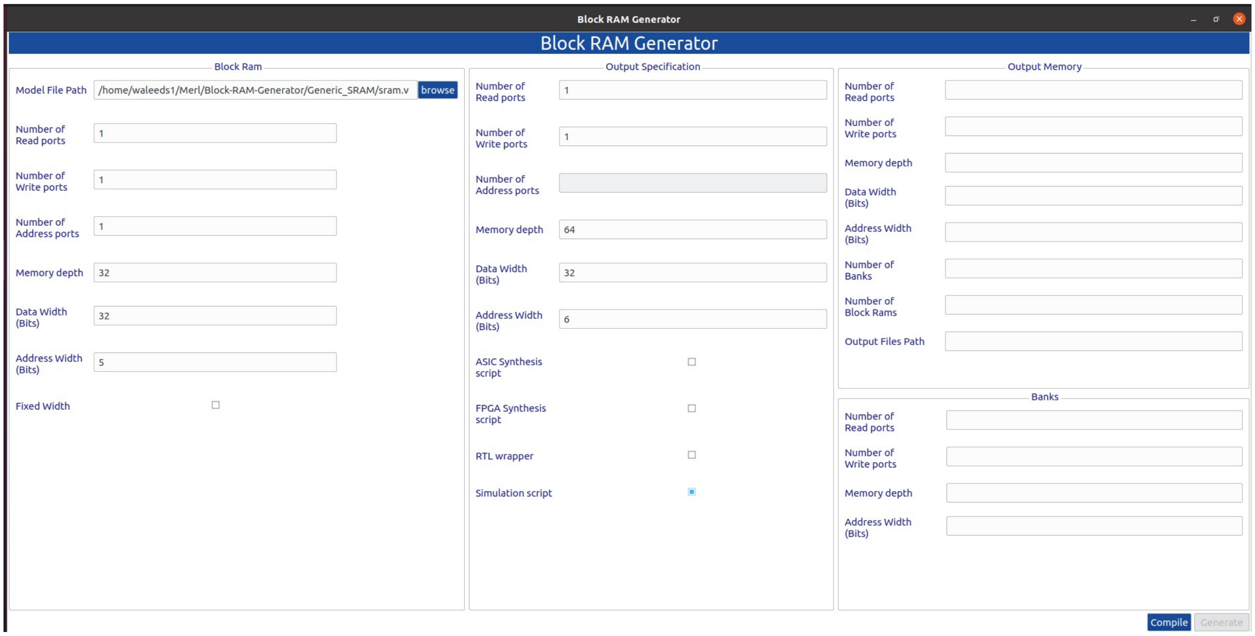
Number of Read ports	
Number of Write ports	
Memory depth	
Data Width (Bits)	
Address Width (Bits)	
Number of Banks	
Number of Block Rams	
Output Files Path	

Banks

Number of Read ports	
Number of Write ports	
Memory depth	
Address Width (Bits)	

3.4.4 Simulation File

To generate the simulation file select the Simulation script check box. The generator will generate the test-bench with the Make File.



Block Ram

Model File Path	/home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports	1
Number of Write ports	1
Number of Address ports	1
Memory depth	32
Data Width (Bits)	32
Address Width (Bits)	5
Fixed Width	☐

Output Specification

Number of Read ports	1
Number of Write ports	1
Number of Address ports	
Memory depth	64
Data Width (Bits)	32
Address Width (Bits)	6
ASIC Synthesis script	☐
FPGA Synthesis script	☐
RTL wrapper	☐
Simulation script	☑

Output Memory

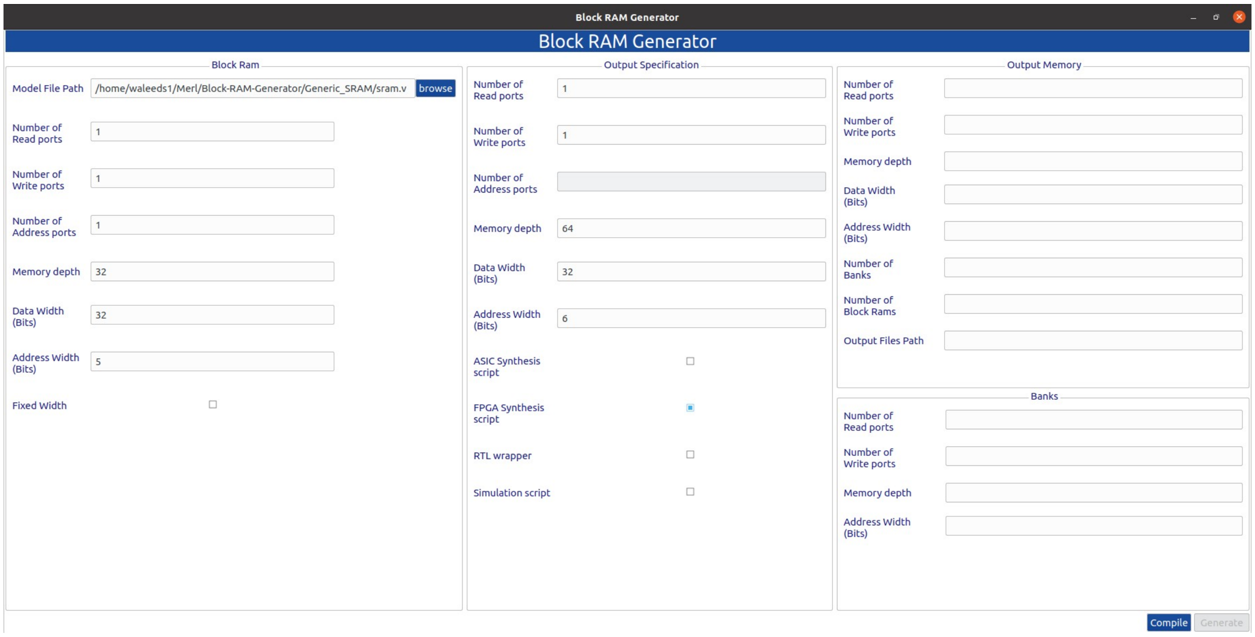
Number of Read ports	
Number of Write ports	
Memory depth	
Data Width (Bits)	
Address Width (Bits)	
Number of Banks	
Number of Block Rams	
Output Files Path	

Banks

Number of Read ports	
Number of Write ports	
Memory depth	
Address Width (Bits)	

3.4.5 FPGA Synthesis Script

To generate the FPGA synthesis script select the FPGA Synthesis script check box. A pop up dialog box will appear asking for the FPGA device name. Input the FPGA device name. The generator will generate the **synth.tcl** file.



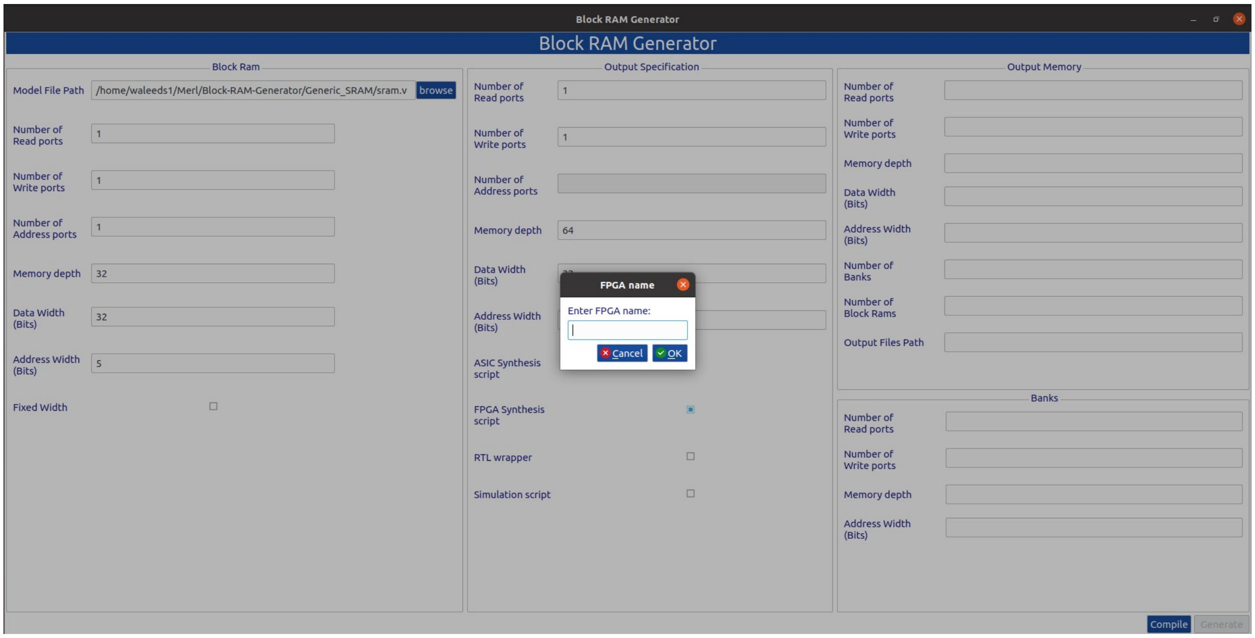
Block RAM Generator

Block Ram

Model File Path	/home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports	1
Number of Write ports	1
Number of Address ports	1
Memory depth	32
Data Width (Bits)	32
Address Width (Bits)	5
Fixed Width	□

Output Specification

Number of Read ports	1
Number of Write ports	1
Number of Address ports	
Memory depth	64
Data Width (Bits)	32
Address Width (Bits)	6
ASIC Synthesis script	□
FPGA Synthesis script	☑
RTL wrapper	□
Simulation script	□



Block RAM Generator

Block Ram

Model File Path	/home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
Number of Read ports	1
Number of Write ports	1
Number of Address ports	1
Memory depth	32
Data Width (Bits)	32
Address Width (Bits)	5
Fixed Width	□

Output Specification

Number of Read ports	1
Number of Write ports	1
Number of Address ports	
Memory depth	64
Data Width (Bits)	
Address Width (Bits)	
ASIC Synthesis script	
FPGA Synthesis script	☑
RTL wrapper	□
Simulation script	□

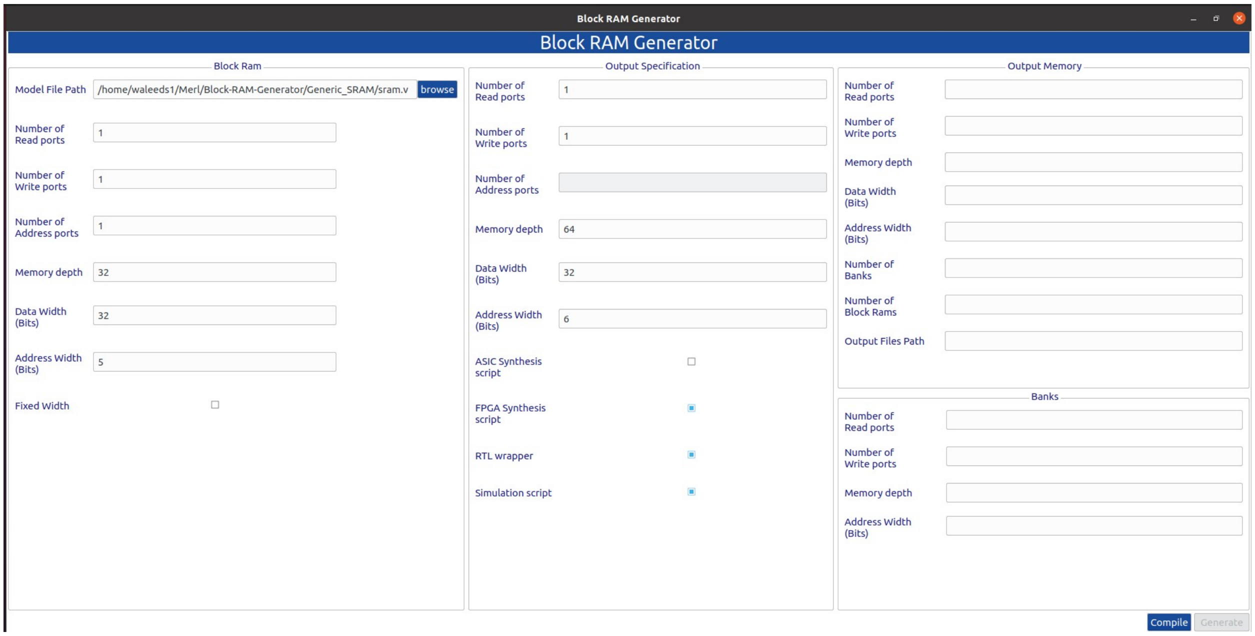
FPGA name

Enter FPGA name:

The example of FPGA device name is **xc7a35ticsg324-1L**

3.4.6 Multiple Files

To generate the multiple files select the multiple check box as per your requirement. The generator will generate the files according to it.



Block Ram

Model File Path: /home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports: 1

Memory depth: 32

Data Width (Bits): 32

Address Width (Bits): 5

Fixed Width: □

Output Specification

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports:

Memory depth: 64

Data Width (Bits): 32

Address Width (Bits): 6

ASIC Synthesis script: □

FPGA Synthesis script: ☑

RTL wrapper: ☑

Simulation script: ☑

Output Memory

Number of Read ports:

Number of Write ports:

Memory depth:

Data Width (Bits):

Address Width (Bits):

Number of Banks:

Number of Block Rams:

Output Files Path:

Banks

Number of Read ports:

Number of Write ports:

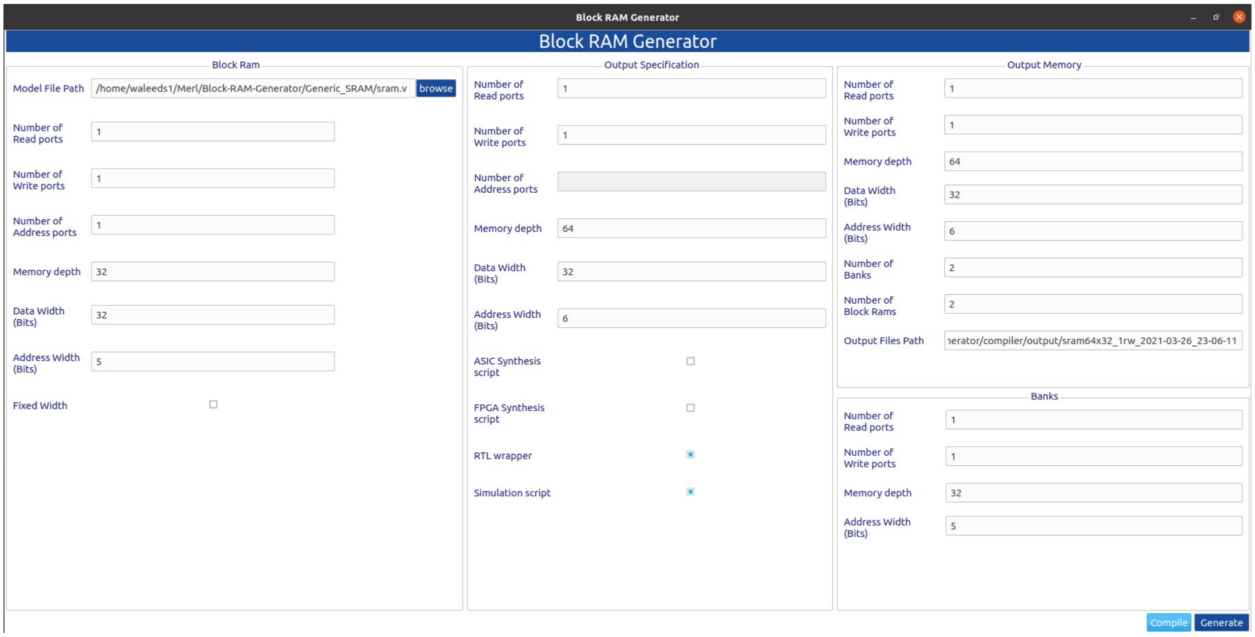
Memory depth:

Address Width (Bits):

3.5 Compile and Generate

3.5.1 Compile

Press the **Compile** button to see the result of your desire specification.



Block Ram

Model File Path: /home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports: 1

Memory depth: 32

Data Width (Bits): 32

Address Width (Bits): 5

Fixed Width: □

Output Specification

Number of Read ports: 1

Number of Write ports: 1

Number of Address ports:

Memory depth: 64

Data Width (Bits): 32

Address Width (Bits): 6

ASIC Synthesis script: □

FPGA Synthesis script: □

RTL wrapper: ☑

Simulation script: ☑

Output Memory

Number of Read ports: 1

Number of Write ports: 1

Memory depth: 64

Data Width (Bits): 32

Address Width (Bits): 6

Number of Banks: 2

Number of Block Rams: 2

Output Files Path: ıerator/compiler/output/sram64x32_1rw_2021-03-26_23-06-11

Banks

Number of Read ports: 1

Number of Write ports: 1

Memory depth: 32

Address Width (Bits): 5

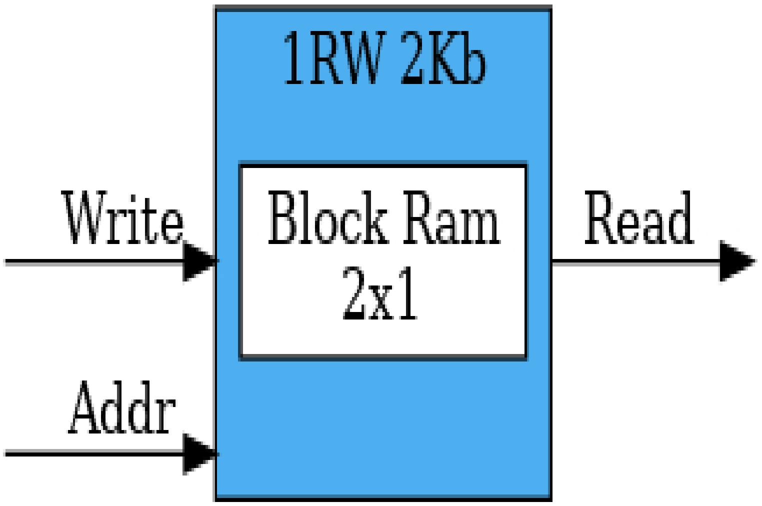
If you want to change your specification, repeat 3.3, 3.4, and 3.5.1.

3.5.2 Specification Block Diagrams

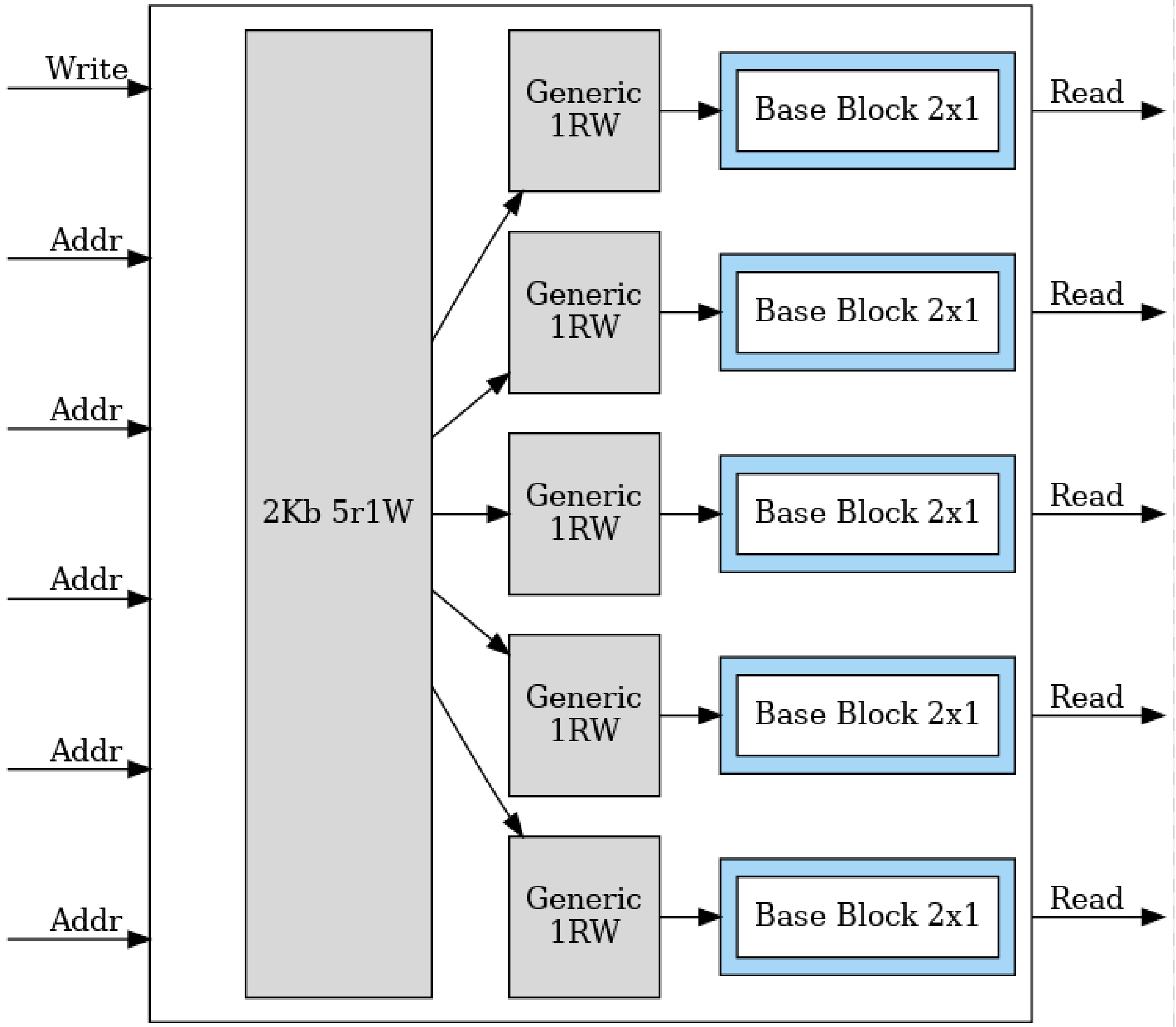
When you press the **Compile** button the block diagram of your desire specification pop up.

3.5.2.1 Model Same as Base Width

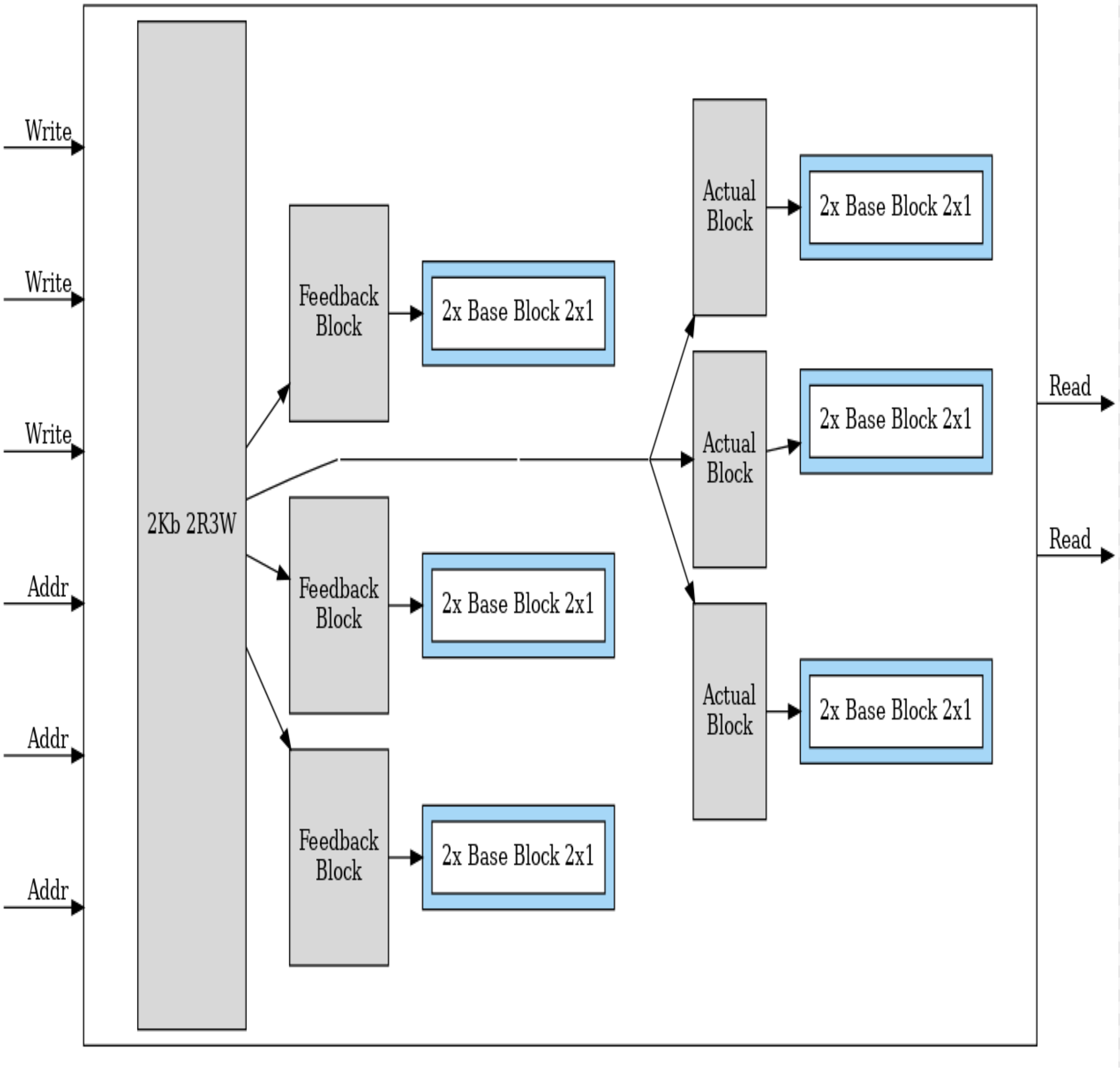
3.5.2.1.1 1R1W Memory



3.5.2.1.2 NR1W Memory

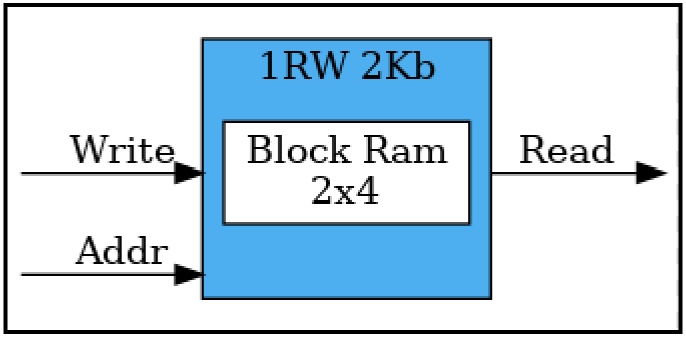


3.5.2.1.3 NRNW Memory

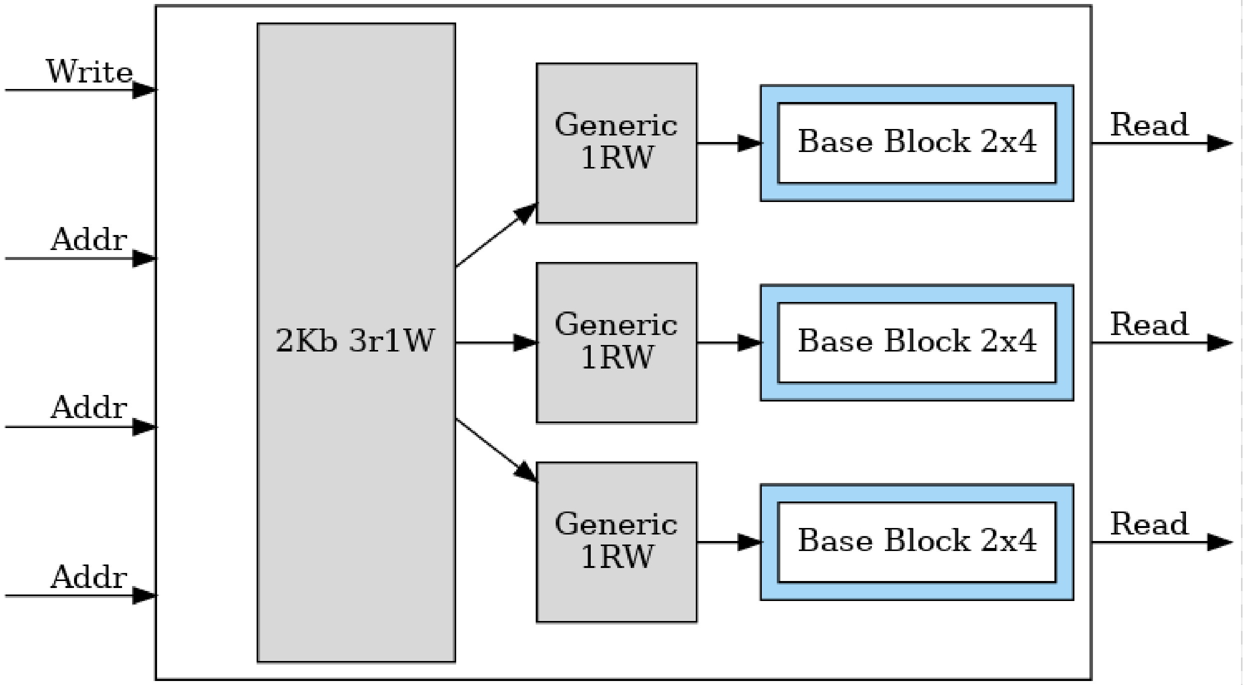


3.5.2.2 Model Greater Than Base Width

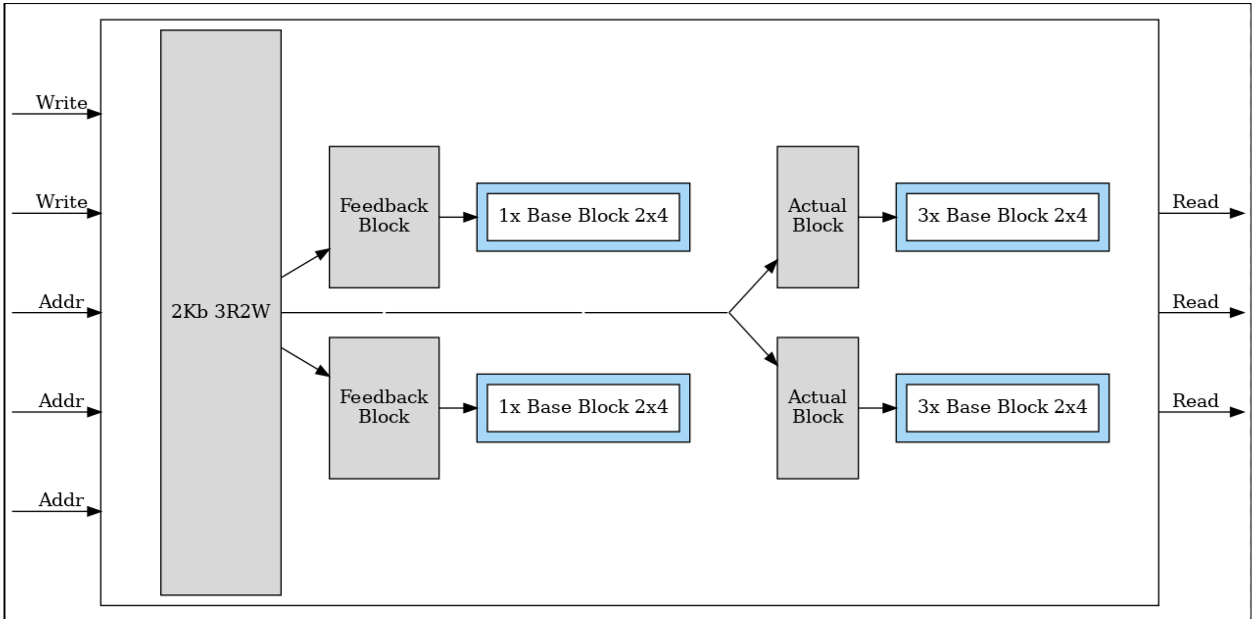
3.5.2.2.1 1R1W Memory



3.5.2.2.2 NR1W Memory

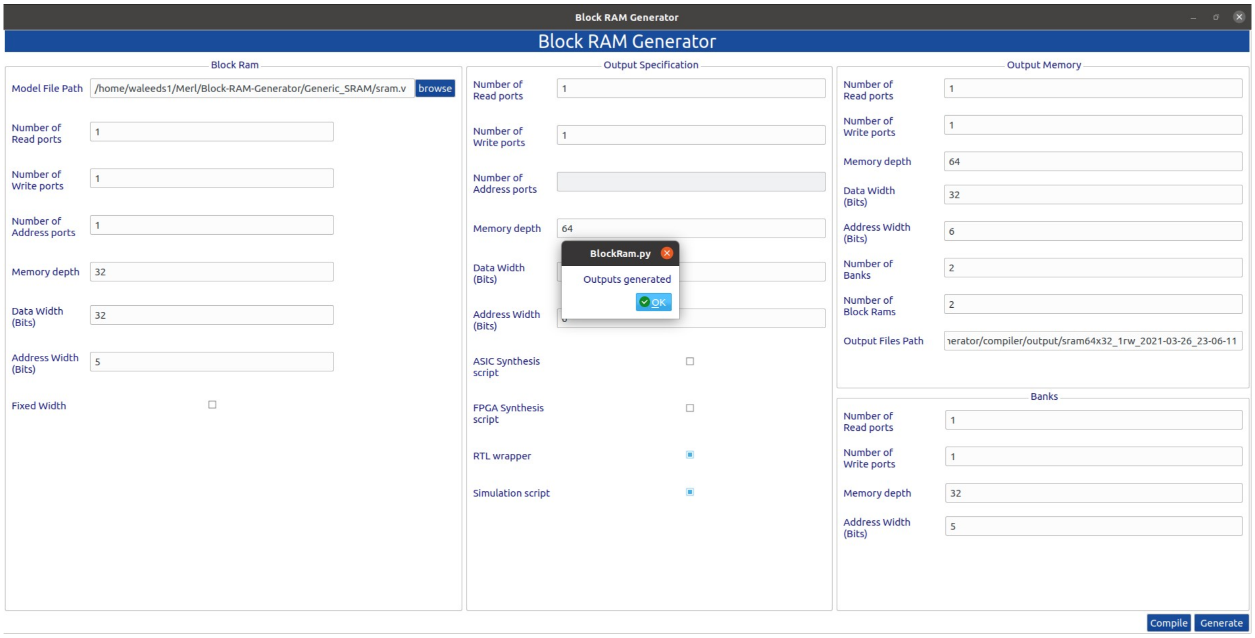


3.5.2.2.3 NRNW Memory



3.5.3 Generate

Press the **Generate** button to generate your files, a pop up message will occur indicating that your files are generated.



Block RAM Generator

Block RAM Generator

Block Ram

Model File Path /home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v

Number of Read ports 1

Number of Write ports 1

Number of Address ports 1

Memory depth 32

Data Width (Bits) 32

Address Width (Bits) 5

Fixed Width □

Output Specification

Number of Read ports 1

Number of Write ports 1

Number of Address ports

Memory depth 64

Data Width (Bits)

Address Width (Bits) 6

ASIC Synthesis script □

FPGA Synthesis script □

RTL wrapper ■

Simulation script ■

BlockRam.py

Outputs generated

Output Memory

Number of Read ports 1

Number of Write ports 1

Memory depth 64

Data Width (Bits) 32

Address Width (Bits) 6

Number of Banks 2

Number of Block Rams 2

Output Files Path ıerator/compiler/output/sram64x32_1rw_2021-03-26_23-06-11

Banks

Number of Read ports 1

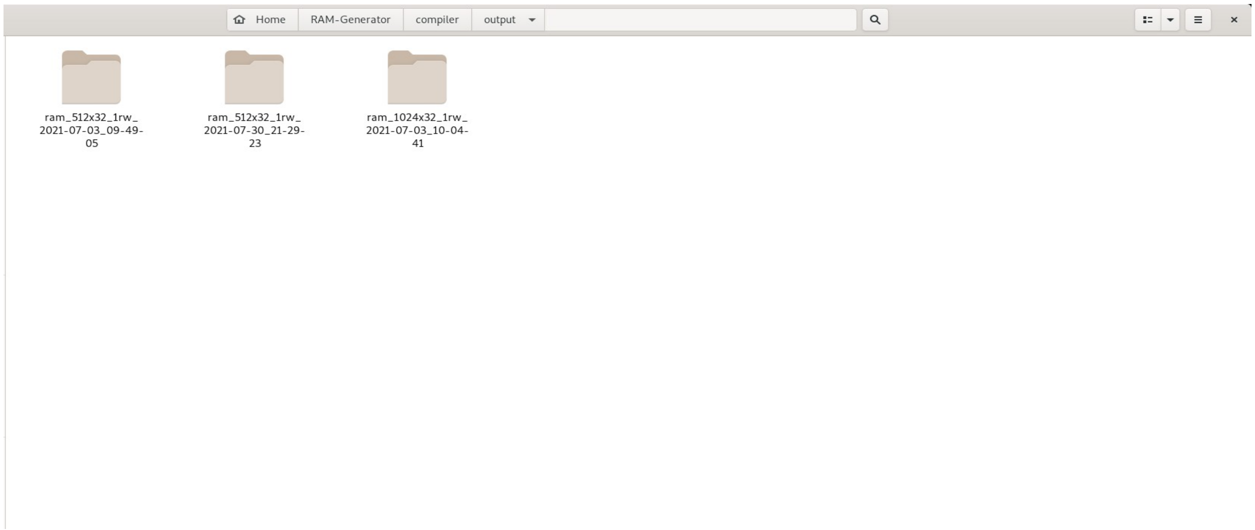
Number of Write ports 1

Memory depth 32

Address Width (Bits) 5

3.6 Files Location

To view your generated files go to **RAM-Generator/compiler/output** folder.



ram_512x32_1rw_2021-07-03_09-49-05

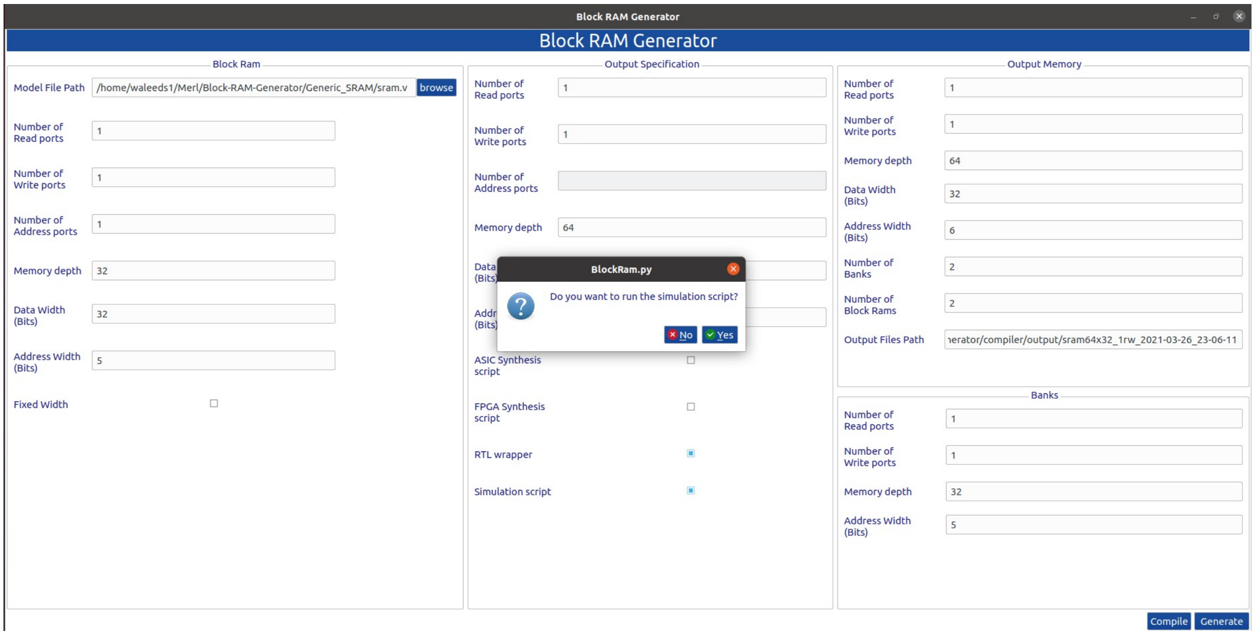
ram_512x32_1rw_2021-07-30_21-29-23

ram_1024x32_1rw_2021-07-03_10-04-41

3.7 Simulation and Verification

3.7.1 Automate

A pop up message will occur after the file generation asking if you want to simulate and verify the design automatically or not.



Block RAM Generator

Block Ram

- Model File Path: /home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
- Number of Read ports: 1
- Number of Write ports: 1
- Number of Address ports: 1
- Memory depth: 32
- Data Width (Bits): 32
- Address Width (Bits): 5
- Fixed Width □

Output Specification

- Number of Read ports: 1
- Number of Write ports: 1
- Number of Address ports:
- Memory depth: 64
- Data (Bits)
- Addr (Bits)
- ASIC Synthesis script □
- FPGA Synthesis script □
- RTL wrapper ☑
- Simulation script ☑

Output Memory

- Number of Read ports: 1
- Number of Write ports: 1
- Memory depth: 64
- Data Width (Bits): 32
- Address Width (Bits): 6
- Number of Banks: 2
- Number of Block Rams: 2
- Output Files Path: ierator/compiler/output/sram64x32_1rw_2021-03-26_23-06-11

Banks

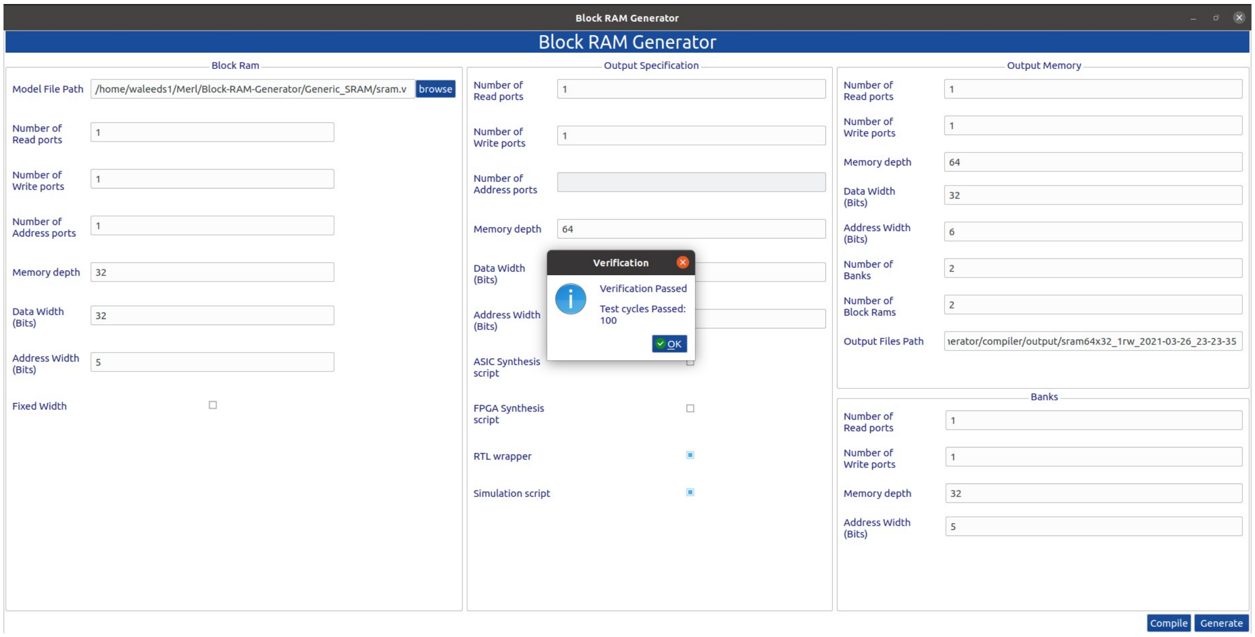
- Number of Read ports: 1
- Number of Write ports: 1
- Memory depth: 32
- Address Width (Bits): 5

BlockRam.py

Do you want to run the simulation script?

Press **yes,** if you want to automate the process.

A pop up message will occur showing that your design is pass or not.



Block RAM Generator

Block Ram

- Model File Path: /home/waleeds1/Merl/Block-RAM-Generator/Generic_SRAM/sram.v
- Number of Read ports: 1
- Number of Write ports: 1
- Number of Address ports: 1
- Memory depth: 32
- Data Width (Bits): 32
- Address Width (Bits): 5
- Fixed Width □

Output Specification

- Number of Read ports: 1
- Number of Write ports: 1
- Number of Address ports:
- Memory depth: 64
- Data Width (Bits)
- Address Width (Bits)
- ASIC Synthesis script
- FPGA Synthesis script □
- RTL wrapper ☑
- Simulation script ☑

Output Memory

- Number of Read ports: 1
- Number of Write ports: 1
- Memory depth: 64
- Data Width (Bits): 32
- Address Width (Bits): 6
- Number of Banks: 2
- Number of Block Rams: 2
- Output Files Path: ierator/compiler/output/sram64x32_1rw_2021-03-26_23-23-35

Banks

- Number of Read ports: 1
- Number of Write ports: 1
- Memory depth: 32
- Address Width (Bits): 5

Verification

Verification Passed

Test cycles Passed: 100

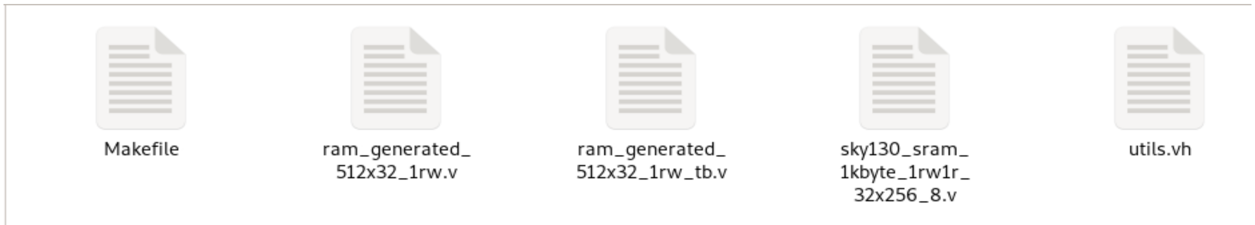
3.7.2 Manual

To simulate the design manually follow the following steps:

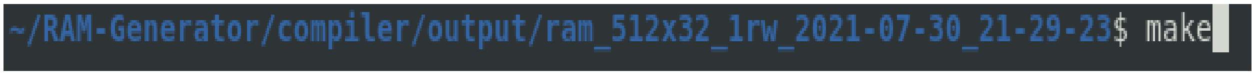
1) Go to the directory where the files are generated.

```
cd Path/to/RAM-Generator/compiler/output/ram_generated_(user_specification)/
```

2) If you have select, the check box to generate the simulation script a **Makefile** will be available in the output folder.

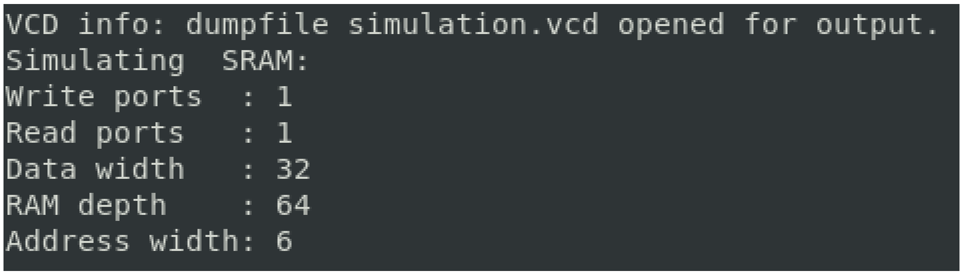

Makefile
ram_generated_512x32_1rw.v
ram_generated_512x32_1rw_tb.v
sky130_sram_1kbyte_1rw1r_32x256_8.v
utils.vh

3) Open the terminal and run **make** command.



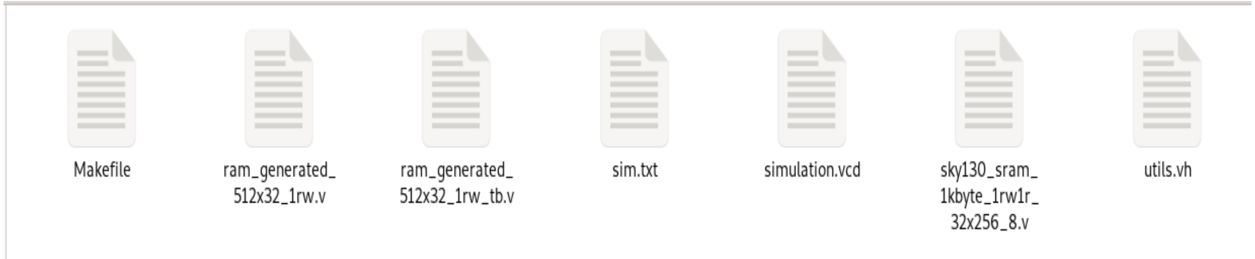
```
~/RAM-Generator/compiler/output/ram_512x32_1rw_2021-07-30_21-29-23$ make
```

4) Will get the following output at terminal.



```
VCD info: dumpfile simulation.vcd opened for output.
Simulating  SRAM:
Write ports   : 1
Read ports    : 1
Data width    : 32
RAM depth     : 64
Address width: 6
```

5) Simulation and log file will be generate.


Makefile
ram_generated_512x32_1rw.v
ram_generated_512x32_1rw_tb.v
sim.txt
simulation.vcd
sky130_sram_1kbyte_1rw1r_32x256_8.v
utils.vh

6) To view the waveform open the **simulation.vcd** file.
7) To view the log file open the **sim.txt** file.

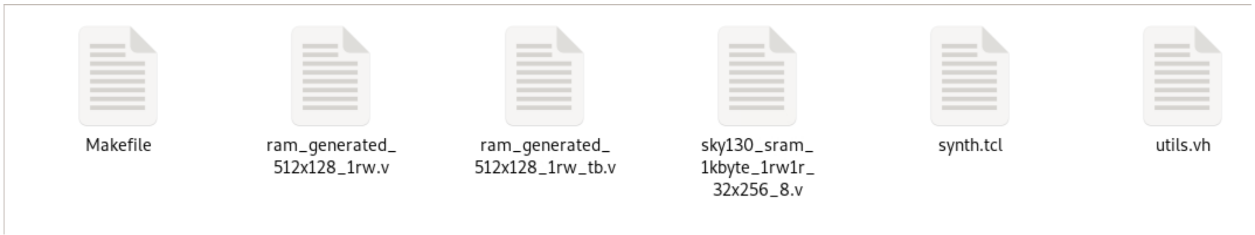
3.8 FPGA Synthesis

To synthesize the design using the tcl file follow the following steps.

1) Go to the directory where the files are generated.

```
cd Path/to/RAM-Generator/compiler/output/ram_generated_(user_specification)/
```

2) If you have select, the check box to generate the FPGA synthesis script a **synth.tcl** file will be available in the output folder.

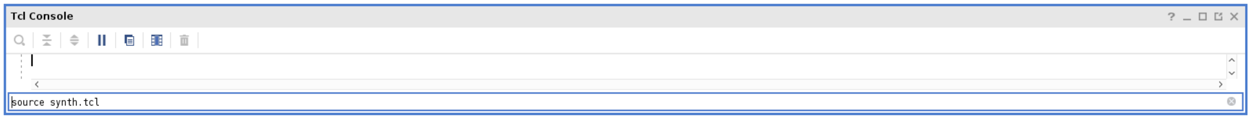

Makefile
ram_generated_512x128_1rw.v
ram_generated_512x128_1rw_tb.v
sky130_sram_1kbyte_1rw1r_32x256_8.v
synth.tcl
utils.vh

3) To execute the **synth.tcl** file from terminal, run the following command.

```
vivado -mode batch -source synth.tcl
```

Note: Run the terminal command from the same folder mention in step 1.

4) To execute the **synth.tcl** file from Vivado, run the following commands.
   1) Open Vivado.
   2) Go to directory where the files are generated.
   3) In Tcl Console type **source synth.tcl** and press enter.



```
source synth.tcl
```