

# Introduction to OpenLane

## Workshop Session 2

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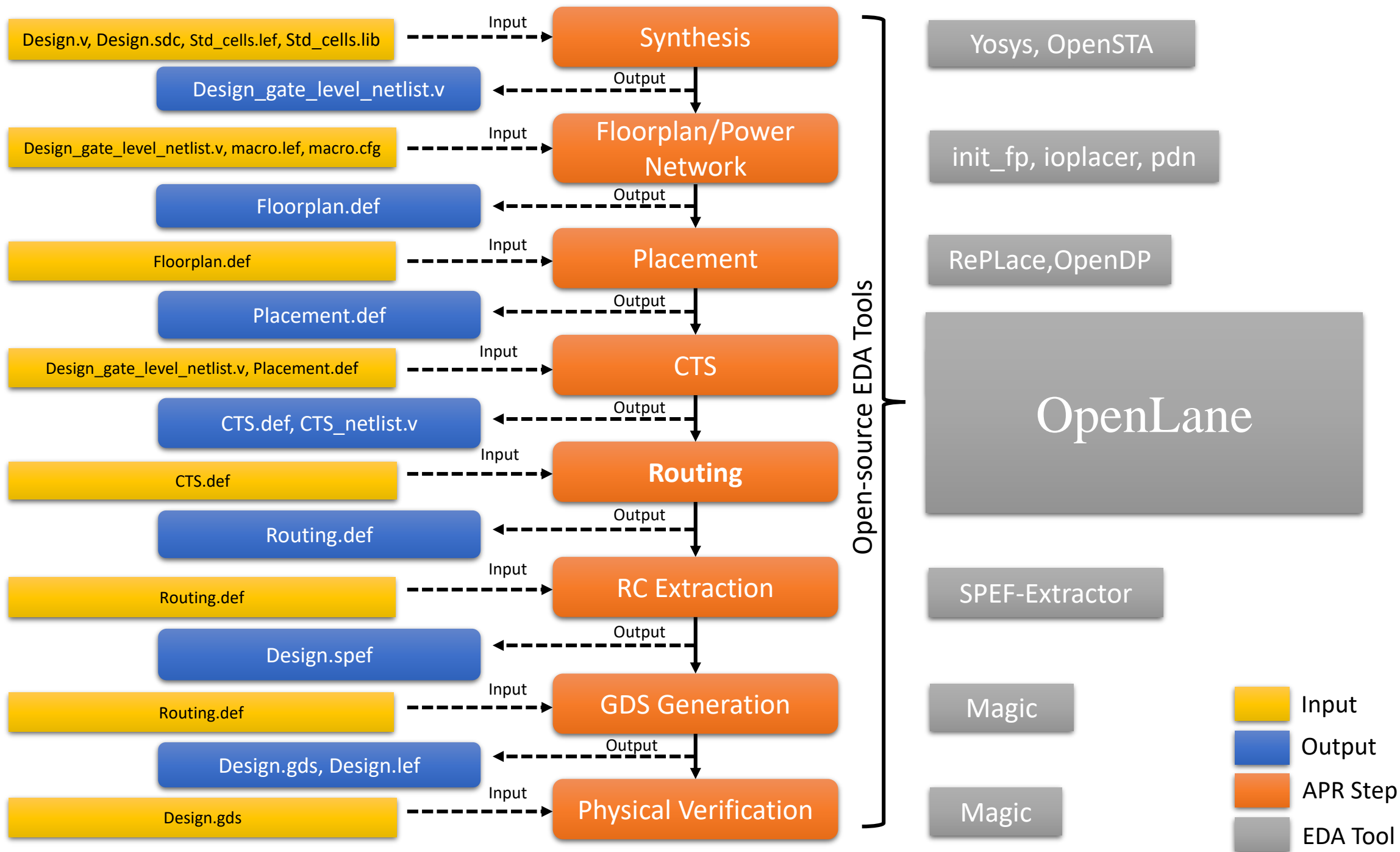
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# OpenLane

## ➤ What is OpenLane?

- OpenLane is an automated RTL to GDSII flow
- The flow performs full ASIC implementation steps from RTL all the way down to GDSII
- Amalgamation of open-source **Electronic design automation (EDA)** Tools

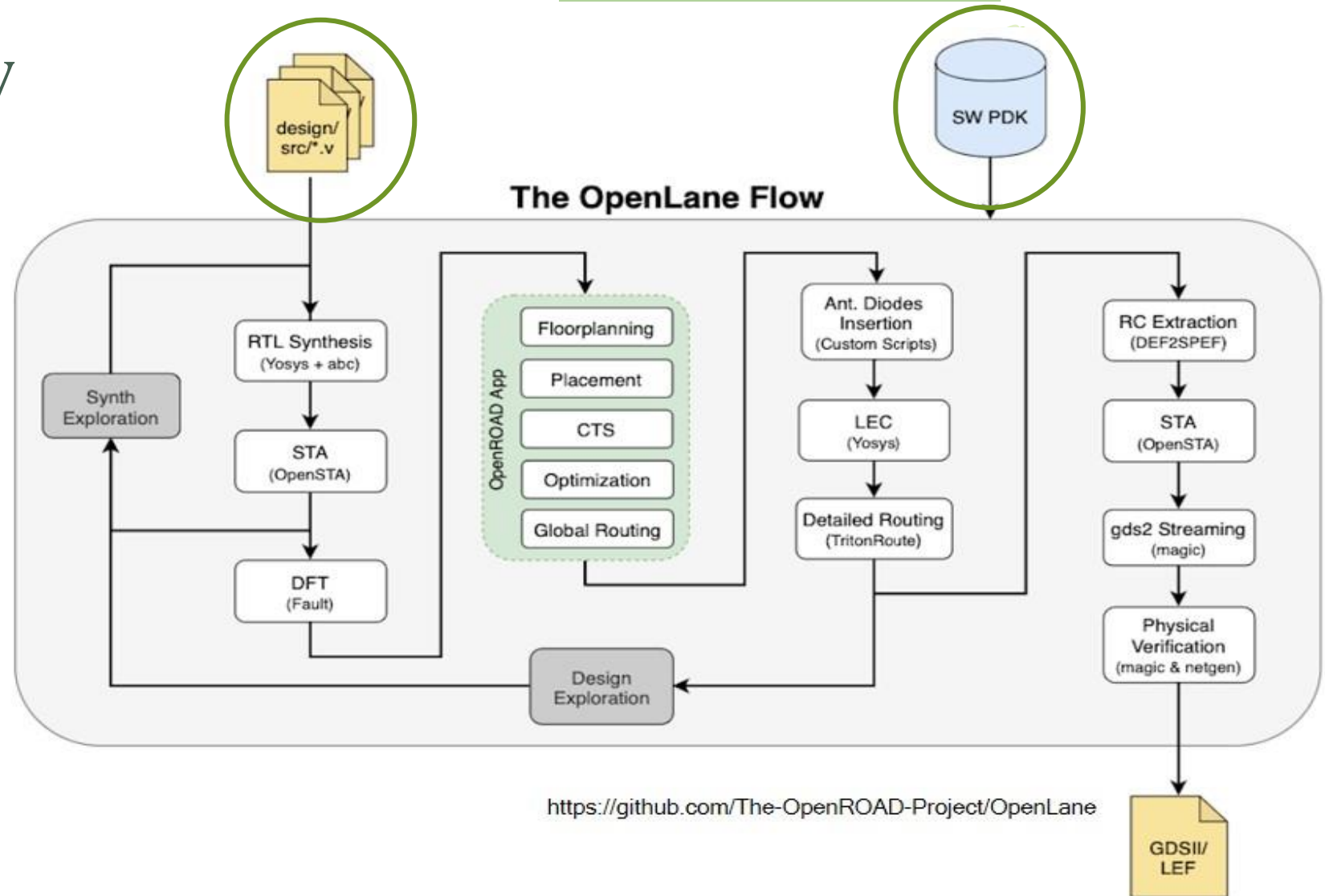


# OpenLane Flow

## ➤ The inputs of the flow?

- Design.v/RTL
- PDK

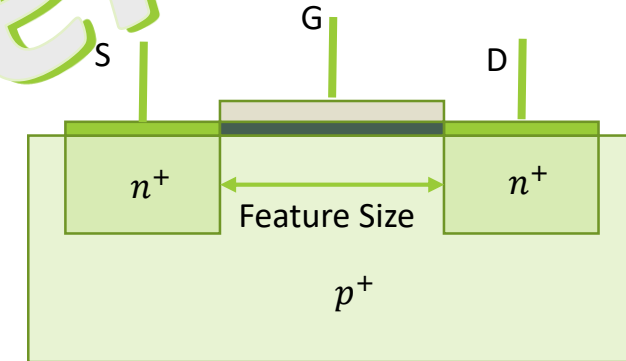
## ➤ What is a PDK?



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# PDK (Process Design Kit)

- It's a set of libraries and associated data to design in a particular technology
- Simpler terms- A PDK contains:
  - Transistors
  - Standard Cells (for digital design)
  - Design Rules
  - Timing/Power Information etc. in library file
  - Layer information



- Technology
    - 130nm
    - 90nm
    - 65nm
    - 45nm
    - 30nm
- Feature Size

# Foundry

- Who provides the PDK?
  - FOUNDRY!
- What is a Foundry?
  - It is a factory where devices such as ICs are manufactured



# Prerequisites for an ASIC Design

## ➤ 3 key ingredients

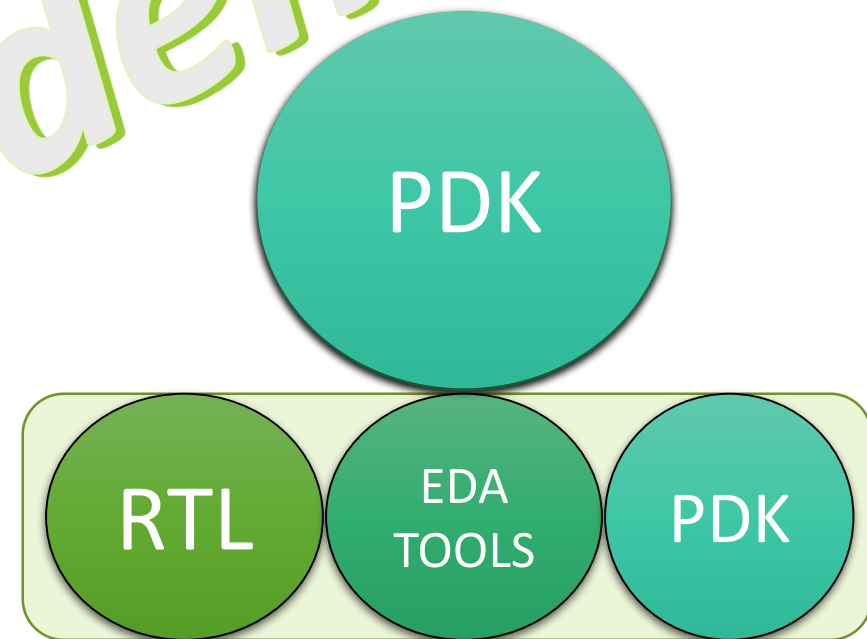
- RTL/Design
- EDA Tools
- PDK

RTL – You can write on your own

EDA TOOLS – You can find open-source tools

PDK - ??????

Until June 2020, the open-source community did not have any solution for accessing PDK!



## ASIC DESIGN



# Sky130 PDK

- First ever open-source PDK
- Multiple process libraries
  - High speed
  - High density etc.
- Contains Standard cells operated at 1.8V
- 1 level of local interconnect, 5 levels of metal

# LAB PRACTICE

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