Synthesis

Workshop Session 3

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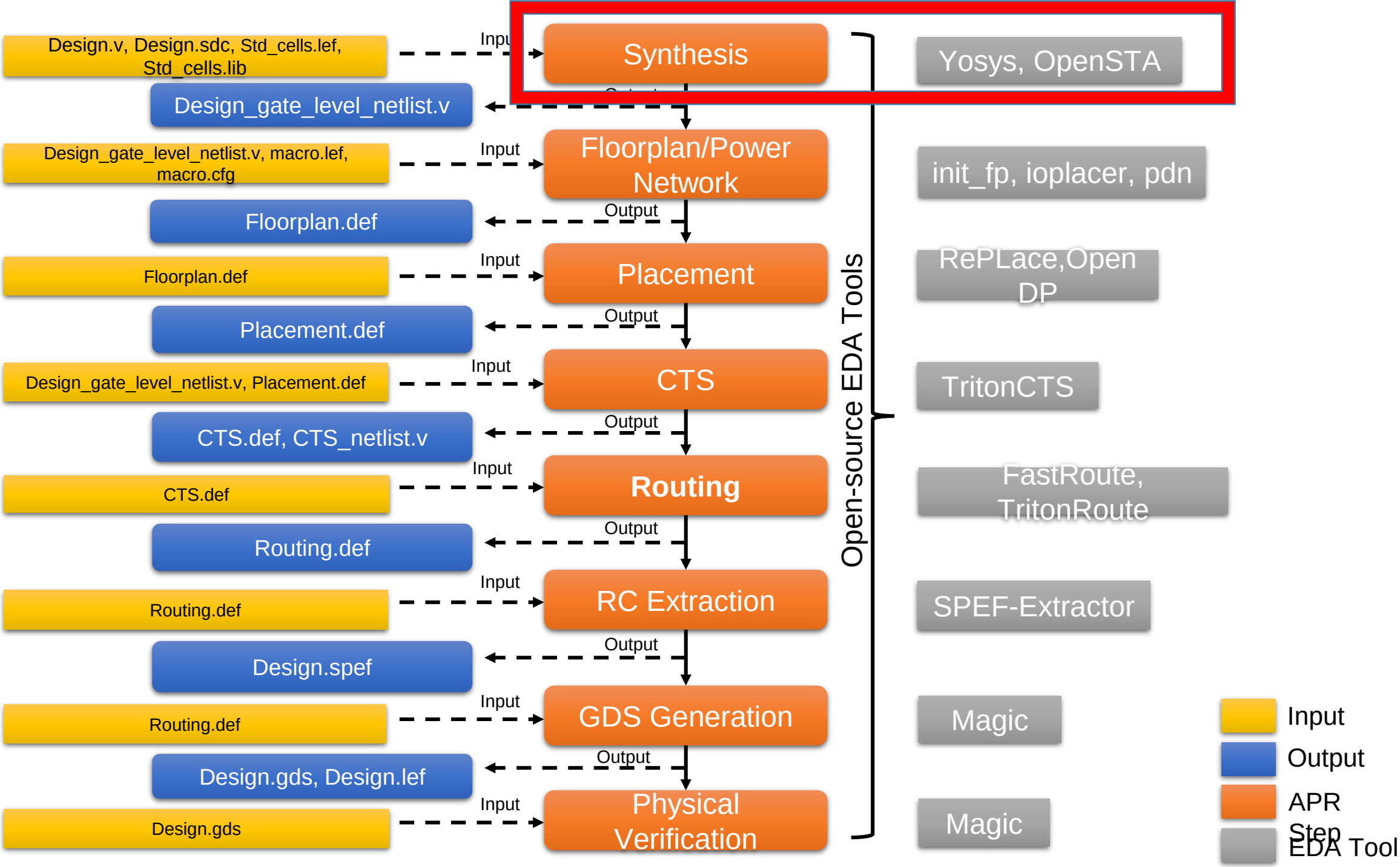
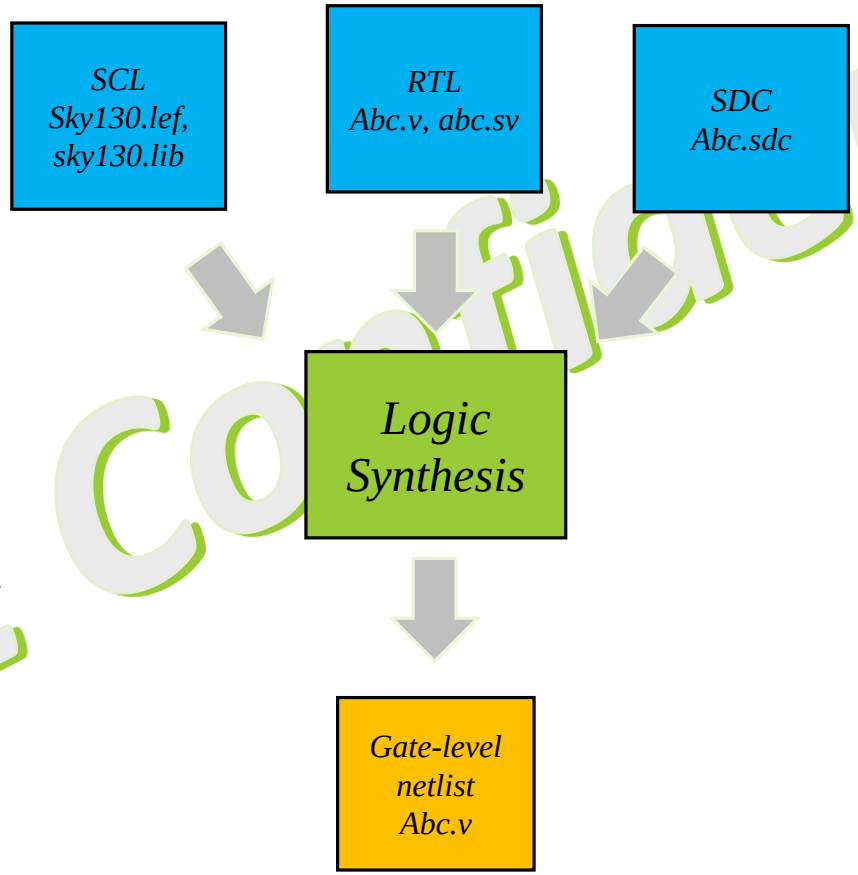
- LAB PRACTICE


Design.v, Design.sdc, Std_cells.lef, Std_cells.lib
Input
Synthesis
Yosys, OpenSTA
Design_gate_level_netlist.v
Design_gate_level_netlist.v, macro.lef, macro.cfg
Input
Floorplan/Power Network
init_fp, ioplacer, pdn
Floorplan.def
Output
Floorplan.def
Input
Placement
RePLace,Open DP
Placement.def
Output
Design_gate_level_netlist.v, Placement.def
Input
CTS
TritonCTS
CTS.def, CTS_netlist.v
Output
CTS.def
Input
Routing
FastRoute, TritonRoute
Routing.def
Output
Routing.def
Input
RC Extraction
SPEF-Extractor
Design.spef
Output
Routing.def
Input
GDS Generation
Magic
Design.gds, Design.lef
Output
Design.gds
Input
Physical Verification
Magic
Open-source EDA Tools
Input
Output
APR Step
EDA Tool

What is Synthesis?

What are SCL?
- Standard cell library
- Collection of building blocks

What is SDC?
- Synopsis Design Constraint
- Timing constraints in a design.



RTL

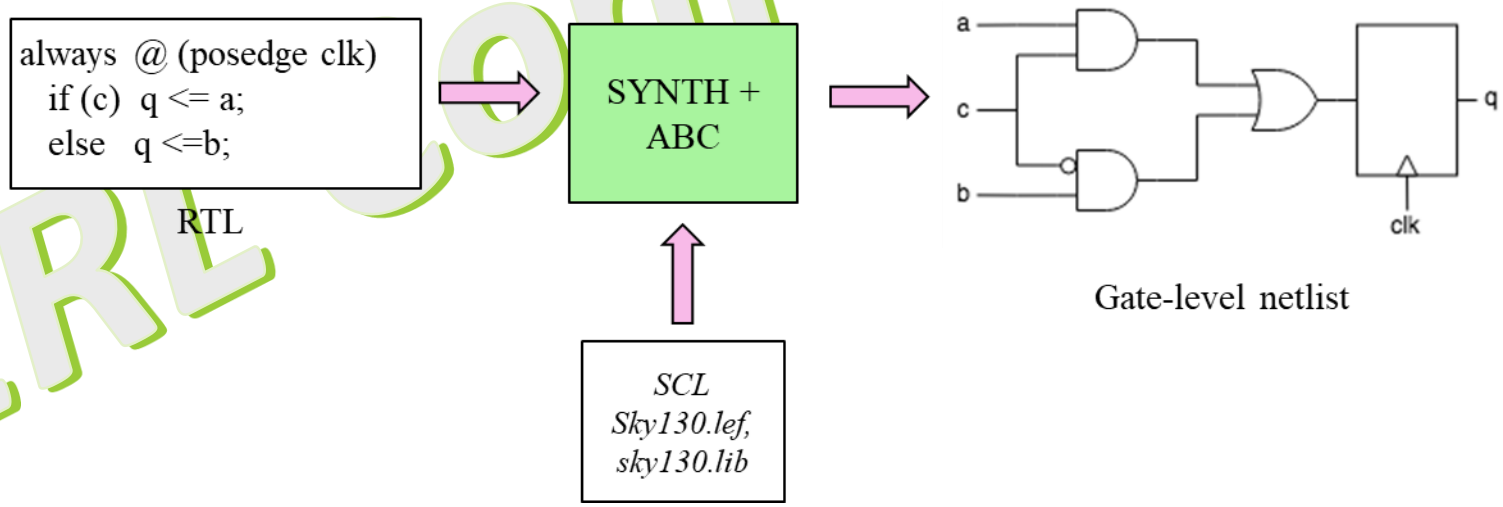
```
module inverter (
   input wire in,
   output out );
   assign out = !in;
endmodule
```

Gate-Level Netlist

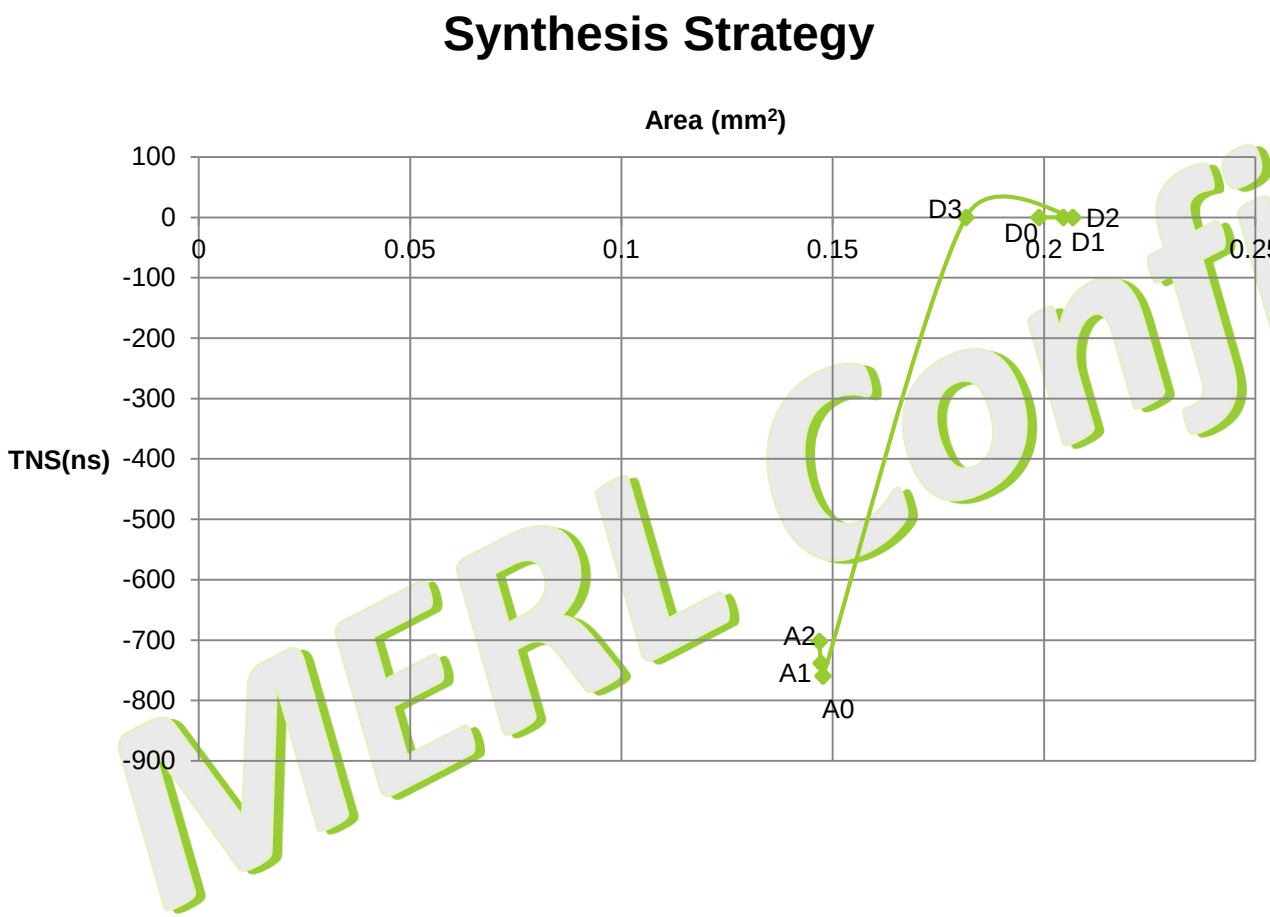
```
module inverter(in, out);
  input in;
  output out;

sky130_fd_sc_hd__inv_
2 _0_ (
    .A(in),
    .Y(out)
  );
endmodule
```

What is Synthesis?

- **Translation**; Identifies logic,
- **Optimization**; Technology-independent optimizations,
- **Mapping**; Map logic elements to target technology (standard cell library).



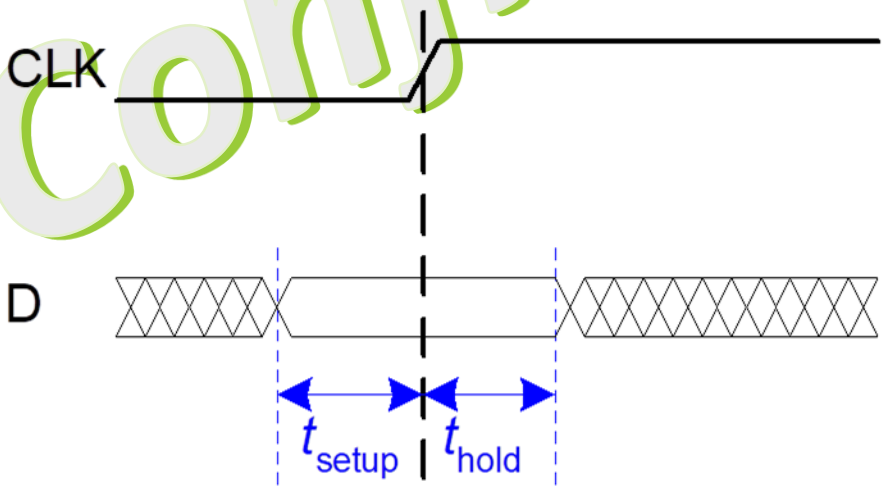
Design Exploration Strategy



Trade-off between Area and Timing

Basics of Timing

- Setup time : t_{setup} = time *before* the clock edge that data must be stable (i.e. not changing)
- Hold time: t_{hold} = time *after* the clock edge that data must be stable



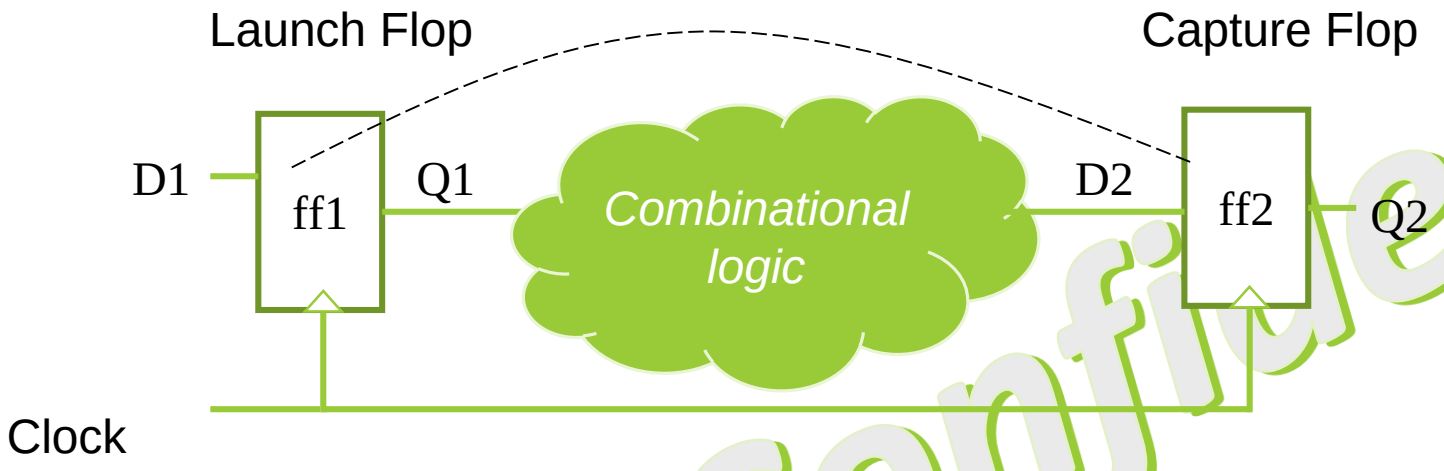
Timing Delays

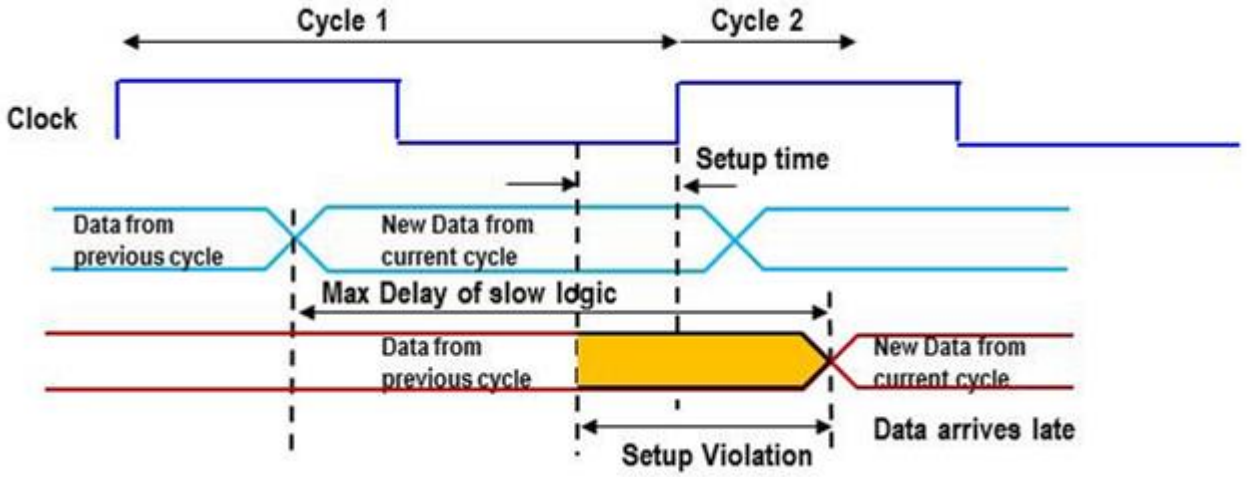
Main delay concerns in circuits:

- Gate delays are due to gate transitions
- Wire delays are due to signal propagation along wires
- Clock skew is due to the difference in time the sequential elements activate.

- **Assume clock skew is negligible, we'll discuss in more detail in Clock Tree Synthesis tutorial.**

Setup time violations



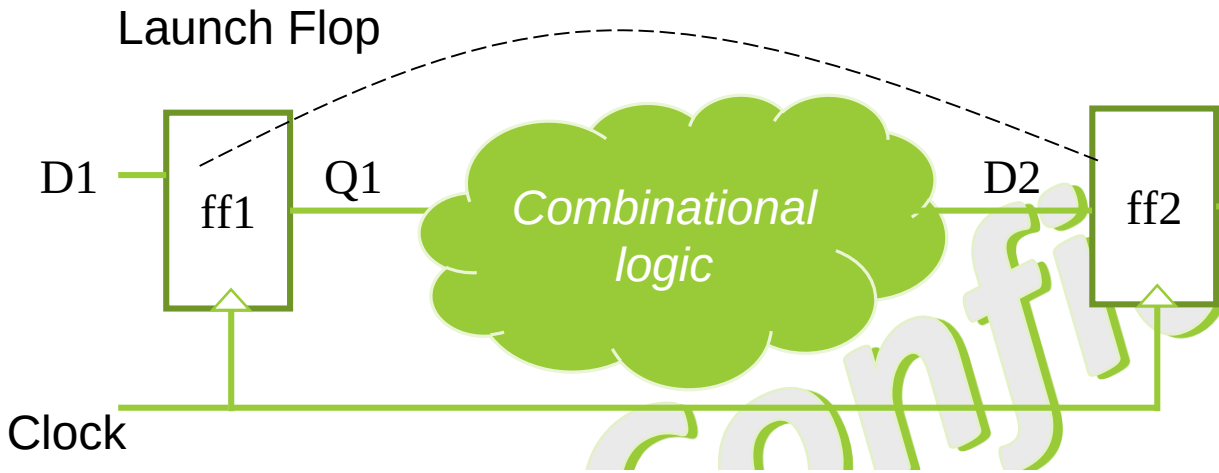


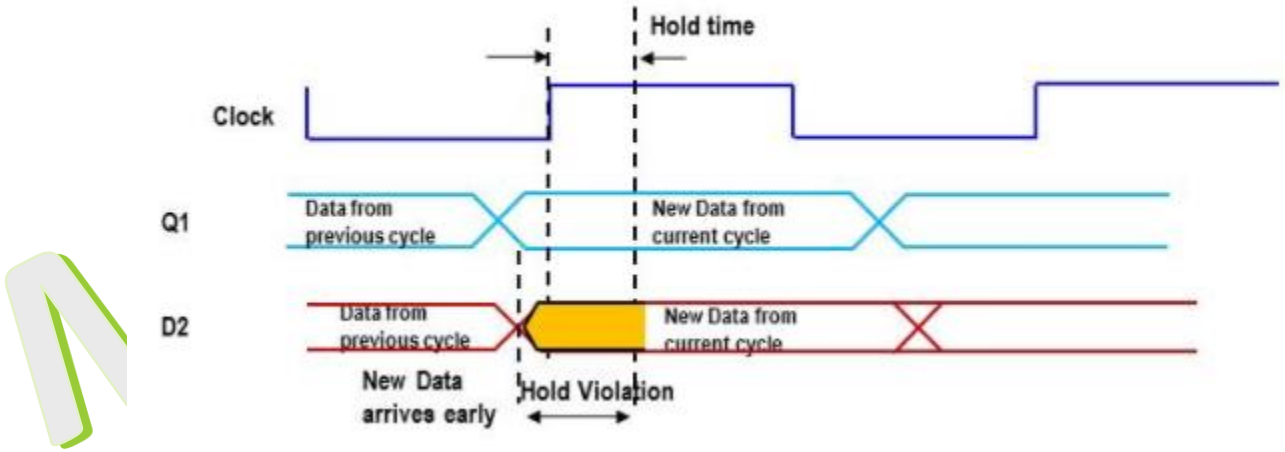
Setup violations can be fixed by either;

- Increasing the clock period
- Decreasing the delay of the data path logic

$$t_{Clock} \geq t_{combDelay} + t_{setup}$$

Hold time violations





$t_{combDelay} \geq t_{hold}$

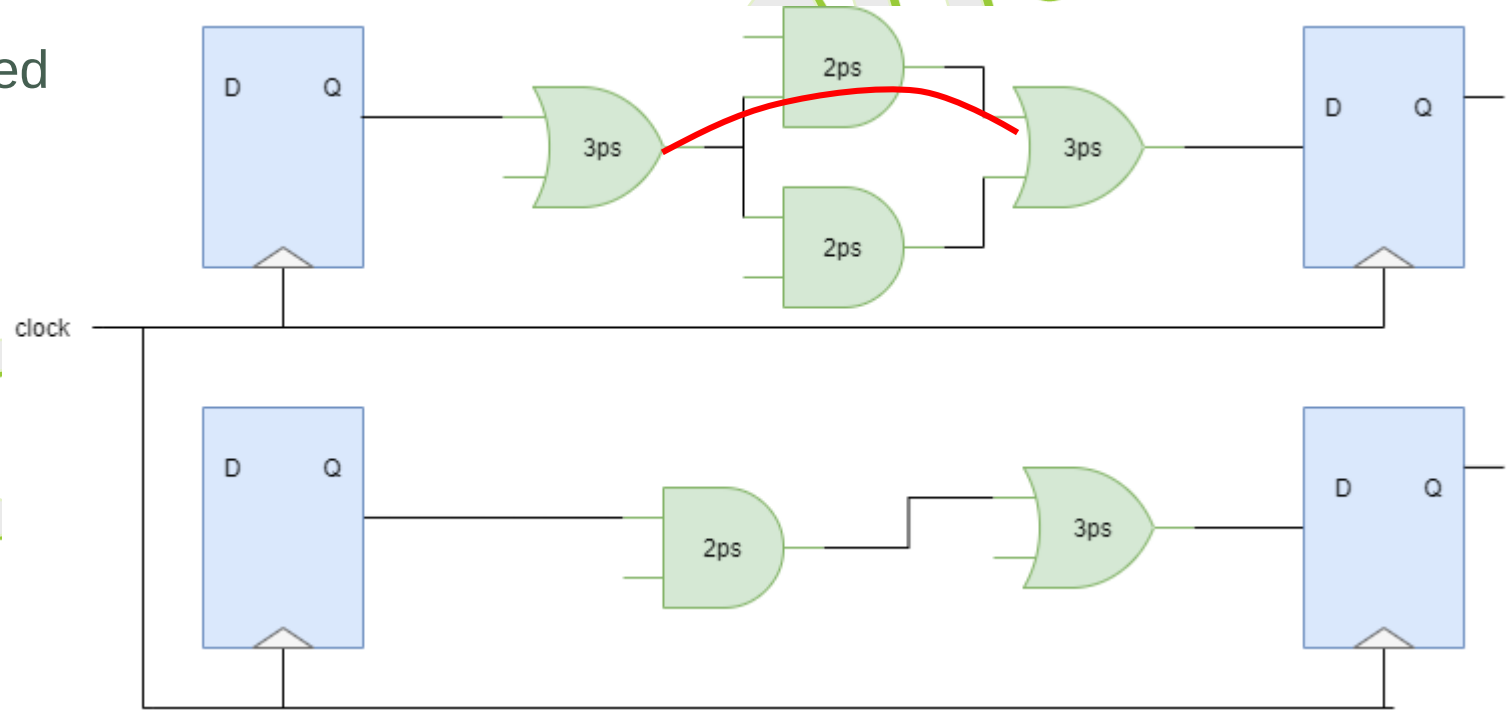
Static Timing Analysis

- Here we will be looking at **SLACK!**
- It is the **difference between the Required arrival times and the actual arrival time for a signal.**
- Compute the slack = RAT – AAT
- RAT is the required arrival time, latest time signal can transition
- AAT is the actual arrival time
- Negative slack at any output means the circuit does not meet timing Positive slack at all outputs means the circuit meets timing

Timing Violations

- Worst Negative Slack (WNS)
- Data arrival time (DAT) > required arrival time (RAT)
  - DAT=Gate delay + Net delay = 3+2+3+Net delay > Arrival time
  - negative slack exists

- Total Negative Slack (TNS)
  - Sum of all the delays



Clock period (T_{RAT}) = 5ps

Thank you