Placement
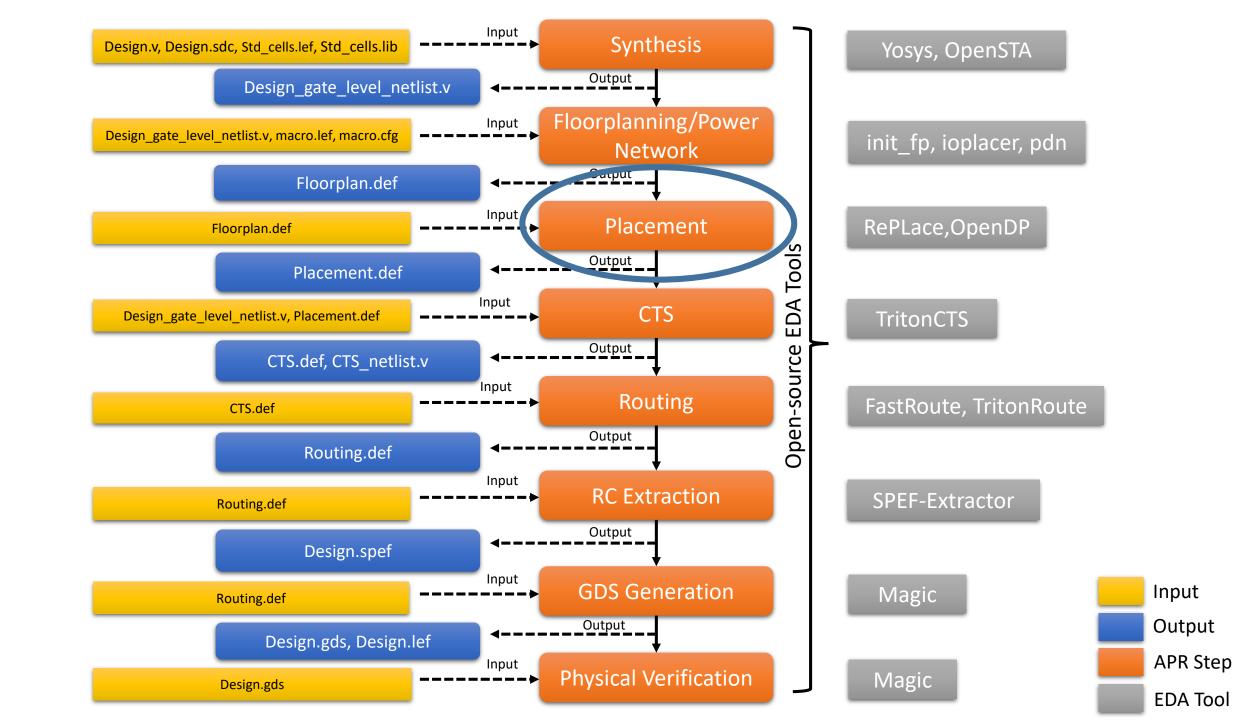
Workshop Session 5

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Step	Input	Output	EDA Tool
Synthesis	Design.v, Design.sdc, Std_cells.lef, Std_cells.lib	Design_gate_level_netlist.v	Yosys, OpenSTA
Floorplanning/Power Network	Design_gate_level_netlist.v, macro.lef, macro.cfg	Floorplan.def	init_fp, ioplacer, pdn
Placement	Floorplan.def	Placement.def	RePLace, OpenDP
CTS	Design_gate_level_netlist.v, Placement.def	CTS.def, CTS_netlist.v	TritonCTS
Routing	CTS.def	Routing.def	FastRoute, TritonRoute
RC Extraction	Routing.def	Design.spef	SPEF-Extractor
GDS Generation	Routing.def	Design.gds, Design.lef	Magic
Physical Verification	Design.gds		Magic

Open-source EDA Tools

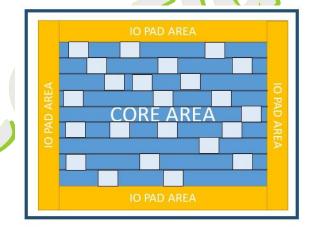Legend:
- Input
- Output
- APR Step
- EDA Tool

Contents

- Placement
  - Global Placement
  - Detailed Placement
- Power connection of Standard Cells
- Target Density
- Macro/IP Placement
  - Macro/IP
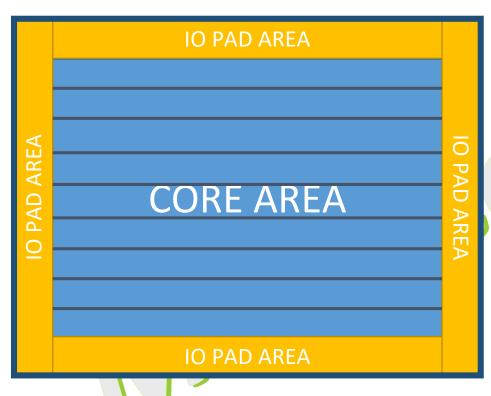   - Soft Macro/IP
    - Hard Macro/IP

- LAB PRACTICE

Placement

➢ What is Placement?
- Placement is the process of finding suitable location for each cell in the block
- Placement of standard cells over the core area

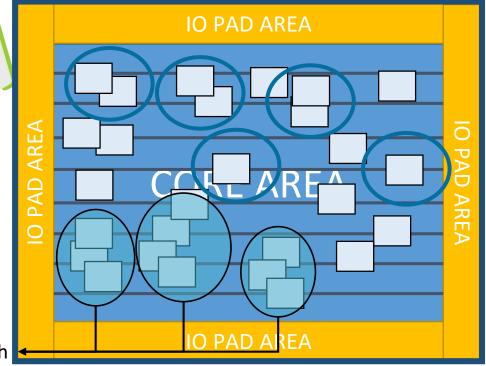 • Global placement
  • Detailed placement

Global Placement

Coarse placement of all the standard cells

- Overlaps
- Row intersection

Global Placement

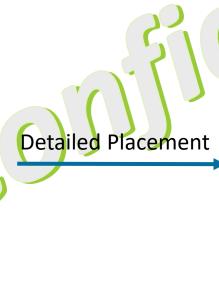It tries to place cells closer which are connected to each other
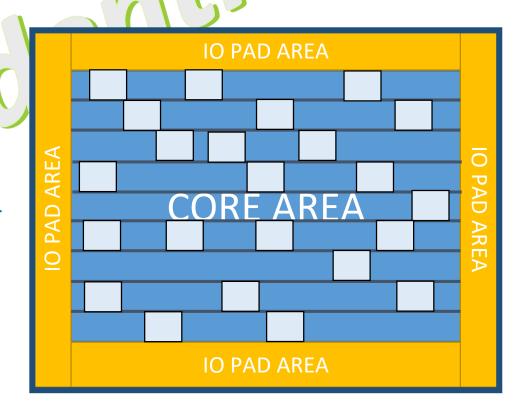
Detailed Placement

Legal placement of all the standard cells

- NO Overlaps
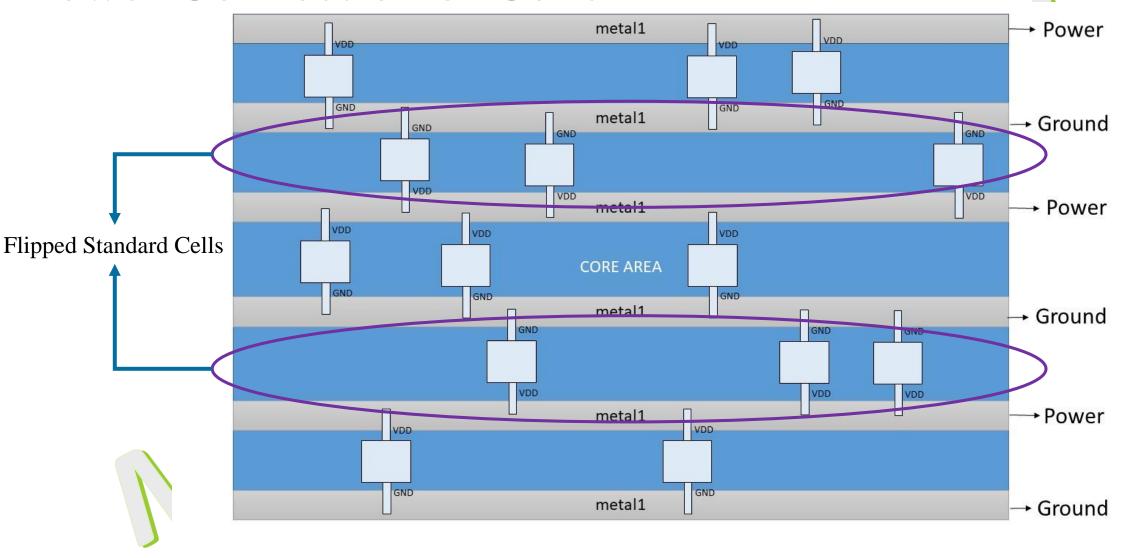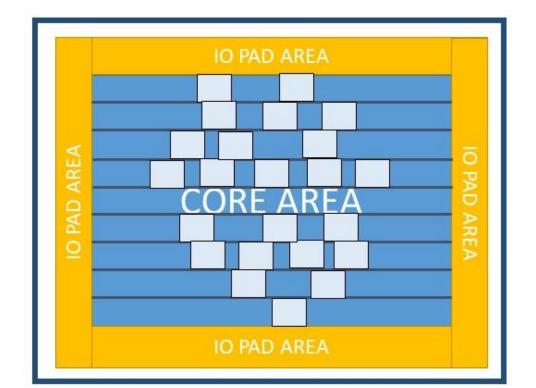- NO Row intersection

Detailed Placement

Power Connection of Cells

Flipped Standard Cells
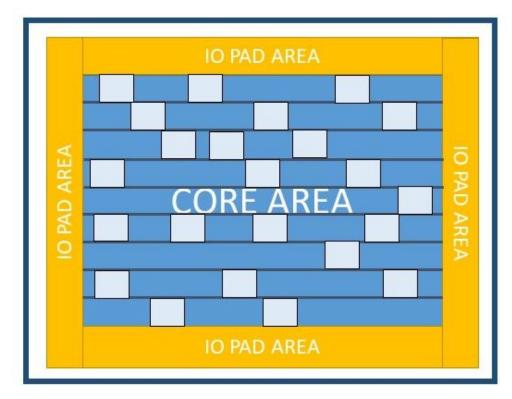
Target Density

TARGET DENSITY = 0.6

TARGET DENSITY = 0.9

IO PAD AREA

IO PAD AREA

IO PAD AREA

IO PAD AREA

CORE AREA

CORE AREA

IO PAD AREA

IO PAD AREA

IO PAD AREA

IO PAD AREA

The above comparison is a rough estimate
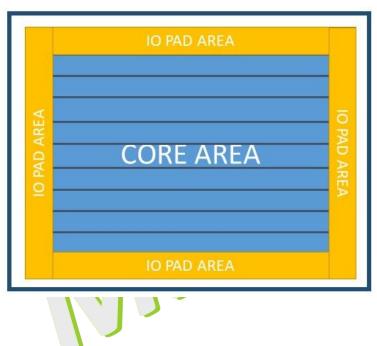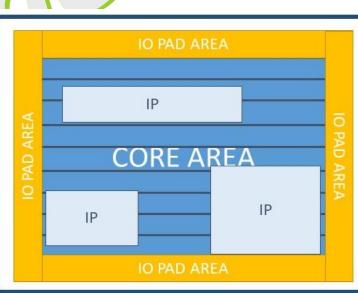
Macro/IP Placement

➢ It is an intellectual property
  - Not your own work, but you have bought it from someone to use it in your design

➢ Two major types
  - Soft Macro/IP
    - RTL
  - Hard Macro/IP
    - Hardened Macro [A black box with only freedom to flip rotate]

You don't know what's inside

Macro/IP Placement

➢ Using hard macros in the design
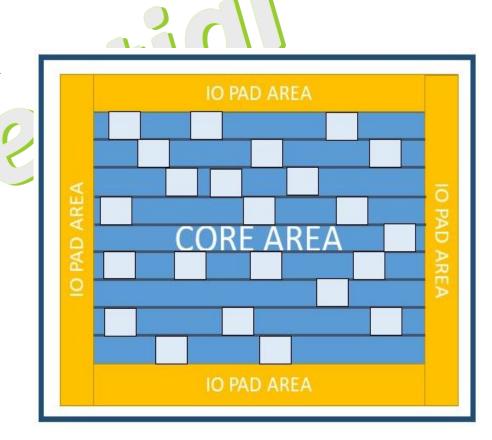

Assuming 3 macros are used

Macro/IP Placement

➢ We were assuming a height of standard cells equal to the rows
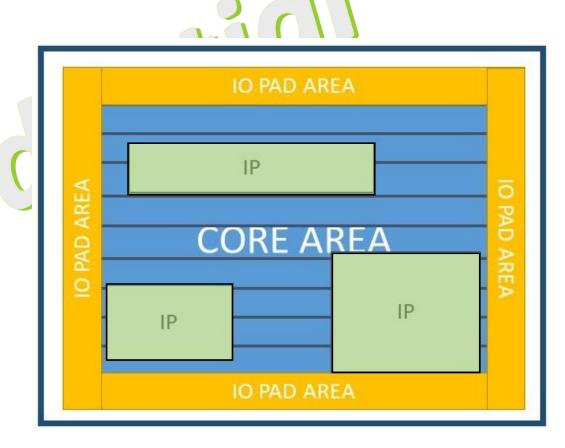
➢ The size here is different

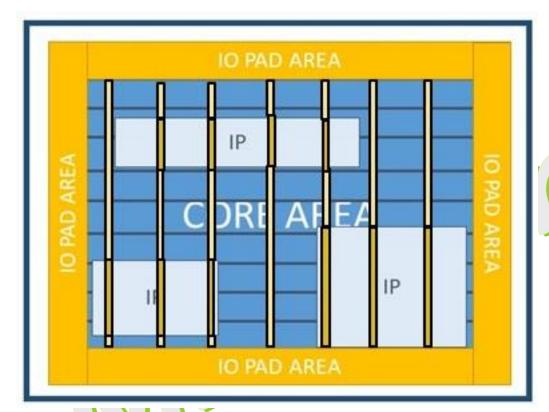➢ Our power network theory went down the drain

Macro/IP Placement

➢How to power these macros?
- Power grid

➢How to restrict routing and placement of standard cells over the macros?
- Blockages!
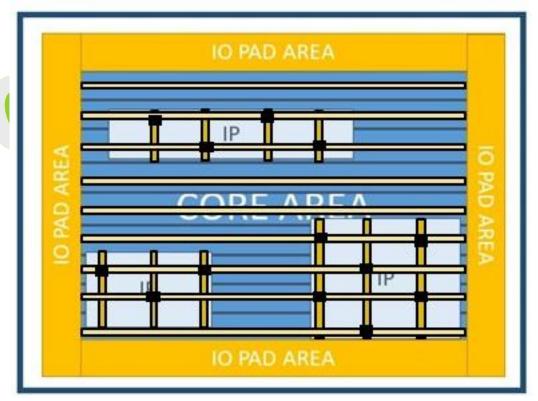 - For blockages you define the macro area to be restricted

Powering the Macros

➢ Here are 2 techniques discussed to power up the macro

Align the vertical straps of Macro to the core connecting them

Connect metal x of core to metal y of the macro through via

Key Point To Remember

➢Placement of macros should be done before the placement of standard cells

LAB PRACTICE