Tutorial Number 6

CLOCK TREE SYNTHESIS (CTS)

LEARNING OUTCOMES:

At the end of this lab, participants will be able to:

1. Identify the CTS Quality Checks (Skew, Power, Latency, etc.) in log file
2. Run the whole flow for CTS
3. Explore its different environment variable
4. View the statistics for a complete CTS flow.
5. Meet the timing requirements for the design using clock Tre buffering.

Running the flow interactively

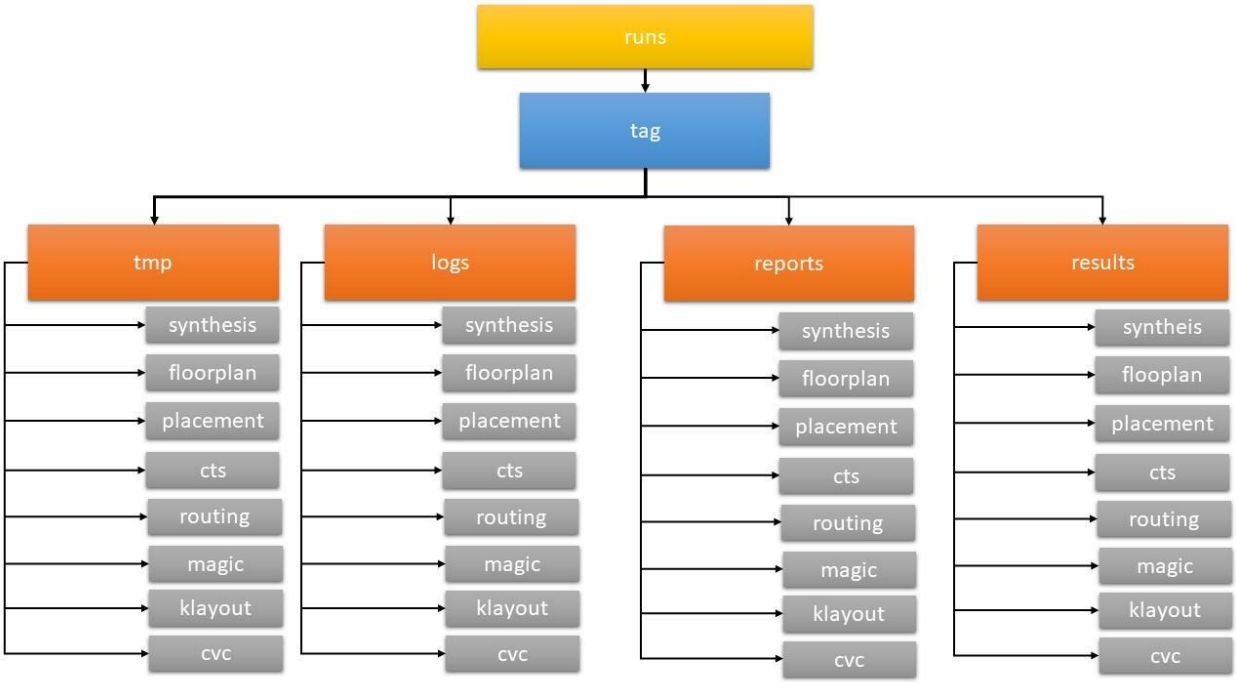
Go to the working directory by:

cd /home/merl-tools/openlane_v0.9/openlane

- ./flow.tcl –interactive
- Prep –design spm_wajeh
- Run_synthesis
- Run_floorplan
- add_macro_placement <macro_name> <x_coordinate> <y_coordinate> [<orientation>]
- manual_macro_placement [f]
- run_placement
- run_cts

Using Klayout to look at the layout

Go to the directory containing the DEF file. It is in the **runs** directory of your design



- Klayout design_name.def

Tasks

1. Explore the different files generated