Tutorial Number 7 & 8

Routing & Checkers

LEARNING OUTCOMES:

At the end of this lab, participants will be able to:

1. How to run routing
2. Differentiate between global and detailed routing
3. How to tackle routing violations
4. Stream out the final GDSII Layout
5. How to run magic
6. How to view GDS on Klayout
7. Check DRC and LVS and Antenna violation error

For this lab we will be exploring the design picorv32a.

LabTask: Create a copy of the design picorv32a with your name in the designs directory as follows **picorv32a_<your_name>.**

Step 1:

Routing in interactive mode:

- ./flow.tcl -interactive
- prep –design apm_<your_name> -tag first_run
- run_synthesis
- run_floorplan
- run_placement
- run_cts
- **run_routing**

- write_powered_verilog followed by set_netlist $::env(lvs_result_file_tag).powered.v
- **run_magic**
- **run_magic_spice_export**
- **run_magic_drc**

- **run_lvs**
- **run_antenna_check**

HomeTasks:

1. Observe the effect of varying GLB_RT_ADJUSTMENT parameters on routing violations for picorv32a.

   (Vary the value of ::env(GLB_RT_ADJUSTMENT**) in design config.tcl file)**

2. Run the whole flow of any design from synthesis to checkers.