Clock Tree Synthesis

Workshop Session 6

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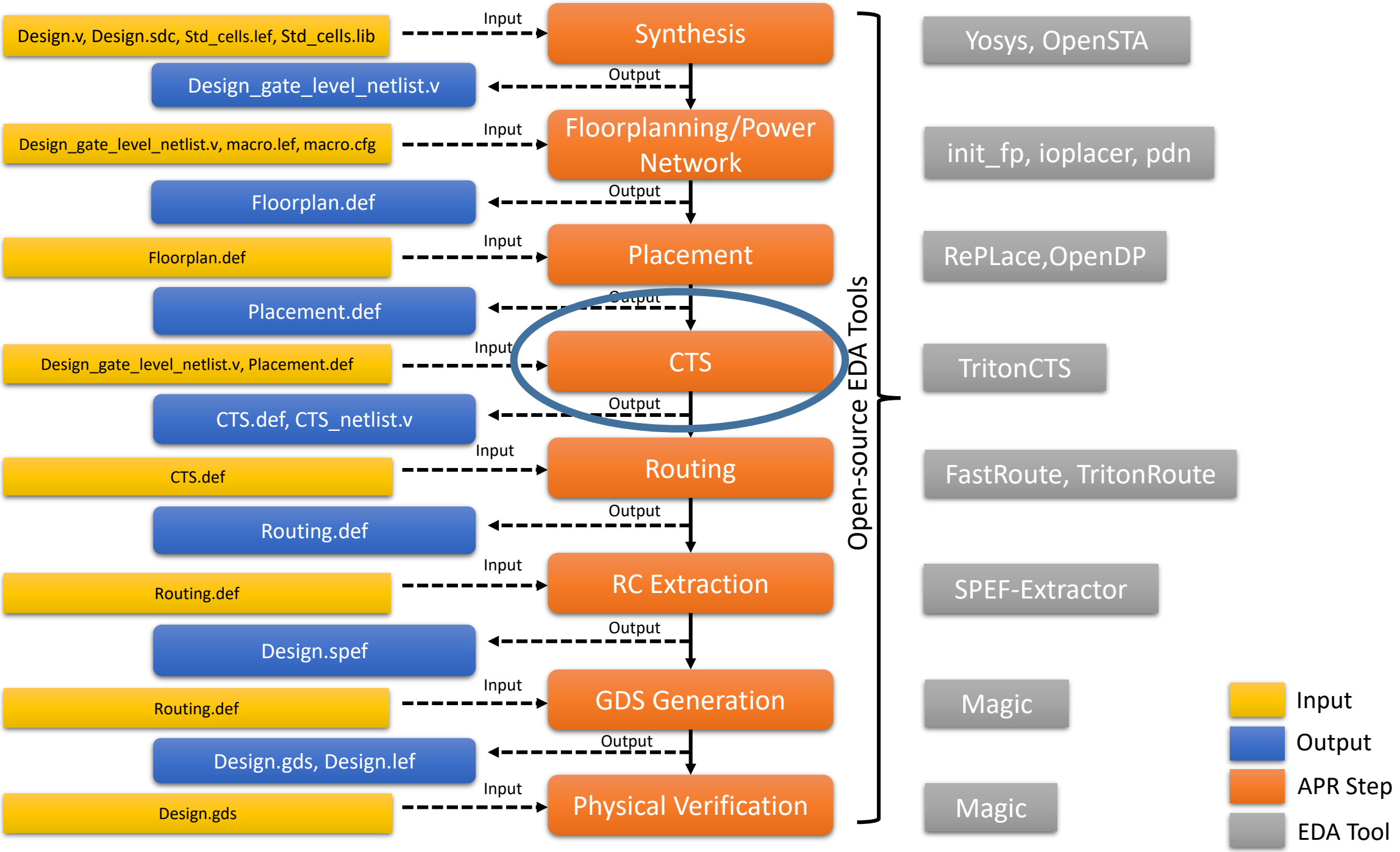
Design.v, Design.sdc, Std_cells.lef, Std_cells.lib
Input
Synthesis
Yosys, OpenSTA
Design_gate_level_netlist.v
Output
Design_gate_level_netlist.v, macro.lef, macro.cfg
Input
Floorplanning/Power Network
init_fp, ioplacer, pdn
Floorplan.def
Output
Floorplan.def
Input
Placement
RePLace,OpenDP
Placement.def
Output
Design_gate_level_netlist.v, Placement.def
Input
CTS
TritonCTS
CTS.def, CTS_netlist.v
Output
CTS.def
Input
Routing
FastRoute, TritonRoute
Routing.def
Output
Routing.def
Input
RC Extraction
SPEF-Extractor
Design.spef
Output
Routing.def
Input
GDS Generation
Magic
Design.gds, Design.lef
Output
Design.gds
Input
Physical Verification
Magic
Open-source EDA Tools
Input
Output
APR Step
EDA Tool

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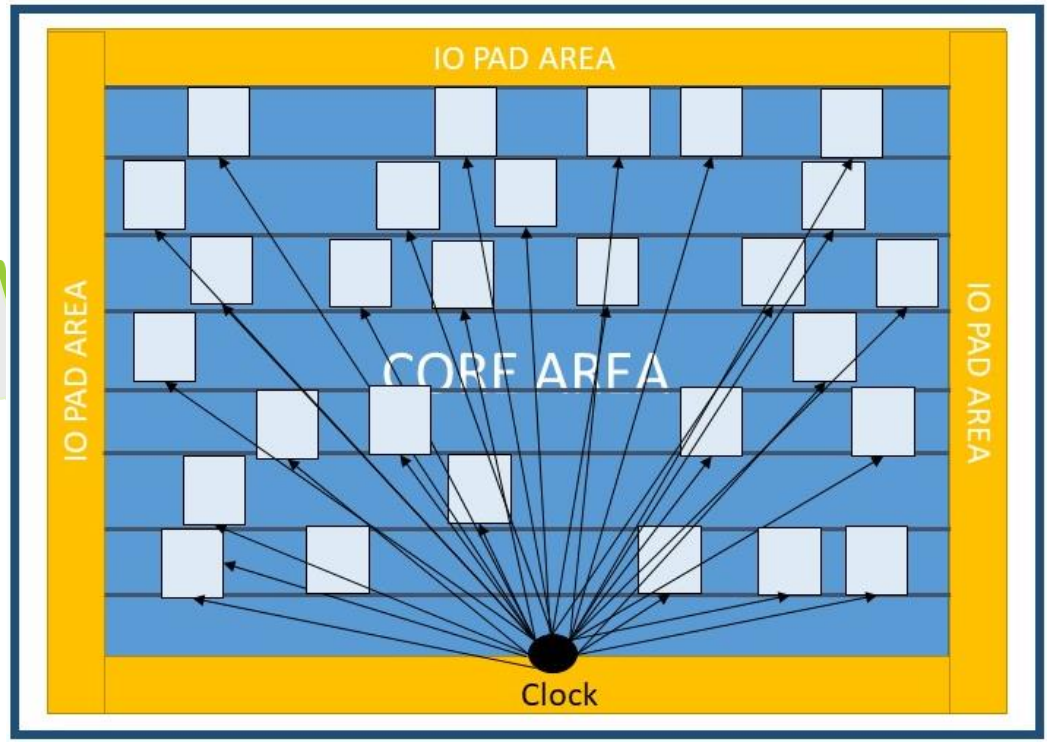
- LAB PRACTICE

Clock Tree Synthesis

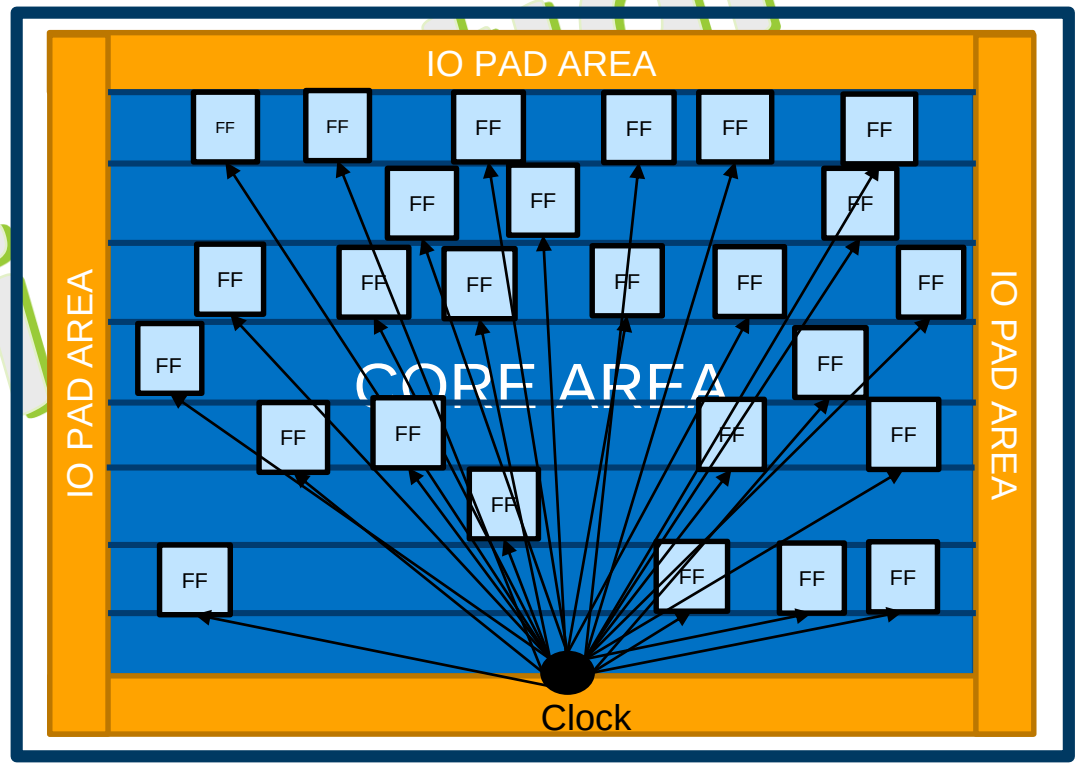
- Clock Tree Synthesis (CTS) is a process which distributes the clock evenly to all sequential elements in a design
- It adds buffers and inverters to achieve zero/minimum skew or balanced skew



Clock Tree Synthesis

- Why can't the clock be routed like any other net?

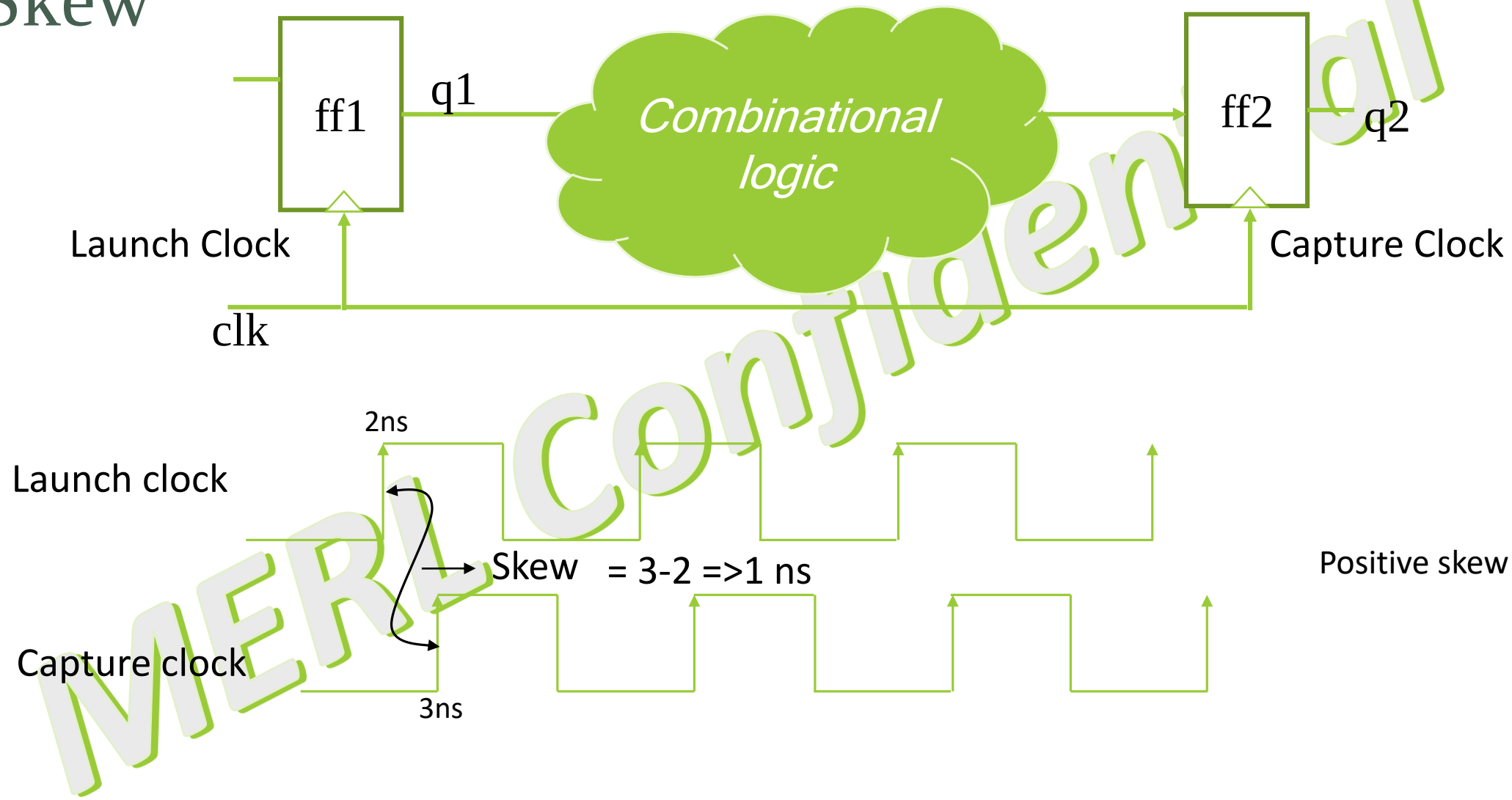
- Implications on clock
  - Timing
  - Power
  - Signal integrity etc.



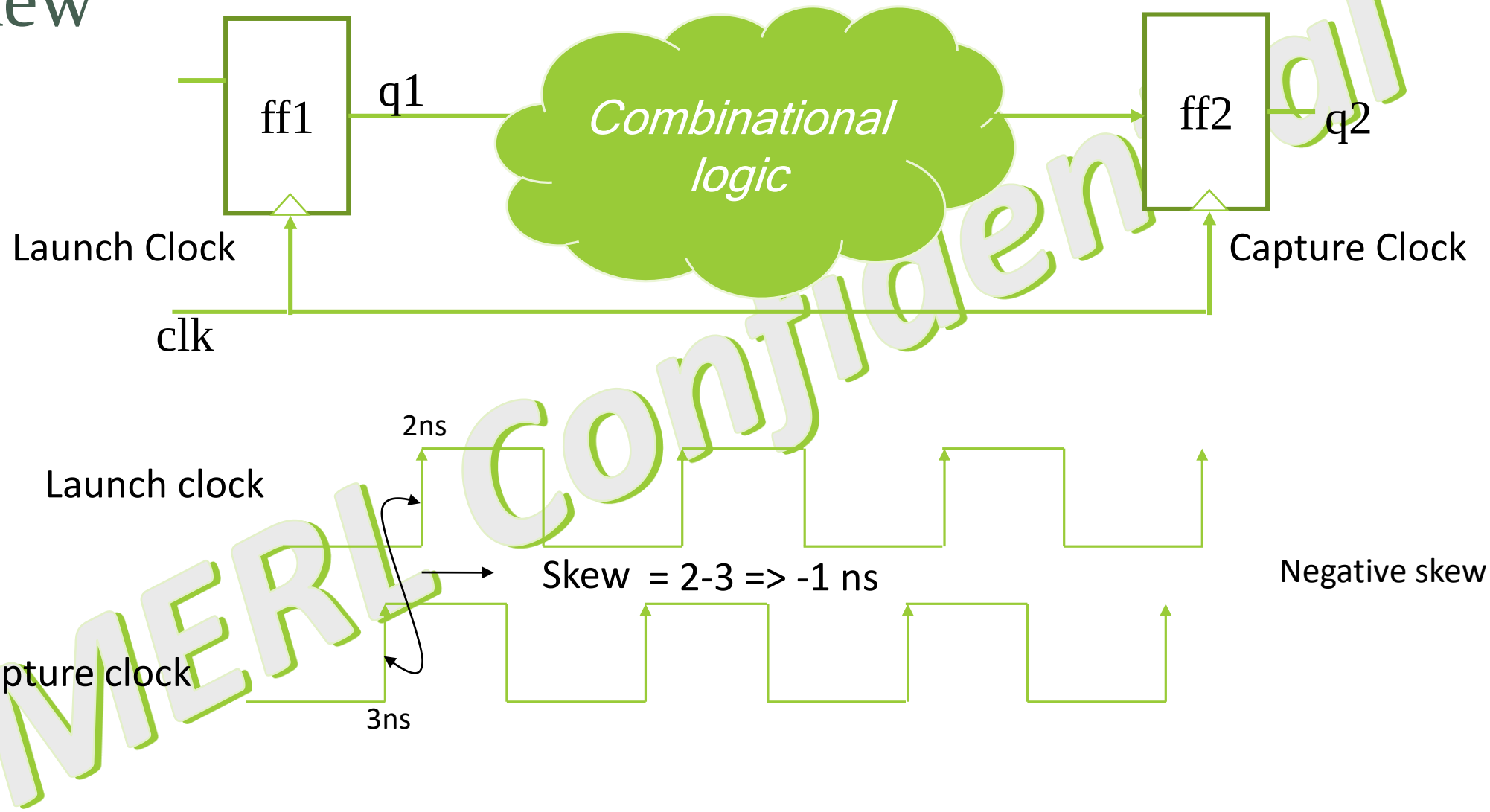
Timing

- **Skew**
  - Clock skew is the difference in the arrival time of a clock signal at two different Flops.
- **Jitter**
  - Clock jitter is the deviation of a clock edge from its ideal position in time
- **Slew**
  - Transition time of the clock- rise/fall time of the clock
- **Insertion Delay**
  - The amount of time taken by the clock signal to travel from source to sinks is called the **insertion delay**

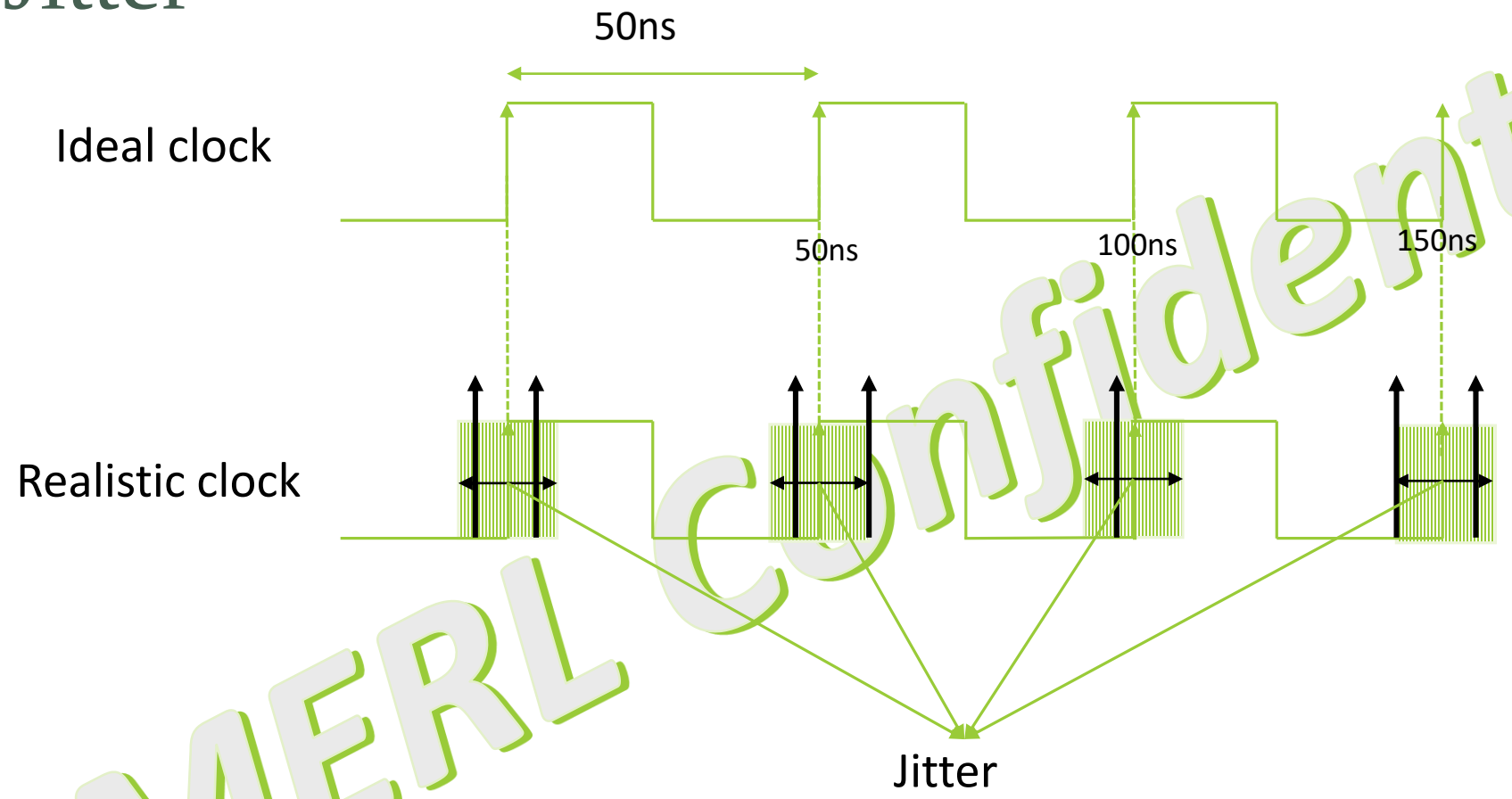
Skew



Skew



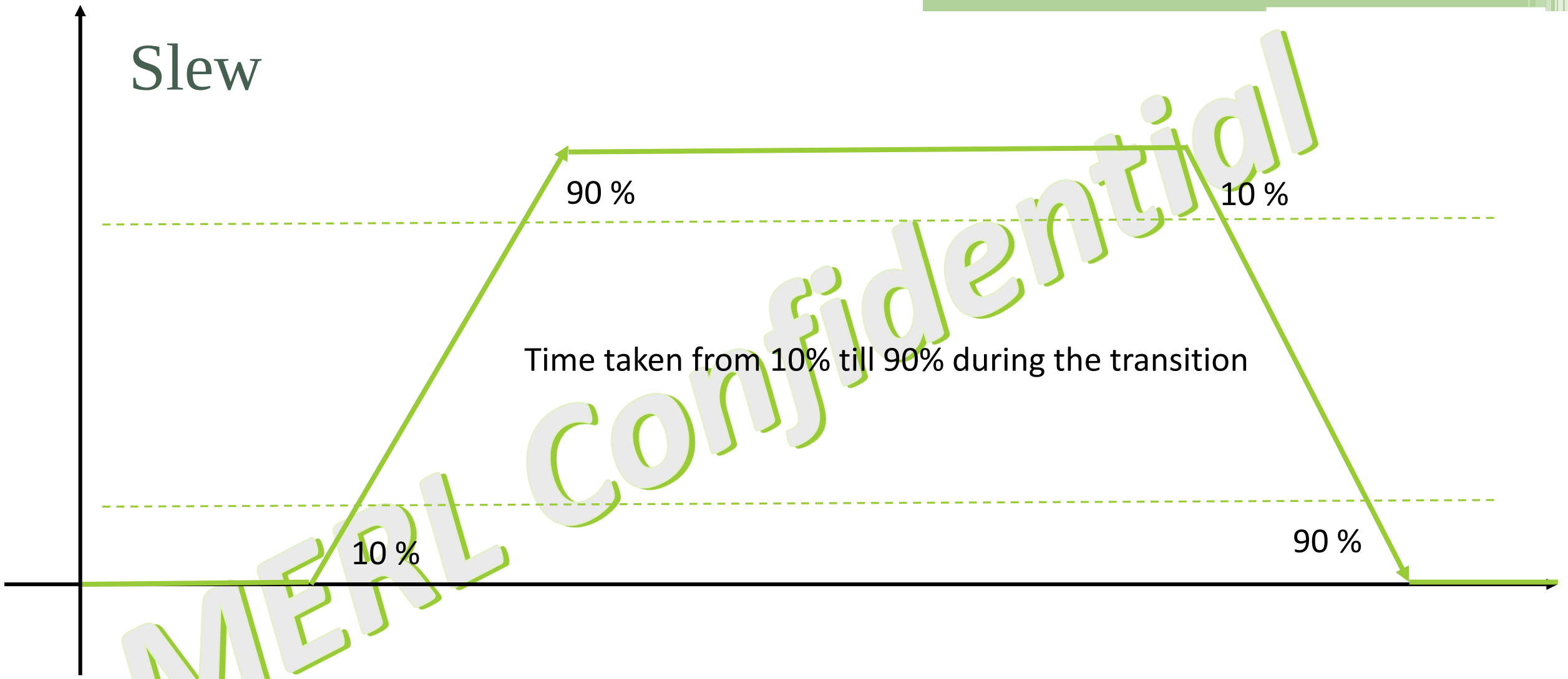
Jitter



CAUSES

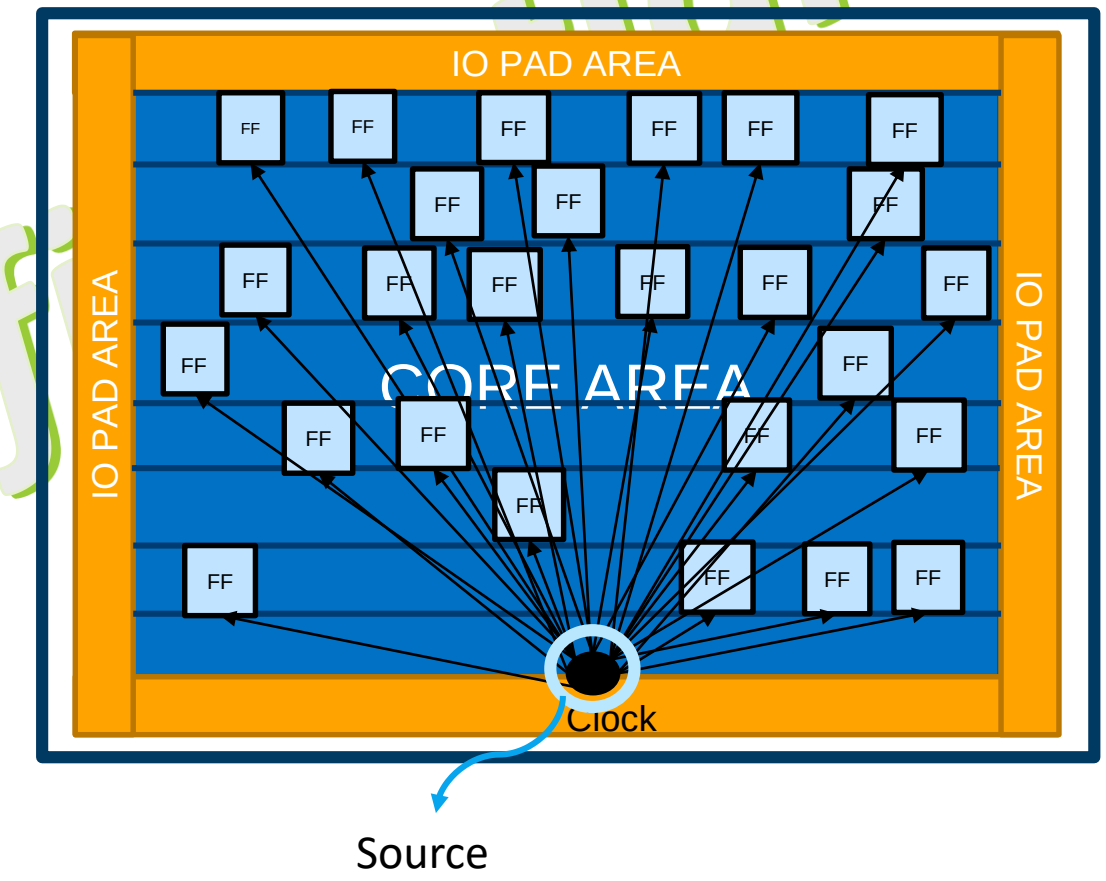
- PLL Noise
- Power Supply Ripples
- Temperature Variations
- Crosstalk Between Signals

Slew



Insertion Delay

The time from the source of the clock to the sink is called insertion delay



Power

$$P_{dyn} = f \,.C_{eff} \,.{V_{dd}}^2$$

- The clock capacitance consists of
  - Clock Generation [PLL etc]
  - Clock Elements [Buffers etc]
  - Clock Wires
  - Clock Load Of Sequential Elements

- The clock networks are so huge that they require a large percentage of the total chip power.

Signal Integrity

- Noise can disrupt the clock
  - Irregular clock edges can effect the register operation
- Slow clock transition
  - Bad $t_{cq}, t_{setup}, t_{hold}$
- Fast clock transition
  - Power
  - Area

Solution?

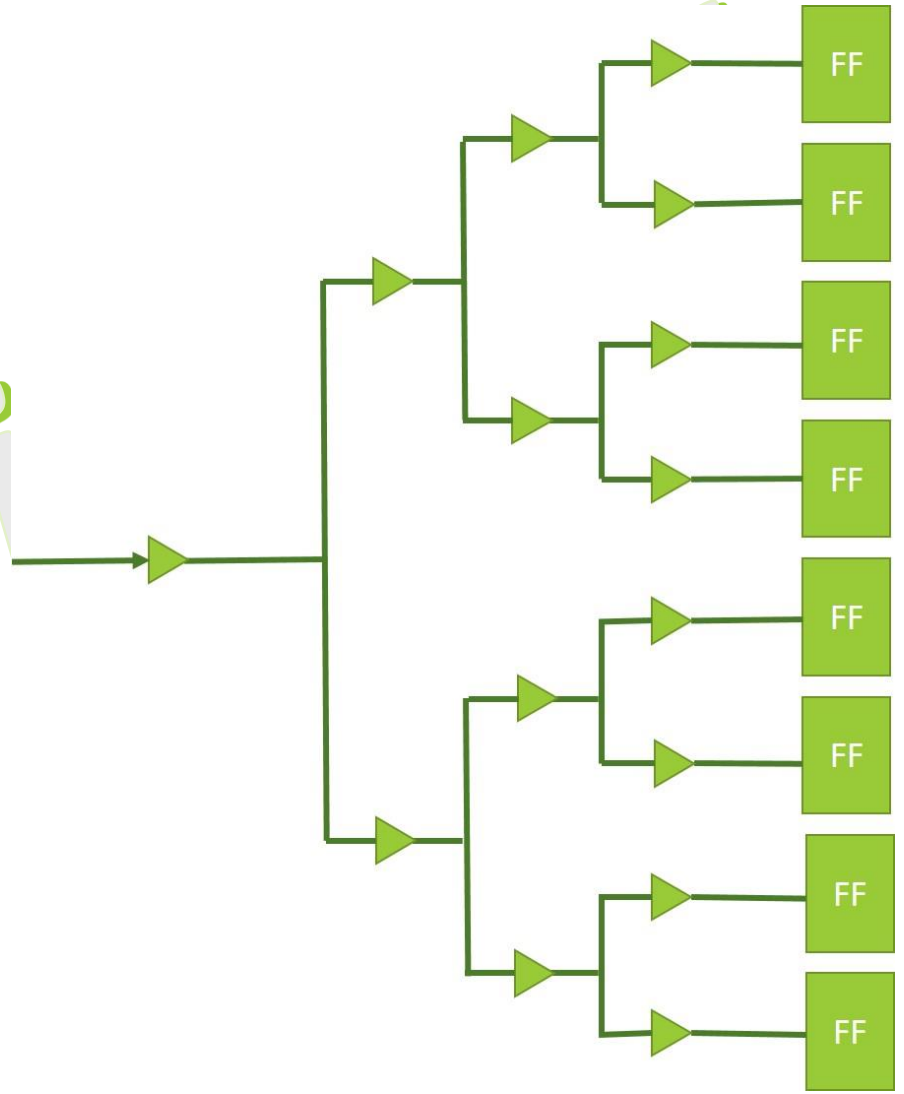
- Trees
  - H-Tree
  - Mesh Tree [Grid]
  - Spine tree

Clock Tree

- Try to make a tree
  - Balance the RC-Delay
- Challenges ?
  - Excessive power usage
  - Large RC for each net
  - Signal integrity at risk
- Solution ?
  - Buffered Tree

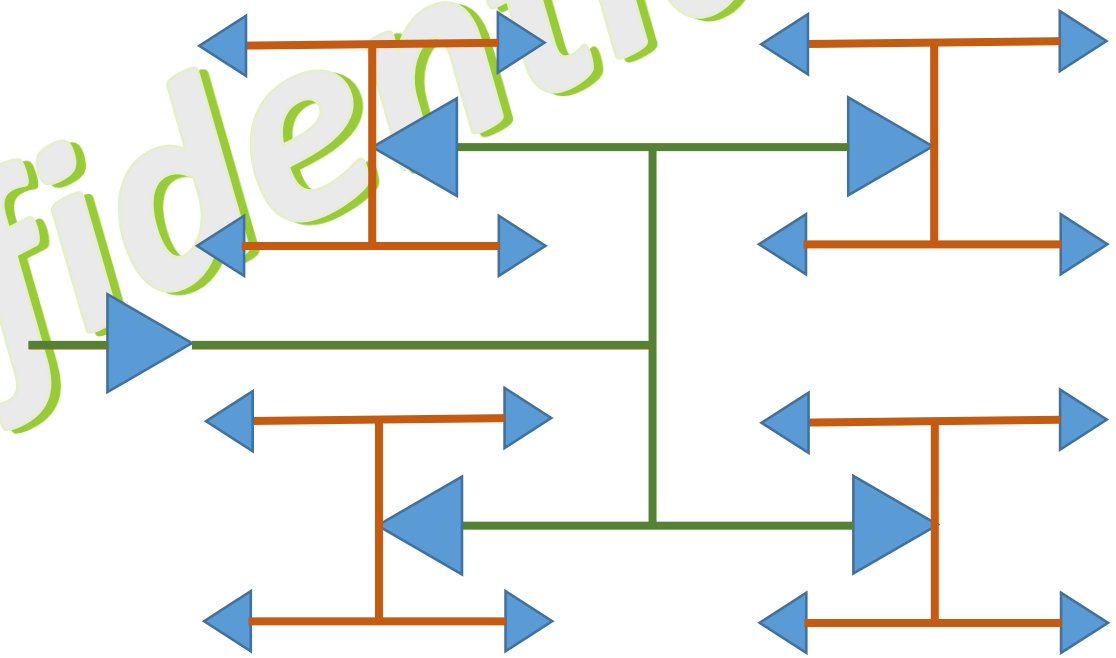
Buffered Tree

- Good slew rates
- Less total switching capacitance
- Lower RC Values



H-Tree

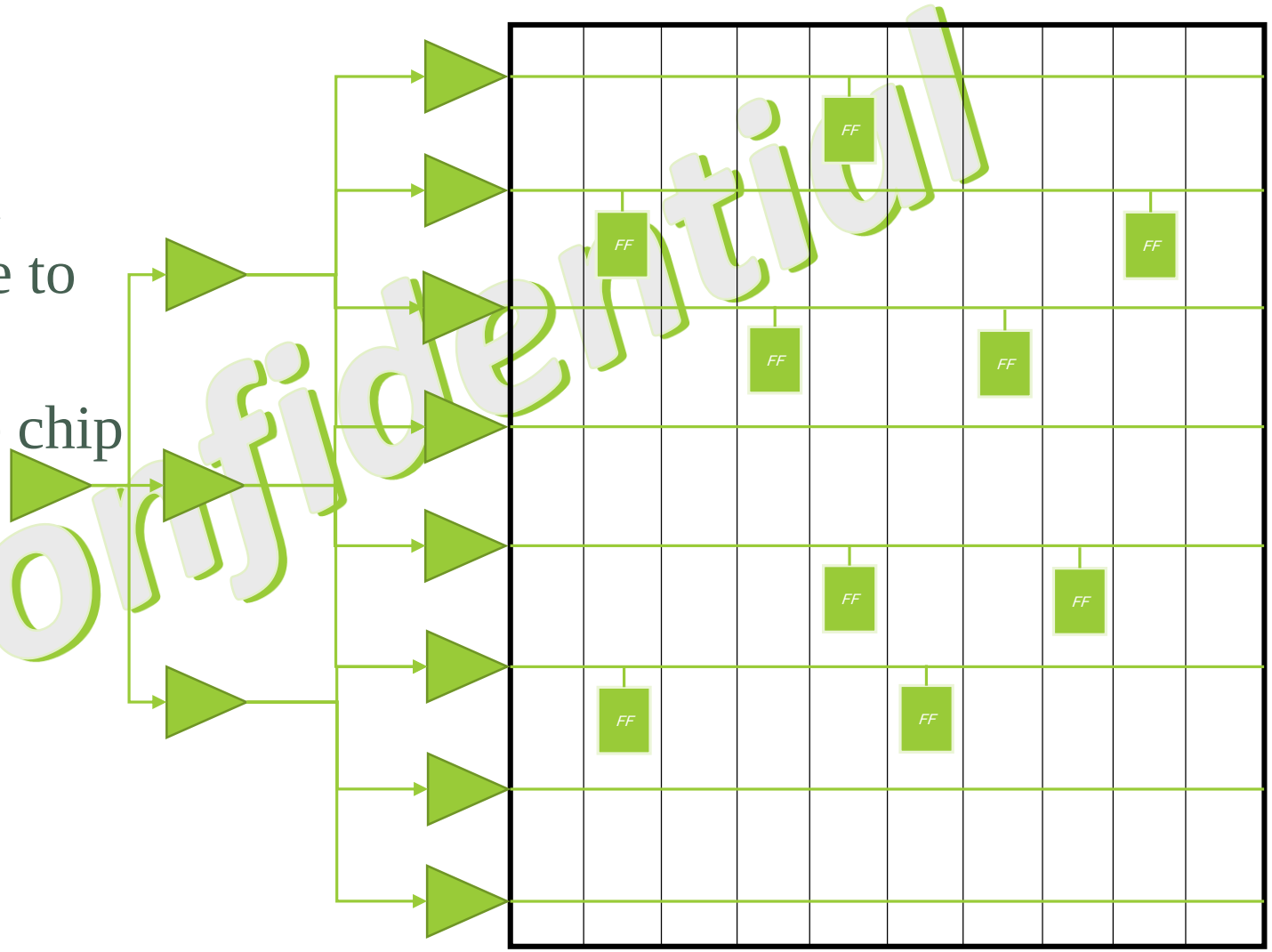
- Advantages
  - The skew in this type of tree is lower
  - Power consumption is tolerable
- Disadvantages
  - Very low floorplan flexibility



H-Tree

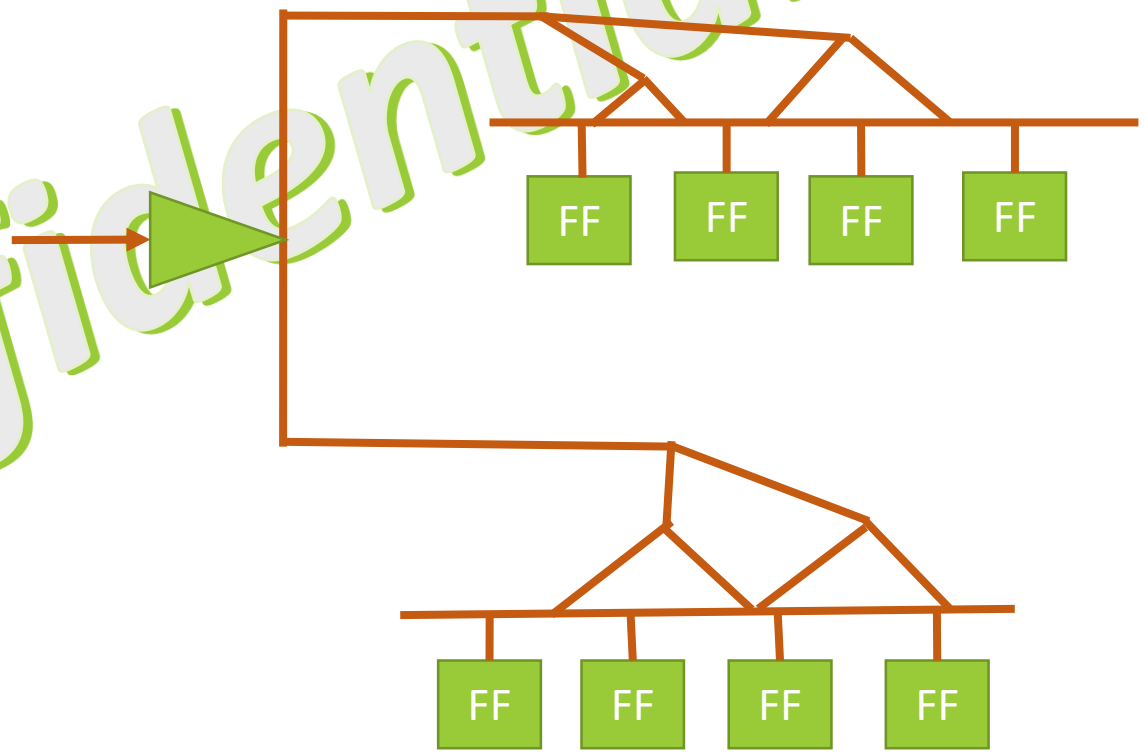
Grid

- Advantages
  - Skew is determined by the grid density and not overly sensitive to load position
  - Signals are available across the chip
  - Extreme low skew values
- Disadvantages
  - Power hungry
    - Large wire cap
    - Large routing area



Spine Tree

- Advantages
  - Small RC delay
  - Floorplan flexibility higher than H-Tree, But lower than Mesh Tree
  - Consumes less power as compared to Mesh Tree/Grid
- Disadvantages
  - Difficult to balance delays, high skew



A Quick Comparison

Structure	Skew	Cap/area/power	Floorplan Flexibility
H-Tree	Low /medium	Low	Low
Grid	Low	High	High
Spine	High	Medium	Medium

LAB PRACTICE