

CHISEL Labs

LAB NO:	01	TOPIC:	Introduction to Scala and Chisel	↓
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Lab 01: Introduction to Scala and Chisel

Objective:

This laboratory session introduces Scala programming and the Chisel hardware description language (HDL) embedded in Scala. The goal is to enable you to write simple Scala programs and use Chisel to design basic hardware modules. This lab has been updated for compatibility with the latest Chisel version (7.0.0 as of August 2025), including minor syntax adjustments to avoid deprecations.



Note on Setup

To run Chisel code, use [Scala Build Tool \(sbt\)](#). Create a build.sbt file with below snippet or simply clone [merledu/Scala-Chisel-Learning-Journey](#):

```
scalaVersion := "3.4.2" // Latest Scala 3 for Chisel 7 compatibility
libraryDependencies ++= Seq(
  "org.chipsalliance" %% "chisel" % "7.0.0-RC3",
  "org.chipsalliance" %% "chisel-plugin" % "7.0.0-RC3" cross CrossVersion.full
)
```

Compile and run with `sbt run`

1.1 Introduction to Scala

Scala is a high-level language combining object-oriented and functional programming paradigms. Scala source code compiles to Java bytecode and runs on the Java Virtual Machine (JVM). It is interoperable with Java. We start with primitive data types, followed by object-oriented programming concepts like classes and objects.

1.1.1 Scala Data Types

n Scala, all values have an associated data type, including numbers and functions. Data types (Table 1.1) are objects. Objects can be immutable (**val**) or mutable (**var**). Use **val** for hardware in Chisel to ensure constancy after elaboration; **var** for tests or variables.

Table 1.1: Scala data types.

Data Type	Description
Byte	8-bit signed two's complement integer
Short	16-bit signed two's complement integer
Int	32-bit signed two's complement integer
Long	64-bit signed two's complement integer
BigInt	Arbitrary-precision signed integer
Char	16-bit unsigned Unicode character
String	A sequence of chars
Float	32-bit single-precision float
Double	64-bit double-precision float
Boolean	true or false

Data types follow a hierarchy (Figure 1.1). **Any** is the supertype, with subclasses **AnyVal** (value types) and **AnyRef** (reference types).

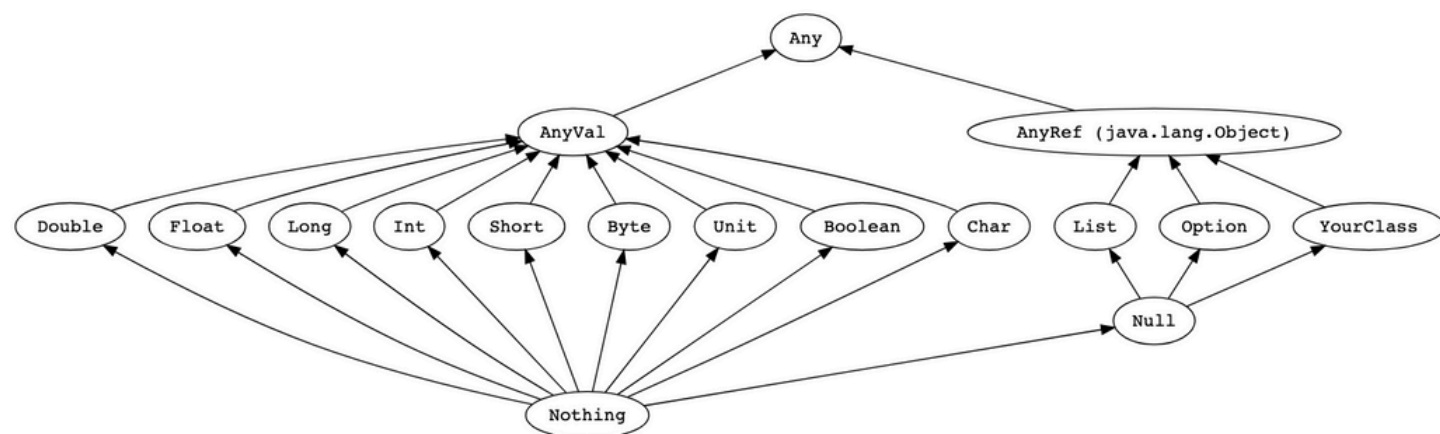


Figure 1.1: Subset of Scala data types hierarchy. (Source: <https://docs.scala-lang.org/tour/unified-types.html>)

1.1.2 Scala Classes and Objects

Classes are defined with class keyword. Example: A simple counter class (Codeblock 1.1). Objects are instances; singleton objects use object.

```
Counter.scala

1 class Counter(counterBits: Int) {
2   val max = (1 << counterBits) - 1
3   var count = 0
4
5   def increment(): Unit = {
6     if (count == max) {
7       count = 0
8     } else {
9       count = count + 1
10    }
11  }
12  println(s"Counter created with max value $max")
13 }
```

Codeblock 1.1: Scala class description.

1.1.3 Scala Type Casting

Use `asInstanceOf[T]` for casting. Numeric example (Codeblock 1.2); object casting (Codeblock 1.3) allows upcasting (child to parent) but not downcasting without checks.

```
TypeCasting.scala

1 val f: Float = 34.6F
2 val c: Char = 'c'
3
4 val ccast = c.asInstanceOf[Int]
5 val fcast = f.asInstanceOf[Int]
6
7 def display[A](label: String, value: A): Unit = {
8   println(s"$label = $value is of type ${value.getClass}")
9 }
10
11 display("Char", c)
12 display("Char to Int", ccast)
13 display("Float", f)
14 display("Float to Int", fcast)
```

Codeblock 1.2: Scala numeric type cast.

```

TypeCasting.scala

1 class Parent {
2     val countP = 10
3     def display(): Unit = {
4         println("Parent counter: " + countP)
5     }
6 }
7
8 class Child extends Parent {
9     val countC = 12
10    def displayC(): Unit = {
11        println("Child counter: " + countC)
12    }
13 }
14
15 object Top {
16     def main(args: Array[String]): Unit = {
17         val pObject = new Parent()
18         val cObject = new Child()
19         val castedObject = cObject.asInstanceOf[Parent]
20
21         pObject.display()
22         cObject.display()
23         cObject.displayC()
24         castedObject.display()
25     }
26 }

```

Codeblock 1.3: Scala object type cast.

1.2 Introduction to Chisel

Chisel (Constructing Hardware in a Scala Embedded Language) is a DSL in Scala for hardware design. A Chisel program elaborates to FIRRTL, which compiles to Verilog. Updated for Chisel 7: Avoid deprecated `.asTypeOf` by using `Wire(...)` or `Reg(...)` directly.

1.2.1 Chisel Datatypes

Chisel types for hardware: `UInt` (unsigned), `SInt` (signed), `Bool`. Use literals like `23.U`, `-45.S`. Widths inferred or specified (e.g., `8.W`).

```

ChiselLiterals.scala

1 // Literals
2 val x1 = 23.S(32.W) // Signed 32-bit
3 val y1 = 23.U.asSInt // UInt to SInt

```

Codeblock 1.4: Defining literals in Chisel.

```

SignalDefinitions.scala

1 // Signals
2 val s1 = WireInit(Bool(), true.B) // Initialized Bool
3 val s2 = Wire(Bool())             // Uninitialized
4
5 val x1 = WireInit(-45.S(8.W))      // Initialized SInt
6 val y1 = WireInit(102.U(8.W))     // Initialized UInt
7 val z1 = Wire(Bits(16.W))         // Uninitialized Bits

```

Codeblock 1.5: Signal definitions

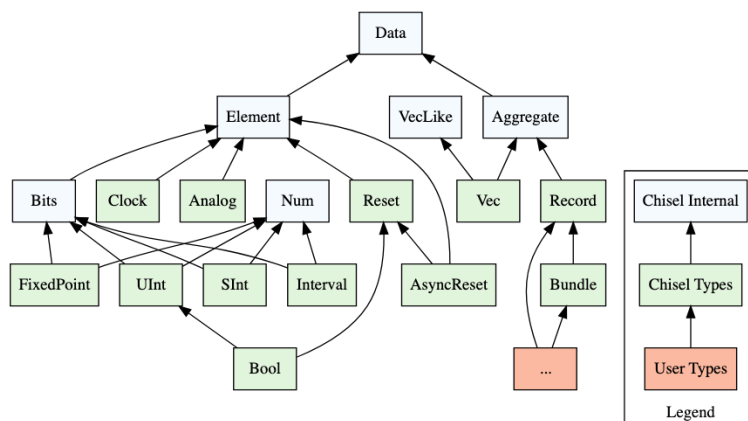


Figure 1.2: Chisel base data types hierarchy.

1.2.2 Counter Class Revisited

Chisel counter module (Codeblock 1.6 partial, 1.7 complete). Extends **Module**; mandatory **io** Bundle.

```

CounterRevisited.scala

1 import chisel3._
2
3 class Counter(counterBits: UInt) extends Module {
4   val max = (1.U << counterBits) - 1.U
5   val count = RegInit(0.U(16.W))
6
7   when(count === max) {
8     count := 0.U
9   }.otherwise {
10    count := count + 1.U
11  }
12  println(s"Counter created with max value $max")
13 }

```

Codeblock 1.6: Chisel counter partial (elaboration-time print).

```

1 import chisel3._
2
3 class Counter(counterBits: UInt) extends Module {
4   val io = IO(new Bundle {
5     val result = Output(Bool())
6   })
7
8   val max = (1.U << counterBits) - 1.U
9   val count = RegInit(0.U(16.W))
10
11   when(count === max) {
12     count := 0.U
13   }.otherwise {
14     count := count + 1.U
15   }
16   io.result := count(15)
17   println(s"Counter created with max value $max")
18 }

```

Codeblock 1.7: Chisel counter complete implementation.

To generate Verilog: Use `chisel3.stage.ChiselStage.emitVerilog(new Counter(8.U))`

1.3 Optimization of Signals and Parametrized Hardware Generation

Chisel optimizes during elaboration. Example: Constant folding (Codeblock 1.8).

```

1 import chisel3._
2
3 class AdderWithOffset extends Module {
4   val io = IO(new Bundle {
5     val x = Input(SInt(16.W))
6     val y = Input(UInt(16.W))
7     val z = Output(UInt(16.W))
8   })
9
10  val y1 = 23.U.asSInt // UInt to SInt
11  val in1 = io.x + y1
12  io.z := in1.asUInt + io.y
13 }
14
15 println(chisel3.stage.ChiselStage.emitVerilog(new AdderWithOffset))

```

Codeblock 1.8: Data optimization (generates Verilog with folded constants).

1.3.1 Parametrized Hardware Generation

Use functions for reusable logic (Codeblock 1.9).

```

1 import chisel3._
2
3 class Counter(size: Int, maxValue: UInt) extends Module {
4   val io = IO(new Bundle {
5     val result = Output(Bool())
6   })
7
8   def genCounter(n: Int, max: UInt): UInt = {
9     val count = RegInit(0.U(n.W))
10    when(count === max) {
11      count := 0.U
12    }.otherwise {
13      count := count + 1.U
14    }
15    count
16  }
17
18  val counter1 = genCounter(size, maxValue)
19  io.result := counter1(size - 1)
20 }
21
22 println(chisel3.stage.ChiselStage.emitVerilog(new Counter(8, 255.U)))

```

Codeblock 1.9: Parametrized Chisel counter.

1.4 Exercises

Exercise 1: Modify the counter in Codeblock 1.7 to use SInt for count (handle signed wrapping carefully).

Exercise 2: Reset the counter when its MSB changes from 0 to 1 (use a register to track previous MSB).

Exercise 3: Change max in Codeblock 1.9 to Int type, then cast to UInt (e.g., maxValue.asUInt).

1.5 Assignments

Task 1: Determine feasible datatype castings (update table for Chisel 7 compatibility, e.g., Bool to UInt is possible via asUInt).

Table 1.2: Different groups of hardware operations.

1 st Type	2 nd Type	Possible?	If not, why?	Languages
SInt	SInt			
SInt	UInt			
UInt	UInt			
Clock	UInt			
UInt	SInt			
Bool	UInt			
Bool	Int			
UInt	Int			
SInt	Int			
Int	SInt			
Int	UInt			

Task 2: Implement an up-down counter. Counts up to data_in, then down to 0; sets out high for one cycle at max/min. Use reload to load data_in.

```

UpDownCounter.scala

1 import chisel3._
2 import chisel3.util._
3
4 class counter_up_down(n: Int) extends Module {
5   val io = IO(new Bundle {
6     val data_in = Input(UInt(n.W))
7     val reload = Input(Bool())
8     val out = Output(Bool())
9   })
10
11   val counter = RegInit(0.U(n.W))
12   val max_count = RegInit(6.U(n.W))
13   val direction = RegInit(true.B) // true: up, false: down
14
15   // Your code: Load max on reload, count up/down, pulse out at peaks
16   io.out := false.B // Default
17
18   // Implement logic...
19 }

```


Codeblock 1.10: Skeleton code for counter implementation.

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