Tutorial Number 4

Introduction to Placement

LEARNING OUTCOMES:

At the end of this lab, participants will be able to:

1. Placement of Standard cells
2. Concept of Legalization
3. Target Density
4. Macro Placement
5. Differentiate between the config file of Core design and Macro design

Placement

- Placement is a step in the Physical Implementation process of placing the standard cell in a standard cell rows in order to meet the timing, congestion, and utilization.
- An input to the placement is floorplan database or def.
- There are two steps in placement:
    1. Global placement
    2. Detail placement

Global Placement: As a part of global placement all the standard cells will be placed in standard cell rows but there may be some overlap of standard cells.

Detail Placement: All standard cells on standard cell rows will be legalized, refined and there will not be any overlaps.

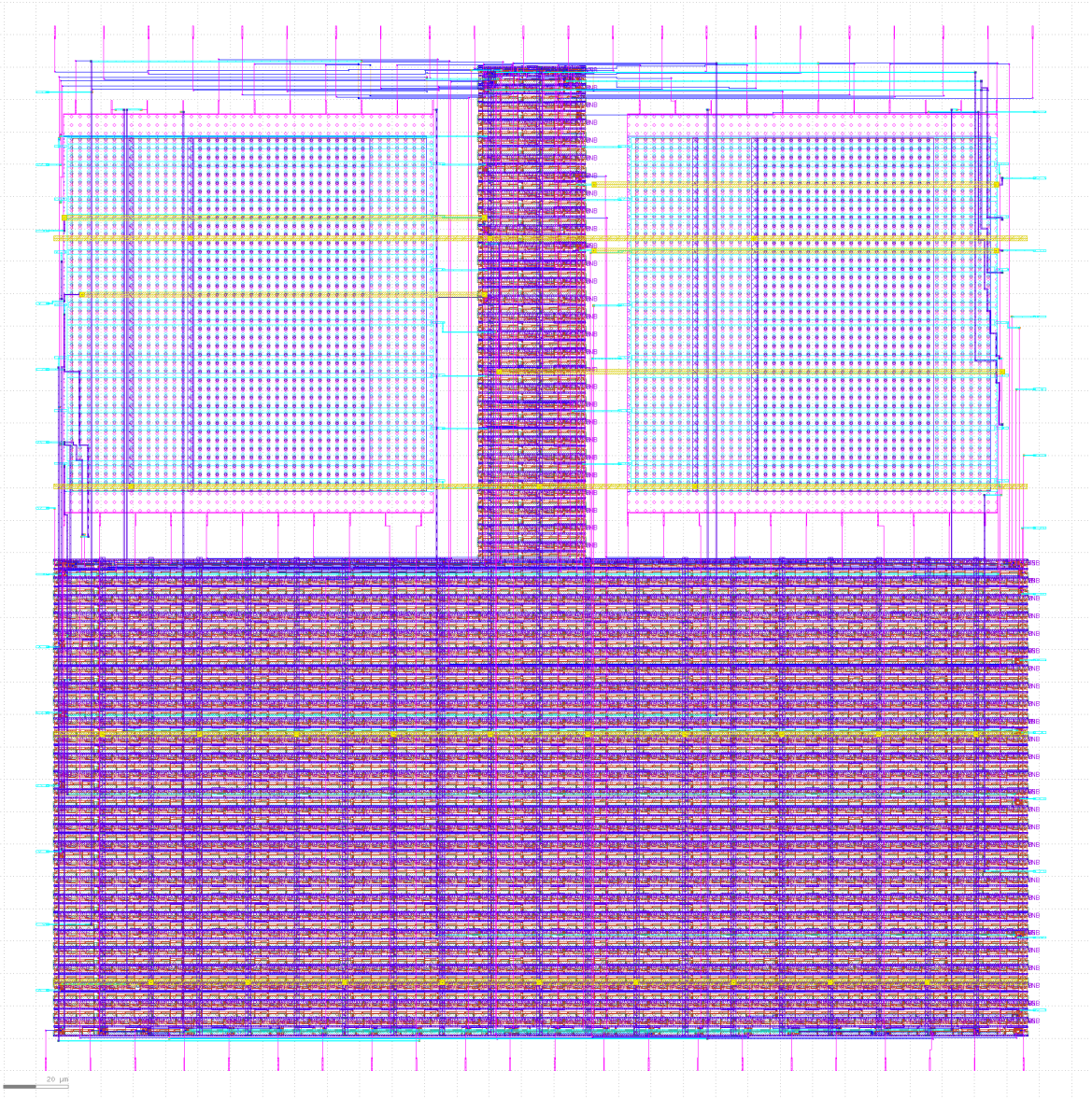
- Once the placement is done, then we have to check timing as well as congestion.
- Outputs from the placement will be netlist, def and spef.
- In the placement stage only different types of special cells are added. They are Spare cells, End cap cells, tie cells, etc.

NOTES:

Standard Cell Row Utilization: It is defined as the ratio of the area of the standard Cells to the area of the chip minus the area of the macros and area of blockages.

$$\frac{\text{Area (Standard Cells)}}{\text{Area (Chip) - Area (Macro) – Area (Region Blockages)}}$$

Congestion: If the number of routing tracks available for routing is less than the required tracks then it is known as congestion.



Variable to be added for macro placement in config.tcl

set ::env(EXTRA_LEFS) <LEF file of the macro>
set ::env(EXTRA_GDS_FILES) <gds file of the macro>
set ::env(VERILOG_FILES_BLACKBOX) <rtl of the blackbox>
set ::env(MACRO_PLACEMENT_CFG) <File containing the macro coordinate information>

If your design is a core then set these variable in configuration file

set ::env(DESIGN_IS_CORE) 1
set ::env(FP_PDN_CORE_RING) 1

If your design is a macro ,it doesn't have a core ring. Also, prohibit the router from using metal 5 by setting the maximum routing layer to met4 (layer 5).Set these variable in configuration file

set ::env(DESIGN_IS_CORE) 0
set ::env(FP_PDN_CORE_RING) 0
set ::env(GLB_RT_MAXLAYER) 5

Running the flow interactively

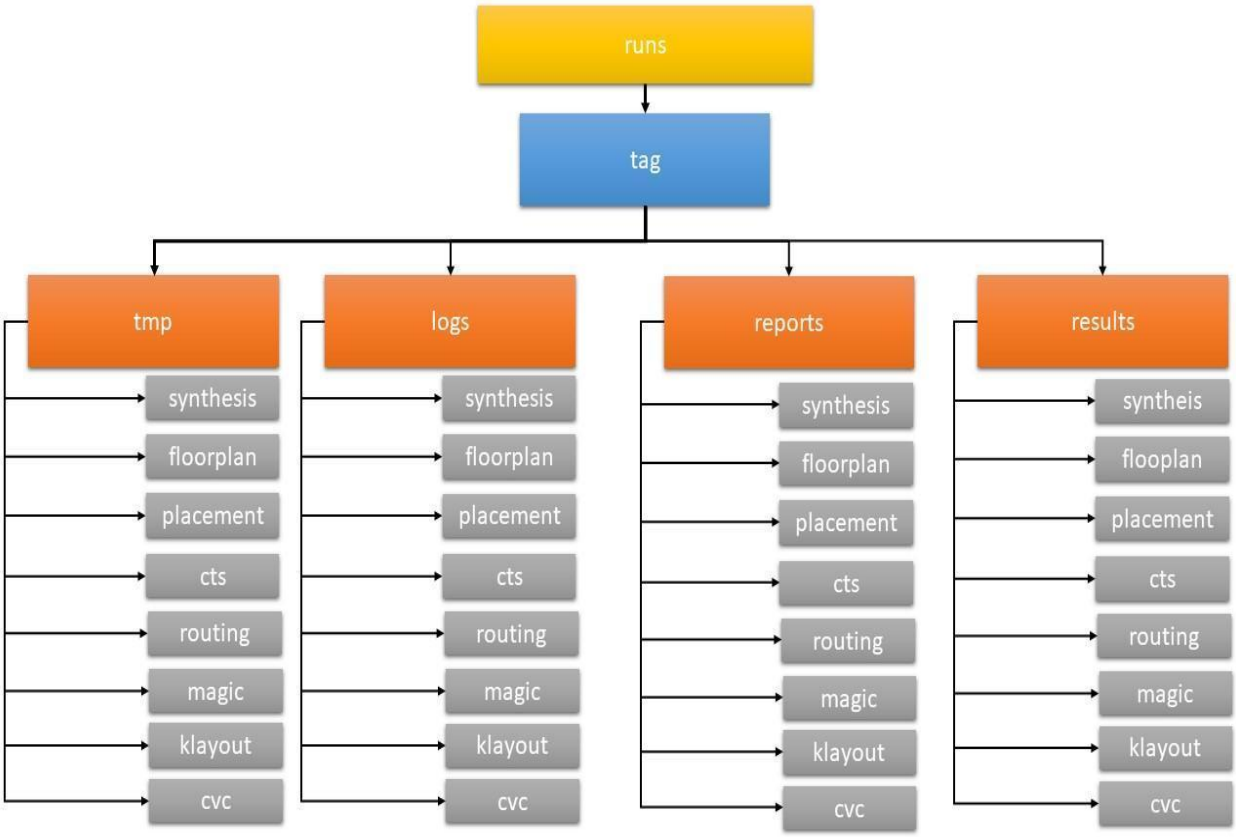
Go to the working directory by:

cd $OPENLANE_ROOT

- ./flow.tcl –interactive
- Prep –design spm -tag run1
- Run_synthesis
- Run_floorplan
- run_placement

Using Klayout to look at the layout

Go to the directory containing the DEF file. It is in the **runs** directory of your design



- Klayout design_name.def

Tasks

1. Place the macros at any 2 corners
2. Try to find the difference between the 2 DEF files, floorplan.def and placement.def.

USEFUL REPO FOR MACRO PLACEMENT

https://github.com/merledu/OpenLane_Workshop/tree/main/manual_macro_placement_test