Tutorial Number 3

Introduction to FloorPlan

LEARNING OUTCOMES:

At the end of this lab, participants will be able to:

1. Initialization of Floorplan
2. I/O pin placement
3. Concept of power distribution network
4. Concept of ring,strap and rails
5. tap and decap cell insertion

Floorplan

Floorplanning is the art of any physical design. A well and perfect floorplan leads to an ASIC design with higher performance and optimum area.

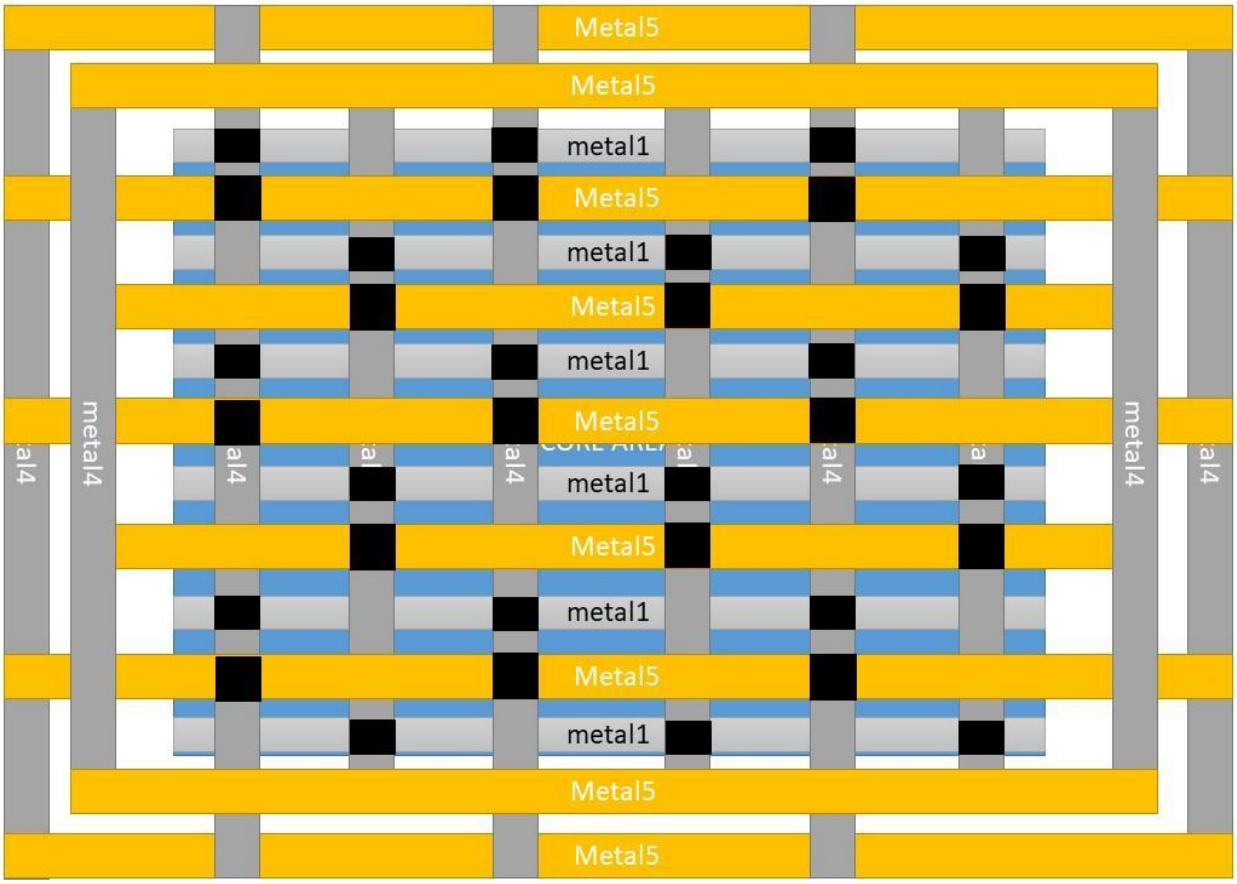
Floorplanning can be challenging in that it deals with the placement of I/O pads and macros as well as power and ground structure.

Running the flow interactively

Go to the working directory by:

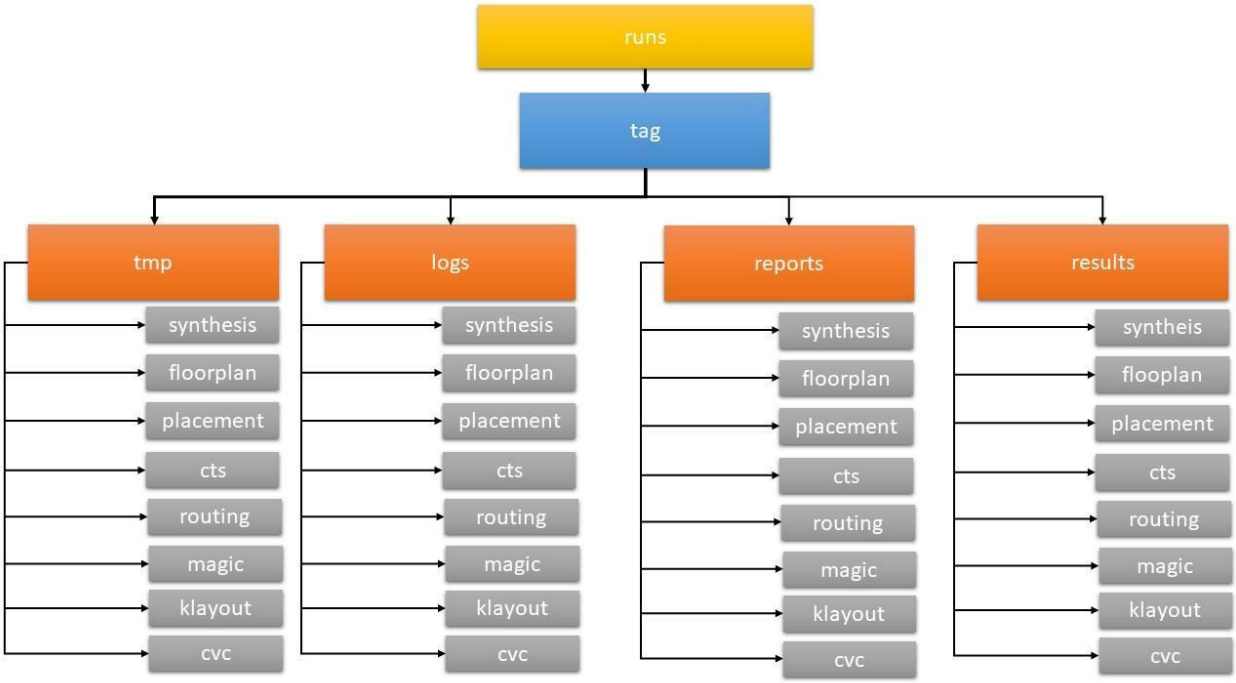
cd $OPENLANE_ROOT

- ./flow.tcl –interactive
- Prep –design <design_name>
- Run_synthesis
- Run_floorplan



Using Klayout to look at the layout

Go to the directory containing the DEF file. It is in the **runs** directory of your design



- Klayout design_name.def

Tasks

1. Switch the pins, i.e. left to the right, top to the bottom and vice versa
2. Generate a layout without the power ring
    a. HINT [Refer to configuration/floorplan.tcl]
3. Generate the layout with 5 vertical straps and 9 horizontal straps
    a. HINT#1 [Play with pitch and offset]
    b. HINT#2 [Refer to configuration/floorplan.tcl]