Processor Meeting 1

→ Type: Load-Store w/ memtomem $ Accumulator

→ Features:

- general computations
  - arithmetic, branch, load/store, jump, loop, logic
- 2 FPGA board
- reg-mem communication
- procedure calls
  - parameterized
  - nested
- 2 Interrupts from 2 devices
- reading from input port at least 4 bits
- 16-bit memory address bus
- 16-bit memory data bus
- Mechanism for basic input
- Mechanism for basic output
- 2 ✱ Assembler, compiler, $ linker or loader
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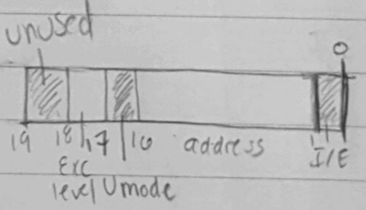
→ Registers:

- Cause



  - I/E — 0 interrupt ; 1 Exception
  - address — where error occurred
  - Umode — 0 reguser ; 1 super user
  - Exclevel — 0 notin except. ; 1 in exception
- Arithmetic Result
  - readonly — takes immediate result of any arithmetic
- Jump return address
- 2 argument (memory address)
- 1 result register
- 7 general purpose
- display

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Instructions

- load address into register
- iteration (branch, jump)
- conditional
- reading data from the input port
- reading from / writing to display register
- writing to output port
- arithmetic

A-type

Arithmetic type (add, sub, logical)

op	r1	r2	func
4	4	4	4

AI-type

op	r1	imm	func	x
4	4	16	4	4

branch (ber, bnr)

op	imm	func
4	16	4

* varying inst. sizes for small programs & lack of empty space

jump, load address, jump reg

op	r1	addr
4	4	16

load / store

op	r1
4	4

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→ Procedure Call conventions

- Argument registers only contain memory addresses
  - more convenient to have access to the access without access
  - we realize it is slow to grab data initially, but we feel it will benefit our design in the long run
- One return value register will also contain memory address of return value
- backup return address register before proc. call $ restore it before jumping to return address (like MIPS)
- backup any used registers at beginning of call on stack and restore before return.

TOMORROW

- Register Descriptions $ Names
- Mach. Lang. semantics description
- Syntax $ semantics of inst.
- Rules for translating assembly to machine language
  - ✗ addressing modes