ELECTRICAL AND ELECTRONICS ENGINEERING
&
COMPUTER ENGINEERING

EEE 248 | CNG 232
Logic Design

21 | SPRING | 22

HW II
Number of Questions: 4

Due: May 09, 2022
Good Luck

Dr. Gürtaç Yemişcioğlu

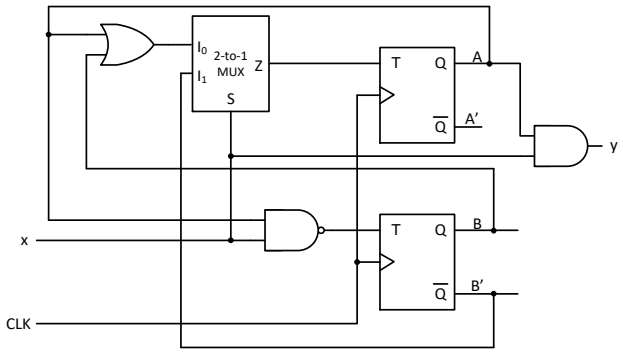
Student Number:

Full Name:

Question	Achieved	Points
1		16
2		20
3		20
4		28
5		16
TOTAL		100

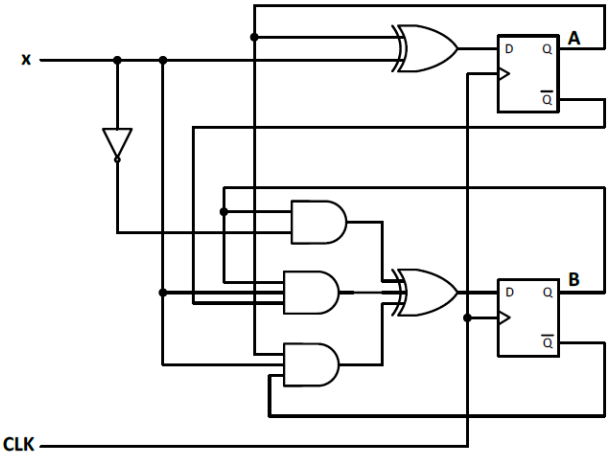
Question 1 (16 pts.): Design a combinational circuit that converts a 4-bit gray code to a 4-bit binary number. Implement the circuit using exclusive-OR gates.

Question 2 (20 pts.): Sequential circuit shown below has two flip-flops A and B and one input x. It consists of a combinatorial logic connected to the flip-flops, as shown in Figure below. Analyse the circuit:



a. (6 pts) Derive the next state equations.
b. (6 pts) Derive the state table of the sequential circuit.
c. (6 pts) Draw the corresponding state diagram.
d. (2 pts) Is this a Mealy or Moore model? Explain.

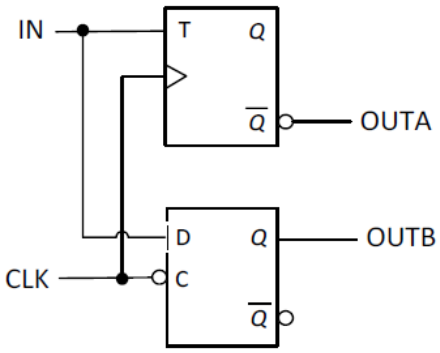
Question 3 (20 pts.): Mod-4 counter is a sequential circuit that has two flip-flops A and B and one input x. It consists of a combinatorial logic connected to the D flip-flops, as shown in Figure below. Analyze the circuit:

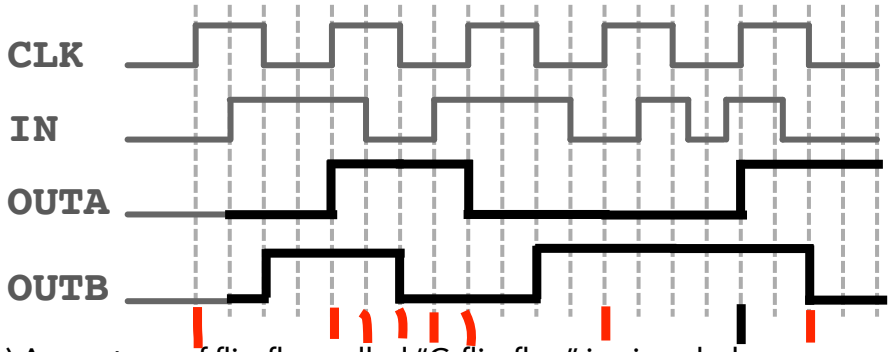


a. (8 pts.) Derive the next state and output equations.
b. (8 pts.) Derive the state table of the sequential circuit.
c. (4 pts.) Draw the corresponding state diagram.

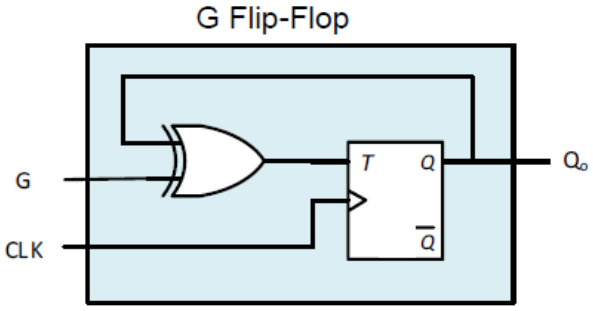
Question 4 (14 pts.):

a. (14 pts.) Given the sequential logic circuit below, complete the timing waveforms for the outputs, assuming the storage elements have zero propagation delays. Initial values of OUTA and OUTB are both logic '0' as shown.





b. (14 pts.) A new type of flip-flop called "G-flip-flop" is given below:



i. (8 pts.) Find the simplified characteristic equation of this G-flip-flop.

ii. (6 pts.) Fill in the following excitation table for G flip-flop.

Question 5 (16 pts.): Use rising edge triggered D-type Flip-Flops and any number and type of combinational gates and building blocks, in order to design a 4-bit universal shift register, for which a specification is provided below. Show the schematic of your design CLEARLY with inputs CLK, CLEAR_B, S1, S0, LEFT_IN, RIGHT_IN, D[3:0], and outputs Q[3:0].

Control S[1:0]	Operation	Example to demonstrate the Next State when the Present State of the universal shift Register is 0110
00	Shift Left	1100
01	Load New Data D[3:0]	D[3:0] – 4 bit input
10	Hold	0110
11	Shift Right	0011