ELECTRICAL AND ELECTRONICS ENGINEERING
&
COMPUTER ENGINEERING

EEE 248 | CNG 232
Logic Design

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HW III
Number of Questions: 4

Due: June 10, 2022
Good Luck

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Question	Achieved	Points
1		30
2		30
3		20
4		24
TOTAL		104

Question 1 (30 pts.): Design a synchronous sequential circuit for detecting specific events. Circuit detects when there are at least two zeroes following after each other "..00.." or at least two ones "..11.." in the sequence of synchronous bits entering the input x. The circuit starts with x = 0 which means that one zero has entered the input. Detector output z should be '1' in the clock interval directly after the sequences has occurred. The sequence circuit is a Moore machine with positive edge triggered JK-flip-flops.

Sample pattern:

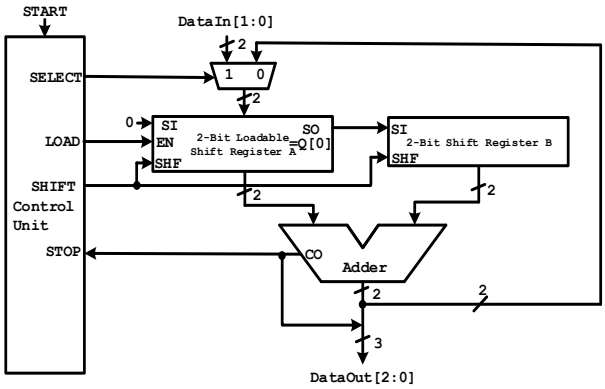
x : 0 1 0 1 0 1 1 0 1 0 1 0 0 0 1 0 1 0
z : 0 0 0 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0

a. (6 pts.) Draw the state diagram of the detector.
b. (10 pts.) Use the binary code to encode the states and set up the encoded state table.
c. (8 pts.) Obtain the minimized expressions for the inputs of the flip-flops and the output functions.
d. (6 pts.) Sketch a schematic of your design.

Question 2 (30 pts.): The vending machine dispenses a drink when a customer has inserted exactly 50 pence. A transaction is cancelled and coins returned to the customer if more than 50 pence is inserted or the reject button (R) is pressed. The vending machine accepts 10, 20 and 50 pence coins. Only one type of drink is available. The only acceptable inputs for the FSM are 10, 20, 50 and R.

a. (10 pts.) Sketch a complete state diagram for the operation of the FSM.
b. (10 pts.) Derive the state table and FF inputs.
c. (6 pts.) Sketch a logic implementation of the FSM.
d. (4 pts.) There are different ways that a customer can provide exactly three inputs that will result in the vending machine dispensing a drink. Three possible permutations are "20, 10, 20", "10, R, 50" and "10, 50, 50". List four other possible permutations of exactly three inputs that will be accepted by the FSM designed in a.

Question 3 (20 pts.): The component AC specifications below apply to the datapath given below. Assume routing delays are negligible, and the paths that include the interface data and control signals have no timing marginality. Show all details of your analysis in answering the below questions for full credit.



Component AC Timing Specifications (all values in ps)

Synchronous	$t_{p\text{-}min}$	$t_{p\text{-}max}$	t_{su}	t_{ho}
Register A Parallel Load	70	120	60	30
Register A and B Shift	50	100	20	10

Comb.	$t_{p\text{-}min}$	$t_{p\text{-}max}$
Adder	220	340
4-to-1 MUX	20	30

a. (10 pts.) What is the maximum possible clock frequency, f_{max}, that ensures correct data transfer among the datapath registers in this circuit?
b. (10 pts.) What is the worst case hold-timing slack in the circuit?

Question 4 (24 PTS.): The asynchronous toggle circuit has a single input 'a' and two outputs 'x' and 'y'. Whenever a is low, both outputs are low. The first time a goes high, output x goes high. On the next rising transition of a, output y goes high. On the third rising input, x goes high again. The circuit continues steering pulses on in alternately between x and y.

a. (4 pts.) Derive the input/output waveform based on the description given above.
b. (4 pts.) Provide a primitive flow table for this machine, and reduce the flow table to minimum number of states, if your table is not reduced already.
c. (4 pts.) Identify state assignments without critical races, and draw the transition table together with an output table that avoids false outputs.
d. (4 pts.) Derive a logic schematic without hazards for the toggle circuit using primitive (AND, OR, inverter) gates.
e. (8 pts.) Design the toggle circuit using one or more SR latches. Show the details of your work for full credit.