CS 223

Section – 6

Project

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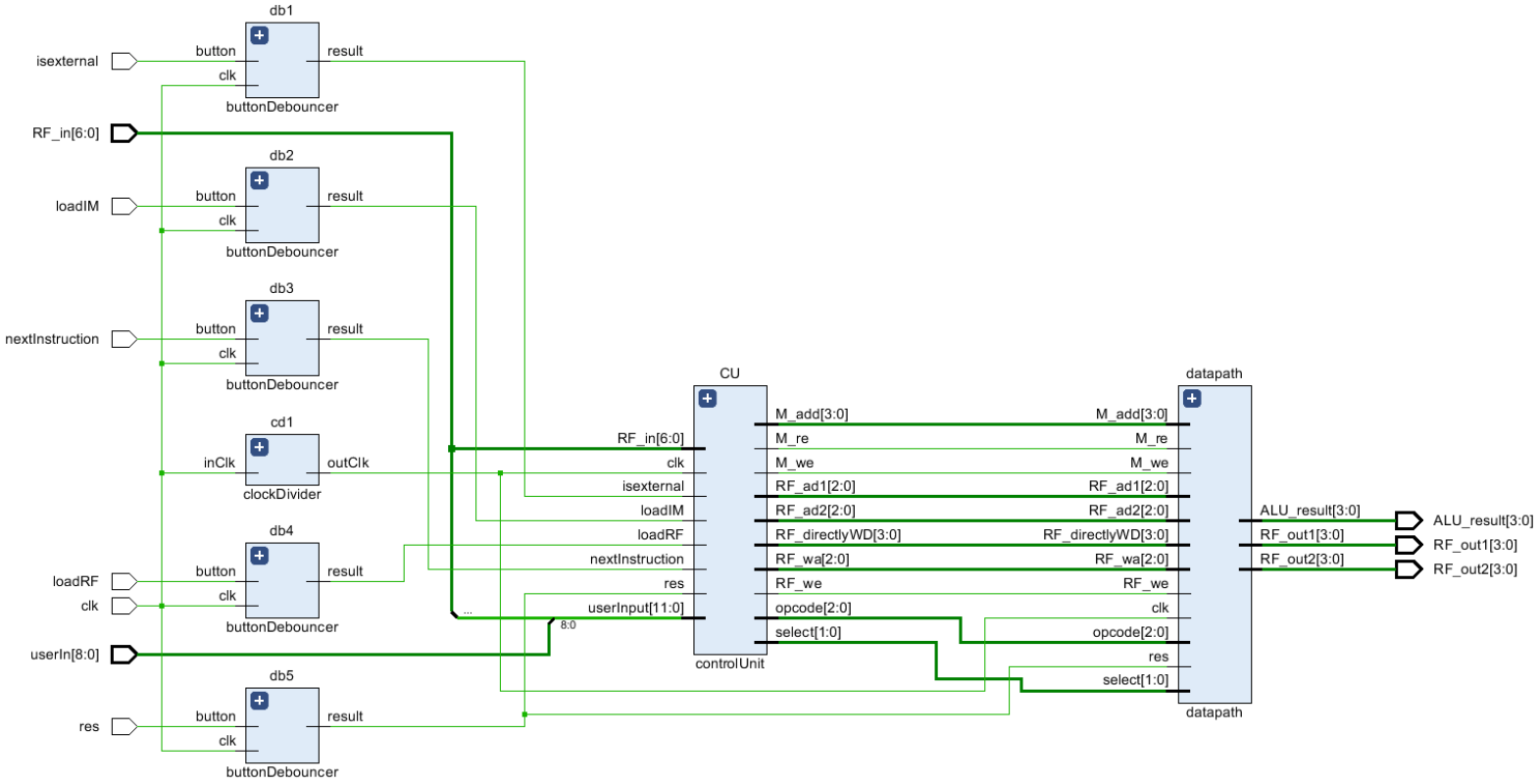
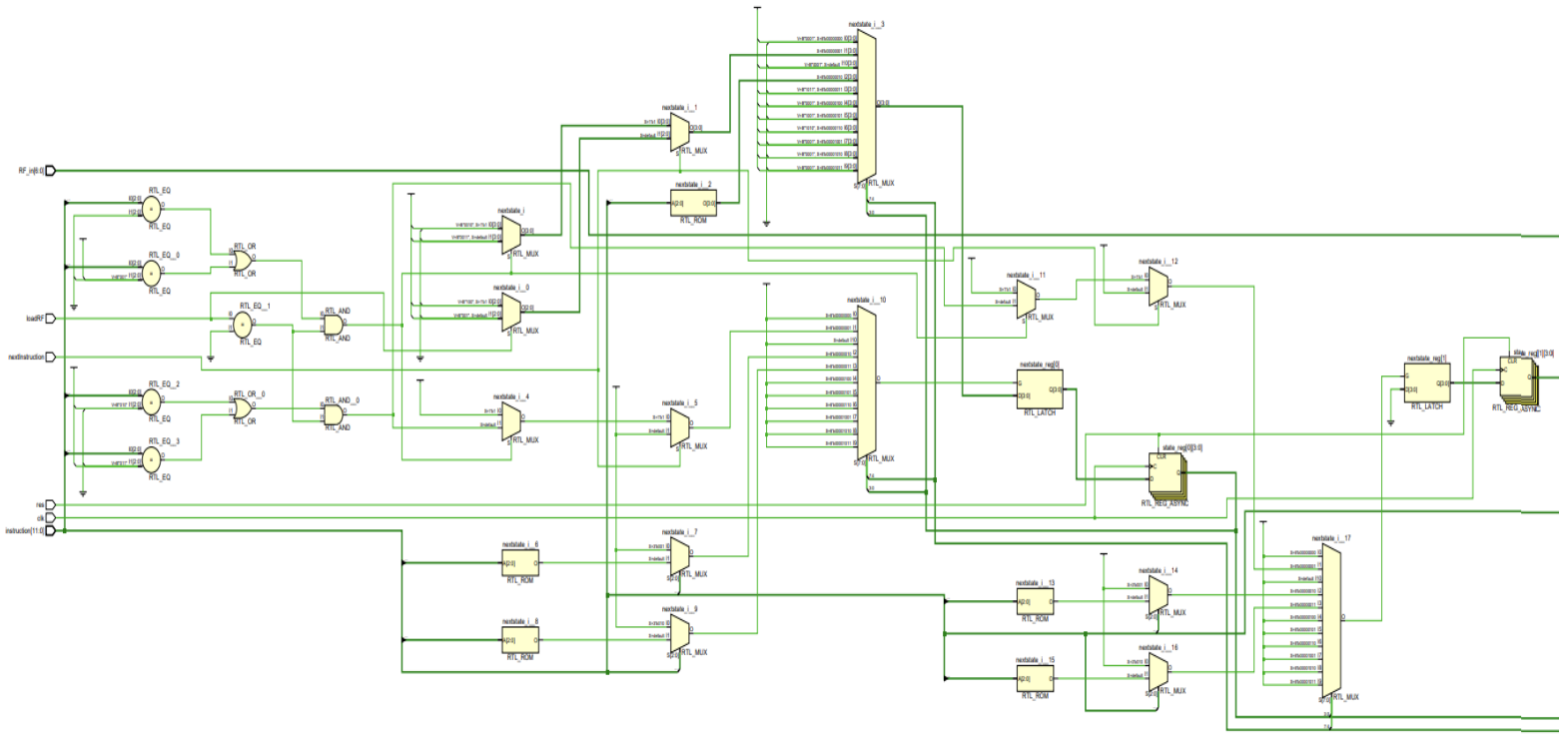
- **Controller HLSM Diagram:**

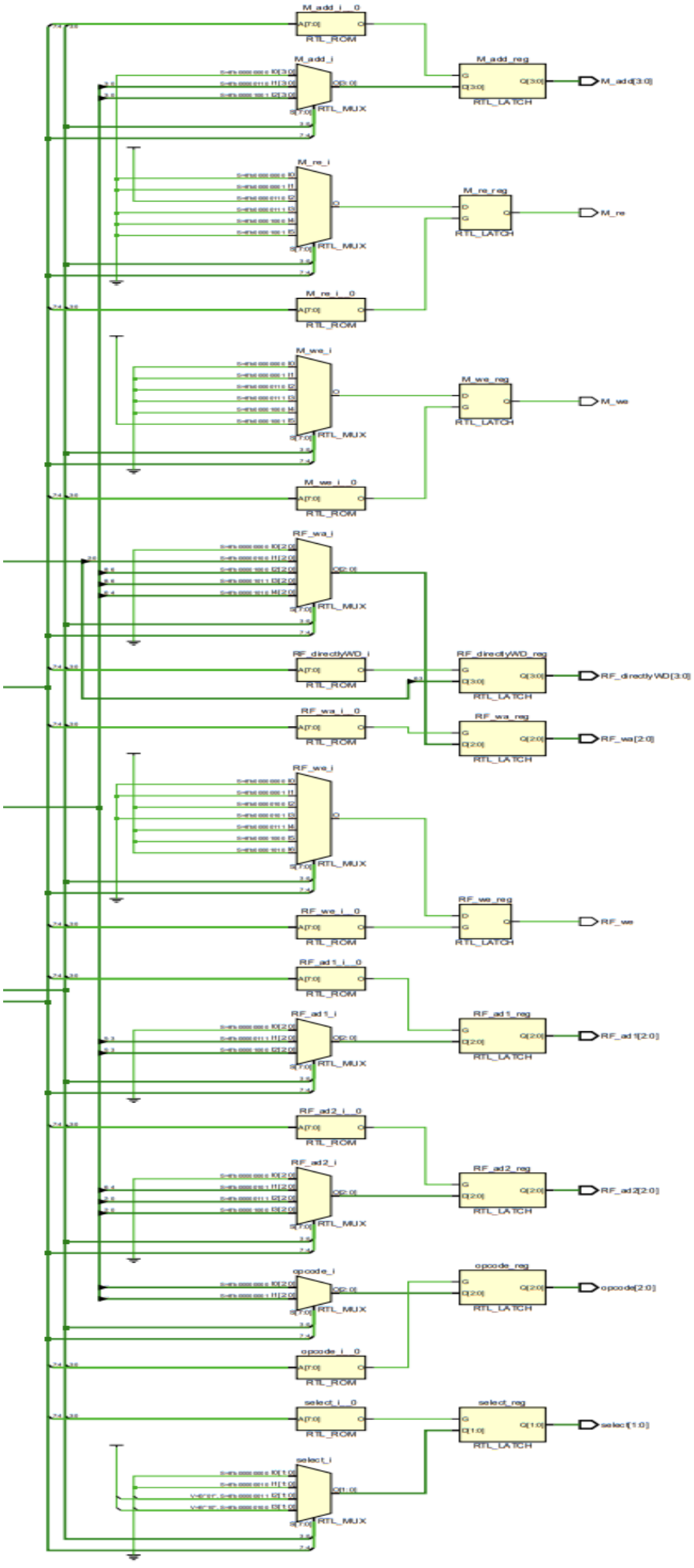


- **Controller Block Diagram:**

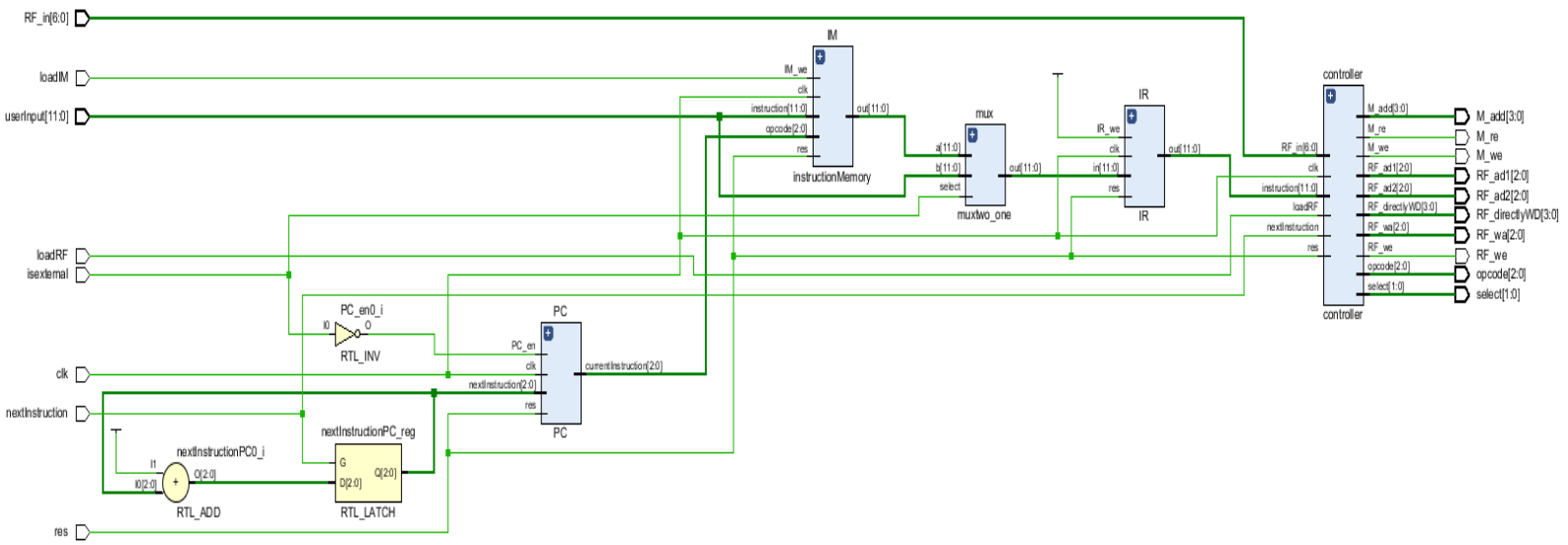
➢ **Next State Logic and State Registers:**



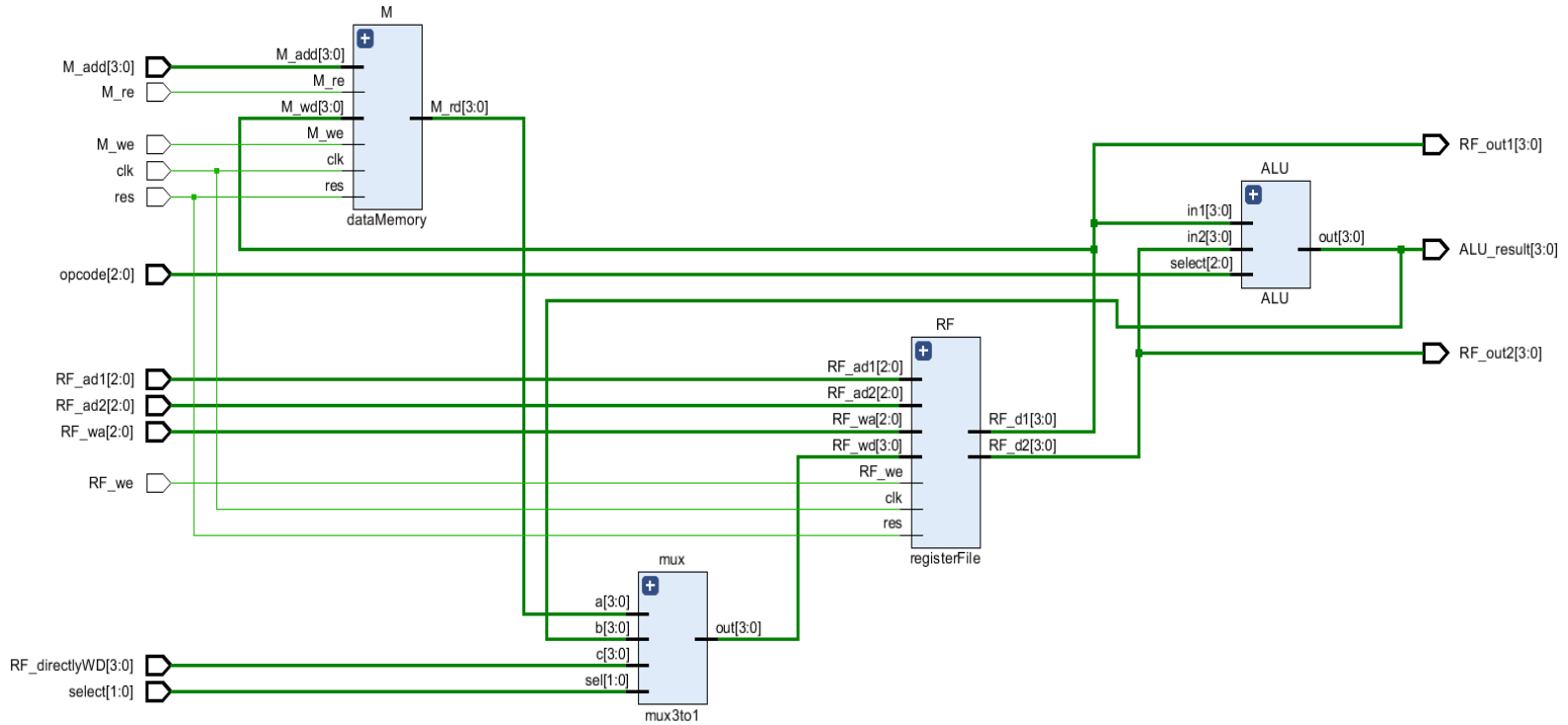
➢ Output Logic:



- **Controller Top Module Block Diagram:**



- **Datapath Top Module Block Diagram:**



- **Clock Divider and D Flip-Flop Module:**

```
module clockDivider(input logic inClk, output logic outClk);
    logic [25:0] counter = {26{1'b0}};
    always @(posedge inClk)
        begin
            counter <= counter + 1;
        end
        logic last = counter[25];
        BUFG BUFG_inst (.I(last),.O(outClk));
endmodule
```

```
module dff(input clk, D, output reg Q);
    always @(posedge clk)
        begin
            Q <= D;
        end
endmodule
```

- **Button Debouncer Module:**

```
module buttonDebouncer(input clk, button, output result);
    wire clkOut;
    wire Q1, Q2, Q2bar;
    clockDivider cd(clk, clkOut);
    dff ff1(clkOut, button, Q1);
    dff ff2(clkOut, Q1, Q2);
    assign Q2bar = ~Q2;
    assign result = Q1 & Q2bar;
endmodule
```

- **Ascending and Descending Sort RTL Schematic:**