CS 223

Section – 6

Lab – 02

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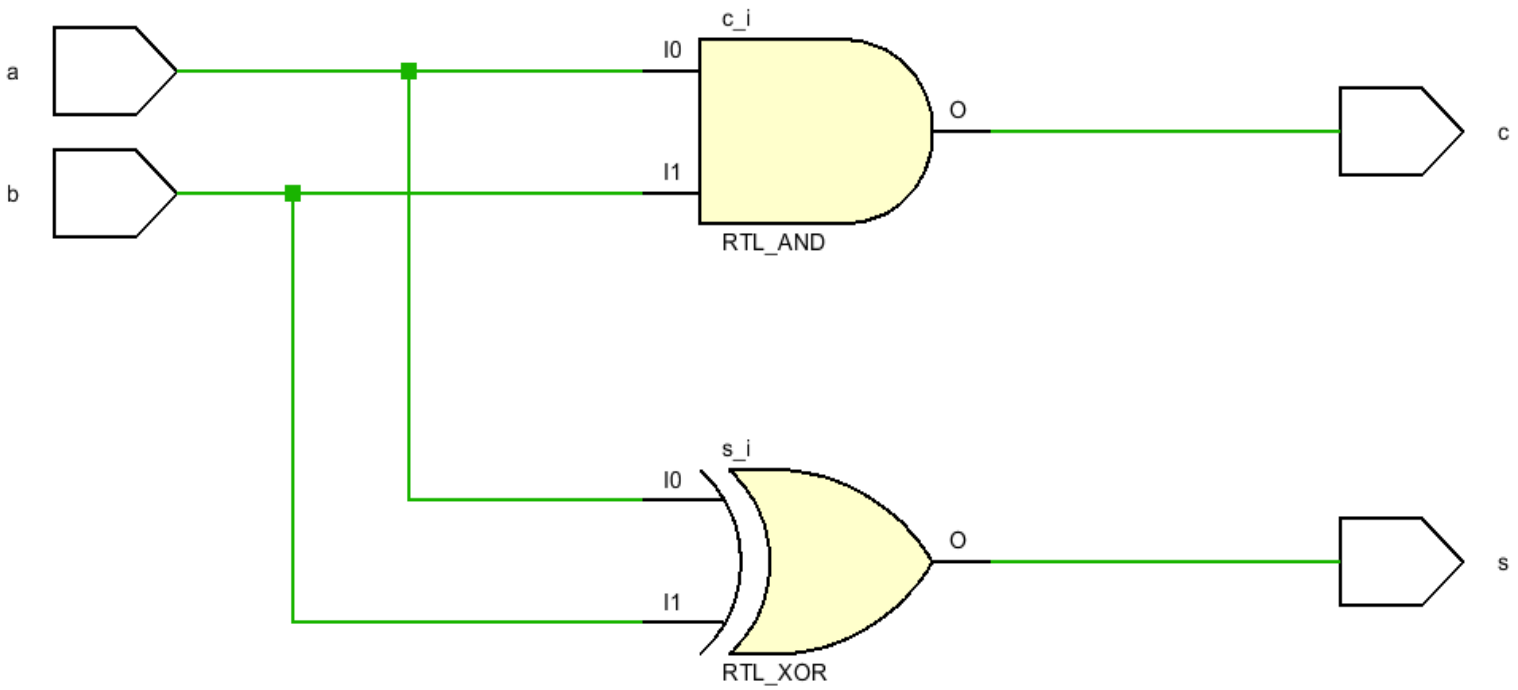
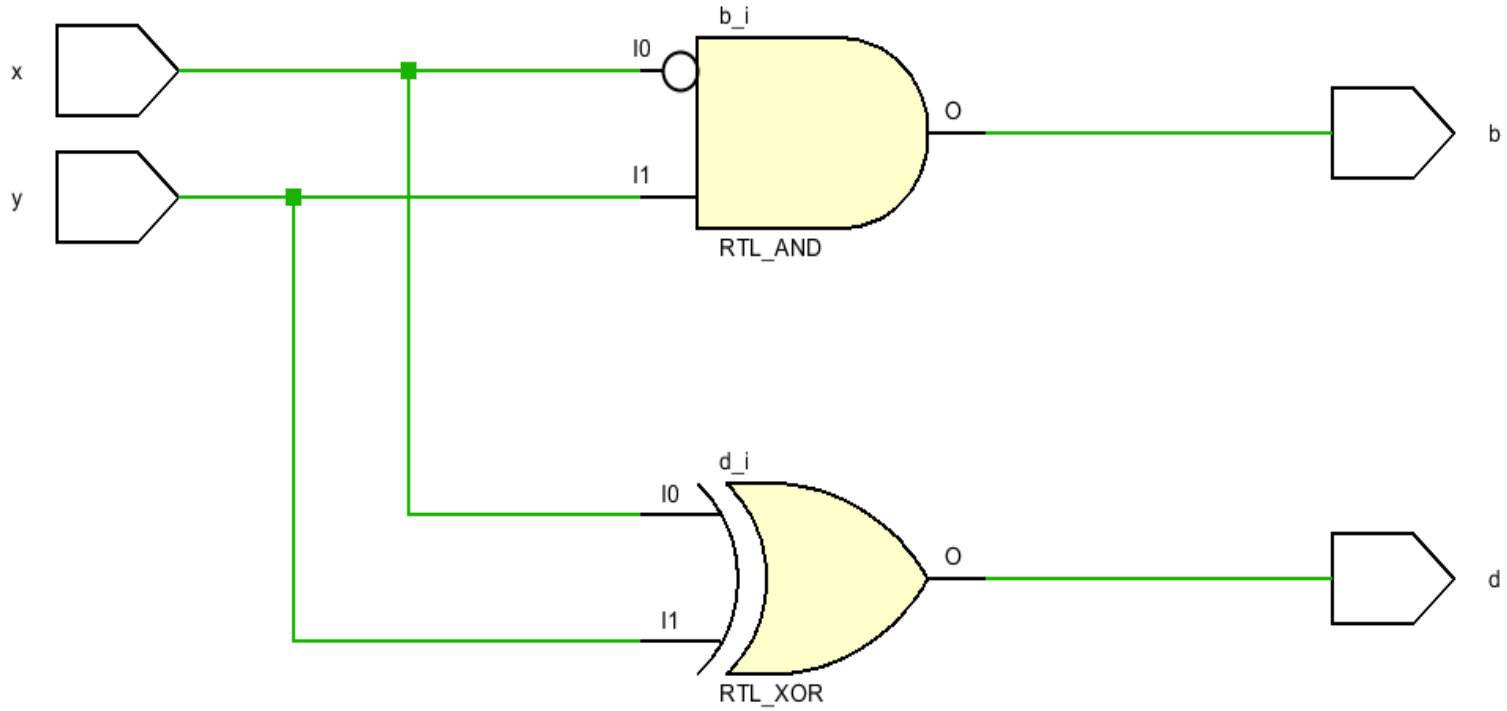
15.10.2022

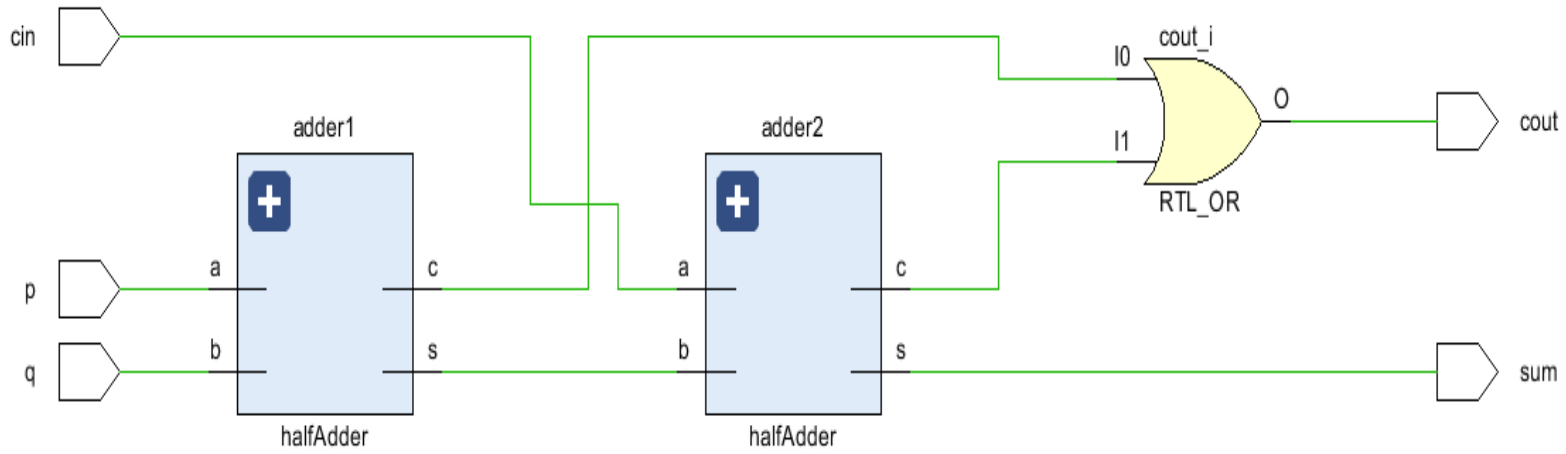
- **Half Adder Circuit Schematic:**



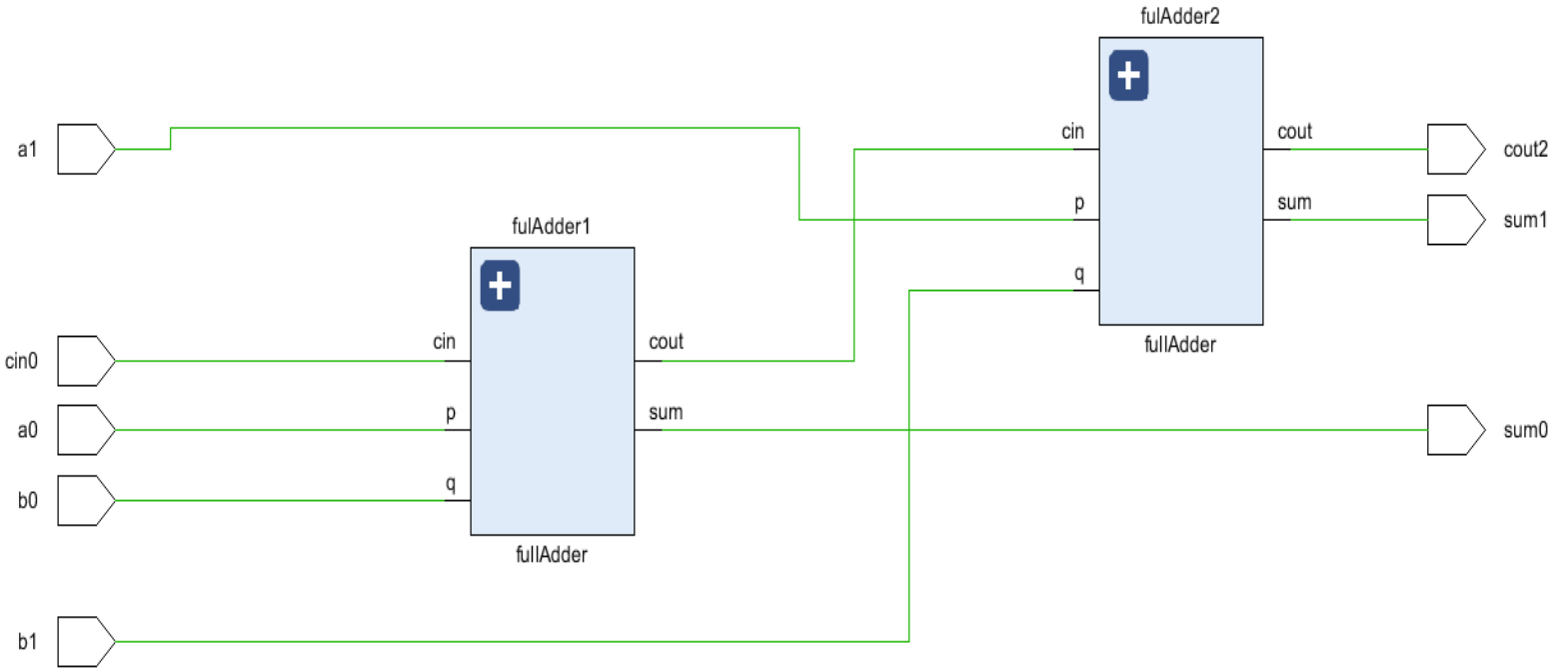
- **Half Subtractor Circuit Schematic:**



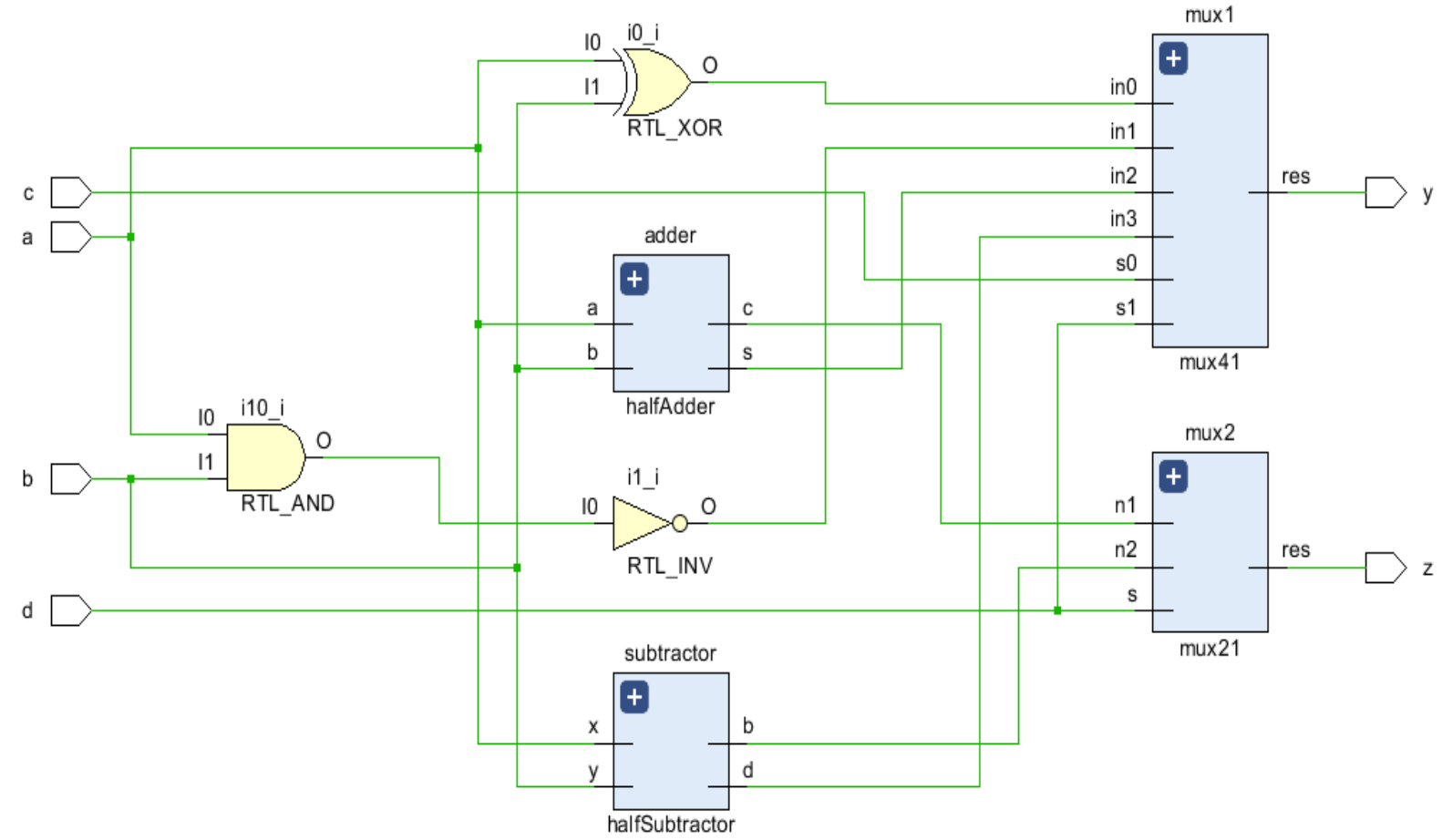
- **Full Adder Circuit Schematic:**



- **2-bit Adder Circuit Schematic:**



- **Lab Calculator Circuit Schematic:**



- **Behavioral 2:1 Multiplexer Module:**

```
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module mux21(input logic n1, n2, s, output logic res);
24      assign res = (~s & n1) + (s & n2);
25  endmodule
26
```

- **Behavioral 4:1 Multiplexer Module:**

```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company:
4   // Engineer:
5   //
6   // Create Date: 16.10.2022 16:47:44
7   // Design Name:
8   // Module Name: mux41
9   // Project Name:
10  // Target Devices:
11  // Tool Versions:
12  // Description:
13  //
14  // Dependencies:
15  //
16  // Revision:
17  // Revision 0.01 - File Created
18  // Additional Comments:
19  //
20  //////////////////////////////////////////////////////////////////////////////////
21
22
23  module mux41(input logic s0, s1, in0, in1, in2, in3, output logic res);
24      assign res = (~s0 & ~s1 & in0) + (~s0 & s1 & in1) + (s0 & ~s1 & in2) + (s0 & s1 & in3);
25  endmodule
26
```

- **Behavioral Half Adder Module:**

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 15.10.2022 16:43:57
// Design Name:
// Module Name: halfAdder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module halfAdder(input logic a, b, output logic s, c);
    assign s = a ^ b;
    assign c = a & b;
endmodule

```

- **Half Adder Testbench:**

```
//
// Create Date: 15.10.2022 17:02:10
// Design Name:
// Module Name: testbench1
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module testbench1();
    logic a, b, s, c;
    halfAdder(a, b, s, c);
    initial begin
        a = 0; b = 0; #10;
        a = 0; b = 1; #10;
        a = 1; b = 0; #10;
        a = 1; b = 1; #10;
    end
endmodule

```

- **Behavioral Half Subtractor Module:**

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 15.10.2022 16:43:57
// Design Name:
// Module Name: halfSubtractor
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module halfSubtractor(input logic x, y, output logic d, b);
    assign d = x ^ y;
    assign b = ~x & y;
endmodule

```

- **Half Subtractor Testbench:**

```
//
// Create Date: 15.10.2022 17:02:10
// Design Name:
// Module Name: testbench2
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module testbench2();
    logic x, y, d, b;
    halfSubtractor(x, y, d, b);
    initial begin
        x = 0; y = 0; #10;
        x = 0; y = 1; #10;
        x = 1; y = 0; #10;
        x = 1; y = 1; #10;
    end
endmodule

```

- **Structural Full Adder Module:**

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////////////////////
3  // Company:
4  // Engineer:
5  //
6  // Create Date: 15.10.2022 16:43:57
7  // Design Name:
8  // Module Name: fullAdder
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module fullAdder(input logic p, q, cin, output logic sum, cout);
24     logic sum1, cout1, cout2;
25     halfAdder adder1(p, q, sum1, cout1);
26     halfAdder adder2(cin, sum1, sum, cout2);
27     assign cout = cout1 | cout2;
28 endmodule
29
```

- **Full Adder Testbench:**

```
9  // Project Name:
10 // Target Devices:
11 // Tool Versions:
12 // Description:
13 //
14 // Dependencies:
15 //
16 // Revision:
17 // Revision 0.01 - File Created
18 // Additional Comments:
19 //
20 //////////////////////////////////////////////////////////////////////////////////
21
22
23 module testbench3();
24     logic p, q, cin, sum, cout;
25     fullAdder(p , q, cin, sum, cout);
26     initial begin
27         p = 0; q = 0; cin = 0; #10;
28         p = 0; q = 0; cin = 1; #10;
29         p = 0; q = 1; cin = 0; #10;
30         p = 0; q = 1; cin = 1; #10;
31         p = 1; q = 0; cin = 0; #10;
32         p = 1; q = 0; cin = 1; #10;
33         p = 1; q = 1; cin = 0; #10;
34         p = 1; q = 1; cin = 1; #10;
35     end
36 endmodule
37
```

- **Structural 2-bit Adder Module:**

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////////
// Company:
// Engineer:
//
// Create Date: 15.10.2022 16:43:57
// Design Name:
// Module Name: twoBitAdder
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module twoBitAdder(input logic a0, b0, a1, b1, cin0, output logic sum0, sum1, cout2);
    logic cout1;
    fullAdder fulAdder1(a0, b0, cin0, sum0, cout1);
    fullAdder fulAdder2(a1, b1, cout1, sum1, cout2);
endmodule

```

- **2-bit Adder Testbench:**

```

module testbench4();
    logic a0, b0, a1, b1, cin0, sum0, sum1, cout2;
    twoBitAdder(a0, b0, a1, b1, cin0, sum0, sum1, cout2);
    initial begin
        a0 = 0; b0 = 0; a1 = 0; b1 = 0; cin0 = 0; #10;
        a0 = 0; b0 = 0; a1 = 0; b1 = 0; cin0 = 1; #10;
        a0 = 0; b0 = 0; a1 = 0; b1 = 1; cin0 = 0; #10;
        a0 = 0; b0 = 0; a1 = 1; b1 = 0; cin0 = 0; #10;
        a0 = 0; b0 = 1; a1 = 0; b1 = 0; cin0 = 0; #10;
        a0 = 0; b0 = 0; a1 = 0; b1 = 1; cin0 = 1; #10;
        a0 = 0; b0 = 0; a1 = 1; b1 = 0; cin0 = 1; #10;
        a0 = 0; b0 = 1; a1 = 0; b1 = 0; cin0 = 1; #10;
        a0 = 0; b0 = 0; a1 = 1; b1 = 1; cin0 = 1; #10;
        a0 = 0; b0 = 1; a1 = 1; b1 = 0; cin0 = 1; #10;
        a0 = 0; b0 = 1; a1 = 0; b1 = 1; cin0 = 1; #10;
        a0 = 0; b0 = 1; a1 = 1; b1 = 1; cin0 = 0; #10;
        a0 = 0; b0 = 1; a1 = 1; b1 = 1; cin0 = 1; #10;
        a0 = 0; b0 = 0; a1 = 1; b1 = 1; cin0 = 0; #10;
        a0 = 0; b0 = 1; a1 = 0; b1 = 1; cin0 = 0; #10;
        a0 = 0; b0 = 1; a1 = 1; b1 = 0; cin0 = 0; #10;
        a0 = 1; b0 = 0; a1 = 0; b1 = 0; cin0 = 0; #10;
        a0 = 1; b0 = 0; a1 = 0; b1 = 0; cin0 = 1; #10;
        a0 = 1; b0 = 0; a1 = 0; b1 = 1; cin0 = 0; #10;
        a0 = 1; b0 = 0; a1 = 1; b1 = 0; cin0 = 0; #10;
        a0 = 1; b0 = 1; a1 = 0; b1 = 0; cin0 = 0; #10;
        a0 = 1; b0 = 0; a1 = 0; b1 = 1; cin0 = 1; #10;
        a0 = 1; b0 = 0; a1 = 1; b1 = 0; cin0 = 1; #10;
        a0 = 1; b0 = 1; a1 = 0; b1 = 0; cin0 = 1; #10;
        a0 = 1; b0 = 0; a1 = 1; b1 = 1; cin0 = 0; #10;
        a0 = 1; b0 = 1; a1 = 0; b1 = 1; cin0 = 0; #10;
        a0 = 1; b0 = 1; a1 = 1; b1 = 0; cin0 = 0; #10;
        a0 = 1; b0 = 1; a1 = 1; b1 = 1; cin0 = 0; #10;
        a0 = 1; b0 = 1; a1 = 0; b1 = 1; cin0 = 1; #10;
        a0 = 1; b0 = 0; a1 = 1; b1 = 1; cin0 = 1; #10;
        a0 = 1; b0 = 1; a1 = 1; b1 = 1; cin0 = 1; #10;
    end
endmodule

```

- **Structural Lab Calculator Module:**

```
// Company:
// Engineer:
//
// Create Date: 16.10.2022 16:13:23
// Design Name:
// Module Name: labCalculator
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module labCalculator(input logic a, b, c, d, output logic y, z);
    logic i0, i1, i2, i3;
    assign i0 = a ^ b;
    assign i1 = ~(a & b);
    halfAdder adder(a, b, i2, z);
    halfSubtractor subtractor(a, b, i3, z);
    mux41 mux(c, d, i0, i1, i2, i3, y);
endmodule
```

- **Lab Calculator Testbench:**

```
// Revision 0.01 - File Created
// Additional Comments:
//
//////////////////////////////////////////////////////////////////////////////////


module testbench5();
    logic a, b, c, d, y, z;
    labCalculator labCalc(a, b, c, d, y, z);
    initial begin
        c = 0; d = 0; a = 0; b = 0; #10;
        c = 0; d = 0; a = 0; b = 1; #10;
        c = 0; d = 0; a = 1; b = 0; #10;
        c = 0; d = 0; a = 1; b = 1; #10;
        c = 0; d = 1; a = 0; b = 0; #10;
        c = 0; d = 1; a = 0; b = 1; #10;
        c = 0; d = 1; a = 1; b = 0; #10;
        c = 0; d = 1; a = 1; b = 1; #10;
        c = 1; d = 0; a = 0; b = 0; #10;
        c = 1; d = 0; a = 0; b = 1; #10;
        c = 1; d = 0; a = 1; b = 0; #10;
        c = 1; d = 0; a = 1; b = 1; #10;
        c = 1; d = 1; a = 0; b = 0; #10;
        c = 1; d = 1; a = 0; b = 1; #10;
        c = 1; d = 1; a = 1; b = 0; #10;
        c = 1; d = 1; a = 1; b = 1; #10;
    end
endmodule
```