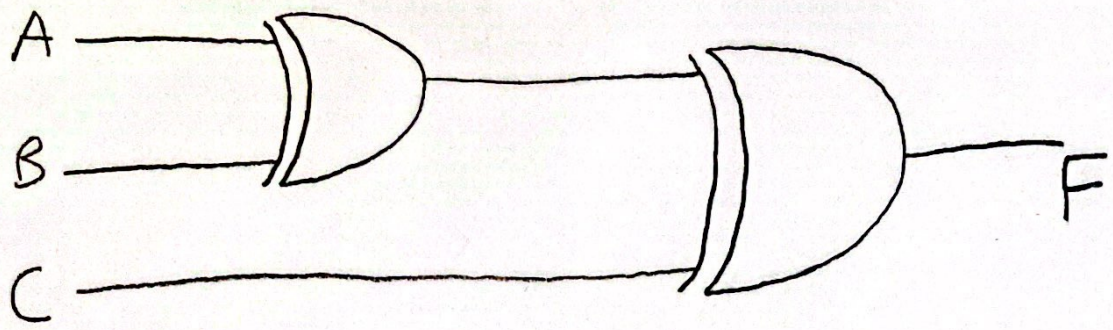
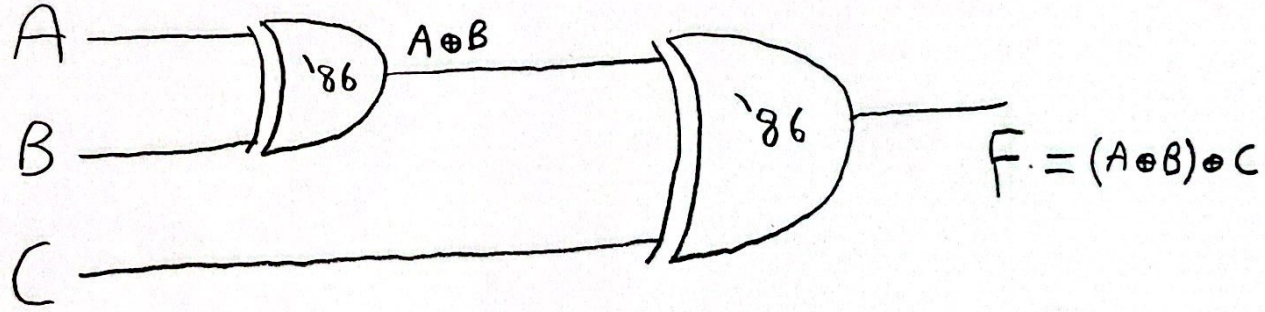
1-) Three input XOR gates using two input X OR gates

* $F = (A \oplus B) \oplus C$

→ Logic Diagram:



→ Circuit Schematic:



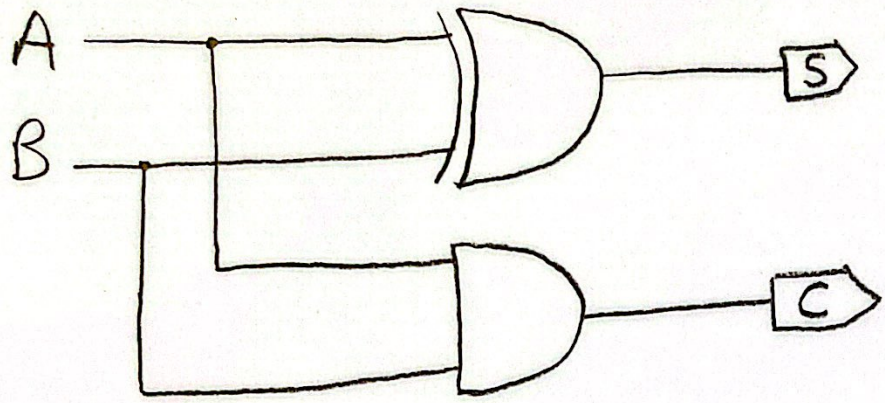
IC List

↳ One 74LS86 Quad 2-Input XOR Gate

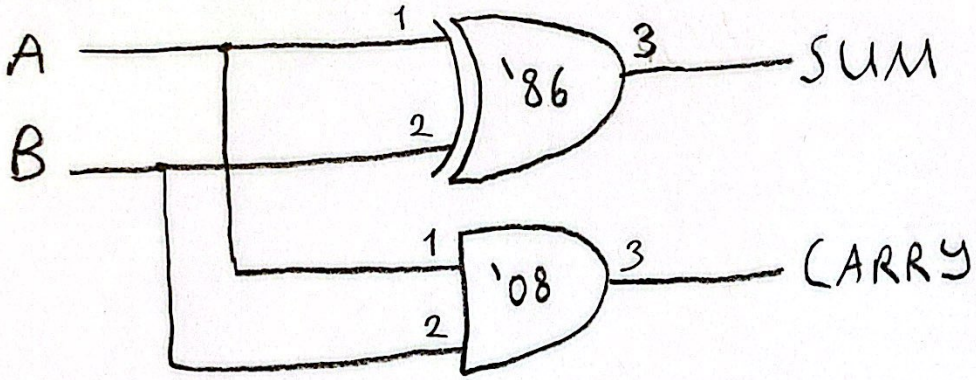
*74LS86
↳GND—7
↳+5V—14

⇒ Half Adder

→ Logic Diagram:



→ Circuit Schematic:



IC List

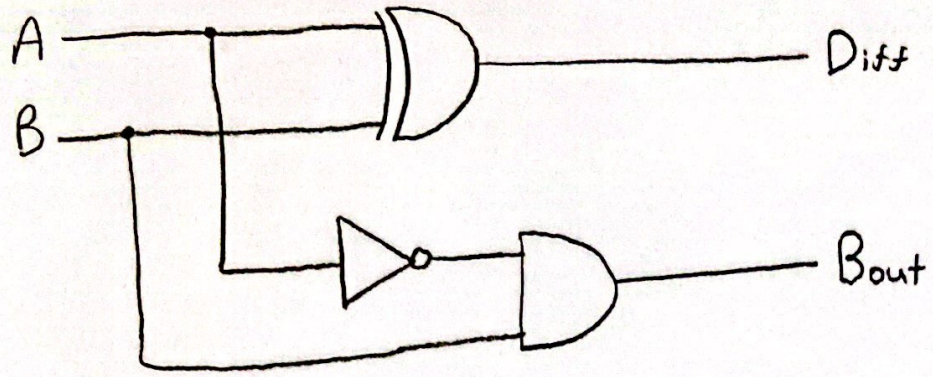
↳ One 74LS86 Quad 2-Input XOR Gate

↳ One 74LS08 Quad 2-Input AND Gate

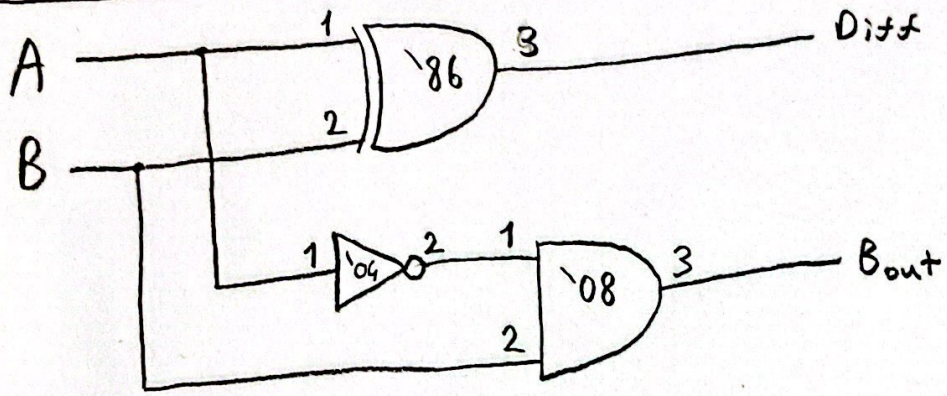
*74LS86	*74LS08
↳GND—7	↳GND—7
↳+5V—14	↳+5V—14

⇒ Half Subtractor

→ Logic Diagram:



→ Circuit Schematic:



IC List

- one 74LS86 Quad 2-Input XOR Gate
- one 74LS04 HEX Inverting Gate
- one 74LS08 Quad 2-Input AND Gate

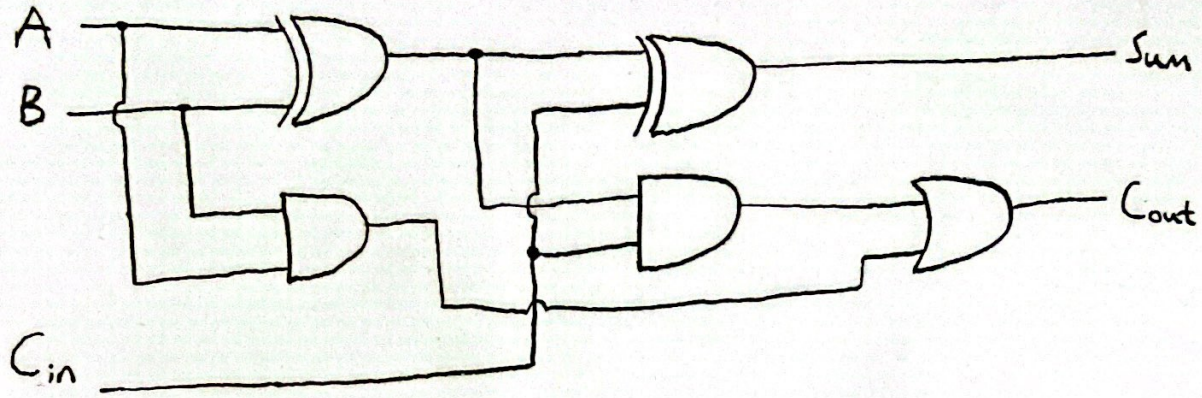
*74LS86
- GND — 7
- +5V — 14

*74LS04
- GND — 7
- +5V — 14

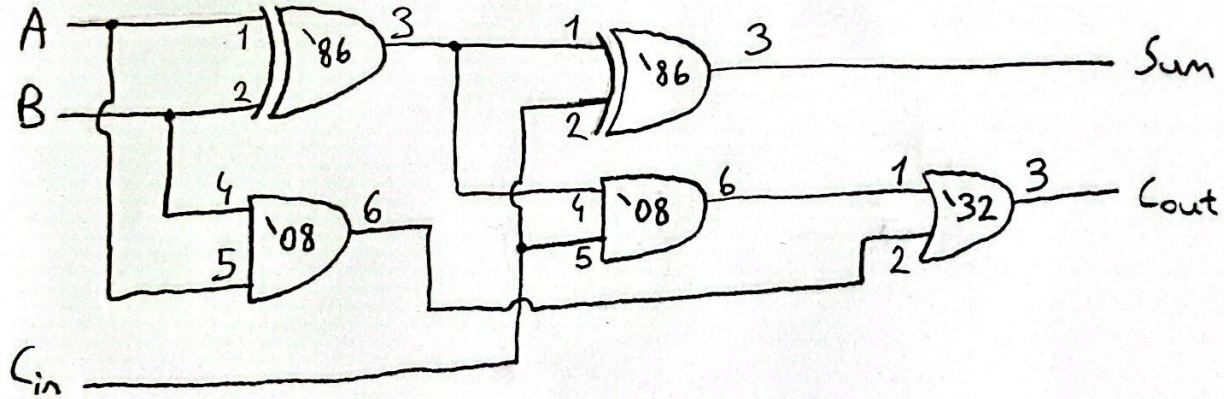
*74LS08
- GND — 7
- +5V — 14

⇒ Full Adder

→ Logic Diagram:



→ Circuit Schematic:



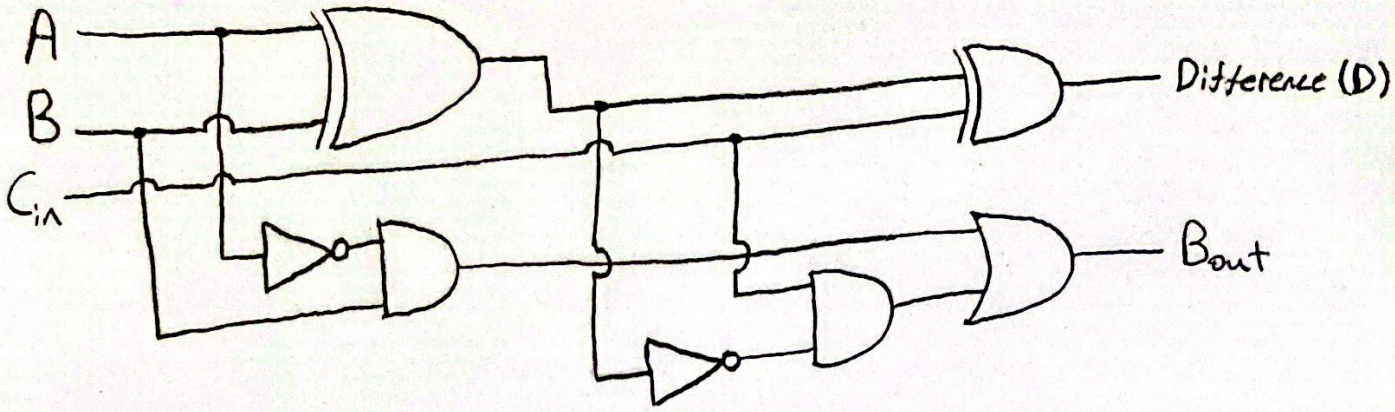
IC List

- One 74LS86 Quad 2-Input XOR Gate
- One 74LS08 Quad 2-Input AND Gate
- One 74LS32 Quad 2-Input OR Gate

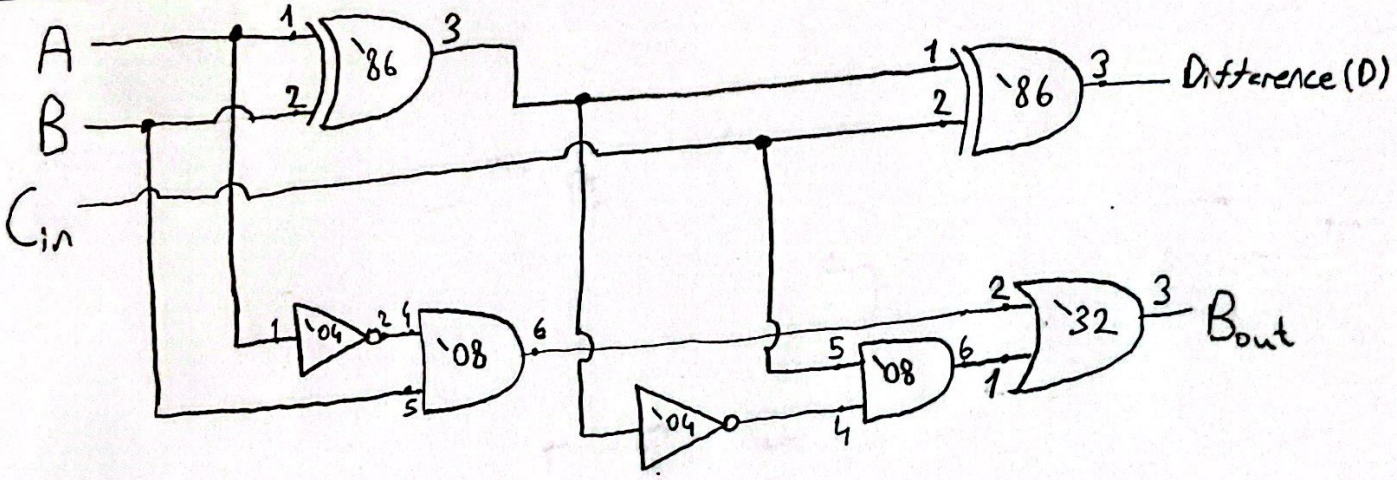
*74LS86	*74LS08	*74LS32
GND — 7	GND — 7	GND — 7
+5V — 14	+5V — 14	+5V — 14

⟹ Full Subtractor

→ Logic Diagram:



→ Circuit Schematic:



IC List

↳ One 74LS86 Quad 2-Input XOR Gate
↳ One 74LS08 Quad 2-Input AND Gate
↳ One 74LS32 Quad 2-Input OR Gate
↳ One 74LS04 HEX Inverting Gate

* 74LS86
↳ GND — 7
↳ +5V — 14

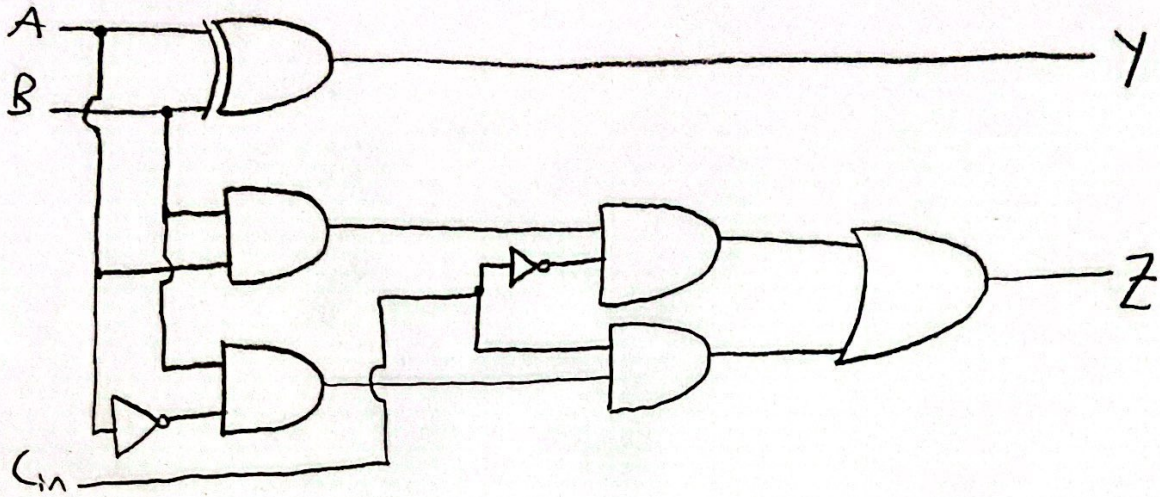
* 74LS08
↳ GND — 7
↳ +5V — 14

* 74LS32
↳ GND — 7
↳ +5V — 14

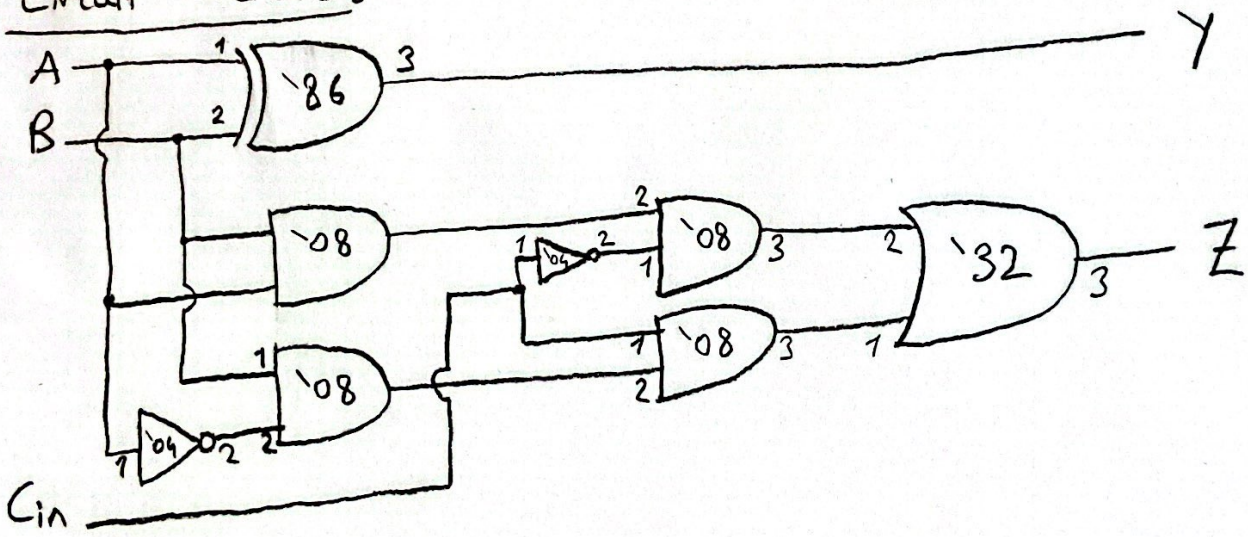
* 74LS04
↳ GND — 7
↳ +5V — 14

⇒ Lab Calculator

→ Logic Diagram:



→ Circuit Schematic:



IC List

- One 74LS86 Quad 2-Input XOR Gate
- one 74LS08 Quad 2-Input AND Gate
- one 74LS32 Quad 2-Input OR Gate
- One 74LS04 HEX Inverting Gate

***74LS86**
- GND — 7
- +5V — 14

***74LS08**
- GND — 7
- +5V — 14

***74LS32**
- GND — 7
- +5V — 14

***74LS04**
- GND — 7
- +5V — 14