Design Report

CS224
Section - 03
Lab - 06
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- **Question 1**

No.	Cache Size KB	N way Cache	Word Size	Block Size(no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits1	Byte Offset Size in bits2	Block Replacement Policy Needed (Yes/No)
1	64	1	32 bits	4	2^{12}	16	12	2	2	No
2	64	2	32 bits	4	2^{11}	17	11	2	2	Yes
3	64	4	32 bits	8	2^{9}	18	9	3	2	Yes
4	64	Full	32 bits	8	1	27	0	3	2	Yes
9	128	1	16 bits	4	2^{14}	15	14	2	1	No
10	128	2	16 bits	4	2^{13}	16	13	2	1	Yes
11	128	4	16 bits	16	2^{10}	17	10	4	1	Yes
12	128	Full	16 bits	16	1	27	0	4	1	Yes

- **Question 2**

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x4($0)	Compulsory Miss	Hit	Hit	Hit	Hit
lw $t2, 0xC($0)	Compulsory Miss	Hit	Hit	Hit	Hit
lw $t3, 0x8($0)	Hit	Hit	Hit	Hit	Hit

b)

Data size = 32 bits
Since N = 1 and cache has 8 words, it is **direct mapped**
Number of blocks in cache = 8/2 = 4 blocks
Number of sets = 4 since N is 1
1 word = 4 bytes
Byte offset = log2(4) = 2
Number of words in one block = 2
Block offset = log2 (2) = 1
Index size = log2 (4) = 2
Tag size = 32 - 2 - 1 - 2 = 27
Every set in the cache contains 1 v(valid) bit, 27 tag bits and 32 + 32 = 64 bits for data.
Cache Size = (1 + 27 + 32 + 32) bits × 4 = 368 bits.
Thus, the cache size is 368 bits.

c)

- **1 Comparator** is needed to check memory address tag and the tag of the set.
- **1 AND Gate** is needed to check if the given tags match AND the data is valid(using v bit) for the associated set.
- **1 32-bit 2x1 Multiplexer** is needed to select between two 32-bit data according to the block offset bit.

- **Question 3**

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x4($0)	Compulsory Miss	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss
lw $t2, 0xC($0)	Compulsory Miss	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss
lw $t3, 0x8($0)	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss	Capacity Miss

b)

Data Size = 32 bits

Since N = 2, cache is **2 way associative** and has 2 words since each block has 1 word

Number of blocks = 2
Number of sets = 1 , as N = 2
1 word = 4 bytes
Byte offset = log2(4) = 2
Number of words in one block = 1
Block offset = log2(1) = 0
Index size = log2(1) = 0
Tag size = 32 - 2 - 0 - 0 = 30 bits
The single set in the cache uses 1-bit for use(U).
One block contains: 1 valid(V) bit, 30 tag bits and 32 data bits.
Cache Size = 1 × (1 + 2 × (1 + 30 + 32)) = 127 bits

c)

- **2 Equality Comparators** are needed to compare the tag of memory address with the tags of each 2 blocks.
- **2 AND Gates** are needed to produce Hit_0 and Hit_1 signals from the outputs of equality comparators and valid bits of each block.
- **1 OR Gate** is needed to produce the Hit signal by Hit_0 OR Hit_1.
- **1 32-bit 2x1 Multiplexer** for selecting the Data from the two blocks using Hit_0 or Hit_1(depending on choice).

- **Question 4**

TL1 = 1 clock cycles
TL2 = 4 clock cycles
TMM = 40 clock cycles
ML1 = 20% miss rate L1
ML2 = 5% miss rate L2
AMAT = TL1 + ML1 . (TL2 + ML2 . TMM) = 1 + 0.2 x (4 + 40 x 0.05) = 2.2 clock cycles
Clock rate with 4GHz = 0.25 ns
10^{12} Instructions requires time = 10^{12}x 0.25 x 2.2
= 0.55 x 10^{12} ns
= **550 seconds**