GEBZE TECHNICAL UNIVERSITY

ELECTRONICS ENGINEERING DEPARTMENT

ELEC 237

EXPERIMENT – 2 REPORT

PREPARED BY

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INGREDIENTS

1. Introduction

An integrator is basically an inverting amplifier that replaces feedback resistor with a capacitor of suitable value.

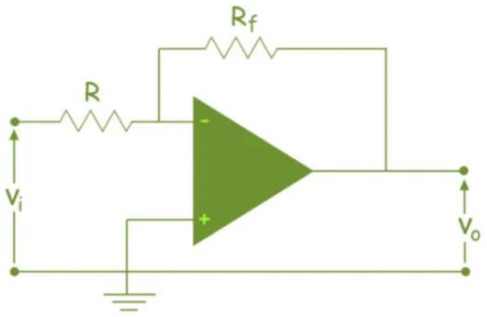


Figure 1. Inverting operational amplifier circuit

The above figure, is an inverting operational amplifier circuit.
This can be modified to an op amp integrator circuit, if the feedback resistor R_f is replaced by a capacitor C as shown below.

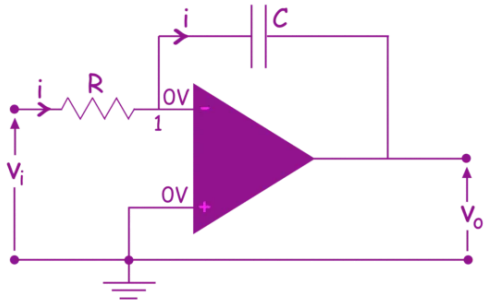


Figure 2. Inverting operational amplifier circuit

In an ideal op amp the voltage at non inverting input terminal is same as that of inverting input.
Here, in the circuit, as the non inverting input is grounded, the electric potential of inverting input will also be zero as non inverting input. In an ideal op amp, no current entires to the op_amp through both inverting and non inverting inputs.
Now, if Kirchhoff's current law is applied at node 1 of the above circuit, shown in Figure 2, we get,

$$\frac{v_i}{R} = -C\frac{\mathrm{d}v_0}{\mathrm{d}t}$$

$$\Rightarrow dv_0 = -\frac{1}{RC}v_i\ dt$$

Integrating both side, it is obtained,

$$v_0 = -\frac{1}{RC}\int v_i \, dt$$

This is the integral function of input voltage.

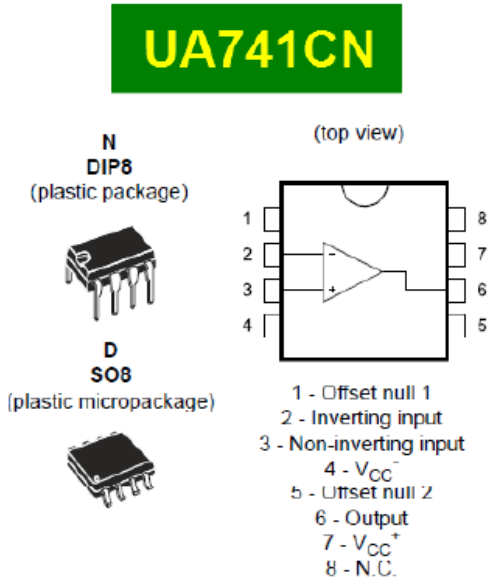


Figure 3. UA741CN Opamp with pin connections.

1. Experiment

2.1. Voltage and Current Offsets

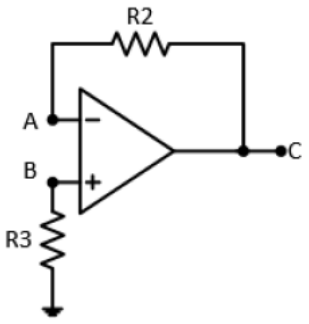


Figure 4. A circuit for the measurement of offsets.

The circuit is assembled as shown in Figure 2. Power supplies are set to ±10V. VC is measured for R2=R3=1MΩ (resistors are used within 5% tolerance). Then, R3 was shorted and VC was measured, and when R3 was shorted, R1=1kΩ was added to ground from the negative input and VC was measured. The measurement results are shown in Table 1.

Table 1. Vc measurements for offset calculations

	$R_3 = 1\ M\Omega$ $R_1 = \infty$	$R_3 = 0$ $R_1 = \infty$	$R_3 = 0$ $R_1 = 1\ k\Omega$
Vc	3.8mV	5mV	0.75V

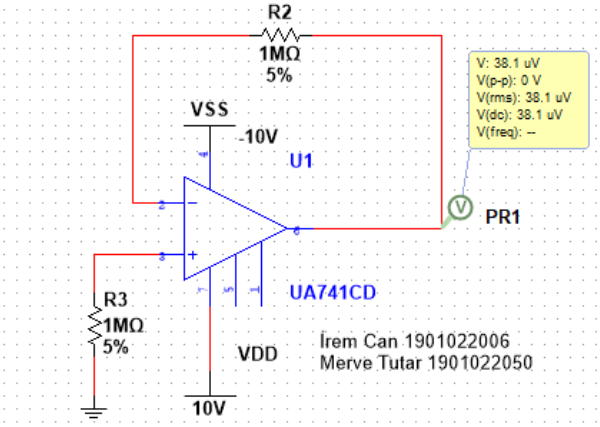


Figure 5. Simulation output for $R_3 = R_2 = 1M\ \Omega$

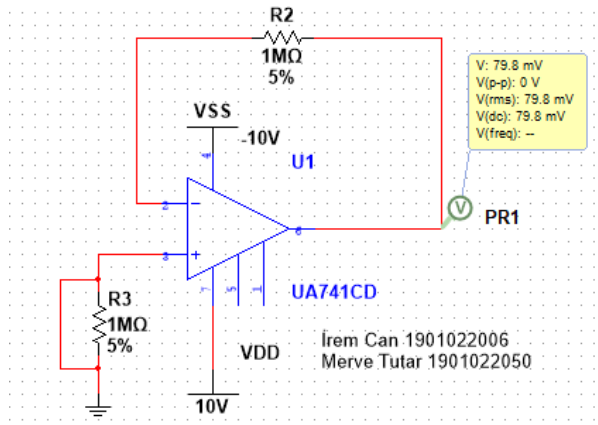


Figure 6. Simulation output for R_3 short circuit

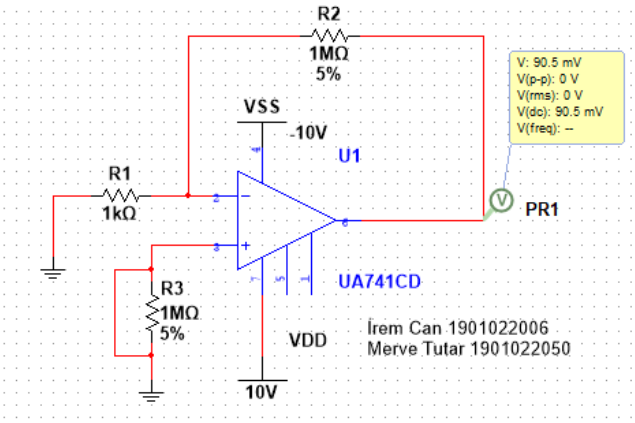


Figure 7. Simulation output for $R_1 = 1k\ \Omega$

Table 2. Vc measurements for offset calculations in Multisim

	R3 = 1 MΩ **R1 = ∞**	**R3 = 0** **R1 = ∞**	**R3 = 0** **R1 = 1 kΩ**
V_c	38.1 uv	79.8 mV	90.5 mV

When the simulations and the measurements made in the experiment were compared, it was seen that the measured results were different. This may be due to the CP type of opamp used.

2.1.1. Offset Measurement

The effects of bias current, offset current and offset voltage on each of these VC values, respectively, are considered. Each one is calculated and their differences from the data sheet values are discussed in the Analysis and Discussion section.

• Approximate ranges for these values in the datasheet are as follows:

o VOS < 6 mV; VOS ≈ 1 mV (typical value)

o IIB < 500 nA; IIB ≈ 80 nA

o IOS < 200nA; iOS ≈ 20 nA

Bearing in mind that all measurements will be different, but the predictive analysis should be similar: Since it is emphasized that these two are independent effects, the contribution from both offset voltage and currents has been taken into account - so superposition is valid here.

VC = Av.VOS + R2.(IIB + IOS/2) and VC = Av.VOS + R2. IOS formulas for VC measurements suitable for calculating bias current, offset current, and offset voltage. Calculation results are transferred to Table 2.

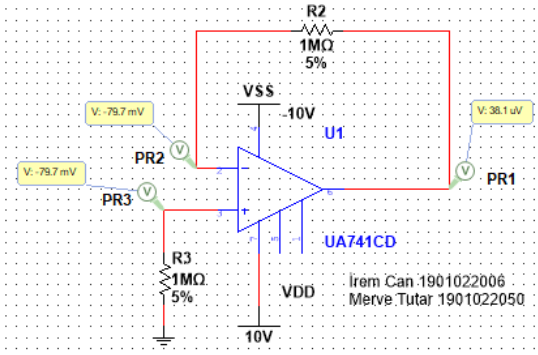


Figure 8. Simulation output for $R_3 = R_2 = 1M\ \Omega$

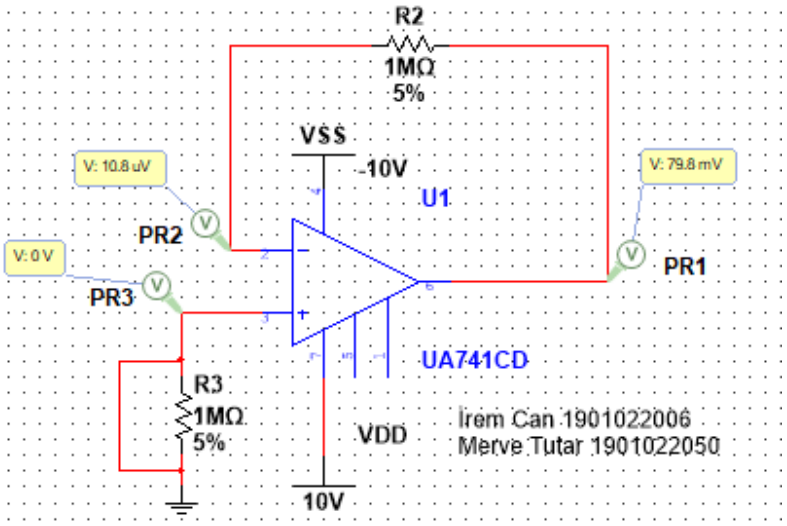


Figure 9. Simulation output for R_3 short circuit

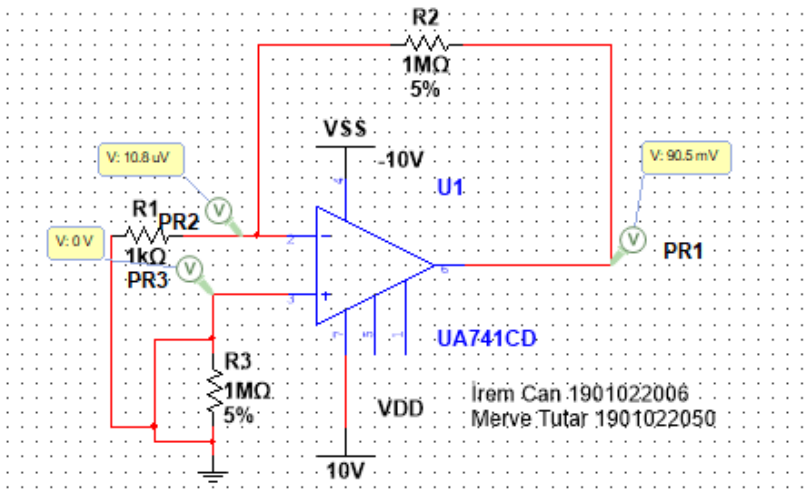


Figure 10. Simulation output for R_1 = 1k Ω

Offset voltage is the result of a difference in voltage between the outputs of two operation amplifiers.

Bias is direct current (DC) deliberately made to flow, or DC voltage deliberately applied, between two points for the purpose of controlling a circuit.

The input offset current (I_{OS}) is equal to the difference between the input bias current at the non-inverting terminal (I_{B+}) minus the input bias current at the inverting (I_{B-}) terminal of the amplifier.

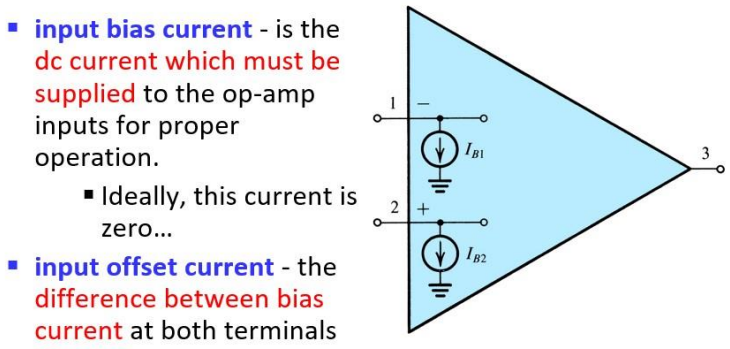


Figure 11. Bias current and Offset curent

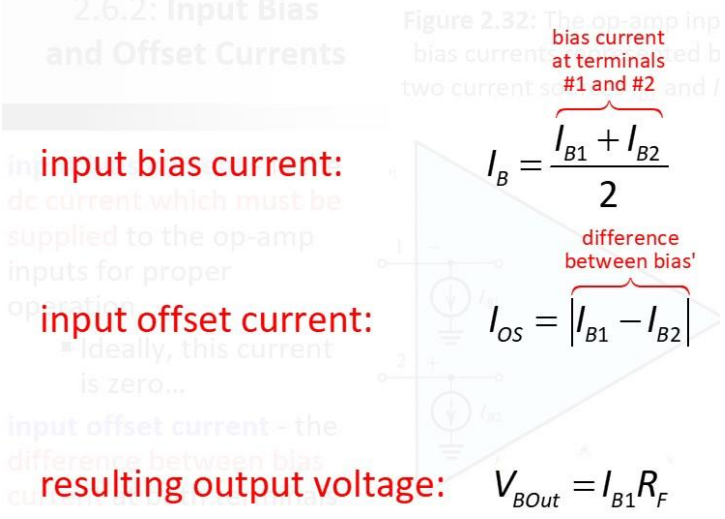


Figure 12. Vout, Ib and Ios equations

Table 3. Calculation Area

V_{OS}	I_{IB}	I_{OS}
R3= 1 MΩ R1= ∞ V_A=-79.7 mV V_B=-79.7 mV V_C=38.1 µV $V_{OS}= V_A- V_B=0$	R3= 1 MΩ R1= ∞ $IB1 = \frac{VC - VA}{R} = \frac{(38.1 \times 10^{-6}) - (-79.7 \times 10^{-3})}{10^6} = 7.974 \times 10^{-8} A$ $IB2 = \frac{-VA}{R} = \frac{-(-79.7 \times 10^{-3})}{10^6} = 7.97 \times 10^{-8} A$ $IB = \frac{IB1 + IB2}{2} = \frac{(7.974 + 7.97) \times 10^{-8}}{2} = 7.972 \times 10^{-8}\ A$	R3= 1 MΩ R1= ∞ $I_{OS}=\lvert I_{B1} - I_{B2}\rvert$ $I_{OS}=\lvert(7.974– 7.97)\times10^{-8}\rvert$ $I_{OS} =4\times10^{-11}$
R3= 0 R1= ∞ V_A=10.8 µV V_B=0 V_C=79.8 mV $V_{OS}= V_A- V_B=10.8$ µV	R3= 0 R1= ∞ $IB1 = \frac{VC - VA}{R} = \frac{(79.8 \times 10^{-3}) - (10.8 \times 10^{-6})}{10^6} = 7.97 \times 10^{-8} A$ $IB2 = \frac{-VA}{R} = \frac{-(10.8 \times 10^{-6})}{10^6} = -1.08 \times 10^{-11} A$ $IB = \frac{IB1 + IB2}{2} = \frac{7.97 \times 10^{-8} + (-1.08 \times 10^{-11})}{2} = 3.984 \times 10^{-8}\ A$	R3= 0 R1= ∞ $I_{OS}=\lvert I_{B1} - I_{B2}\rvert$ $I_{OS}=\lvert(7.97\times10^{-8})– (-1.08\times10^{-11})\rvert$ $I_{OS} =7.97\times10^{-8}$
R3= 0 R1= 1 kΩ V_A=10.8 µV V_B=0 V_C=90.5 mV $V_{OS}= V_A- V_B=10.8$ µV	R3= 0 R1= 1 kΩ $IB1 = \frac{VC - VA}{R} = \frac{(90.5 \times 10^{-3}) - (10.8 \times 10^{-6})}{10^6} = 9.04 \times 10^{-8} A$ $IB2 = \frac{-VA}{R} = \frac{-(10.8 \times 10^{-6})}{10^6} = -1.08 \times 10^{-11} A$ $IB = \frac{IB1 + IB2}{2} = \frac{9.04 \times 10^{-8} + (-1.08 \times 10^{-11})}{2} = 9.03 \times 10^{-14}\ A$	R3= 0 R1= 1 kΩ $I_{OS}=\lvert I_{B1} - I_{B2}\rvert$ $I_{OS}=\lvert(9.04\times10^{-8})– (-1.08\times10^{-11})\rvert$ $I_{OS} =9.04\times10^{-8}$

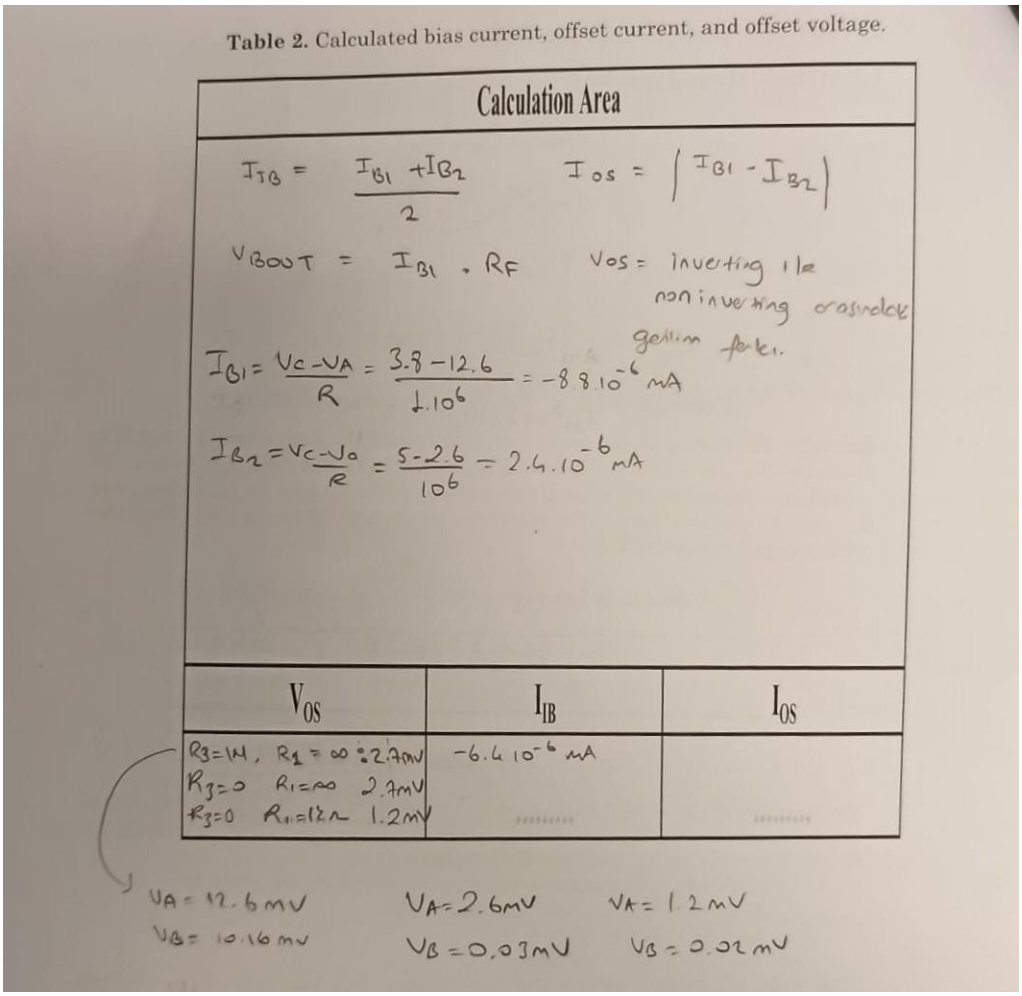


Table 2. Calculated bias current, offset current, and offset voltage.

Calculation Area

$I_{IB} = \frac{I_{B1} + I_{B2}}{2}$ $I_{os} = |I_{B1} - I_{B2}|$

$V_{BOUT} = I_{B1} \cdot R_F$ Vos = inverting ile non inverting arasındaki gerilim farkı.

$I_{B1} = \frac{V_C - V_A}{R} = \frac{3.8 - 12.6}{1.10^6} = -8.8.10^{-6}$ mA

$I_{B2} = \frac{V_C - V_O}{R} = \frac{5 - 2.6}{10^6} = 2.4.10^{-6}$ mA

V_{OS}	I_{IB}	I_{OS}
R_3=1M, R_1=∞ 2.7mV R_3=0 R_1=∞ 2.7mV R_3=0 R_1=1kΩ 1.2mV	$-6.4\ 10^{-6}$ mA	

V_A = 12.6 mV V_B = 10.16 mV

V_A = 2.6mV V_B = 0.03mV

V_A = 1.2mV V_B = 0.02 mV

Figure 13. Table filled during the experiment

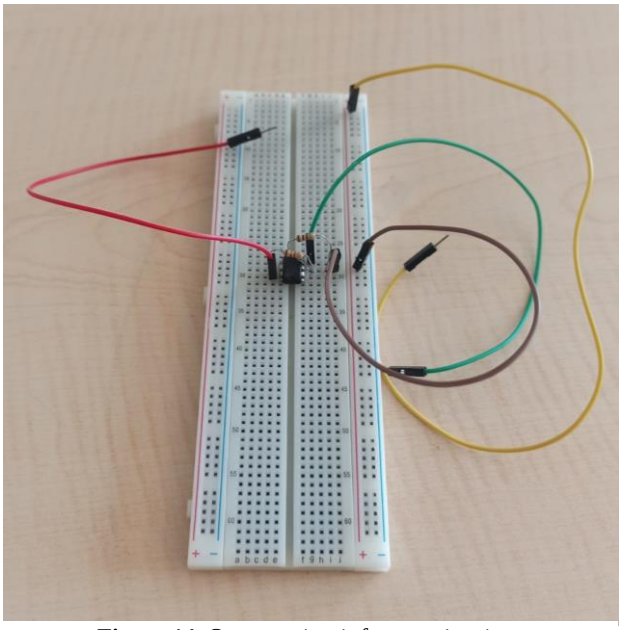


Figure 14. Op-amp circuit for question 1

The circuit shown in figure 10 is a circuit with two 1M resistors with a tolerance of 5%. During the experiment, updates were made on this circuit and progress was made.

2.2.Compensated Miller Integrator

2.2.1. Integrator Offset Control

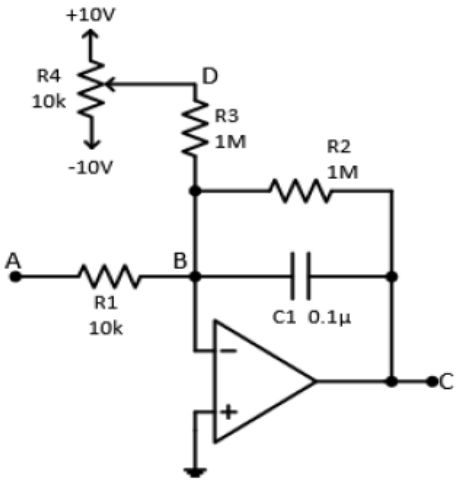


Figure 15. A compansated integrator

The circuit is assembled as shown in Figure 15 With the power supplies set to ±10V:

a) With node A open and measuring V_C, R_4 is adjusted 50% to make V_C = 0 V.

b) Ground node A. Node C and node D were measured and recorded in Table 4.

c) To measure node C and make V_C = 0 V, R_4 is adjusted 50% and node D is measured.

Table 4. Compensation measurements.

	a)	b)	c)
V_C	79.8mV	80.7mV	7.87V
V_D	27,0mV	27.0mV	-10,2V

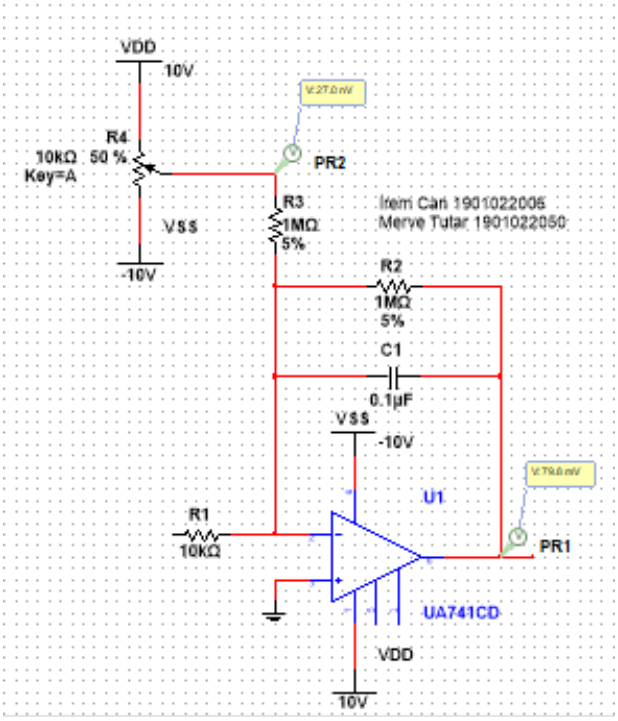


Figure 16. Simulation output for R_4 = %50

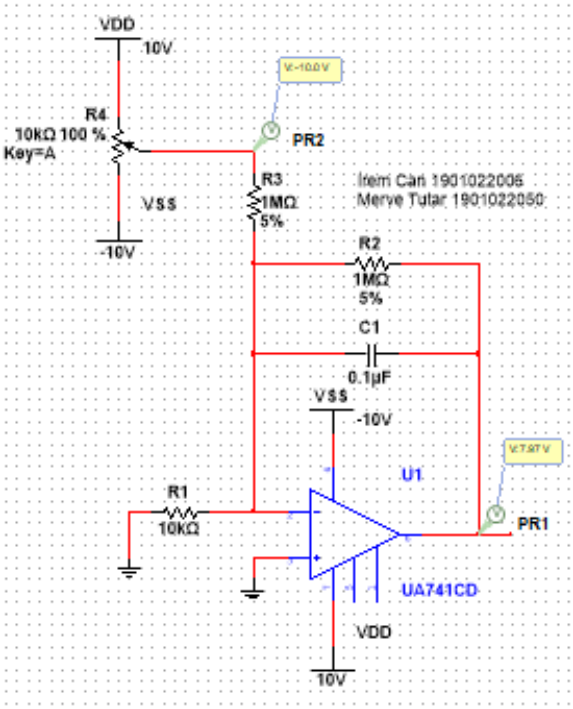


Figure 17. Simulation output for node A is grounded

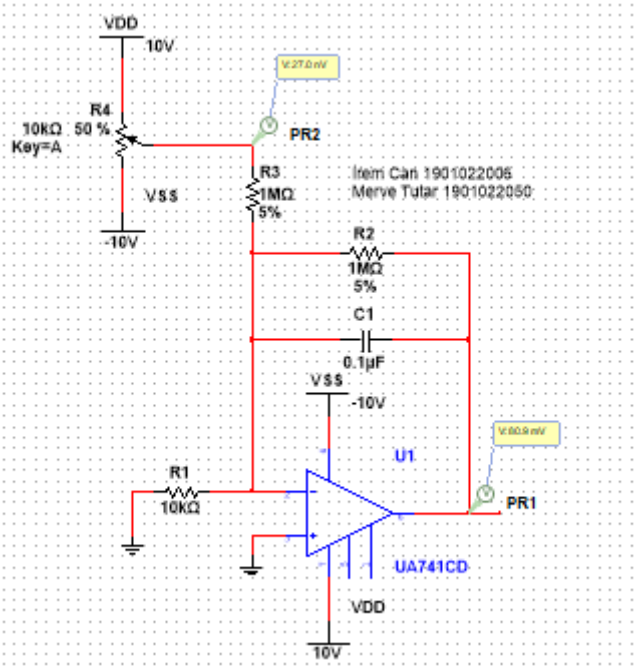


Figure 18. Simulation output for R_4 = %50 and node A is grounded.

Table 5. Compensation measurements of Multisim

	a)	**b)**	**c)**
V_C	27.0 nV	-10.0 V	27.0 nV
V_D	79.8 mV	7.97 V	80.9 mV

Simulation outputs are given in Table 5.

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the input offset voltage, VOS.

Measuring input offset voltages of a few microvolts requires that the test circuit does not introduce more error than the offset voltage itself. The measurement is made at the amplifier output using an accurate digital voltmeter. The offset referred to the input (RTI) is calculated by dividing the output voltage by the noise gain. The small source resistance seen by the inputs results in negligible bias current contribution to the measured offset voltage.

2.2.2 Integrator Operation

The circuit shown in Figure 15 is used with the compensation set in 2.1. A function generator is connected to input A.

a) The generator is set to provide 1 Vpp amplitude at input A and 1 kHz symmetrical square wave at A and C.

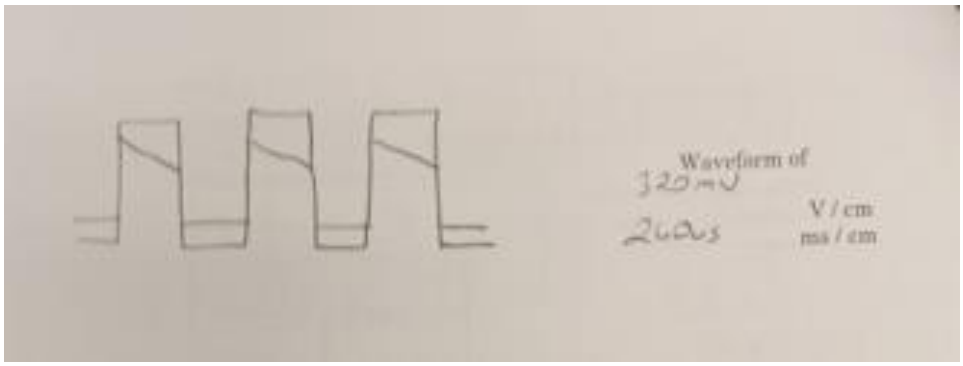


Figure 19. Integrator operation square waveform

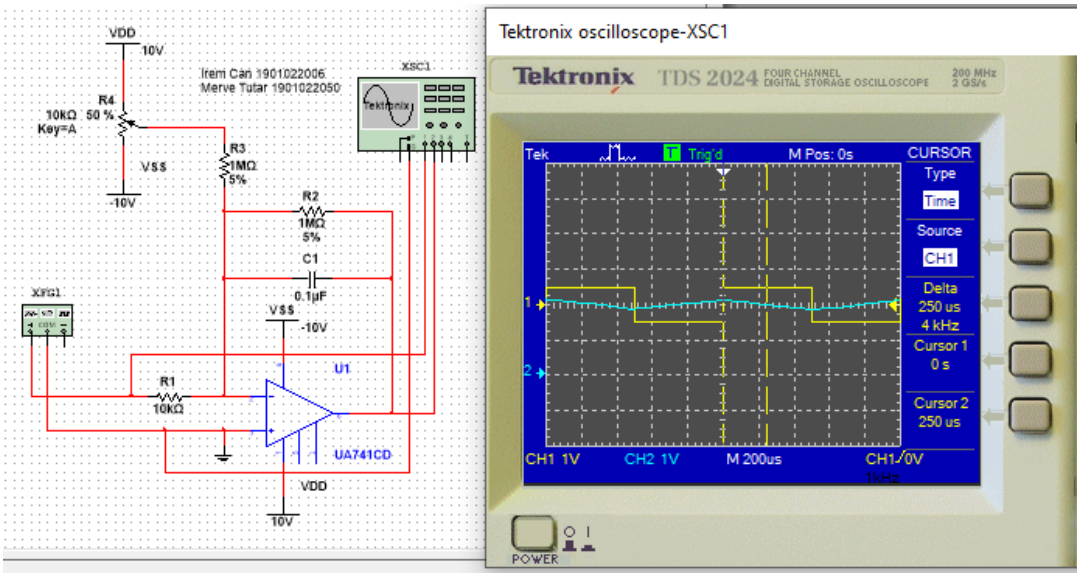


Figure 20. Relative timing simulation measurement for square wave

Relative timing = 250 us

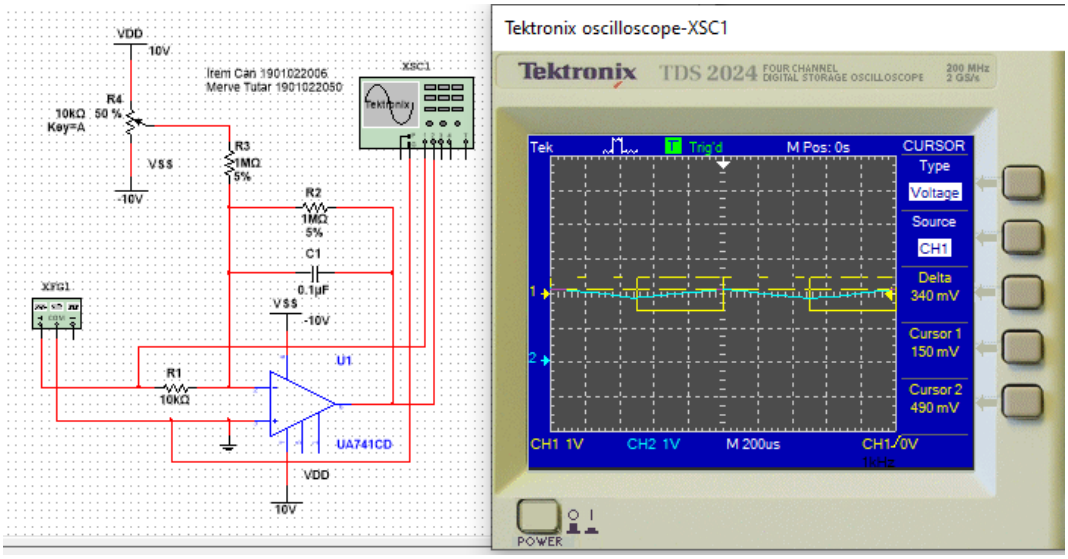


Figure 21. Peak amplitudes simulation measurement for square wave

Peak amplitudes = 340 mV

b) Its generator is set to produce a sine wave to provide 1 Vpp sine wave at input A. Waveforms, peak amplitude and relative timing are noted.

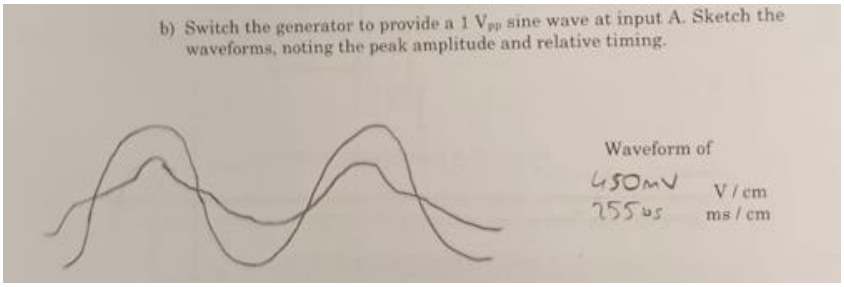


Figure 22. Integrator operation sinusoidal waveform

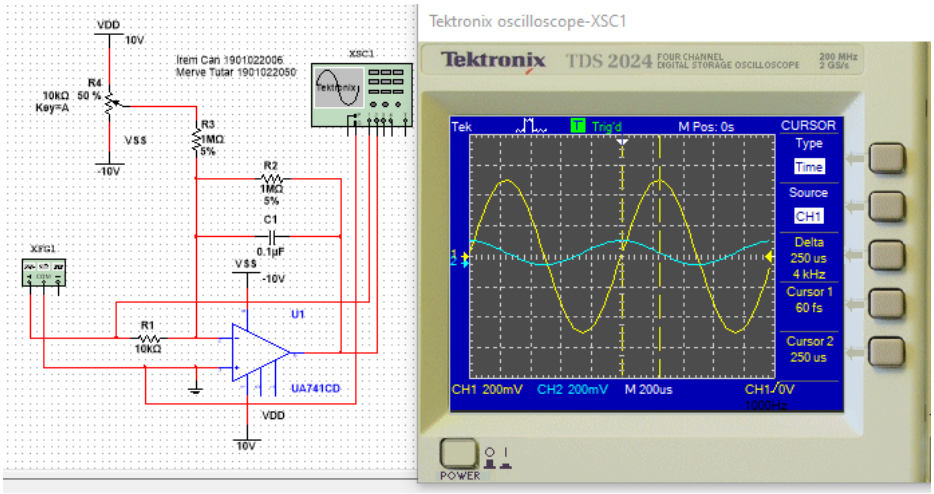


Figure 23. Relative timing simulation measurement for sinusoidal wave

Relative timing = 250 us

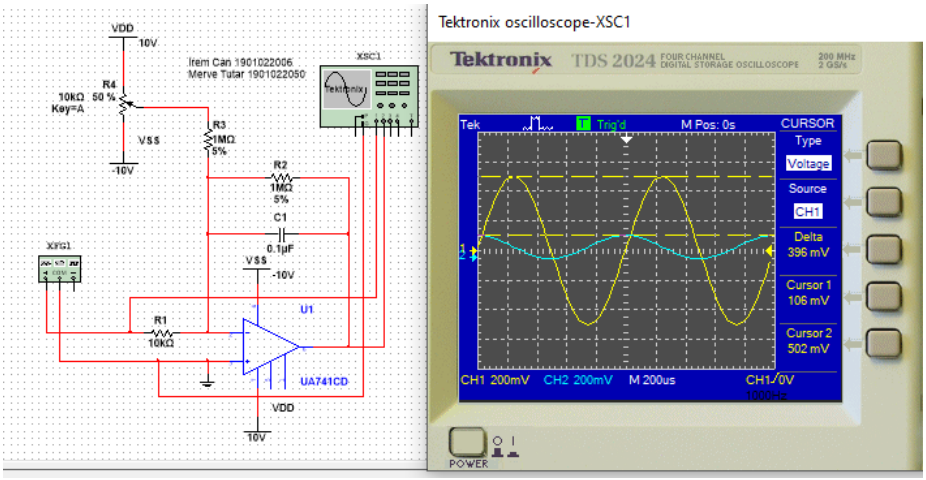


Figure 24. Peak amplitudes simulation measurement for sinusoidal wave

Peak amplitudes = 340 mV

c) The frequency of the signal at the nodes was adjusted so that the amplitudes of the A and C nodes of the generator had the same magnitude. It has been observed that this frequency value is 160 Hz.

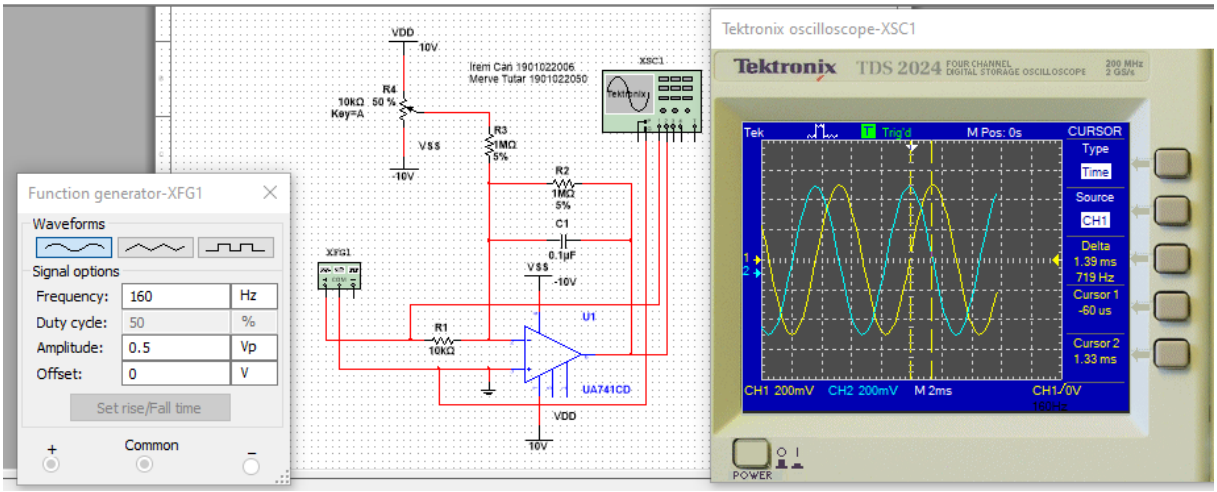


Figure 25. Simulation measurement

f = 160 Hz Φ = 1.39 ms

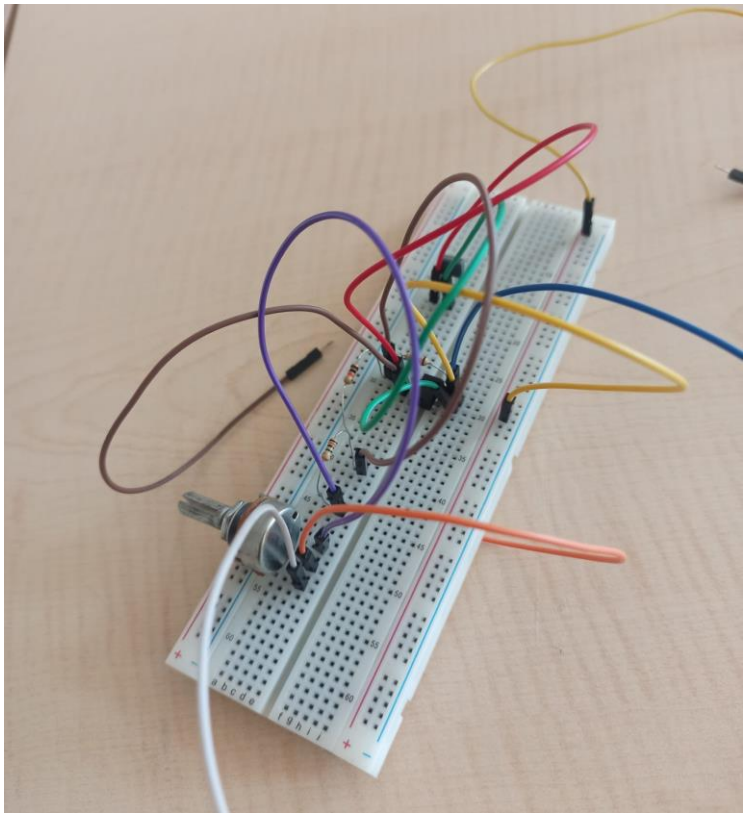


Figure 26. Op-amp circuit for question 2

2.3. Frequency Effects

2.3.1. Small Signal Frequency Response

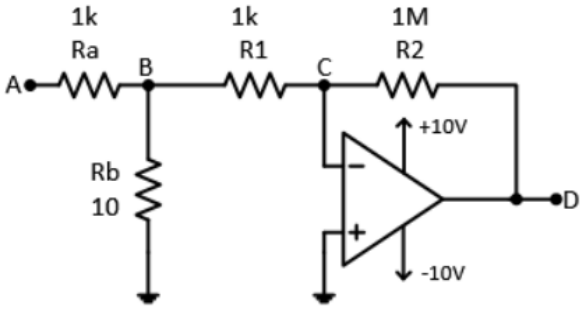


Figure 27. A high-gain inverting amplifier for frequency measurement

Frequency Response of an electric or electronics circuit allows us to see exactly how the output gain (known as the *magnitude response*) and the phase (known as the *phase response*) changes at a particular single frequency, or over a whole range of different frequencies from 0Hz, (d.c.) to many thousands of mega-hertz, (MHz) d epending upon the design characteristics of the circuit.

Generally, the frequency response analysis of a circuit or system is shown by plotting its gain, that is the size of its output signal to its input signal, Output/Input against a frequency scale over which the circuit or system is expected to operate. Then by knowing the circuits gain, (or loss) at each frequency point helps us to understand how well (or badly) the circuit can distinguish between signals of different frequencies.

The frequency response of a given frequency dependent circuit can be displayed as a graphical sketch of magnitude (gain) against frequency (f). The horizontal frequency axis is usually plotted on a logarithmic scale while the vertical axis r epresenting the voltage output or gain, is usually drawn as a linear scale in decimal divisions. Since a systems gain can be both positive or negative, the y-axis can therefore have both positive and negative values.

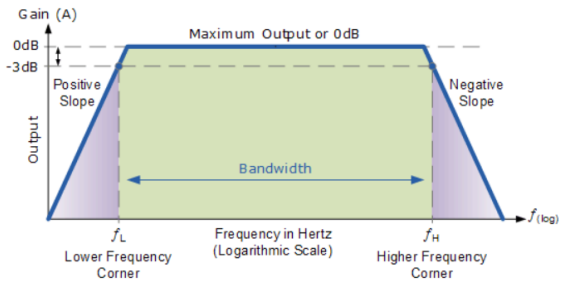


Figure 28. Frequency Response Curve

Frequency Response -3dB Point

$$-3\text{dB} = 20\log_{10}(0.7071)$$

Figure 29. Equation for -3 dB

These -3dB corner frequency points define the frequency at which the output gain is reduced to 70.71% of its maximum value. Then we can correctly say that the -3dB point is also the frequency at which the systems gain has reduced to 0.707 of its maximum value.

The -3dB point is also known as half power points as the output power at these corner frequencies will be half of the maximum 0dB value as shown.

-The circuit was assembled as shown in Figure 27. Power supplies are set to ±10V.Connected the function generator to input A at 100 Hz. Measured nodes A and D. The generator amplitude was adjusted to provide a peak output of 2 Vpp at 100 Hz at the D node. Changed resistor R2 from 1MΩ to 100kΩ and repeated.

Table 6. Small-signal frequency measurements for R2 = 1MΩ

R_2 = 1MΩ	a)	b)	c)
V_A	68.0mV	64.8mV	62.4mV
V_D	2 V_{pp}	rms: 0.94V	rms 0.935V
f_4	100 Hz	141.5 Hz	141.5 Hz

a) Measured nodes A and D. The generator amplitude is adjusted to provide a peak output of 2 Vpp at 100 Hz at the D node.

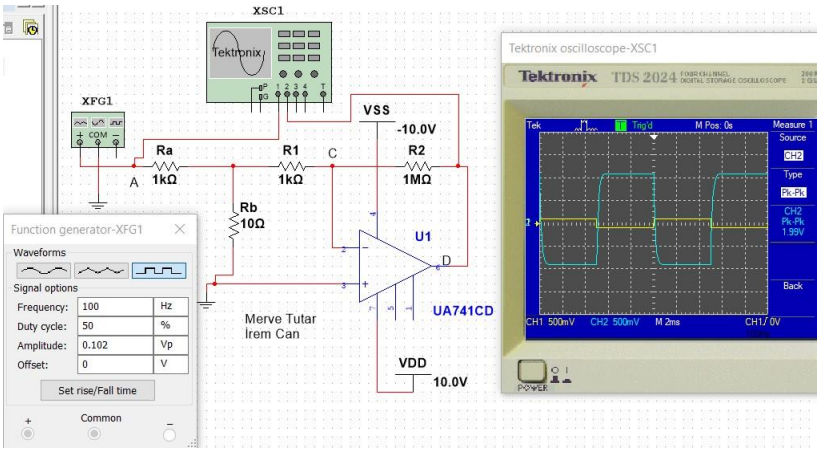


Figure 30. Circuit for 1MΩ

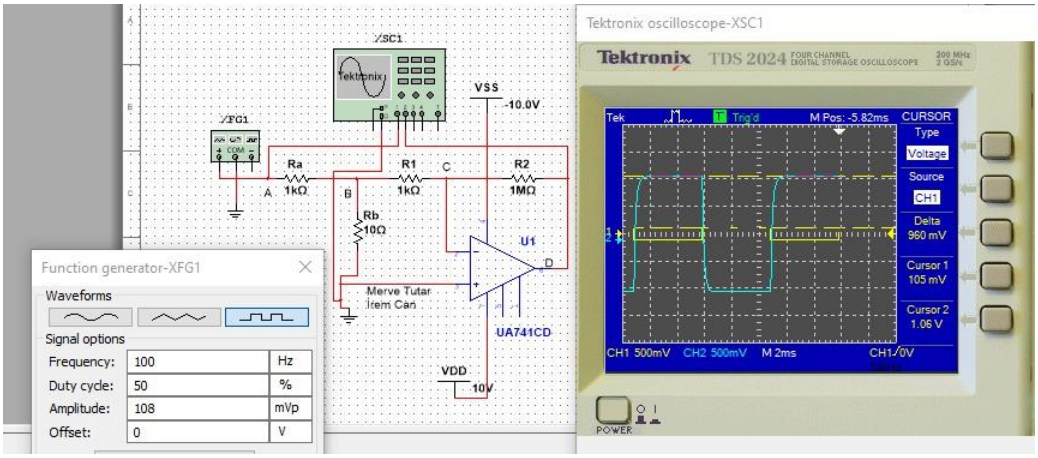


Figure 31. 100 Hz voltage measurement

b) The frequency of the generator is increased to the value at which vD is reduced by 3dB. ($1/\sqrt{2} = 0.707$ of 100 Hz).

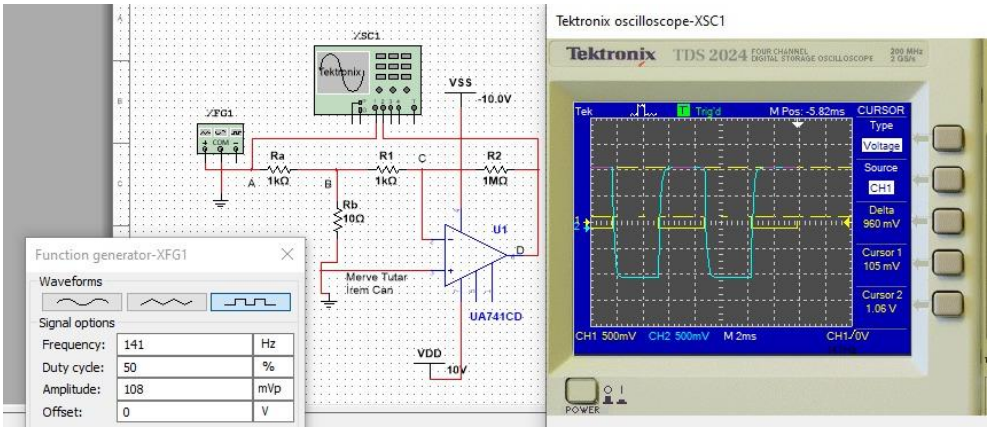


Figure 32. 141.5 Hz voltage measurement

c) The frequency is increased to 10 f4. The peak-to-peak output value was measured.

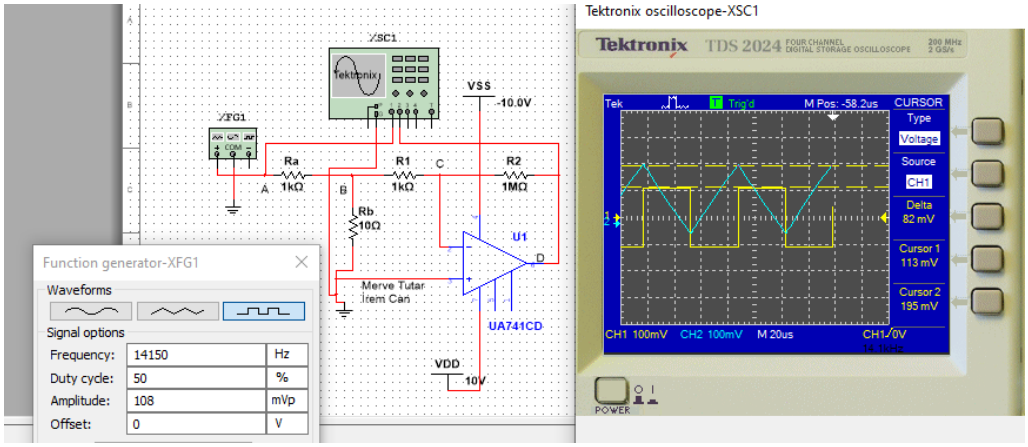


Figure 33. 14150 Hz voltage measurement

Table 7. Small-signal frequency measurements $R_2 = 1M\Omega$ in Multisim

R2 = 100kΩ	**a)**	**b)**	**c)**
V_A	105 mV	105 mV	113 mV
V_D	2 V_{PP}	1.6 V	116 mV
f_4	100 Hz	141.5 Hz	14150 Hz

d) Changed resistor R2 from 1MΩ to 100kΩ and repeated a), b), c).

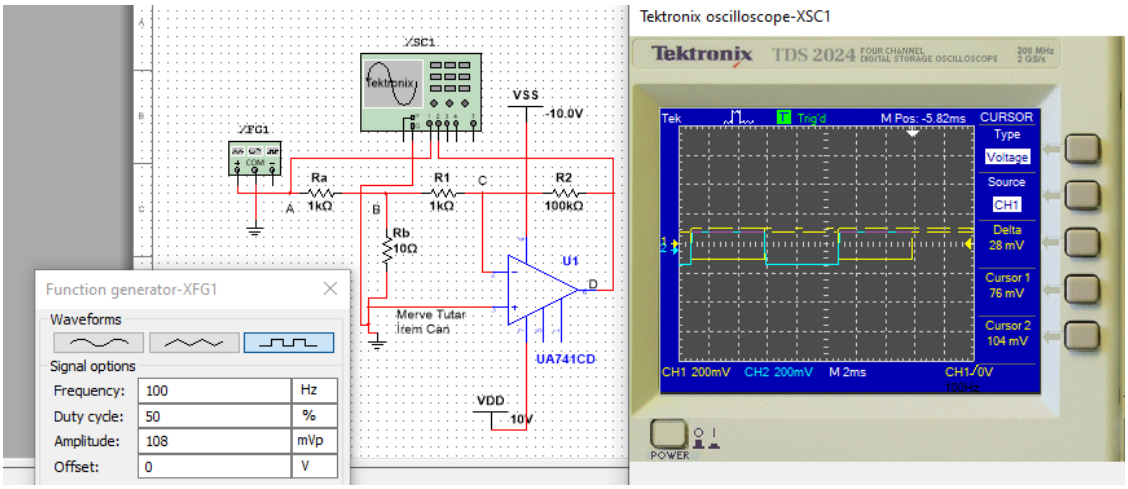


Figure 34. 100 Hz voltage measurement

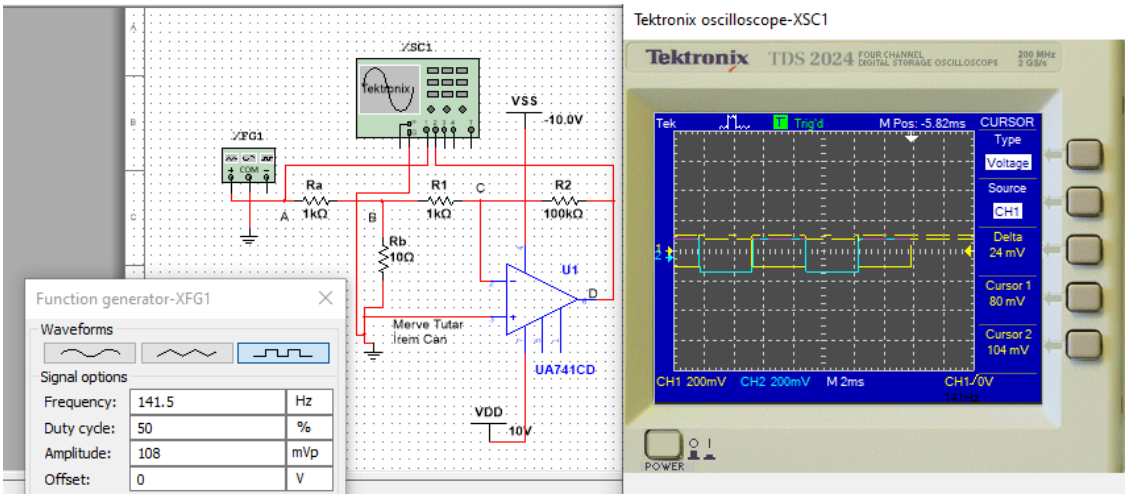


Figure 35. 141.5 Hz voltage measurement

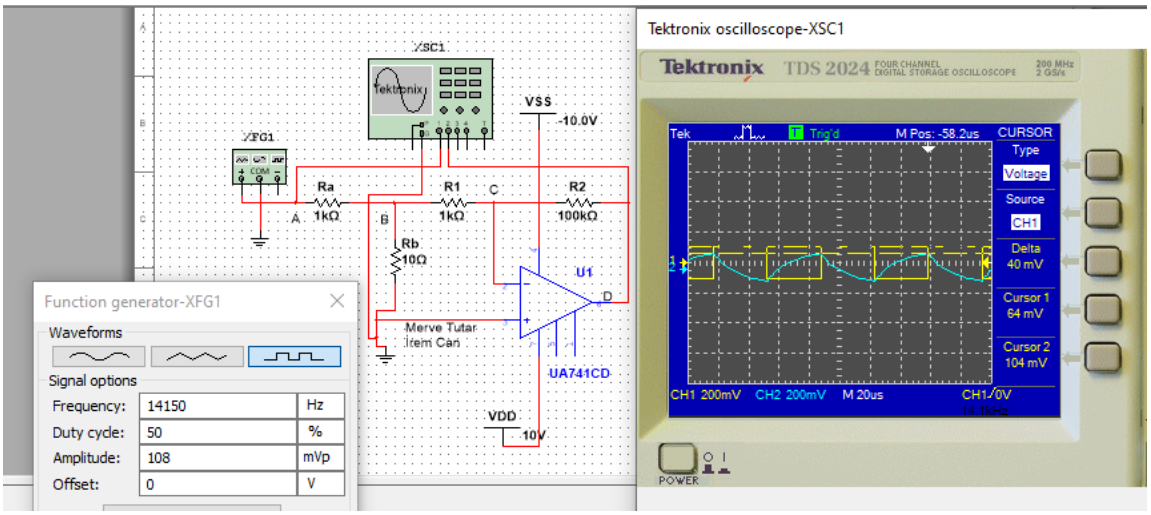


Figure 36. 14150 Hz voltage measurement

Table 7. Small-signal frequency measurements R_2 = 100kΩ in Multisim

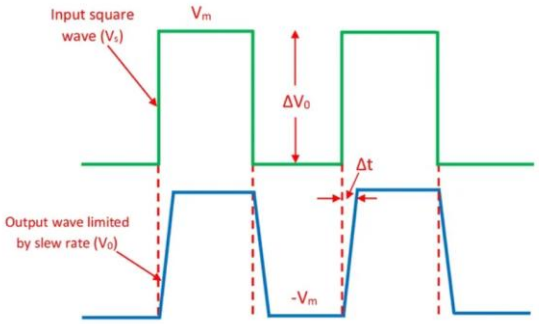
R2 = 100kΩ	**a)**	**b)**	**c)**
V_A	76 mV	80 mV	64 mV
V_D	2 V_{PP}	104 mV	104 mV
f_4	100 Hz	141.5 Hz	14150 Hz

2.3.2. Slew-rate limiting

The slew rate is defined as the maximum rate of output voltage change per unit time. It is denoted by the letter S. The slew rate helps us to identify the amplitude and maximum input frequency suitable to an operational amplifier (opamp) such that the output is not significantly distorted.

Slew rate is a critical factor in ensuring that an OP amp can deliver an output that is reliable to the input. Slew rate changes with the change in voltage gain. Therefore, it is generally specified at unity (+1) gain condition.

The input and slew limited output voltage waveform are shown in the figure below.



Şekil 37. Input and Slew Limited Output Voltage Waveform

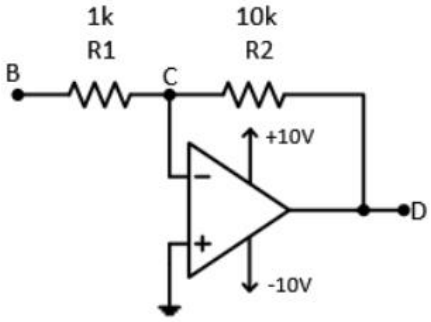


Figure 38. A circuit for evaluatig slew rate

The circuit was assembled as shown in Figure 38. Power supplies are set to ±10V. The function generator is connected to input B at 1 kHz.

a)Nodes B and D were measured. The generator amplitude was adjusted to provide a peak output of 0.2 Vppat 1 kHz at the D node.

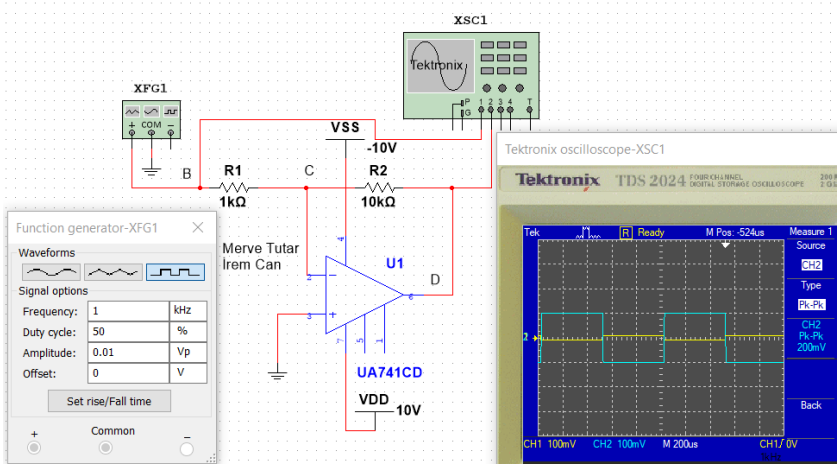


Figure 39. The generator amplitude is set for Pk-Pk=0.2V

b) Raise the frequency of the generator to the value at which vDis reduced by3dB(to $1/\sqrt{2} = 0.707$ of its 1 kHz value). Note the frequency as f5. Verify that it's 100 times that in E3.1 b), namely 100 f4.

$$\mathbf{f_5}=1414{,}4\text{s}$$

c) Reduce the frequency to 1 kHz. Raise the input signal amplitude until V_D reaches 8 Vpp. Note vB.

$$V_B=(V_{P\text{-}P})=784\text{ mV}$$

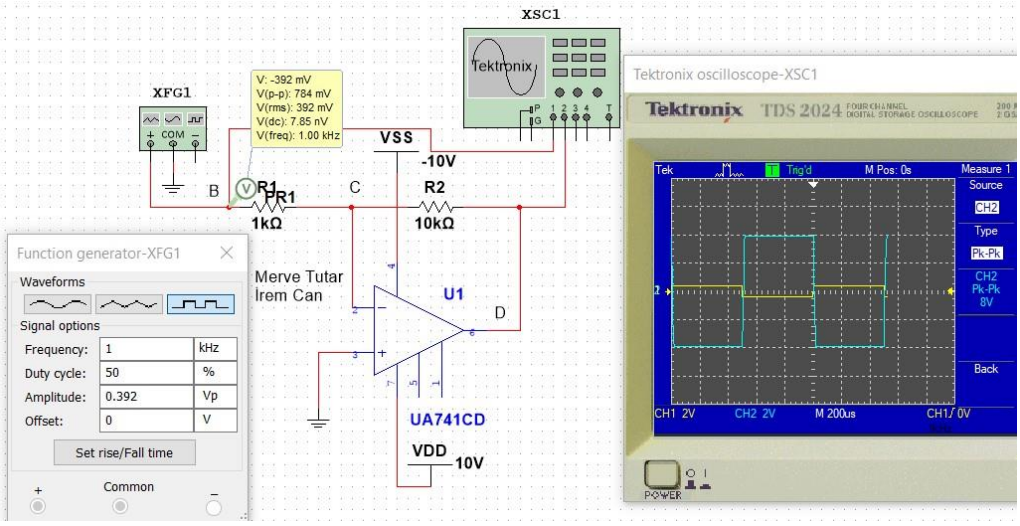


Figure 40. Vb value for Vp-p=8V

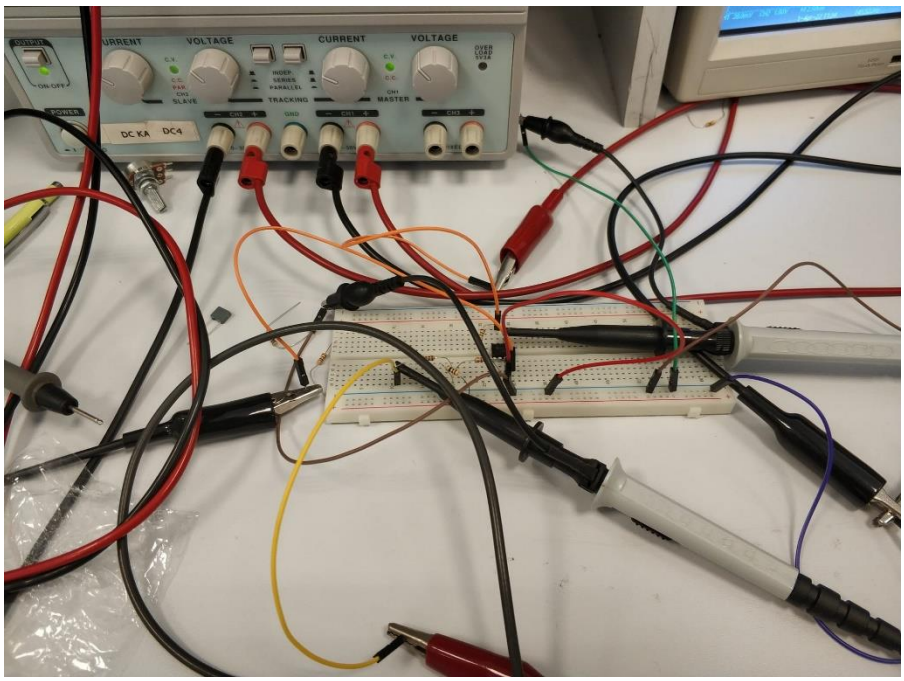


Figure 41. Experimental circuit of question 3

3. Conclusion

In this experiment, Operational-Amplifier Imperfections and Applications Basics is used. We used concepts such as bias current, offset current, and offset voltage,peak to peak and frequency.

It has been learned that the offset voltage is the result of the voltage difference between the outputs of the two processing amplifiers. It was learned that the input offset current (IOS) is equal to the difference between the input bias current at the non-inverting terminal (IB+) and the input bias current at the inverter (IB-) terminal of the amplifier. It was concluded that the bias current refers to the DC currents entering or leaving the input pins of the amplifier to create a defined operating point during normal operation.

We have applied various formulas (for example: VC = Av.VOS + R2.(IIB + IOS/2) and VC = Av.VOS + R2) to calculate the bias current, offset current, and offset voltage.

It was observed that the VC voltage was zero when it was brought to the 50% level by obtaining information about the effect of potentiometers on the opamp.

Waveforms were plotted taking into account the peak amplitudes and the relative timing. According to frequency changes, resistance changes and amplitude changes, different measurements were taken from the wave graphs and examined.

There are some differences between the measurements we took during the experiment and the measurements made in the multism program. We think that these may be due to the opamp characteristic or calculation errors.

4. References

[1] https://www.electronics-tutorials.ws/amplifier/frequency-response.html

[2] https://en.wikipedia.org/wiki/Input_offset_voltage

[3] https://www.sciencedirect.com/topics/engineering/offset-voltage

[4] https://www.analog.com/media/en/training-seminars/tutorials/mt-037.pdf