GEBZE TECHNICAL UNIVERSITY

ELECTRONICS ENGINEERING DEPARTMENT

ELEC 237

EXPERIMENT – 5 REPORT

PREPARED BY

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INGREDIENTS

1. Introduction

Mosfet – **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor

In electronic terms, the working principle of a transistor is very simple: it has three main terminals, and the current flowing through one of its terminals can be controlled by the voltage between the other two terminals. In the case of a MOSFET, the voltage between the gate and the source ports controls the current flowing through the drain. The relationship between the drain current (ID) and the gate-to-source voltage (VGS) is highly non-linear, and it is divided in three operation regions. Each region has its own conditions, properties and equations, as described in the table below:

Table 1. Conditions and Features for Regions

Operation Mode	Type	Condition	Equation
Cut-Off	NMOS	$V_{GS} < V_{TH}$	$I_D = 0$
	PMOS	$\|V_{GS}\| < \|V_{TH}\|$	$I_D = 0$
Linear	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \leq V_{GS} - V_{TH}$	$I_D = K_n(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2)$
	PMOS	$\|V_{GS}\| \geq \|V_{TH}\|$ $\|V_{DS}\| \leq \|V_{GS}\| - \|V_{TH}\|$	$I_D = K_p(2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2)$
Saturation	NMOS	$V_{GS} \geq V_{TH}$ $V_{DS} \geq V_{GS} - V_{TH}$	$I_D = K_n(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$
	PMOS	$\|V_{GS}\| \geq \|V_{TH}\|$ $\|V_{DS}\| \geq \|V_{GS}\| - \|V_{TH}\|$	$I_D = K_p(V_{GS} - V_{TH})^2(1 - \lambda V_{DS})$

There are two types of MOSFETs: the NMOS and the PMOS. The difference between them is the construction: NMOS uses N-type doped semiconductors as source and drain and P-type as the substrate, whereas the PMOS is the opposite. This has several implications in the transistor functionality (Table 1). The most evident one is the drain current direction and the voltages polarity: the threshold voltage VTH, the VGS and the VDS are negative. Secondly, the charge carriers are not the same: NMOS uses electrons and PMOS uses holes as majority carriers. This greatly affects the K constant.

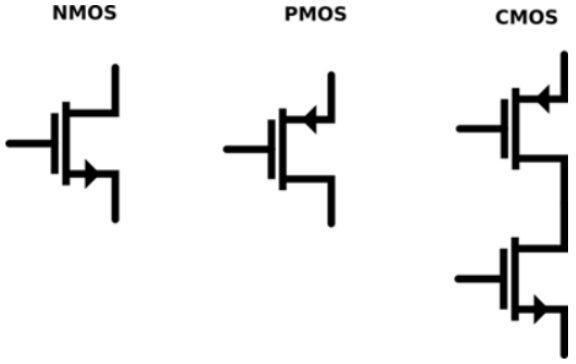
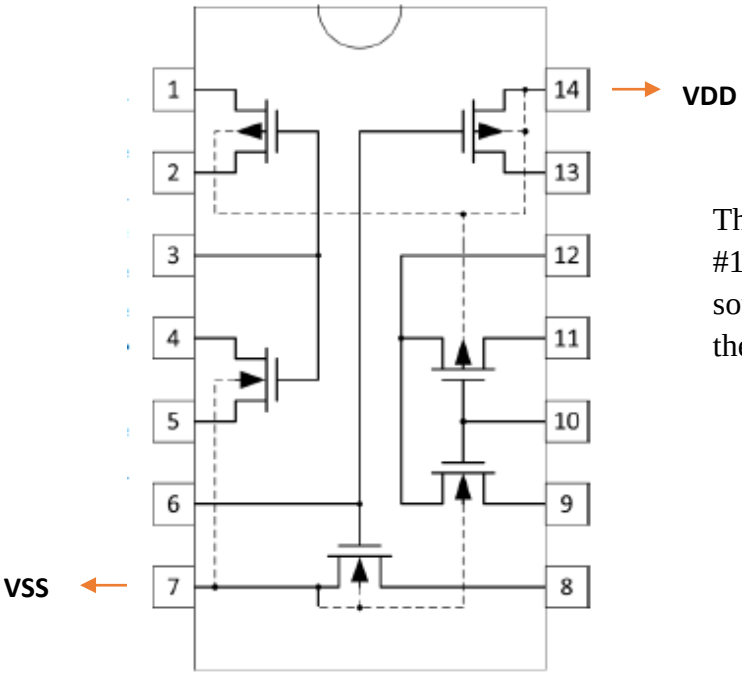


Figure 1. The NMOS symbol, PMOS symbol and CMOS symbol

2. Experiment

2.1 Device Parameters

Throughout the experiments, a 4007 MOS array package was used, the layout of which is shown in Figure 2.



Throughout the experiment, #14 was the most positive source, #7 is connected to the most negative source.

Figure 2. Layout of 4007 MOS array.

2.1.1 Measuring Device Thresholds

a) By selecting Pin #1 as the source terminal (a PMOS device), the circuit shown in Figure 3 was assembled. 10 V was used as the supply. The voltage from A to ground (VA) was measured Vtp predicted..

Pin #1 and Pin#14 → 10 V

Pin#7 → GND Pin#2 → open

Pin #2 and Pin#3 → connected

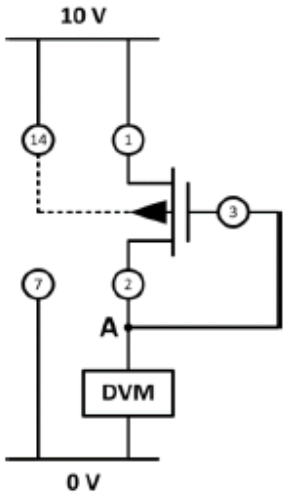


Figure 3. Setup to measure

b) The measurement was repeated by changing the drain and source: Pin #2 was used as the source terminal.

Pin #2 and Pin#14 → 10 V

Pin#7 → GND Pin#1 → open

Pin #1 and Pin#3 → connected

Vtp = 10-VA

Pin # as Source	V_A	V_{tp}
#1 (a)	9.57 V	10 - 9.57 = 0,43 V
#2 (b)	9,55 V	10 - 9.55 = 0.45V

Figure 4. DC voltage measurements and threshold voltage estimations of single transistor

c) Using the configuration in Figure 3, node A was shunted to ground with a 1 kΩ resistor. The voltage value was noted in table 2. The gate drain is disconnected and the gate is connected to an adjustable voltage source. The gate voltage was carefully and slowly adjusted so that the

VSG would pass over the values given in the table below. VA was noted and Id calculated. Vtp was estimated as the voltage allowing ID > 10 µA for this technology.

$$ID = \frac{1}{2} \times kp \times (Vgs - Vtp)^2$$

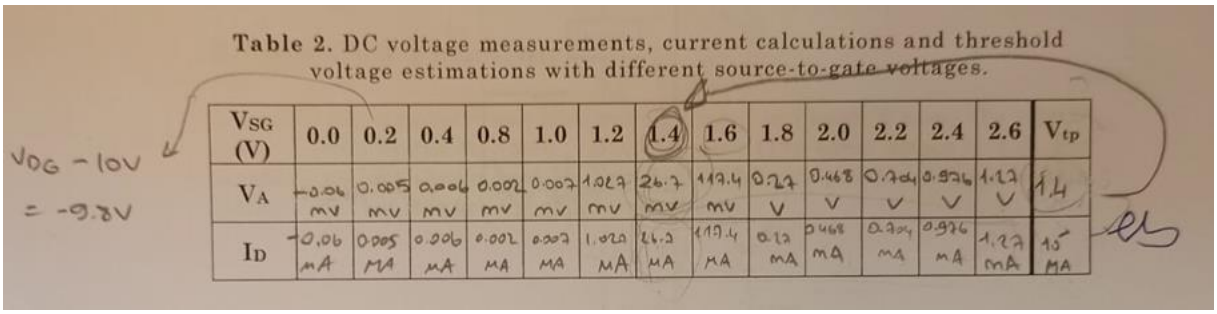


Table 2. DC voltage measurements, current calculations and threshold voltage estimations with different source-to-gate voltages.

V_{SG} (V)	0.0	0.2	0.4	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	V_{tp}
V_A	-0.06 mV	0.005 mV	0.006 mV	0.002 mV	0.007 mV	1.029 mV	26.7 mV	119.4 mV	0.27 V	0.468 V	0.724 V	0.926 V	1.27 V	1.4
I_D	-0,06 mA	0.005 mA	0.006 mA	0.002 mA	0.007 mA	1.029 mA	26.2 mA	119.4 mA	0.27 mA	0.468 mA	0.724 mA	0.926 mA	1.27 mA	15 mA

$V_{DG} - 10V = -9.8V$

Figure 5. DC voltage measurements, current calculations and threshold voltage estimations with different source-to-gate voltages.

2.1.2 Measuring Device Conductivity (Transconductance) Parameter, kp

The configuration in Figure 3 was continued to be used.

a) VA for pin #1 was measured and noted.
b) Node A was shunted to ground with a resistor RD (10 kΩ) for VA to drop by a fixed amount such as 1 V. The VA and the resistance we applied for each case were measured. Using the available parameters and the Vtp we estimated in section 2.1.1 c), the transconductance parameter kp = µpCox(W/L) was calculated for each case.
c) Repeated with pin #11 and #14 used as source terminals.

Table 2. Pin assignments for terminals

Source Pin	1	11	14
Gate Pin	3	10	6
Drain Pin	2	12	13

Pin # as source	#1	#11	#14
V_A (when open)	9.39V	9.38V	9.36V
V_A (shunted by R_D)	7.57V	7.55V	7.58V
R_D (manually set)	10kΩ	10kΩ	10kΩ
$k_p = \mu_p C_{ox}(W/L)$ (calculated)	1.43×10^{-6}	$1.37 \cdot 10^{-6}$	$1.46 \cdot 10^{-6}$

Figure 6. DC voltage measurements, current calculations and threshold voltage estimations for p-channel device

- It has been observed that the values are very close to each other when the same applications are performed on different pins of Mos.

2.1.3 Measuring n Channel Device Parameters

By selecting pin #4 as the source terminal (a NMOS device), the circuit shown in Figure 7 was assembled.

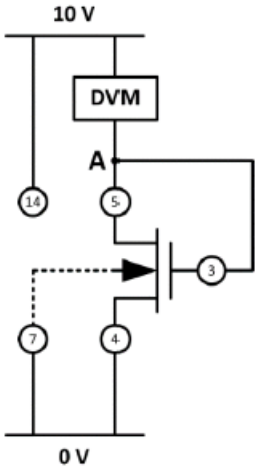
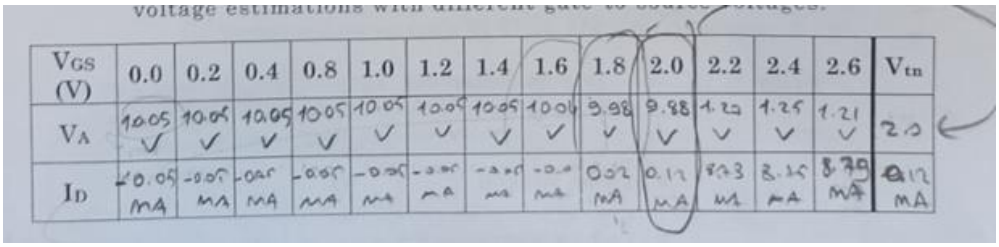


Figure 7. Setup to measure Vtn. Pin numbers given are in accordance with part a).

a) Measured VA and estimated Vtn.

Pin#14 → 10V
Pin#7 and Pin#4 → GND Pin#5 → open
Pin #3 and Pin#5 → connected

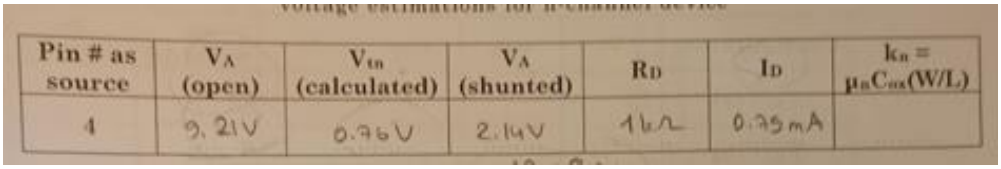
b) Node A shunted to VDD with a 1 kΩ resistor .The gate drain is disconnected and the gate is connected to an adjustable voltage source. The gate voltage was adjusted so that the VGS would pass over the values given in the table below. VA was noted and ID calculated. Vtn was estimated as the voltage allowing an ID > 10 µA for this technology.



V_{GS} (V)	0.0	0.2	0.4	0.8	1.0	1.2	1.4	1.6	1.8	2.0	2.2	2.4	2.6	V_{tn}
V_A	10.05 V	10.05 V	10.05 V	10.05 V	10.05 V	10.05 V	10.05 V	10.05 V	9.98 V	9.88 V	1.23 V	1.25 V	1.21 V	2.0
I_D	0.05 mA	0.05 mA	0.05 mA	0.05 mA	0.05 mA	0.05 mA	0.05 mA	0.05 mA	0.02 mA	0.12 µA	8.23 µA	8.25 µA	8.29 µA	0.12 mA

Figure 8. DC voltage measurements, current calculations and threshold voltage estimations with different gate-to-source voltages

c) The configuration in Figure 7 is returned. Node A is shunted with a 1 kΩ resistor. A similar resistor adjustment method was used as we did in 2.1.2. Measured VA and applied resistance. kn was calculated using a similar way to the one we used to calculate kp.



Pin # as source	V_A (open)	V_{tn} (calculated)	V_A (shunted)	R_D	I_D	$k_n = \mu_n C_{ox}(W/L)$
4	9.21V	0.76V	2.14V	1kΩ	0.39mA	

Figure 9. DC voltage measurements, current calculations and threshold voltage estimations for n-channel device

2.2. Amplifier Function

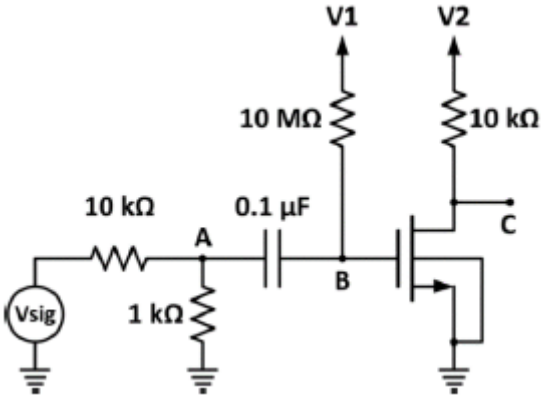


Figure 10. Simplistic amplifier topology.

Figure 10 shows a common-source amplifier using n-channel D-MOSFET. Since the source terminal is common to the input and output terminals, the circuit is called common source amplifier.

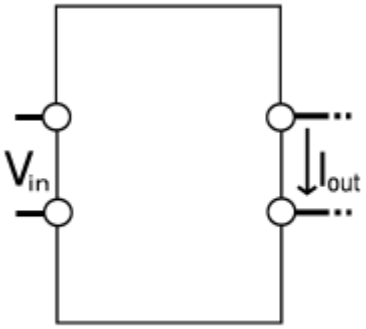
2.2.1. Transconductance gm

Transconductance is the property of certain electronic components. Conductance is the reciprocal of resistance; transconductance is the ratio of the current change at the output port to the voltage change at the input port. It is written as gm. For direct current, transconductance is defined as follows:

$$g_m = \frac{\Delta I_{\text{out}}}{\Delta V_{\text{in}}}$$

For small signal alternating current, the definition is simpler:

$$g_m = \frac{i_{\text{out}}}{v_{\text{in}}}$$



A transconductance amplifier (gm amplifier) puts out a current proportional to its input voltage. In network analysis, the transconductance amplifier is defined as a voltage controlled current source (VCCS). It is common to see these amplifiers installed in a cascode configuration, which improves the frequency response.

2.2.2. Signal Distortion

For a signal amplifier to operate correctly without any distortion to the output signal, it requires some form of DC Bias on its Base or Gate terminal. A DC bias is required so that the amplifier can amplify the input signal over its entire cycle with the bias "Q-point" set as near to the middle of the load line as possible.

The bias Q-point setting will give us a "Class-A" type amplification configuration with the most common arrangement being the "Common Emitter" for Bipolar transistors or the "Common Source" configuration for unipolar FET transistors.

The Power, Voltage or Current Gain, (amplification) provided by the amplifier is the ratio of the peak output value to its peak input value (Output ÷ Input).

However, if incorrectly design our amplifier circuit and set the biasing Q-point at the wrong position on the load line or apply too large an input signal to the amplifier, the resultant output signal may not be an exact reproduction of the original input signal waveform. In other words the amplifier will suffer from what is commonly called Amplifier Distortion.

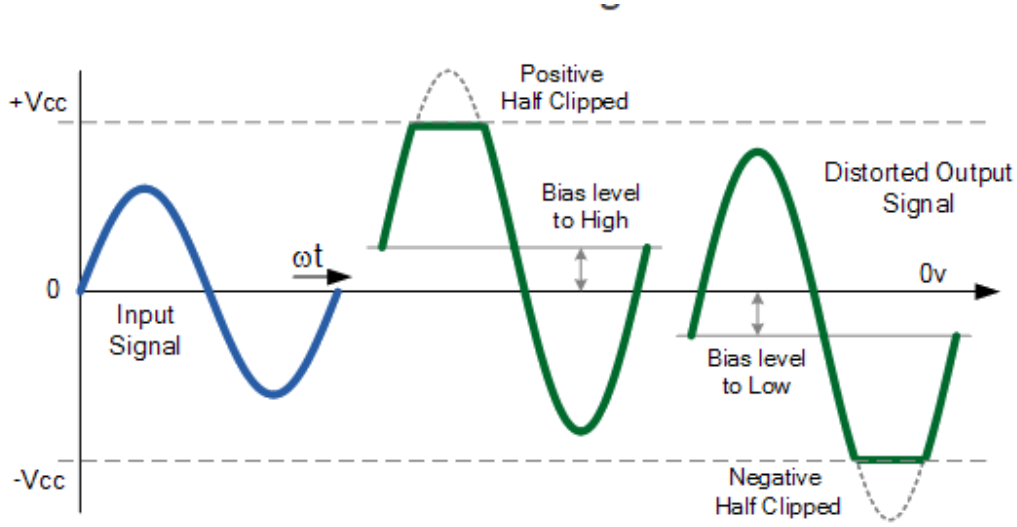


Figure 11. Transistor amplifier distortion example graphic

3. Conclusion

In this experiment MOS transistors is used. We used concepts such as NMOS and PMOS model, transconductance, transistor parameters.

It has been observed that there are multiple pmos and nmos models in the transistor used and there are small differences when measured separately in these models. It has been examined that the pins we use for these models may differ. It is understood how to comment on the concepts of drain and source. learned how these concepts change and work for PMOS and NMOS.

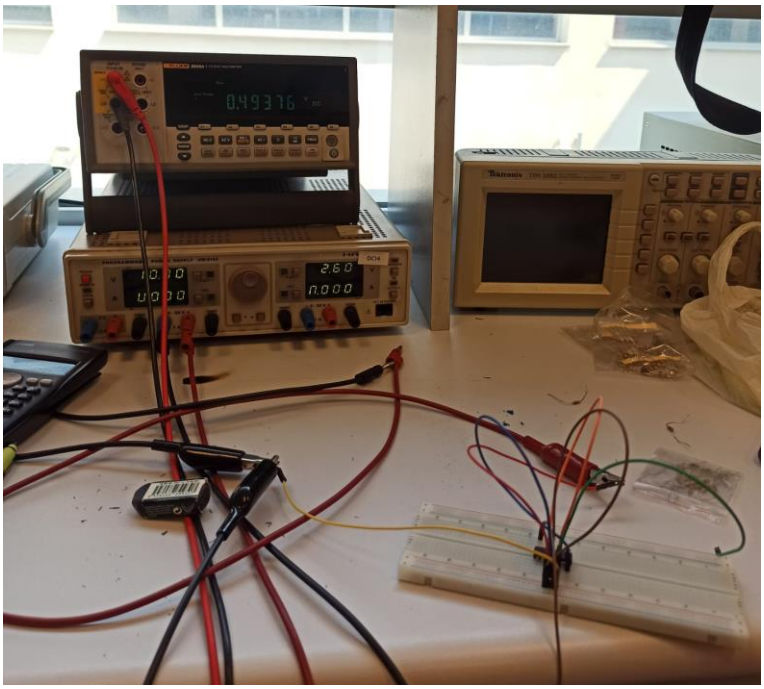


Figure 12. Transistor circuit measuring area

For this experiment, it was simulated with multisim and the results could not be compared. This is due to the lack of suitable MOS transistors in the simulation.

It is thought that the measurements made during the experiment are correct by using the theoretical information. The formulas used are specified in the report.

4. References

[1] https://diyot.net/mosfet/

[2] https://anysilicon.com/introduction-to-nmos-and-pmos-transistors/

[3] https://www.electronics-tutorials.ws/amplifier/amp_4.html

[4] https://electronicspost.com/mosfet-amplifier/