Advanced Design Features Proposal

1Hz CPU

The following list is Advanced Design Features we plan on implementing based on the priority that we want to implement them in.

1. SuperScalar Design Multi-Issue [15 points]
    a. For our Advanced design feature we will be mostly focused on turning our pipelined cpu into a superscalar design. We will initially focus on making it a two-wide decode and two-issue design. This will make up the brunt of our advanced design features. We plan on planning out the datapath again first for this design before going straight to coding.
2. Zbb group of the BitManip extension (B) for RISC-V [??? points]
    a. We are very interested in using more bit manipulated focused instructions. Particularly because they can be used to replace many instructions through 1 instruction.
3. RISC-V M Extension [3 Points]
    a. We plan on also implementing a basic multiplier design for some mild performance benefits.

While implementing these designs. We of course will need a way to test them against our original basic pipeline design. We can benchmark designs with or without the advanced design features. We will be using performance counters as mentioned in the MP4 documentation to hopefully document any increases in performance.