

# Checkpoint 1 Progress Report/RoadMap

1-Hz CPU

For this checkpoint we predominantly focused on creating the simple BASIC RV32i pipelined datapath. Initially we started with creating the datapath for the initial checkpoint. We met together and worked together to create a 5 stage datapath. Afterwards we split up the work and began working on the design in system verilog. For our initial design we decided to lay our superscalar ambitions to the side and wait until the advanced design features checkpoint to implement superscalar. For this checkpoint Suchir and Victor worked on the decoder and interface. Mesa worked on the regfile, ALU and design of Arbiter. Victor worked on the Data Hazard Unit Design and Data Forwarding Unit Design as well as restructuring the datapath according to our TA's suggestion. Suchir also worked on creating other modules for the datapath. We have most of the datapath working but it is not done 100% yet. This is due to us starting late because of prior commitments. For future checkpoints we have all agreed to start much earlier since starting later in the week significantly hindered our progress. Since we did not finish our entire datapath we are also planning on working hard and have plans to meet together to at least turn it in late to recover the 8 points for turning it in. We did test some of our units by feeding in certain inputs and making sure that the correct results were displayed like for our ALU, Regfile and Decode units. For Checkpoint 2 we are planning on finishing the implementation early so that we can have ample time to test for bugs as well as verify the functionality of our units.

In terms of roadmap the entire team will be meeting over the next few days to finish the initial datapath. As well as to get started working early on objectives for checkpoint two. Victor will work on Data Forwarding and Hazard Detection. Suchir will work on the branch predictor. Mesa will work on integrating the L1 Cache as well as the Arbiter. In addition the group will come together in the 2nd week of checkpoint two in order to work on creating a paper design for the advanced features that we plan to come up with. We hope that our checkpoint 2 will be a success. A problem that we may run into is integrating these new modules into our datapath. Successful verification of each individual module before integrating it into the datapath will allow for us to more easily integrate the checkpoint 2 modules.