# Checkpoint 2 Progress Report/RoadMap

1hz cpu

For this checkpoint we began by fixing our original basic RV32i pipelined datapath. During the night that the first checkpoint was due, we still had some issues to debug. We originally were going to let the autograder run and check our code but we had some issues setting up the RVFI monitor. Instead we opted to demo to our TA directly by showing the correct register values after executing the checkpoint 1 assembly file. After this initial delay we got to work on implementing the next parts of our design for checkpoint 2. Initially we tried to rewrite a lot of the code since we felt it would have made it easier to work with for future checkpoints. We also had a lot of the framework that we needed as well to integrate the units for checkpoint 2. Unfortunately at the time of writing this, we are still debugging our units and hope to get them done by the end of the 11th. If not, then we will demo with our TA at a later time. For this checkpoint we implemented Stalling, Forwarding, the arbiter, integration of the data cache/instruction cache, and data hazard detection unit. We all split up the work based on which features we were drawn to the most. We also will make some simple testbenches to verify the units before integrating them with our CPU.

Road map wise we are looking forward to implementing our advanced design features for the next checkpoint. We were a bit slow on this checkpoint again due to our group mates having many conflicts with other classes and midterms. However for the next 2 weeks, the 3 of us are relatively free and plan on putting most of our effort into our advanced design features. We plan to also recompile RVFI monitor as well to support our superscalar design to change some of the monitored signals. We will be doing a lot of reading and planning on how we want to set up our superscalar design before coding it in systemverilog. We also plan to support another advanced feature. We want to implement the Zbb group of the BitManip extension for RISC-V.