BLG 212 Final

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1-) $f_s = 5760$ Hz => Baud rate nyquist frekansından yüksek olmalı.

$f_B \geq 2f_s = 11520$

$f_{Bmax} \rightarrow$ TH = FDh => 10000 baudrate ($f_{XTAL} = 12$ MHz)

Timer 1 seri port için

Timer 0 paralel port için kullanılsın

Timer 1 → mod 2
Timer 0 → mod 1
} TMOD = 21h

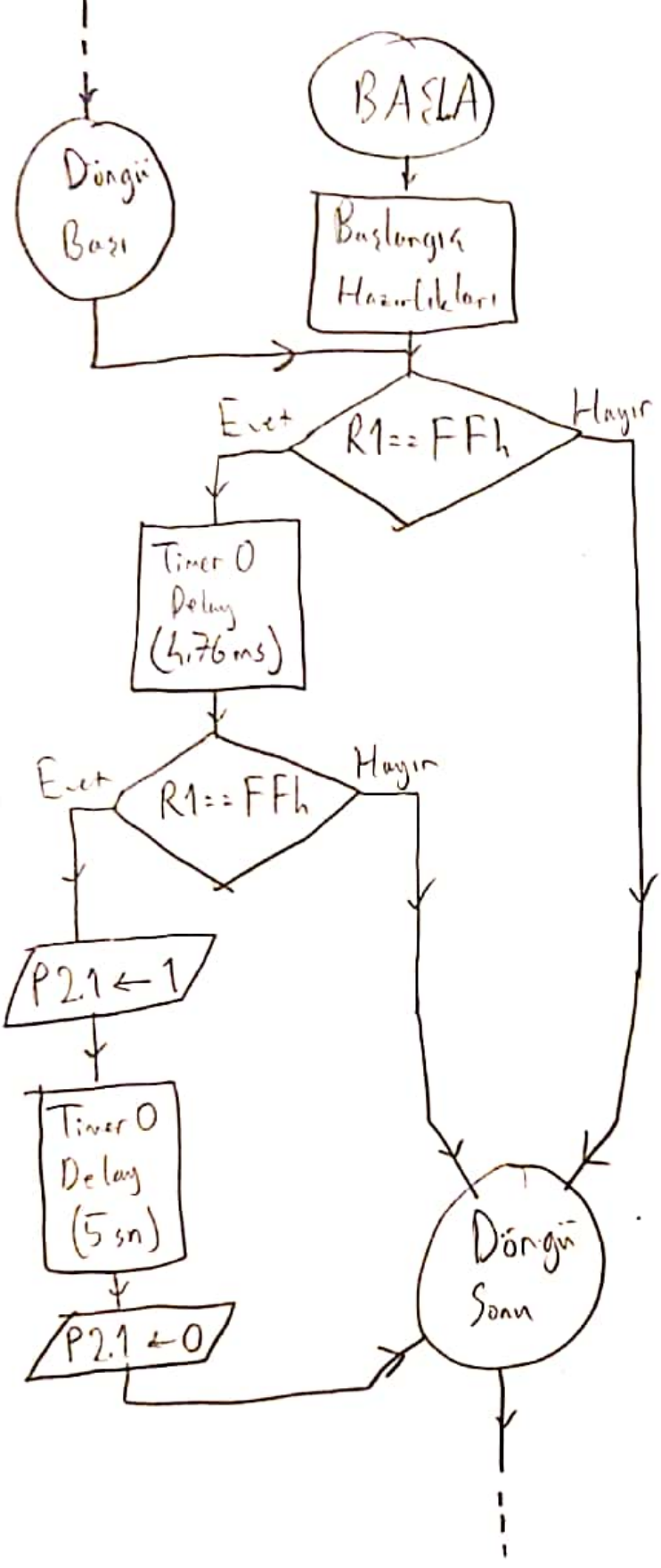
SCON = 50h → seri mod 1 , seri interrupt → IE = 90h (EA ve Seri interrupt → 1)

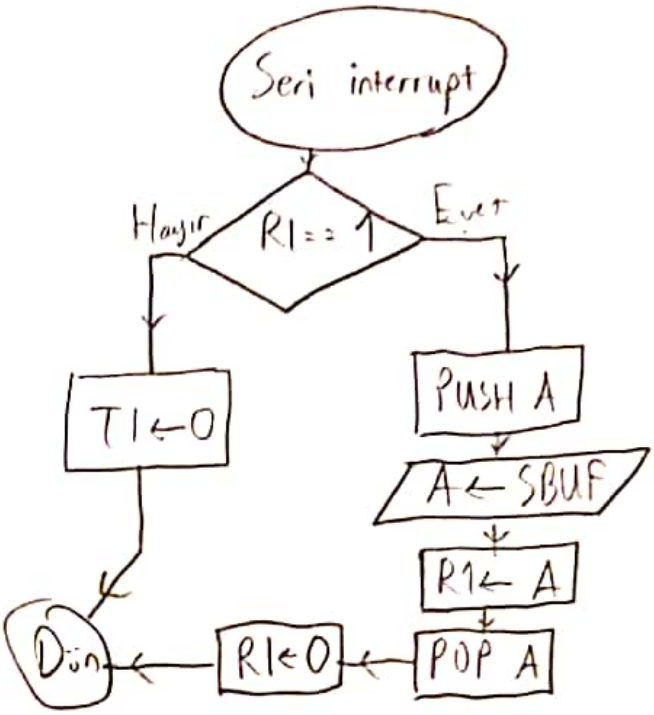
5 sn delay (Buzzer için) → TH0 = 3Ch
TL0 = AFh

$f_0 = 210$ Hz

$T_0 = \frac{1}{210} \cong 4{,}76$ ms

Buzzer P2.1'de.



Delay:

4,76 ms => $f_{XTAL}$ = 12 MHz =>

4,76 ms = 4760 mc. → 65535 - 4760 = 60775 = ED67h

THO = 0EDh

TLO = 67h

5 sn => $5 \cdot 10^6$ mc = 50000.100

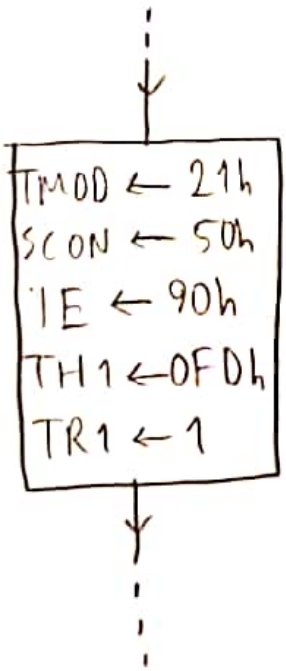
R2 ← 100, 100 kere 50 ms Delay = 5 sn

65535 - 50000 = 15535 = 3CAF

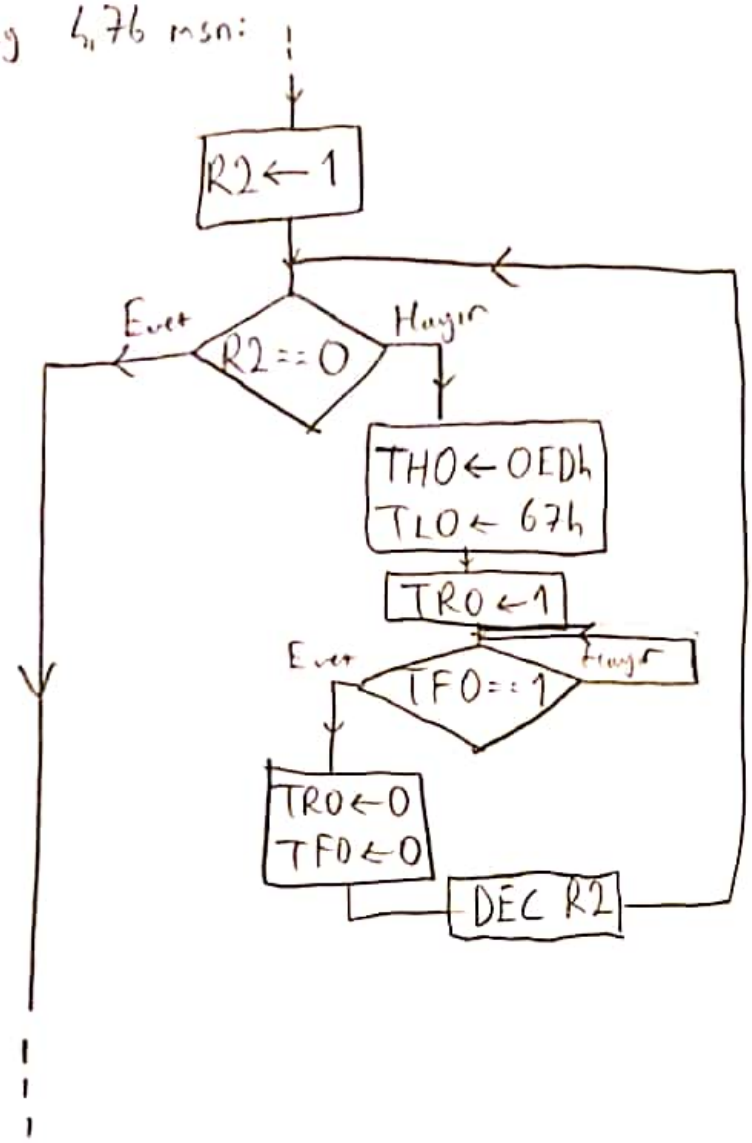
THO = 3Ch

TLO = 0AFh

Başlangıç hazırlıkları:



Delay 4,76 msn:




Delay 5 sn:

4,76 msn ile aynı yapıda,

yalnızca R2 ← 100

TH0 ← 3Ch

TL0 ← 0AFh

```
ORG 0000H
LJMP MAIN

ORG 23H
LJMP SERIAL

ORG 30H
MAIN: MOV TMOD, #21H
      MOV SCON, #50H
      MOV IE, #90H
      MOV TH1, #0FDH
      SETB TR1
      MOV R1, #0
LOOP: CJNE R1, #0FFH, NOT_FREQ
      ACALL DELAY1.
      CJNE R1, #0FFH, NOT_FREQ
      SETB P2.1
      ACALL DELAY2
      CLR P2.1
NOT_FREQ: SJMP LOOP
SERIAL: JNB RI, TRANS
        PUSH A
        MOV A, SBUF
        MOV R1, A
        POP A
        CLR RI
TRANS:  CLR TI
        RETI
```

```
DELAY1: MOV R2, #1
DELSTART1: CJNE R2, #0, DELAY_LOOP1
           RET
DELAY_LOOP1:
           MOV TH0, #0EDH
           MOV TL0, #67H
           SETB TR0
DLOOP1:    JNB TF0, DLOOP1
           CLR TR0
           CLR TF0
           DEC R2
           SJMP DELSTART1

DELAY2: MOV R2, #100
DELSTART2: CJNE R2, #0, DELAY_LOOP2:
           RET
DELAY_LOOP2:
           MOV TH0, #3CH
           MOV TL0, #0AFH
           SETB TR0
DLOOP2:    JNB TF0, DLOOP2
           CLR TR0
           CLR TF0
           DEC R2
           SJMP DELSTART2
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