1. Find a race-free assignment for the four-state machine as given in the table below: Also, if needed, draw the augmented state table.

Present state	Next State			
	$x_1 x_2$			
	00	01	11	10
A	Ⓐ	Ⓐ	D	C
B	Ⓑ	A	Ⓑ	C
C	A	Ⓒ	D	Ⓒ
D	Ⓓ	C	Ⓓ	Ⓓ

1. Design a mod-8 asynchronous counter with verilog and show the timing diagram.