CS221-Digital Design
Assignment No: 8
Due date for submission: 22 Nov 2020

Submission procedure: Submit/upload zipped/compressed folder (with Roll No as name of the folder) containing scan copy of solution, HDL code, test benches, readme files on to CS221 MS Team assignment upload.

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Design a hardware system, that accepts two inputs (a) start signal (b) a 32-bit number (N), and produce outputs (a) done, (b) a 32-bit number output which is sum of all the even numbers up to N excluding the numbers divisible by 8.

- Part I (Submit scan copy of hand written solution)
    - Design ASM chart for the same problem
    - Infer the required data path components for the problem.
    - Implement the required ASM controller for the same.

- Part II (Submit HDL code with test benches)
    - Write Verilog HDL code to implement the above hardware system. You are allowed to use in built 32-bit adder and 32-bit comparator from the HDL library.