CS221-Digital Design
Assignment No: 7
Due date for submission : 14 Nov 2020

Submission procedure: Submit/upload zipped/compressed folder (with RollNo as name of the folder) containing your HDL code, testbenches, readme files on to CS221 MS Team assignment upload.

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Design a sequence detector that detects 010 or 110. A stream of input X enters into the system continuously, the system alert/assert after each 3-bit input sequence if it consists of 110 or 010. The same example is explained in Lect 30/31 of the CS221 course.

Design Moore FSM for this problem and write Verilog HDL code for the sequence detector and simulate the same using proper test benches. (As described in verilog HDL lecture Lecture 7, 8 and 9 of CS221 course)

- Implement the sequence detector in high level verilog HDL with if-else and case constucts.

- Implement the sequence detector in low level verilog HDL using FSM implementation methodology (State encoding, NS logic, Z logic) as described in the class. In this case, use FF to store states, combination circuit for NS and Z logic.

Test both of your designs using this test input: “111 010 010 110 010 000 111 010 001 100 110 101 010 110 101”.