Lastname, Name:_____
ID:_____

Elec-204: Digital Systems Design

Final Exam [1]

June 12, 2010

Duration: 120 min

Q	Pts	Score
1	25	
2	10	
3	15	
4	20	
5	10	
6	20	
Total	100	

[1] This is a closed-book and closed-notes exam. Please read each question carefully, and give your solution in a formal and clean way. It's the best way to get partial credits. *GOOD LUCK!*

1. **[25 pts]** Given Boolean function,

$$F(X, Y, Z, W) = \Pi M(3, 4, 11, 12)$$

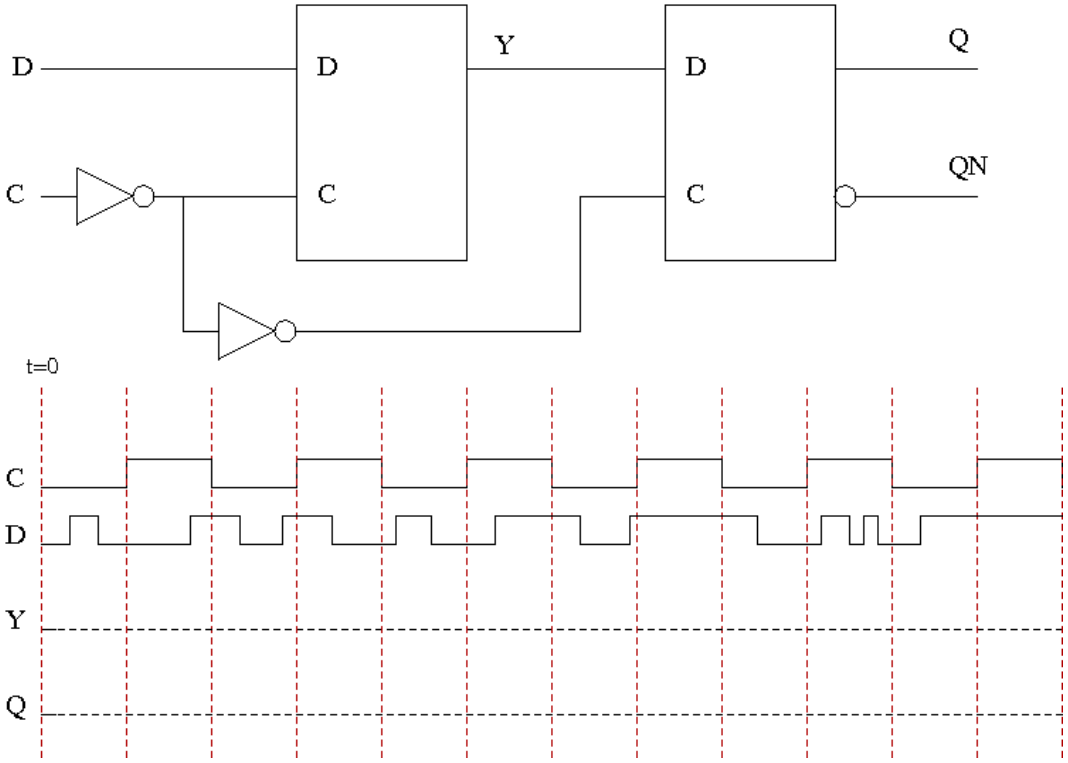
(a) Find and list all prime implicants of the F function.

(b) Find and list all essential prime implicants of the F function.

(c) Find the minimal two level NAND gate implementation of the F function. Find the gate input cost.

(d) Find the minimal two level NOR gate implementation of the F function. Find the gate input cost.

2. [**10 pts**] Perform the timing analysis of the following master-slave flip-flop architecture by ploting the state variables, Y and Q, along with the given clock. You can assume no observable propagation delay in your plots. Note that at time $t = 0$, both Y and Q state variables are at LOW level. (Be careful and plot clean, no partial credits!)



3. **[15 pts]** A sequential circuit with three D-type flip-flops $Y_1Y_2Y_3$, input X and output Z is defined with the following input/output functions:

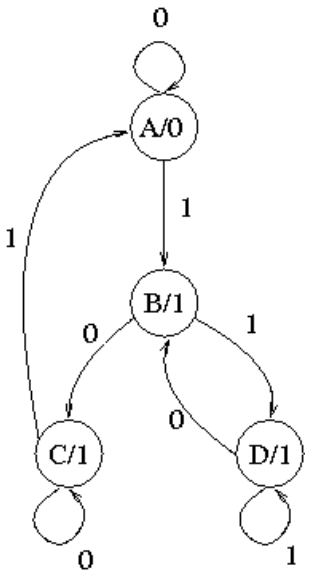
$$
\begin{aligned}
D_1 &= X\bar{Y}_3 + \bar{X}\bar{Y}_1Y_3 \\
D_2 &= \bar{X}(\bar{Y}_3 + Y_2) + X\bar{Y}_2Y_3 \\
D_3 &= X\bar{Y}_3 + \bar{Y}_2Y_3 \\
Z &= Y_3
\end{aligned}
$$

(a) Find the state table for the circuit and replace the state codes with single letter state identifiers. Note that, states 100 and 111 were unused in the design.

(b) Check for, identify and combine equivalent states.

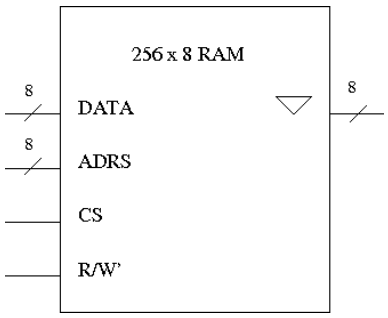
4. **[20 pts]** A synchronous sequential circuit with input X and output Z is described with the following state transtion diagram.

   (a) Extract the state table by making a state assingment such that output is one of the state variables.



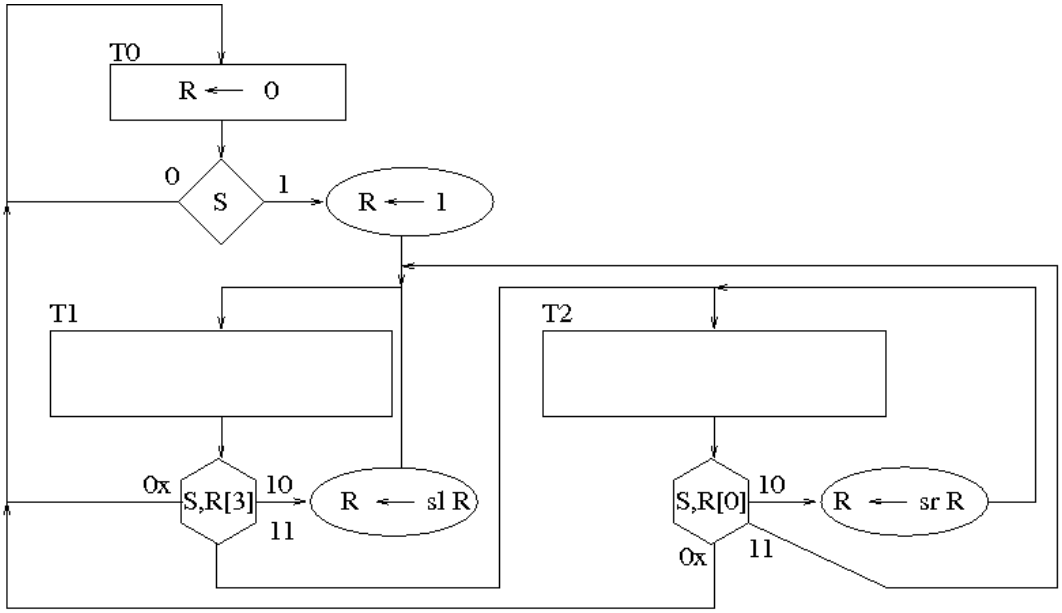
   (b) Design the synchronous sequential circuit using set-dominant master-slave flip flops. A set dominant master-slave flip flop has set (S) and reset (R) inputs. It differs from a conventional master-slave flip flop by setting output state with $S = 1$ and $R = 1$ inputs.

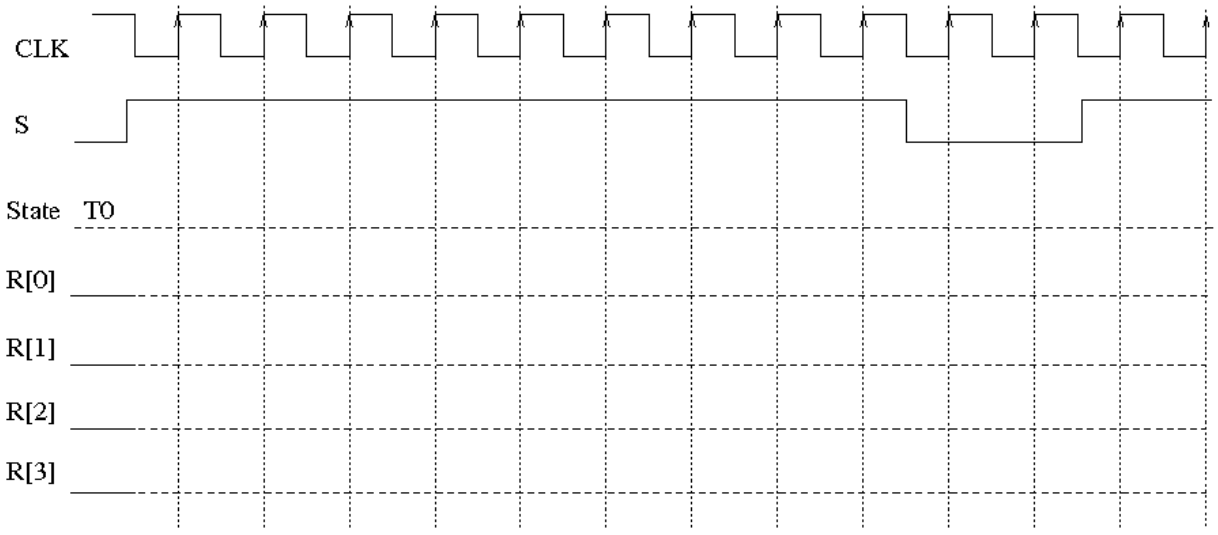
5. [**10 pts**] Design a 1024x16 RAM using the following 256x8 RAM blocks and neccessary combinational circuit. Note that, 256x8 RAM block has 8 bit data (DATA), 8 bit address (ADRS), chip select (CS), read/write ($R/\bar{W}$) inputs and a three-state output bus.



6. **[20 pts]** In the following ASM chart, S is an input signal and R is a 4-bit shift register. The shift left and shift right instructions take zero from the serial inputs. Considering this ASM chart answer the following questions,

   (a) Given the system's clock and S input in the following figure, plot the content of register R and write the present state for each clock cycle **on the figure**. Note that, at the first clock cycle R was reset to all logic zeros. (Be careful and plot clean, no partial credits!)





(b) Design the control unit of this ASM chart with minimum number of (any type) flip-flips and combinational circuit elements.