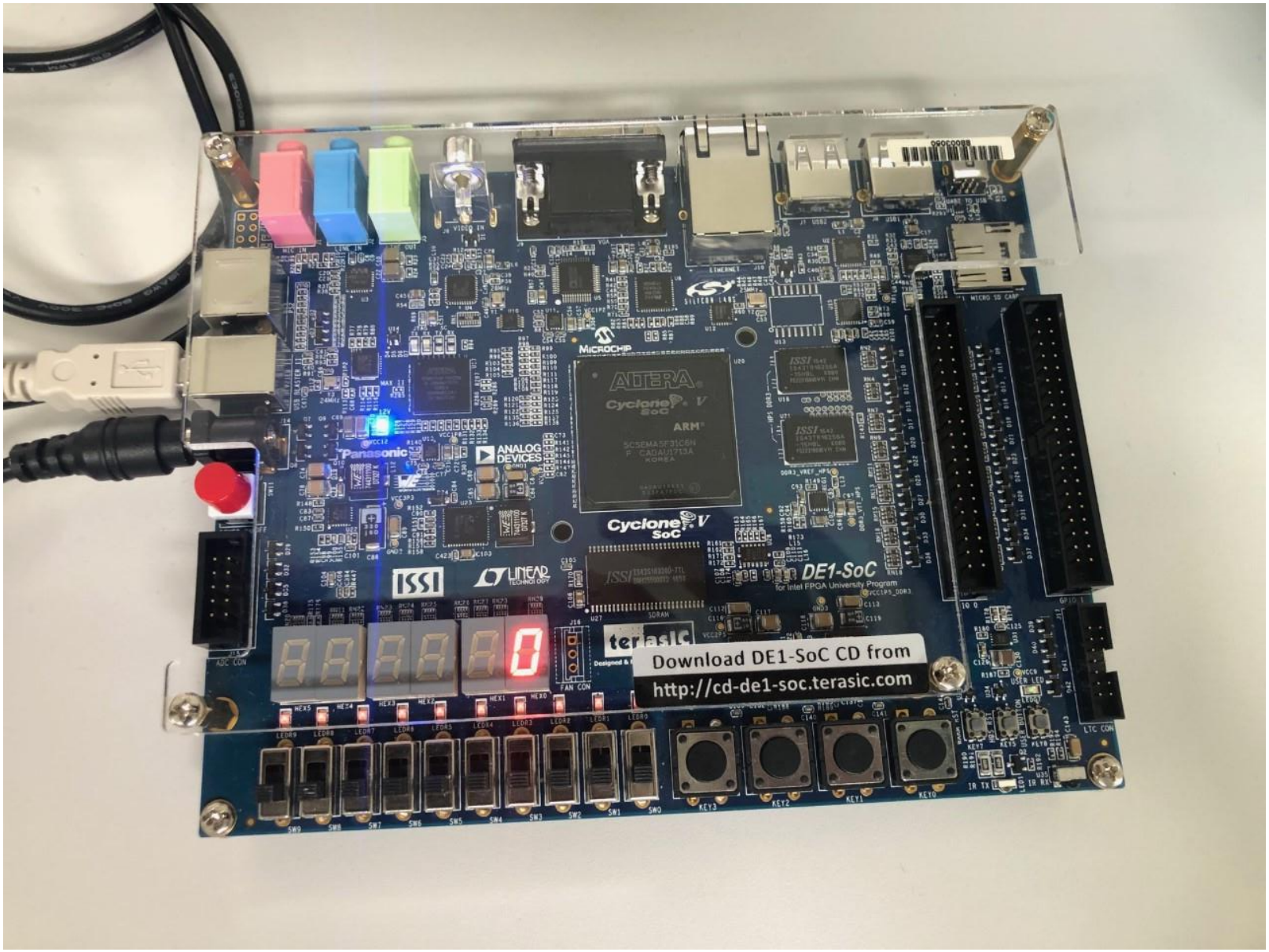
X5 LAB – 19/11/2020

Does the 7-segment display correctly show the values of the switches as a hexadecimal number?

Yes it does

```
21
22 module sevenseg(output logic [6:0] data,
23                  input logic [3:0] address);
24
25  always_comb
26    unique casez (address)
27      4'b0000 : data = 7'b1000000;
28      4'b0001 : data = 7'b1111001;
29      4'b0010 : data = 7'b0100100;
30      4'b0011 : data = 7'b0110000;
31      4'b0100 : data = 7'b0011001;
32      4'b0101 : data = 7'b0010010;
33      4'b0110 : data = 7'b0000010;
34      4'b0111 : data = 7'b1111000;
35      4'b1000 : data = 7'b0000000;
36      4'b1001 : data = 7'b0010000;
37      4'b1010 : data = 7'b0001000;
38      4'b1011 : data = 7'b0000011;
39      4'b1100 : data = 7'b0100110;
40      4'b1101 : data = 7'b0100001;
41      4'b1110 : data = 7'b0000110;
42      4'b1111 : data = 7'b0001110;
43      default : data = 7'b1111111;
44    endcase
45  endmodule
46
```

```
37 # -------------------------------------------------------------------------- #
38
39
40 set_global_assignment -name FAMILY "Cyclone V"
41 set_global_assignment -name DEVICE 5CSEMA5F31C6
42 set_global_assignment -name TOP_LEVEL_ENTITY sevenseg
43 set_global_assignment -name ORIGINAL_QUARTUS_VERSION 16.1.2
44 set_global_assignment -name PROJECT_CREATION_TIME_DATE "15:57:28  NOVEMBER 19, 2020"
45 set_global_assignment -name LAST_QUARTUS_VERSION "16.1.2 Standard Edition"
46 set_global_assignment -name SYSTEMVERILOG_FILE sevenseg.sv
47 set_global_assignment -name PROJECT_OUTPUT_DIRECTORY output_files
48 set_global_assignment -name MIN_CORE_JUNCTION_TEMP 0
49 set_global_assignment -name MAX_CORE_JUNCTION_TEMP 85
50 set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 256
51 set_global_assignment -name PARTITION_NETLIST_TYPE SOURCE -section_id Top
52 set_global_assignment -name PARTITION_FITTER_PRESERVATION_LEVEL PLACEMENT_AND_ROUTING -section_id Top
53 set_global_assignment -name PARTITION_COLOR 16764057 -section_id Top
54 set_location_assignment PIN_AB12 -to address[0]
55 set_location_assignment PIN_AC12 -to address[1]
56 set_location_assignment PIN_AF9 -to address[2]
57 set_location_assignment PIN_AF10 -to address[3]
58 set_location_assignment PIN_AE26 -to data[0]
59 set_location_assignment PIN_AE27 -to data[1]
60 set_location_assignment PIN_AE28 -to data[2]
61 set_location_assignment PIN_AG27 -to data[3]
62 set_location_assignment PIN_AF28 -to data[4]
63 set_location_assignment PIN_AG28 -to data[5]
64 set_location_assignment PIN_AH28 -to data[6]
65 set_instance_assignment -name PARTITION_HIERARCHY root_partition -to | -section_id Top
66 set_global_assignment -name CDF_FILE output_files/Chain1.cdf
```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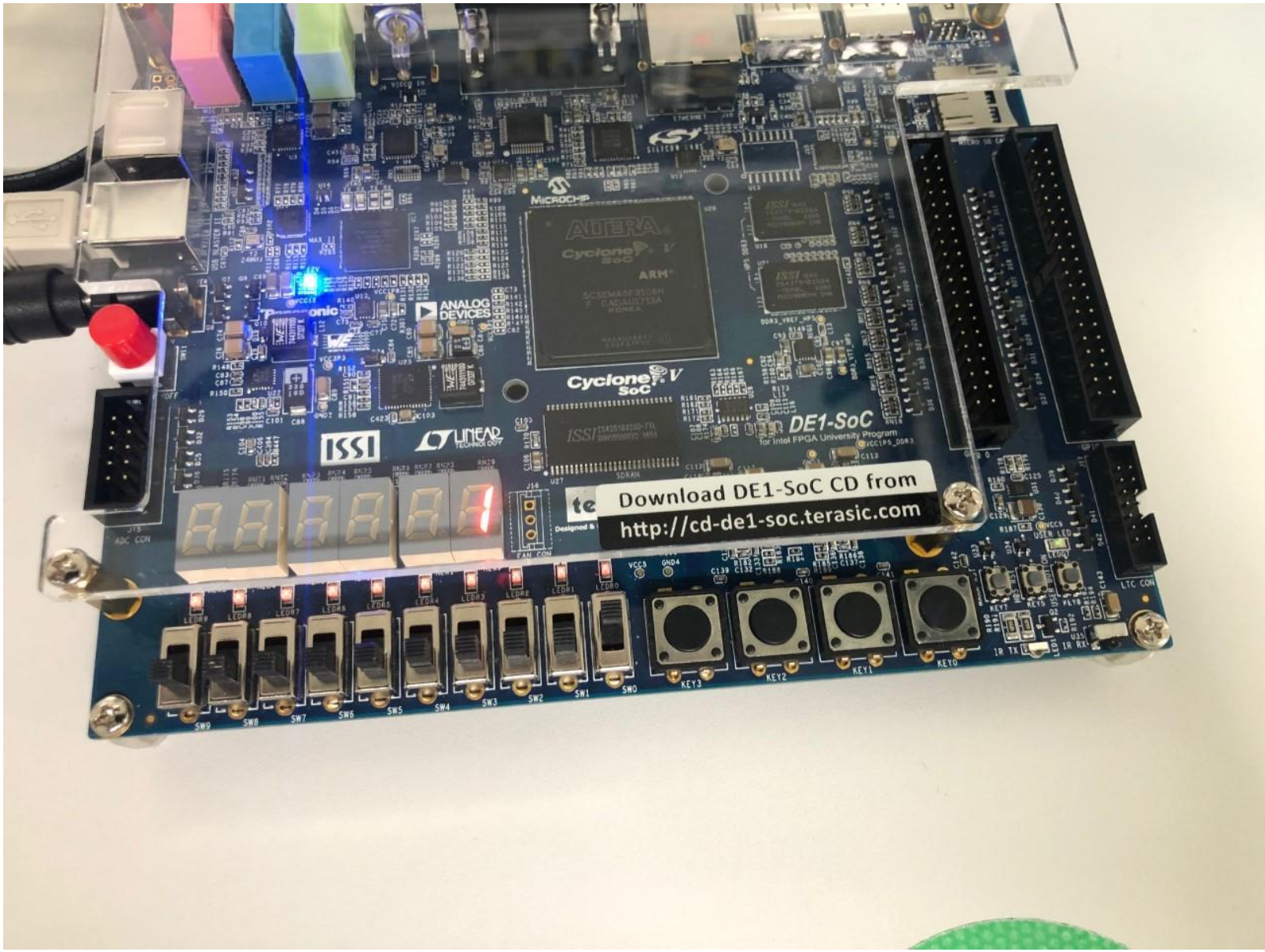
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SW8
SW7
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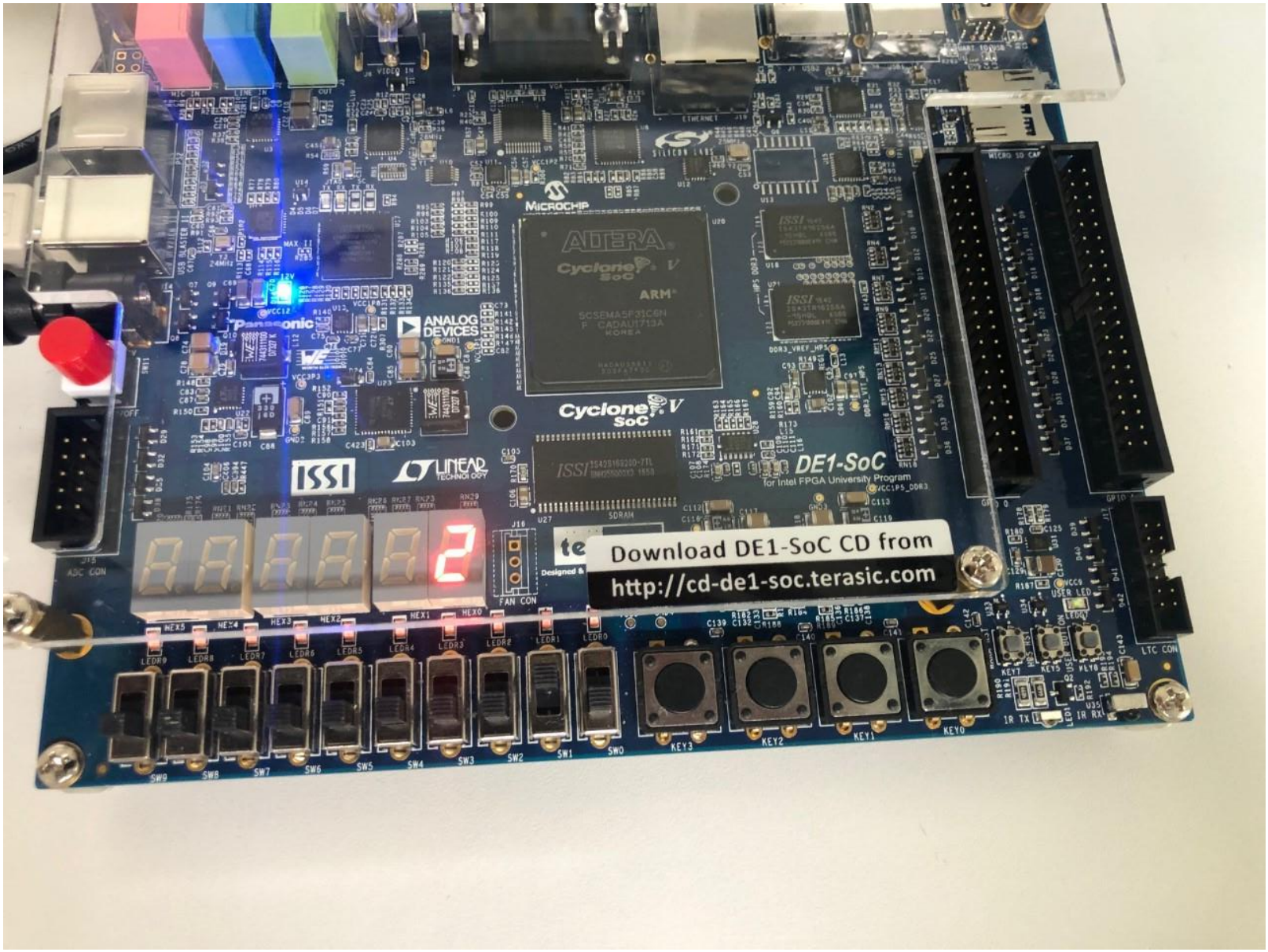
SW5
SW4
SW3
SW2
SW1
SW0
KEY3
KEY2
KEY1
KEY0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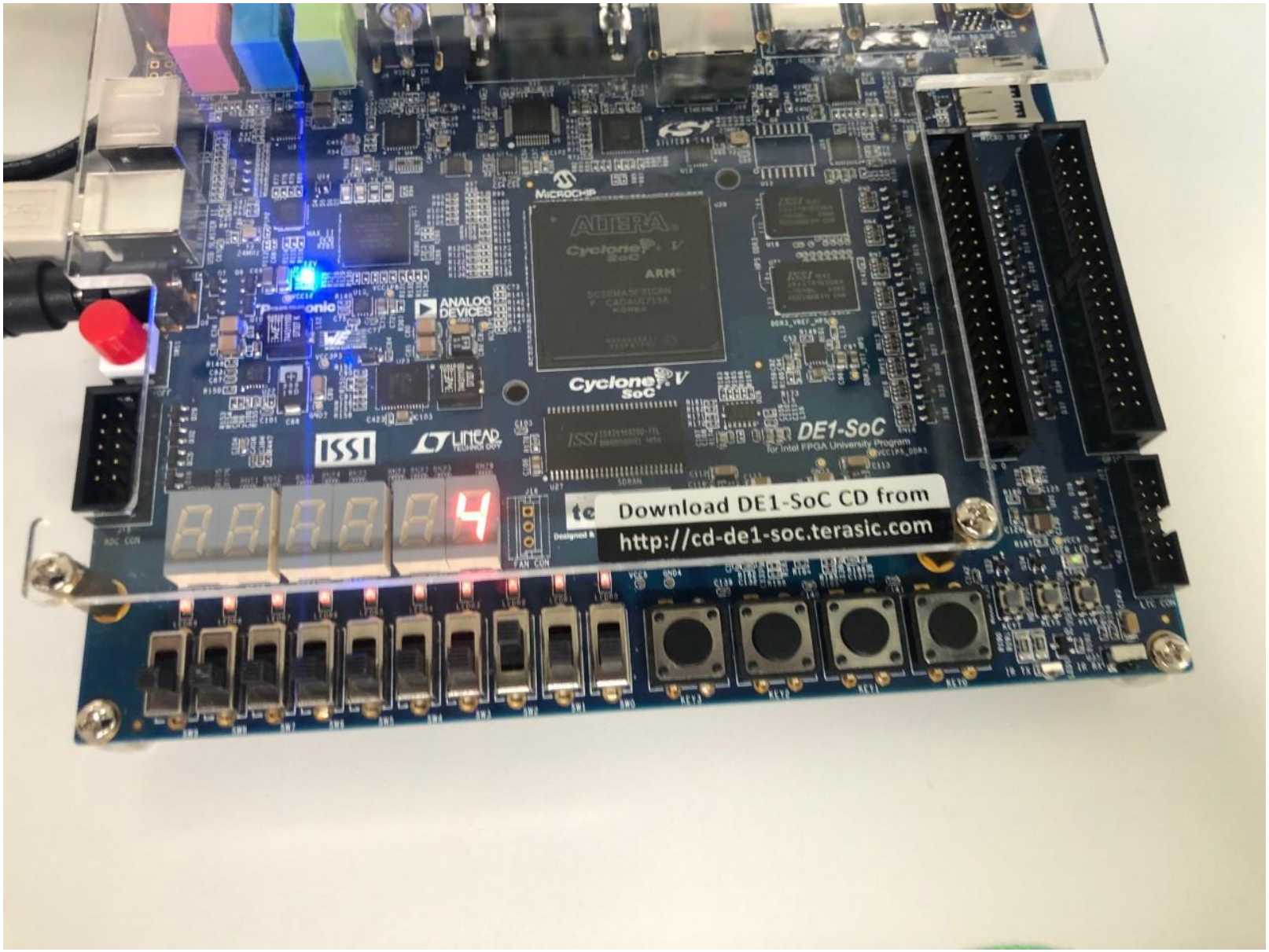
LEDR8
LEDR7
LEDR6
LEDR5
LEDR4
LEDR3
LEDR2
LEDR1
LEDR0
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
KEY3
KEY2
KEY1
KEY0
FAN CON
A3C CON
LTC CON
USER LED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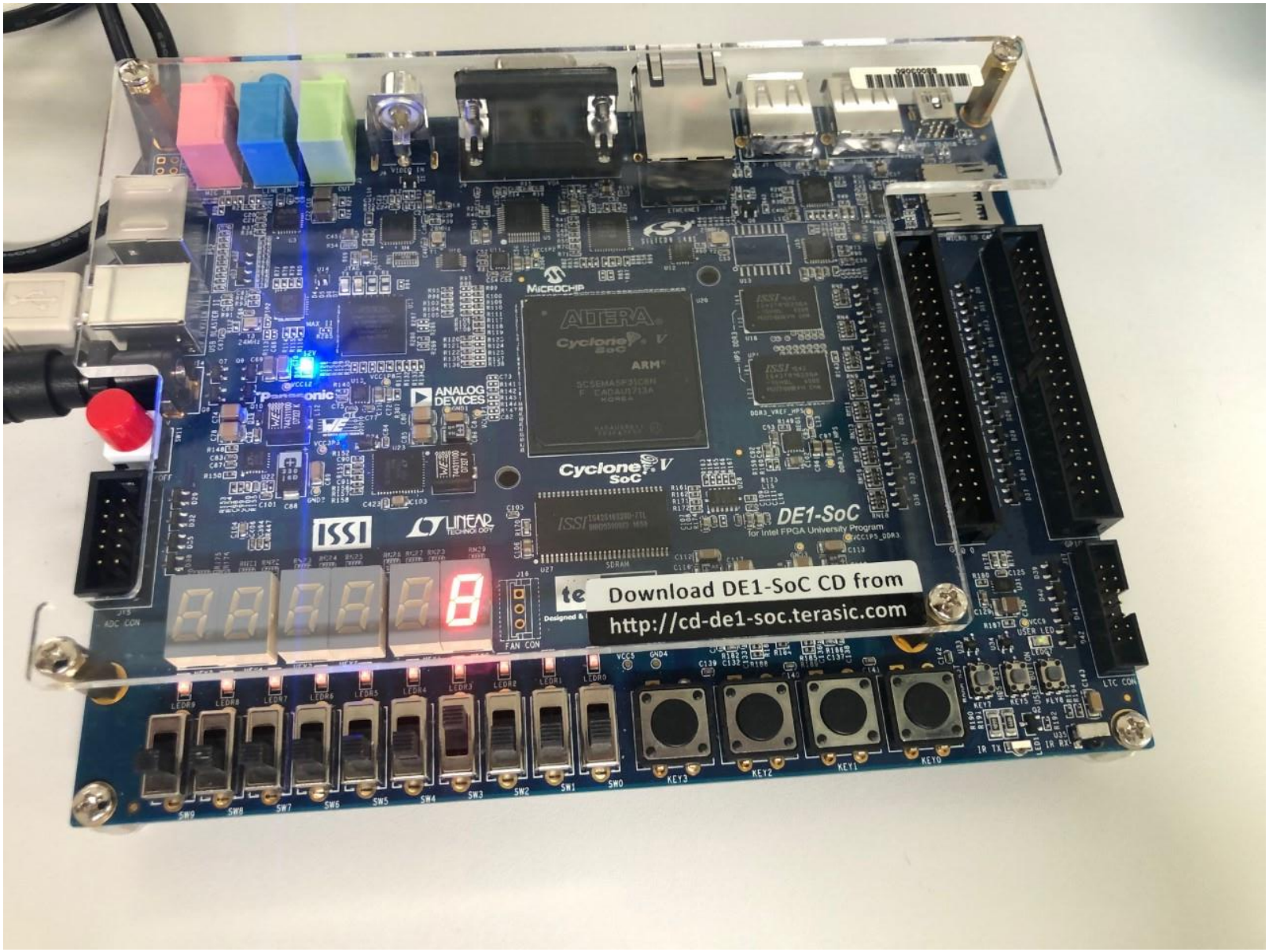
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ADC CON
LTC CON
USER LED
IR TX
IR RX
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
KEY3
KEY2
KEY1
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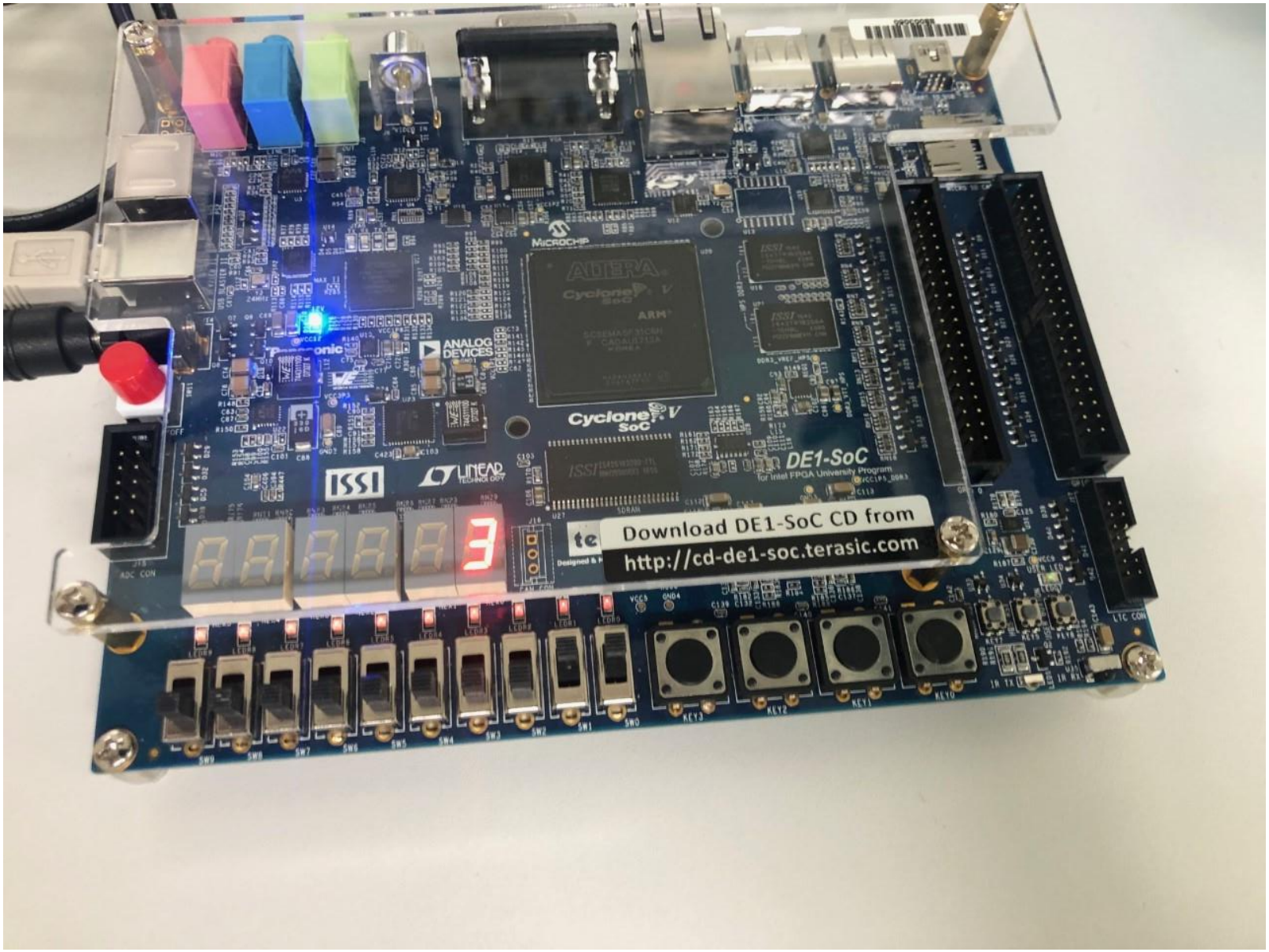
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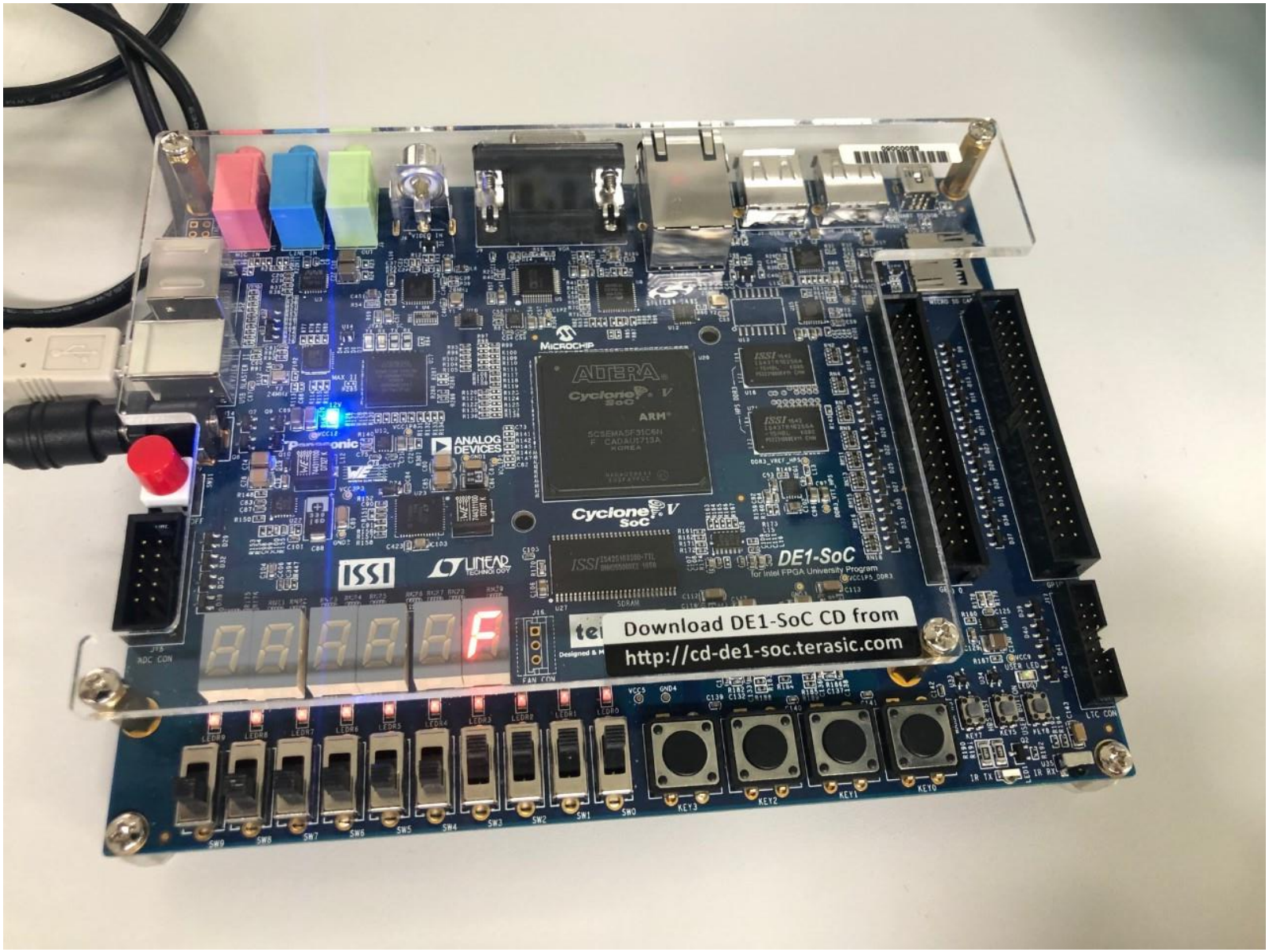
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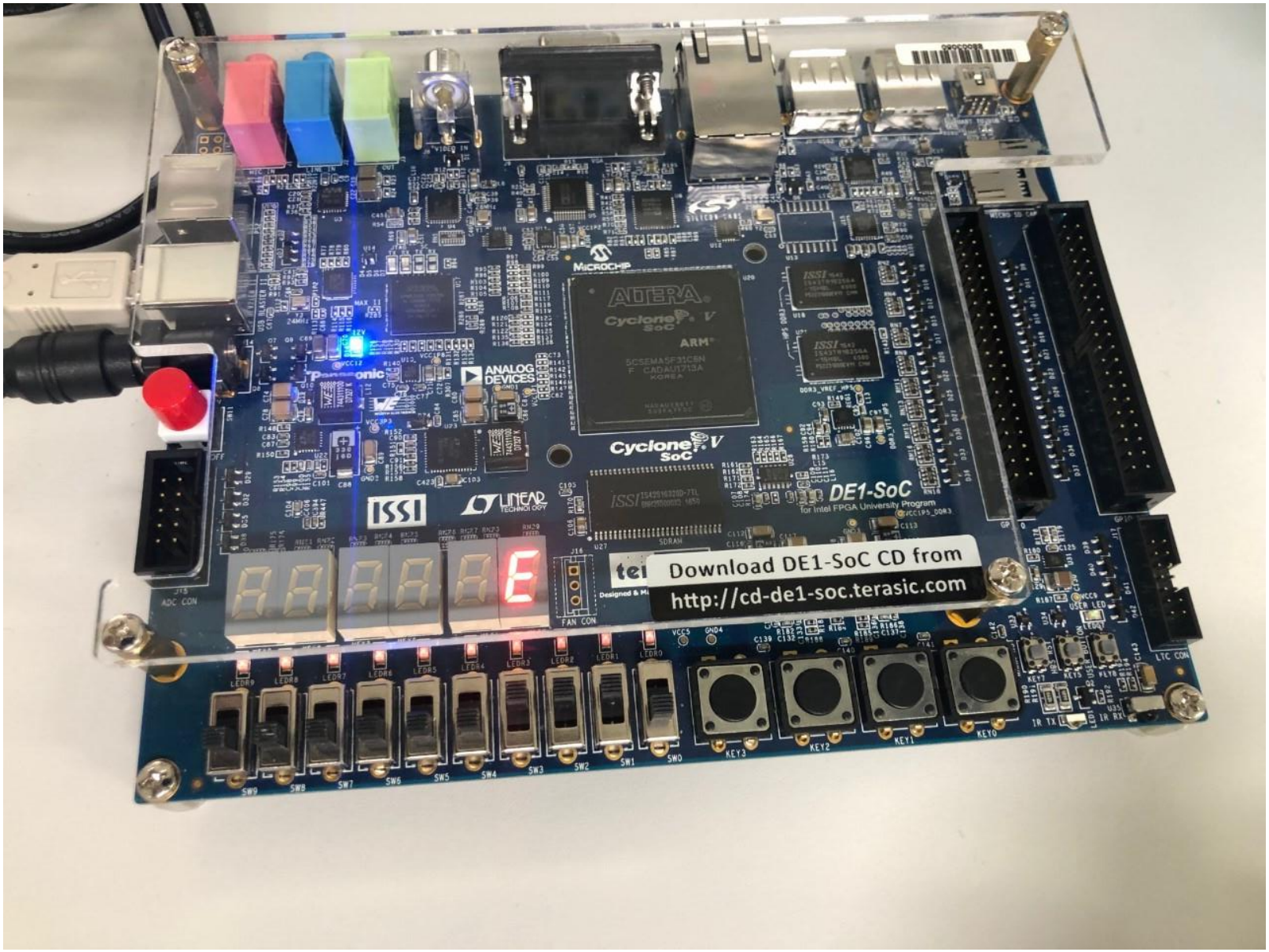
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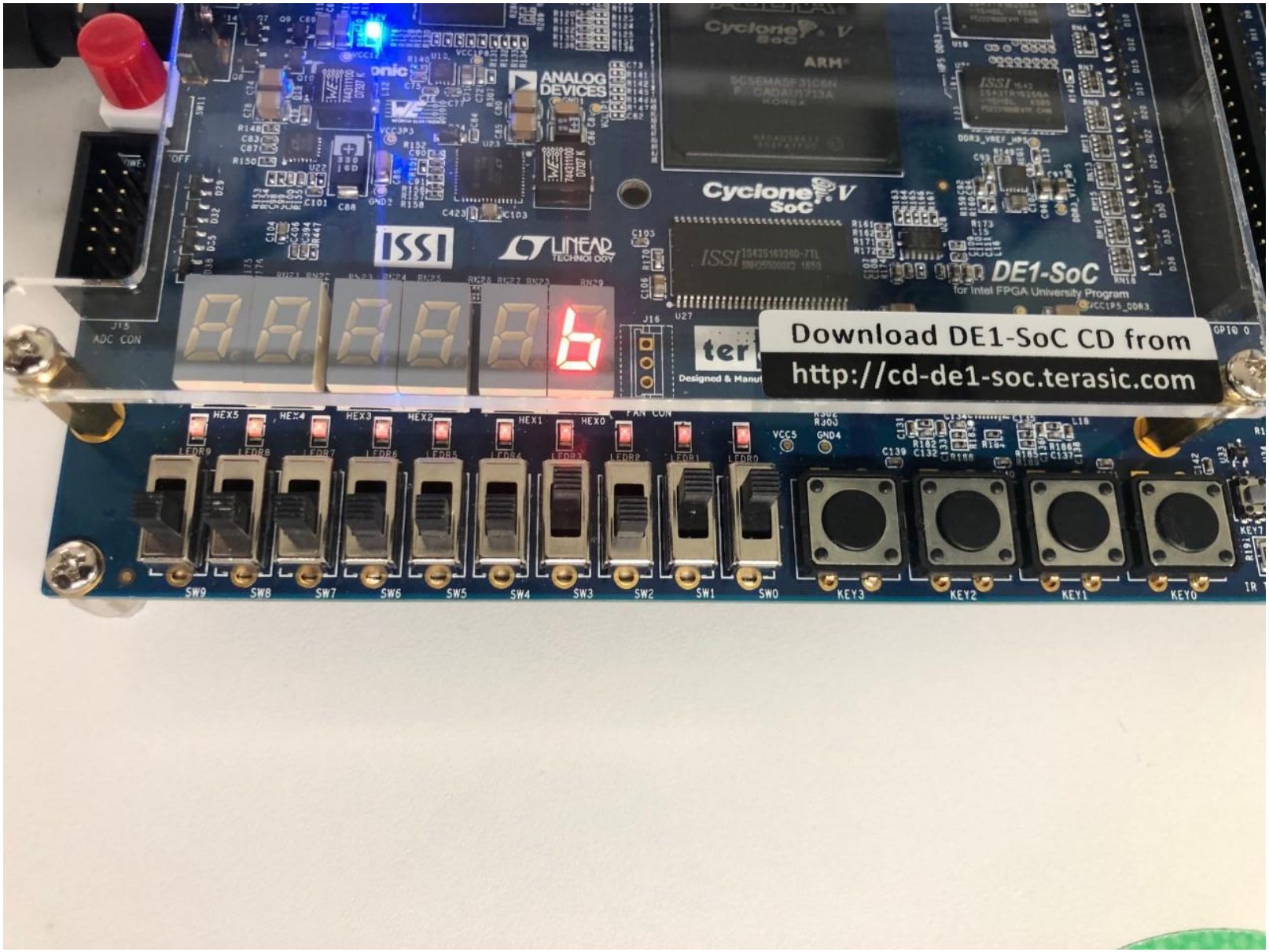
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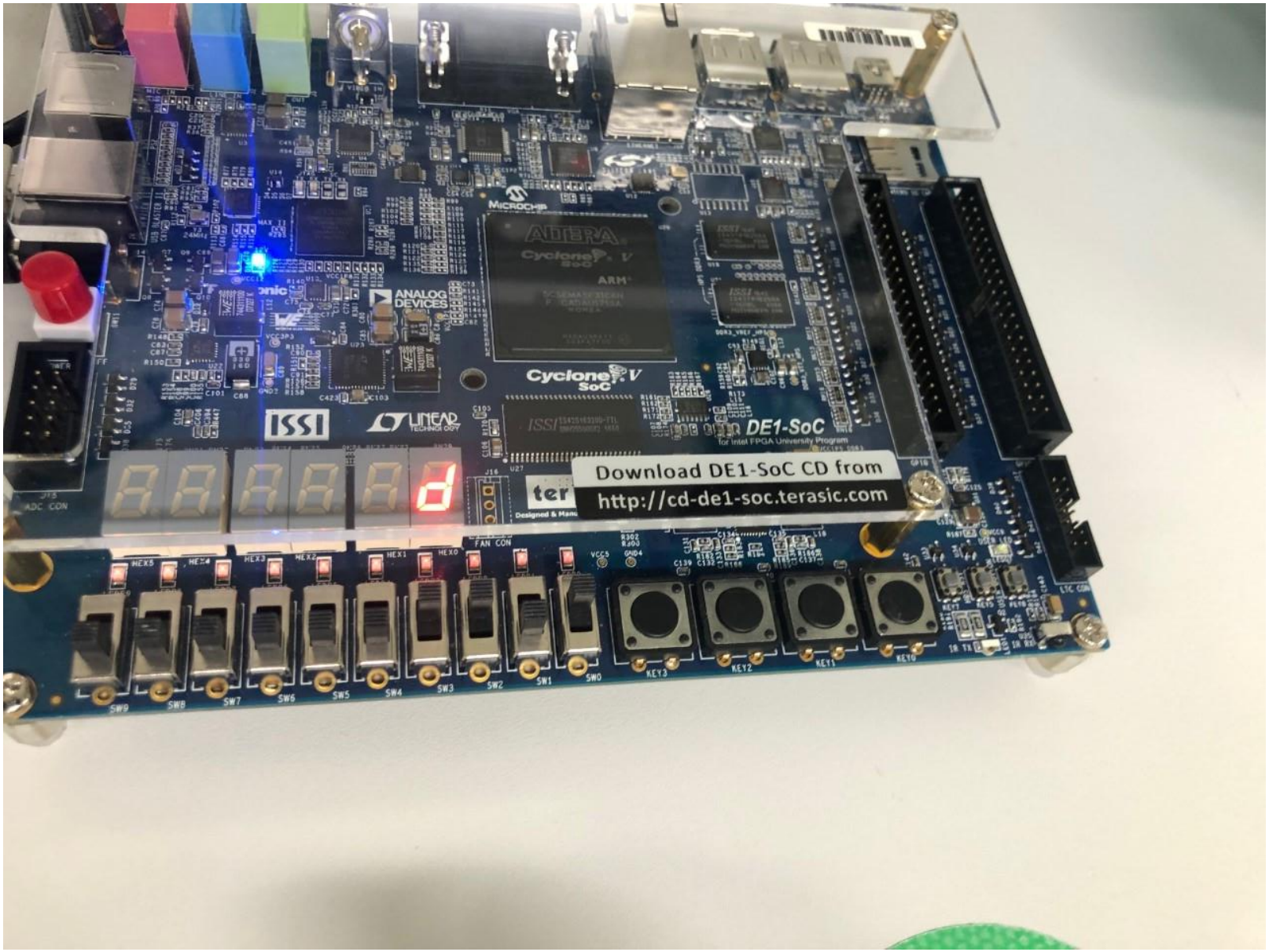
LEDR0
SW9
SW8
SW7
SW6
SW5
SW4
SW3
SW2
SW1
SW0
KEY3
KEY2
KEY1
KEY0
J15
ADC CON
J16
FAN CON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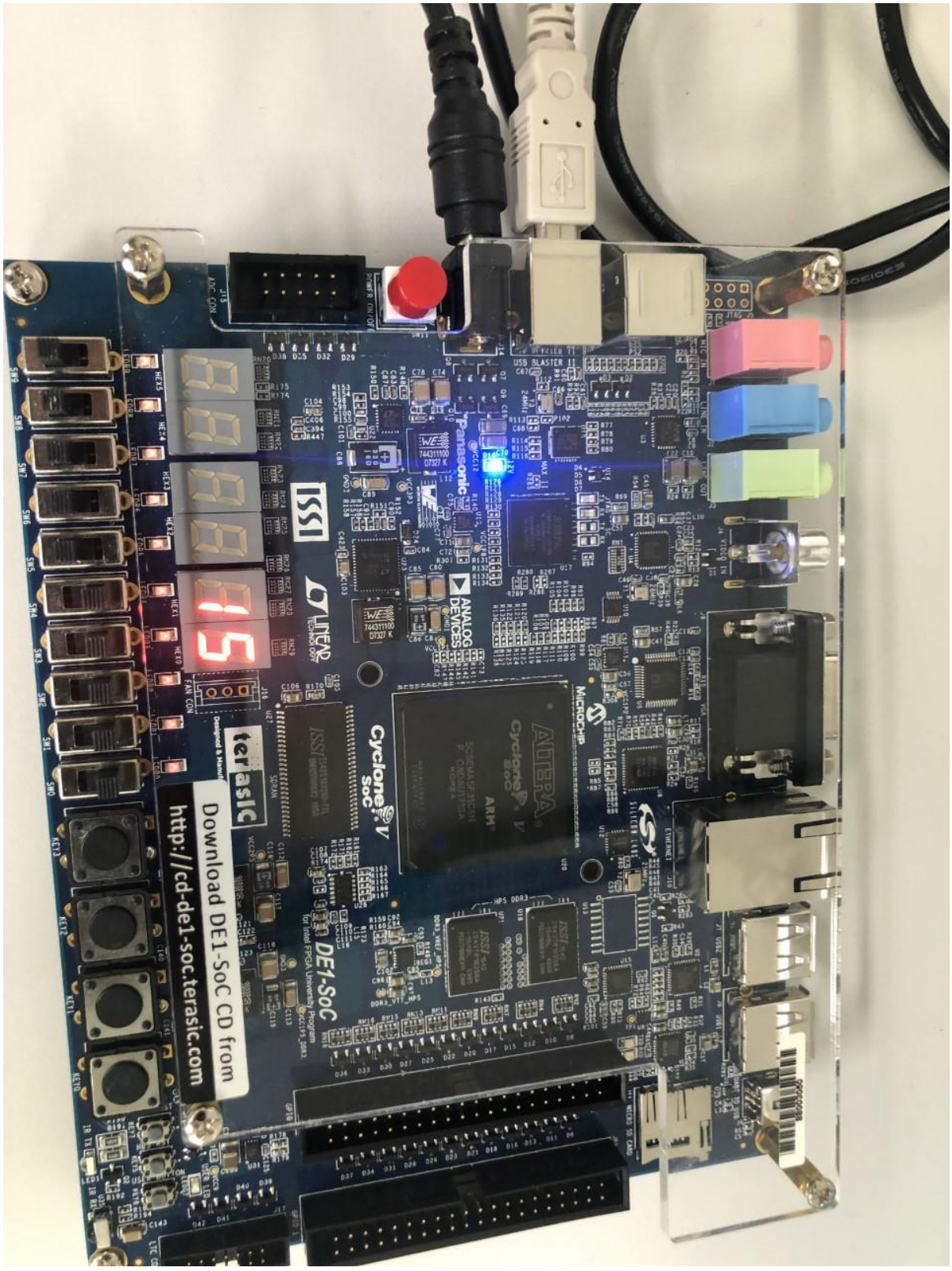
3.2

```
module test_twodigits;

logic [6:0] HEX0;
logic [6:0] HEX1;
logic [3:0] SW;
integer i;

//Instantiate the Unit Under Test (UUT)
twodigits uut(
.HEX0(HEX0),
.HEX1(HEX1),
.SW(SW)
);

//Apply inputs
initial begin
for (i=0;i<16;i=i+1) //run loop for 0 to 15.
begin SW = i;
#10;//wait for 10ns
end
end

endmodule
```

```
set_global_assignment -name FAMILY "Cyclone V"
set_global_assignment -name DEVICE 5CSEMA5F31C6
set_global_assignment -name TOP_LEVEL_ENTITY twodigits
set_global_assignment -name ORIGINAL_QUARTUS_VERSION 16.1.2
set_global_assignment -name PROJECT_CREATION_TIME_DATE "16:29:47  NOVEMBER 19, 2020"
set_global_assignment -name LAST_QUARTUS_VERSION "16.1.2 Standard Edition"
set_global_assignment -name SYSTEMVERILOG_FILE twodigits.sv
set_global_assignment -name PROJECT_OUTPUT_DIRECTORY output_files
set_global_assignment -name MIN_CORE_JUNCTION_TEMP 0
set_global_assignment -name MAX_CORE_JUNCTION_TEMP 85
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 256
set_global_assignment -name PARTITION_NETLIST_TYPE SOURCE -section_id Top
set_global_assignment -name PARTITION_FITTER_PRESERVATION_LEVEL PLACEMENT_AND_ROUTING -section_id Top
set_global_assignment -name PARTITION_COLOR 16764057 -section_id Top
set_location_assignment PIN_AE26 -to HEX0[0]
set_location_assignment PIN_AE27 -to HEX0[1]
set_location_assignment PIN_AE28 -to HEX0[2]
set_location_assignment PIN_AG27 -to HEX0[3]
set_location_assignment PIN_AF28 -to HEX0[4]
set_location_assignment PIN_AG28 -to HEX0[5]
set_location_assignment PIN_AH28 -to HEX0[6]

set_location_assignment PIN_AJ29 -to HEX1[0]
set_location_assignment PIN_AH29 -to HEX1[1]
set_location_assignment PIN_AH30 -to HEX1[2]
set_location_assignment PIN_AG30 -to HEX1[3]
set_location_assignment PIN_AF29 -to HEX1[4]
set_location_assignment PIN_AF30 -to HEX1[5]
set_location_assignment PIN_AD27 -to HEX1[6]
set_instance_assignment -name PARTITION_HIERARCHY root_partition -to | -section_id Top
```

```
//Display on 7 segment
module sevenseg (output logic [6:0] seg, input logic [3:0] value);

always_comb
unique casez (value)
4'b0000 : seg = 7'b1000000;
4'b0001 : seg = 7'b1111001;
4'b0010 : seg = 7'b0100100;
4'b0011 : seg = 7'b0110000;
4'b0100 : seg = 7'b0011001;
4'b0101 : seg = 7'b0010010;
4'b0110 : seg = 7'b1000010;
4'b0111 : seg = 7'b1111000;
4'b1000 : seg = 7'b0000000;
4'b1001 : seg = 7'b0010000;
default : seg = 7'b1111111;
endcase
endmodule

//Divide the input with 10
module twodigits (input logic [3:0] SW,
output logic [6:0] HEX0,
output logic [6:0] HEX1);
reg [3:0] tensbcd;
reg [3:0] onesbcd;
sevenseg s0 (.seg(HEX0), .value(onesbcd));
sevenseg s1 (.seg(HEX1), .value(tensbcd));

always@ (SW)
begin
onesbcd = SW % 10;
tensbcd = SW / 10;
end
endmodule
```



The number shows as expected.

Q: Quartus issues a warning that certain output pins are stuck at VCC or GND. Why is this?

A: This error is shown because one or more of the outputs are permanently high or low during the simulation. Usually this problem arises when testbench is not considering all outputs and some are assigned default values.

3.3

```
1  // simple counter for X5
2  module counter(
3  input logic clk, reset,
4  output logic [3:0] value);
5
6  always_ff @(negedge clk, negedge reset)
7    if (~reset)
8      value <= 0;
9    else
10     value <= value + 1;
11 endmodule
12
```