EE26 Digital Logic Systems

Spring Semester 2020

Notes 11 (3/4/2020)

Project 4 Design, implementation and testing of a Non-pipelined 8 Point FFT algorithm using butterfly structures.

(Implementation due on March 23
Report due one week after.)

SUMMARY

The goals of this lab are to become familiar with FFT butterfly structures, 8 point FFT algorithms and the VHDL implementation of non-pipelined version of the FFT.

INTRODUCTION

Please study the handouts on the Xilinx software on Trunk Site under Resources. Xilinx Vivado software integrates several tools into a complete software package. Tools of interest for this lab are Schematic, VHDL Editor and Simulator. The Schematic Editor is a schematic capture program, VHDL Editor are text editors for VHDL language, and the Simulator is a waveform analyzer and editor that graphically display the simulation. The software is installed on most of the PC's in Room 225. These PC's are on the network. All of your work should be saved in a removable drive or in your NT account at the end of the lab. All work on the hard disk will be deleted at the end of the day. Saving your work in a removable drive will allow you to move your work between computers and avoid logistic problems with directories and file names. YOU ARE RESPONSIBLE FOR MAKING SURE THAT YOUR WORK IS SAVED!!

In this lab, we will implement a controller in VHDL for a non-pipelined 8 point FFT algorithm using butterfly architecture designed in lab 3. You are going to design the 8 point FFT algorithm and simulate your design.

ASSIGNMENT

1. Learn the design principle of a butterfly and an 8 point DIT FFT algorithm.

2. Using Xilinx floating-point IP and record type to design a non-pipelined 3 stage 8 point DIT FFT algorithm.

3. Simulate your designs to check if you can get the correct outputs from given inputs.

4. Write a report which should include all VHDL codes and simulation results. Discuss what works and what not and what failures you encounter. Use the report format handout for your report format.