Assignment 4 - FPGA Implementation

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<u>Functionality of the mvm_uart_system RTL and the python script</u>

Mvm_uart_system

This system is a wrapper for serial communication modules and computational modules. For serial communication two modules uart_rx and uart_tx are designed where uart_rx convert input serial data to parallel data while uart_tx convert output parallel data to serial data for sending. The main computation block is a wrapper named axis_matvec_mul with two modules named matvec_mul and skid_buffer with a shifter. skid_buffer handles axi stream signals and matvec_mul handles the matrix multiplication, the intended operation of the design.

Python script

Since the communication is serial between computer and Zybo, the following code initatie the serial connection.

#serial.Serial(NAME OF UART PORT, BAUD RATE, READ TIME OUT)

#serial.Serial(NAME_OF_UART_PORT, BAUD_RATE, READ_TIME_OUT)
ser = serial.Serial('COM3', 115200, timeout=0.050)

The script generate two matrices (k,x) with random integers of range ± 128 such that they can undergo vector multiplication. Each element in these arrays are written in 1 byte. The result of the vector multiplication is stored in another array (y_exp) with 4 bytes elements.

The arrays k and x are then prepared to sent through a serial connection by flattening and concatenated to a single 1 dimensional array.

kx = np.concatenate([x, k.flatten()])
kx_bytes = kx.tobytes()

Next the script monitors the receiving connection and extract the resultant matrix as an array (y). Then the script compares the received array and the computed result and display an error message if any mismatches present.

```
assert (y == y_exp).all(), f"Output doesn't match: y:\{y\} != y_exp:\{y_exp\}"
```

Process of programming the FPGA (using Vivado)

- 1. In the creation of a new RTL project after adding the required source files select the FPGA board for implementation (Zybo in the session conducted) as the default part and create the project.
- 2. Add the constraints file to map the properties of the board according to the RTL design. Set the top module appropriately from the sources tab, in case of the design containing several source files. Next from generate bit stream from Program and Debug section.
- 3. Upon successful completion, a separate tab named Open Hardware manager will appear. Now connect the FPGA board to the computer. A red colour bulb will indicate the power on state of the board. Once the device is recognized the following message will appear.

HARDWARE MANAGER - localhostxilinx_tcf/Digilent/210279545026A

1 There are no debug cores. Program device Refresh device

4. Click on the program device button to program the device. Once it is successfully completed a green colour bulb will light up as follows.



Utilization reports of synthesis and implementation

Resources

Synthesis

Name 1	Slice LUTs (17600)	Slice Registers (35200)	Bonded IOB (100)	BUFGCTRL (32)
∨ N fpga_module	5399	3373	4	1
> I mvm_uart_syste	5399	3373	0	0

Implementation

Name 1	Slice LUTs (17600)	Slice Registers (35200)	Slice (4400)	LUT as Logic (17600)	Bonded IOB (100)	BUFGCTRL (32)
√ N fpga_module	5394	3373	1691	5394	4	1
> I mvm_uart_sys	5394	3373	1691	5394	0	0

Timing

Synthesis

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.279 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	3.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	6737	Total Number of Endpoints:	6737	Total Number of Endpoints:	3374
All user specified timing constra	ints are met				

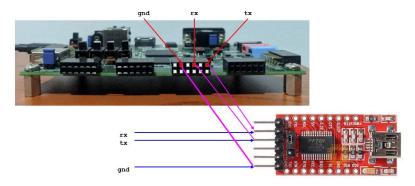
Implementation

Setup	Hold		Pulse Width	
Worst Negative Slack (WNS): 0.247 n	Worst Hold Slack (WHS):	0.036 ns	Worst Pulse Width Slack (WPWS):	3.500 ns
Total Negative Slack (TNS): 0.000 n	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints: 6737	Total Number of Endpoints:	6737	Total Number of Endpoints:	3374

Matrix vector multiplication

Video of performing a matrix multiplication could not be captured due to several issues in troubleshooting. The following is the complete process in performing the matrix multiplication.

USB-tty is used to communicate between FPGA and the computer using serial communication. First connect USB-tty to the FPGA board using JC Pmod Ports as shown below.



Now connect the USB-tty to computer and get the USB serial port of connection by device manager. Rename the python script with the port identification as follows.

Now program the FPGA and reset the circuit with sw[0] on the board. Connect the USB-tty and run the python script. Upon successful completion the results will be as follows.

```
(197, 7, -1, -34, -46, -13, 126, -71]], ttype=int8)

x=array([-41, -115, -63, 85, 38, -116, 29, -75], dtype=int8)

x=array([-41, -115, -63, 85, 38, -116, 29, -75], dtype=int8)

85, -16, 85, -3, -2, -44, -169, 53, -64, 122, 13, 23, -94, -31, 28, 49, -2, -126, -8, -68, -28, -18, 115, -33, 33, -94, -184, -65, 114, -83, 82, 77, -28, -8, -8, -8, -8, -8, -8, -91, -11, -96, 94, -34, -93, 40, -66, -128, 86, 86, 122, 74, 26, 97, 7, -1, -34, -46, -13, 126, -71], dtype=int8)
Sent: kz_bytes= b^\xd7\x8d\xc1U$\x8c\x1d\xb5r<\xb8U\xf6U\xf6U\xf6\xd4\x935\xc8z\r\x17\xa2\xe1\x1c1\xfe\x8z\xf8\xbc\xc4\xees\xdf!\xa2\x98\xbfr\xad8M\xcc\xd8\xcd\xe4\xe4\xe5\xa5\xf5\xa6^\xde\xa2\x88V\z1\x1a\x98\xbfr\xad8M\xcc\xd8\xc2\x98\xbfr\xad8M\xcc\xd8\xe4\xe4\xe4\x88V\z1\x1a\x98\xbfr\xad8M\xcc\xd8\xff\xa6\xd6\xde\xa5\xf5\xa6^\xde\xa3\(\xbe\x86V\z2\x1a\x)
 y_exp=array([ -9486, 16485, -8938, -9546, -24138, -7294, 18636, 956])
                                                                   79, -66, -75, -120, 87, 59],

-77, 22, -71, -82, 165],

-53, 11, -116, 2, -30],

83, -31, 124, 69, -126],

31, 39, 55, -48, -121],

53, -68, 57, 16, 99],

-188, 4, 112, 120, 1],

-38, -25, -32, -53, 111]], dtype=int8)
                ay([[-118, -12, 7

[-183, -24, -88,

[ 41, -15, -114,

[ 54, -55, 17,

[ -37, 118, 68,

[ 124, 75, -112,

[ -75, -95, -117,

[ -67, 48, 122,
                            31, 188, 1-10, 53, -113, -72, -66, -198, -110, -12, 7, 6, -75, -120, 87, 59, -183, -24, -88, -77, 22, -71, 2, 165, 41, -15, -114, -53, 11, -116, 2, -36, 54, 5, 17, 83, -31, 124, 69, -126, -37, 118, 68, 31, 8, 55, -48, -121, 124, 75, -112, 53, -68, 57, 16, 9, -75, -95, -117, -188, 4, 112, 126, 1, -67, 48, 2, -39, -25, -32, -53, 111], dtype=int8)
Sent: kx_bytes=b'x1flxf65x8fxb6xbexecx92xf40xbexb5x88w;x99xe8xa8xb3x16xb9xaei)xf1x8excbx8bx92x62xe26xc9x115xe1[ex82xdbv0x1fx1e7xd8x87]xx9exbc9x16cxb5xa1x8bx94x84pxx81xb2xe2xe7xe9xcbo'
       ************** TEST 20 ***************
    **Array([[ 99, -127, 112, 87, -18, -42, 29, -19], [ -57, 122, -25, 32, -51, 56, -85, 112], [ 76, 37, 33, -116, -85, -119, 99, -74], [ -118, -65, -124, -66, 125, -37, -112, 19], [ 122, -134, 88, 59, -47, 184, 17, -48], [ 182, 117, 93, 117, 186, 93, 69, -94], [ 41, -15, 97, 36, -66, -116, 82, -94], [ -65, -114, 99, 9, -23, 87, 61, -22]], dtype=int8)
```