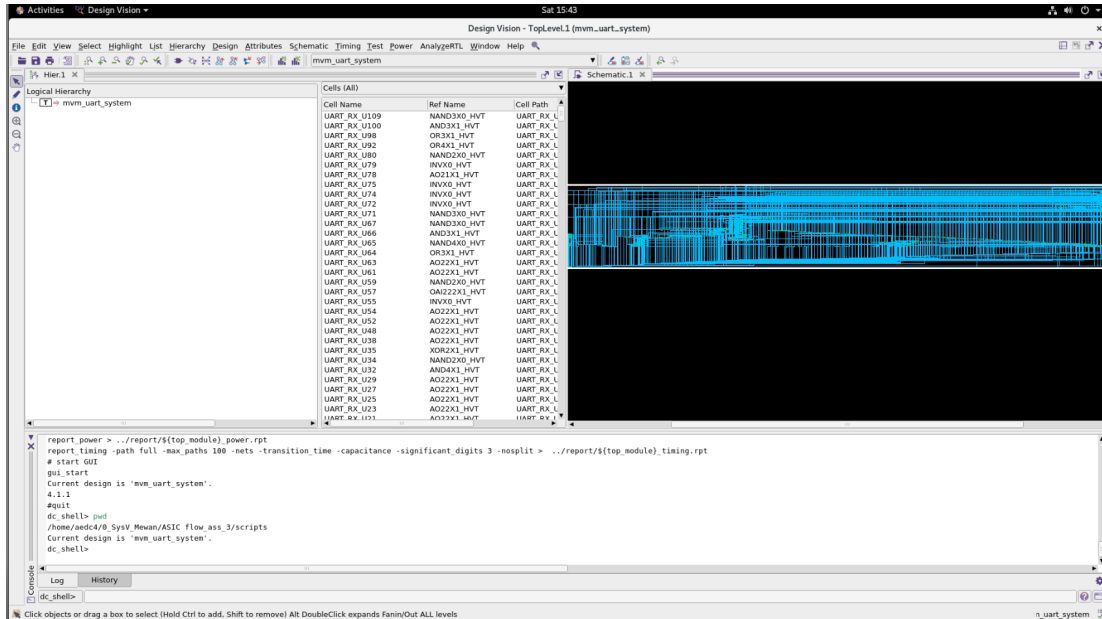


Assignment 3 - ASIC Flow Report

Submission – Chandira R.M.

1. The synthesized RTL design schematic visualized in Design Vision of DC



2. Information from reports

Ports and cells

Number of ports:	4
Number of nets:	1068
Number of cells:	923
Number of combinational cells:	612
Number of sequential cells:	310
Number of macros/black boxes:	0
Number of buf/inv:	119
Number of references:	51

Area (Units μm^2)

Combinational area:	1728.941639
Buf/Inv area:	394.177350
Noncombinational area:	2163.527918
Macro/Black Box area:	0.000000
Net Interconnect area:	923.917724
Total cell area:	3892.469557
Total area:	4816.387281

Power

Global Operating Voltage = 0.7

Power-specific unit information :

Voltage Units = 1V

Capacitance Units = 1.000000ff

Time Units = 1ns

Dynamic Power Units = 1uW (derived from V,C,T units)

Leakage Power Units = 1pW

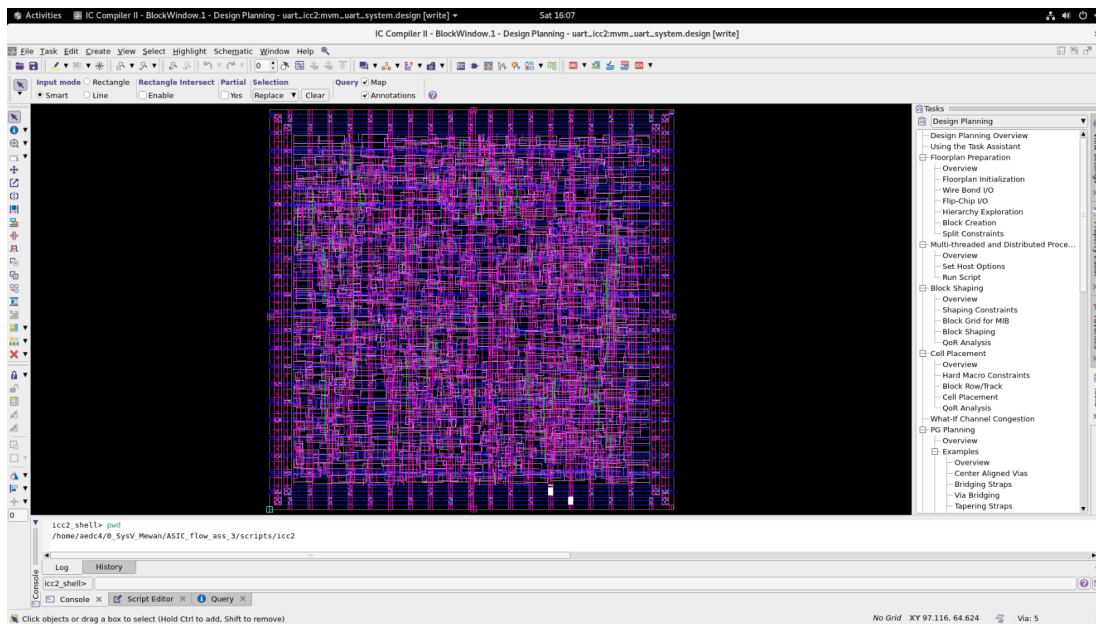
Timing

data required time 0.364

data arrival time -4.042

slack (VIOLATED) -3.678

3. The completed PnR layout visualized inside ICC2



4. The final exported GDSII file visualized using kLayout

