Gowin Power Analyzer

User Guide

SUG282-2.0E,09/17/2020

Disclaimer

Revision History

Date	Version	Description
01/30/2018	1.2E	Initial version published.
08/16/2018	1.3E	● The value range of V_{CC}/V_{CCX} updated; ● Interface screenshots updated.
10/26/2018	1.4E	GW1NZ-1 and GW1NSR-2C supported.
11/15/2018	1.5E	● GW1NSR-2 supported; ● GW1N-6ES, GW1N-9ES and GW1NR-9ES removed;
02/25/2019	1.6E	● The voltage configuration updated; ● VCD File configuration supported; ● Specified IO toggle rate configuration removed.
05/17/2019	1.7E	GW1N-1S supported.
03/09/2020	1.8E	GW1NRF-4B, GW1NS-4, GW1NS-4C, GW1NSE-2C, GW1NSER-4C GW1NSR-4, GW1NSR-4C, GW2A-18C, GW2A-55C and GW2AR-18C supported.
05/09/2020	1.9E	● GW1N-9C, GW1NR-9C and GW2ANR-18C supported; ● GW1N-2, GW1N-2B and GW1N-6 removed.
09/17/2020	2.0E	Power analysis of automotive grade devices supported.

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1 About This Guide

1.1 Purpose

This guide describes how to use the Gowin Power Analyzer. It provides an introduction to the tool and an analysis of the power consumption report. It is designed to help users estimate and analyze power consumption more easily. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

- SUG100, Gowin Software User Guide
- SUG918, Gowin Software Quick Start Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology that are used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
FPGA	Field Programmable Gate Array
GPA	Power analyzer
GPC	Power Estimator
θJA	Junction to Ambient
θJB	Junction to Board
θSA	Sink to Ambient

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail:support@gowinsemi.com

2 Introduction

The GPA tool is independently developed by Gowin. It is designed to analyze FPGA power consumption to help users estimate system power consumption and improve the performance and reliability of the design.

FPGA power consumption includes static power consumption and dynamic power consumption.

- Static power consumption refers to the power consumption caused by leakage current in the device. It is determined by the design, package, process, voltage, and working environment of the chip.
- Dynamic power consumption refers to the power consumption during operating, which is determined by the user-designed logic circuit and the characteristics of the circuit.

2.1 Principle

Users set the chip type, operating environment, resource utilization, and signal toggle rate parameters according to their requirements. These parameters have an impact on chip power consumption. The GPA automatically estimates the power consumption and generates a power consumption analysis report according to the parameters.

2.2 Features

The GPA has the following features:

- Supports environment temperature, airflow, heat sink performance, and board thermal model that affect static power consumption;
- Supports setting the customized thermal impedance parameters;
- Supports the toggle rate of specified I/O and the net signal. According to the waveform files generated by the simulation, supports default toggle rate and the rate calculating by non-vector estimation, etc.;
- Enables/disables clock, B-SRAM, I/O, and DFF;
- The generated power consumption analysis report supports the analysis of the power consumption in terms of block type, hierarchy, clock domain, etc.
- Supports GW1NZ using BandGap to reduce power.

3 GPA

The GPA helps users accurately estimate the power consumption by chip type, operating environment, voltage, signal toggle rate and clock enable configuration. For a simple GPA example, see 3.6 section GPA Configuration of SUG918, Gowin Software Quick Start Guide.

3.1 Start GPA

Before starting GPA, you need to create or load the config file (.gpa).

3.1.1 Create/Load Config File

Create Config File

The steps are as follows:

1. In the "Design" view, right-click and select "New File...".
   The "New" dialog box pops up;
2. Create "GPA Config File", as shown in Figure 3-1;
3. Click "OK", and the "New GPA Config File" dialog box will open, as shown in Figure 3-2;
4. Enter Config File name and select create path, then click "OK". The GPA Config File appear in "Design > GPA Config Files".

Figure 3-1 Create Config File

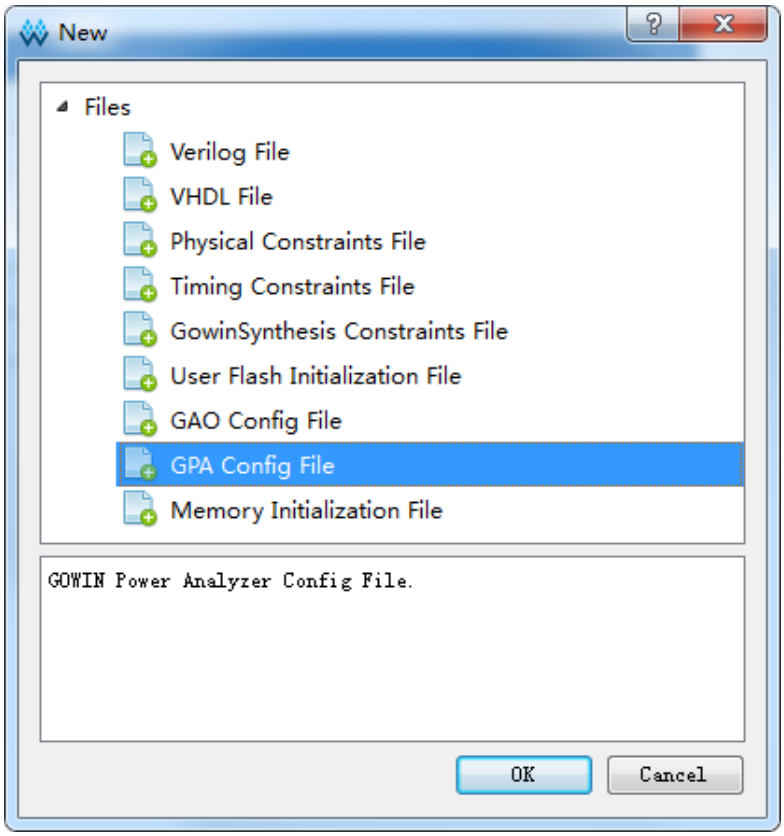
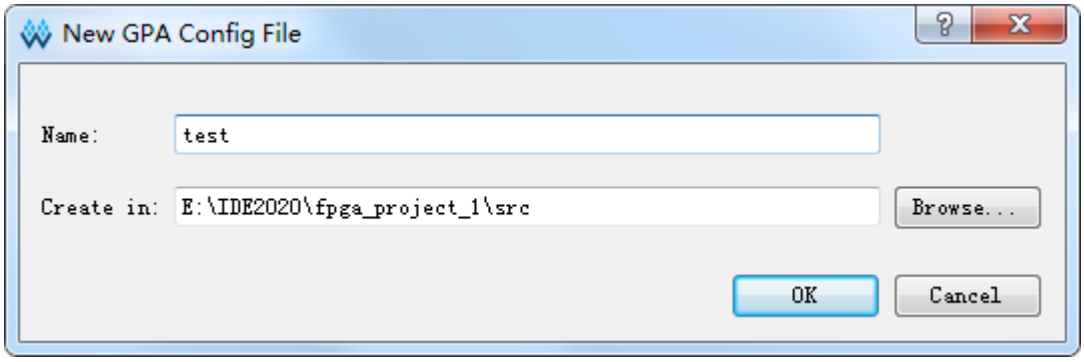


Figure 3-2 New GPA Config File

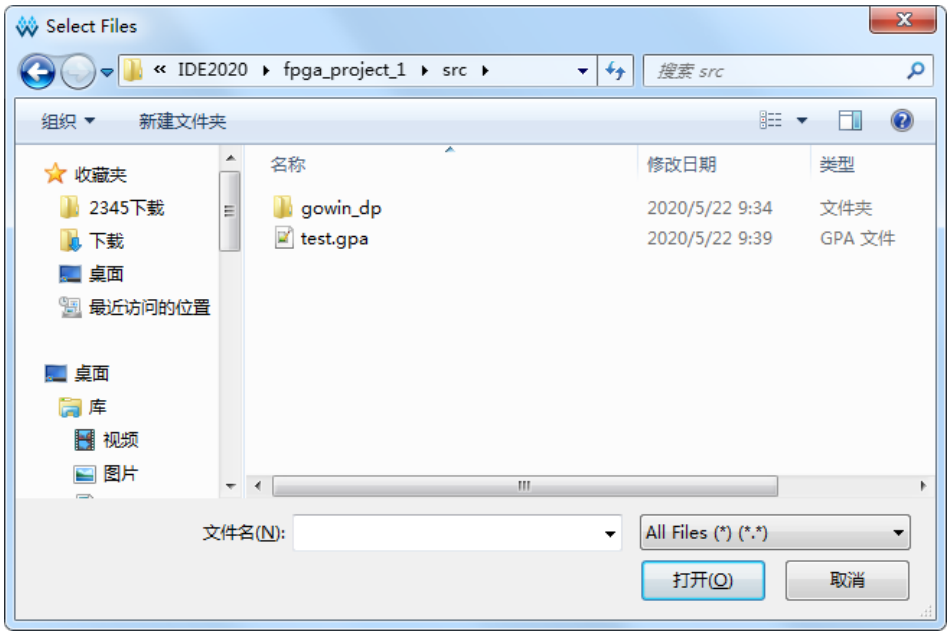


Add Config File

The steps are as follows:

1. In "Design", right-click and select "Add Files...", The "Select Files" window will open;
2. Select the existing Config File (.gpa), as shown in Figure 3-3, click "Open". See GPA Config File in "Design > gpa Config Files".

Figure 3-3 Load Config File

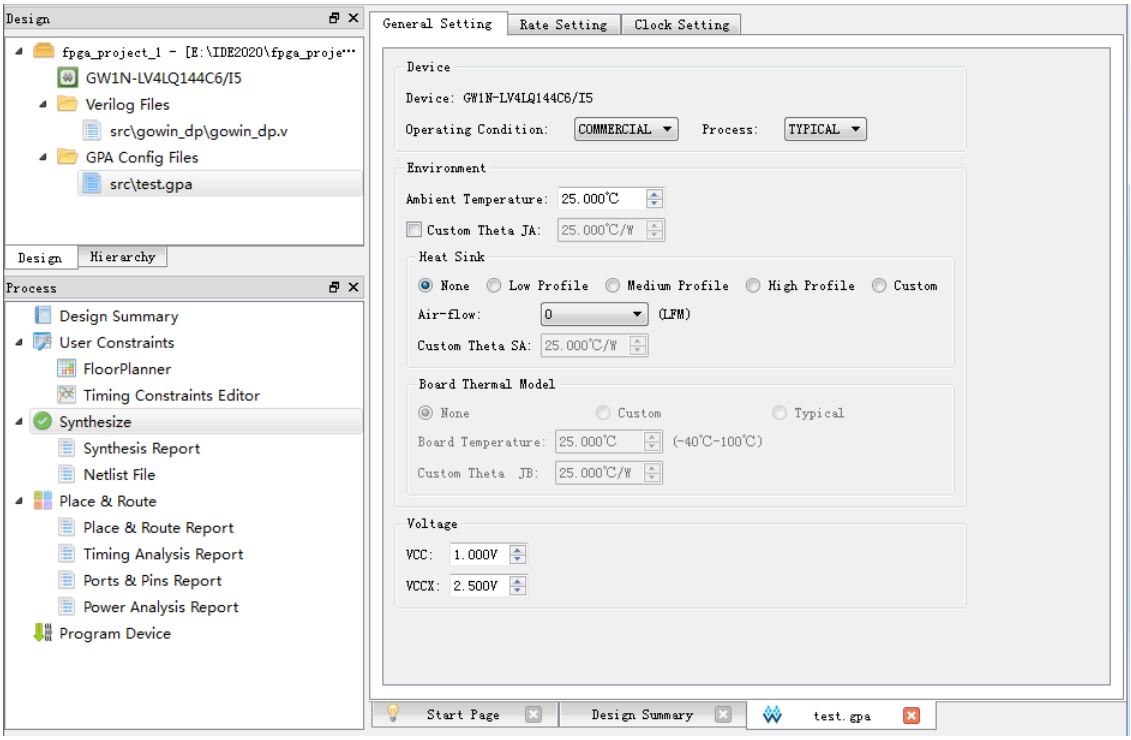


3.1.2 Start the GPA

Double-click the Config File (.gpa) in "Design" window, and the configuration window pops up, and GPA starts, as shown in Figure 3-4.

The GPA configuration view includes "General Setting" (used for configuring operating conditions), "Rate Setting" (used for configuring signal toggle rate) and "Clock Setting" (used for configuring clock enable).

Figure 3-4 GPA Interface



Note!

- GPA supports power consumption analysis for netlists after synthesis or PnR;
- Start the tool only after synthesis.

3.2 Configuration

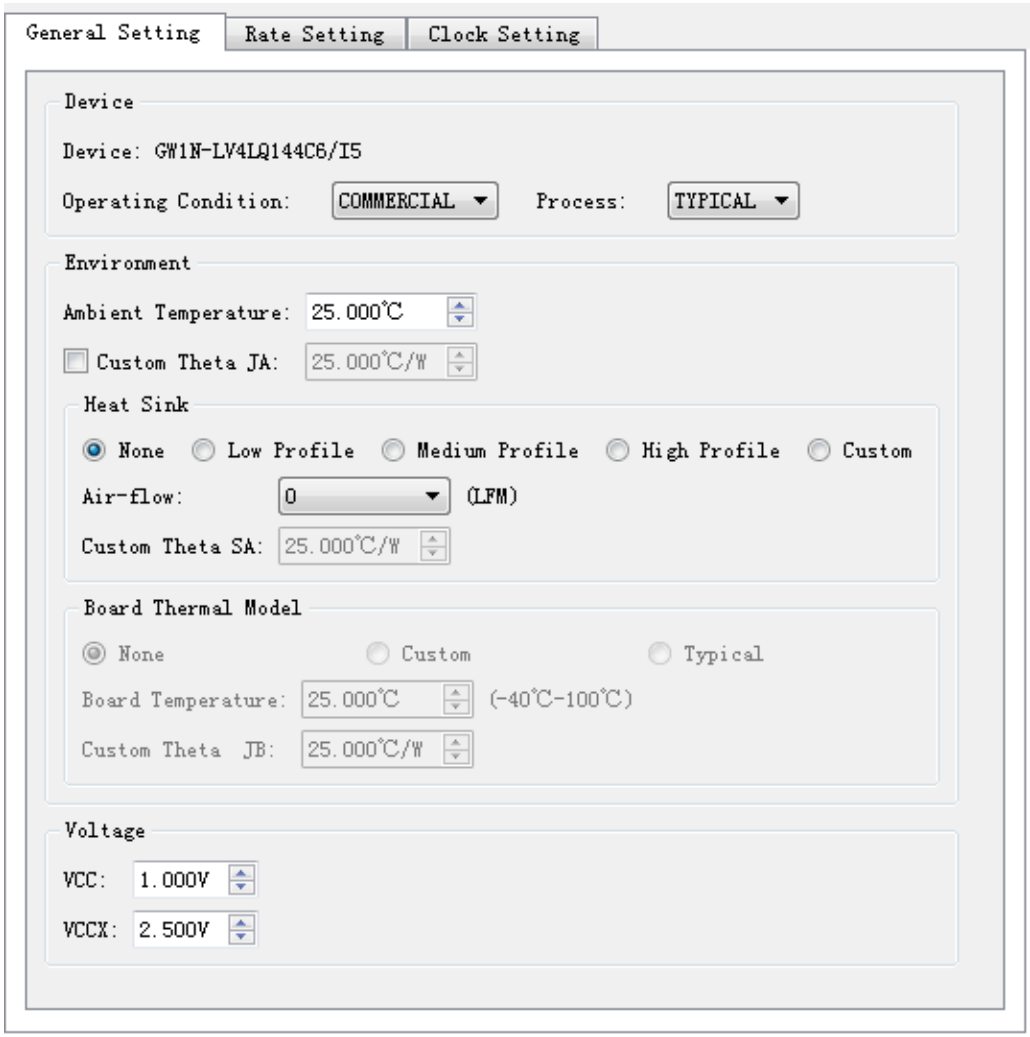
To ensure the accuracy of the power consumption analysis, it is necessary to set the chip operating conditions, toggle rate of the signal, and enable/disable clock, B-SRAM, I/O, DFF etc. according to the design.

3.2.1 Operating Conditions

The "General Setting" view displays the parameters of the chip, package, speed level and temperature grade, thermal impedance, and voltage.

As shown in Figure 3-5, the "General Setting" view displays "Device" for setting the chip type, "Environment" for setting the chip operating conditions, and "Voltage" for setting the chip voltage.

Figure 3-5 General Setting View



Parameters

1. Device
   - Device: Family, device, package, and speed of chip;
   - Operating Condition: The operating condition includes

COMMERCIAL, INDUSTRIAL and AUTOMOTIVE. And the operating condition setting affects the minimum and maximum operating temperature of the chip. The min. operating temperature of commercial device is 0 ℃, and the max. operating temperature is 85 ℃; the min. operating temperature of industrial devices is minus 40 ℃, and the max. operating temperature is 100 ℃; the min. operating temperature of automotive devices is minus 40 ℃, and the max. is 125 ℃

- Process The process of the chip includes TYPICAL or WORST.

2. Environment

"Environment" is used to configure the environmental temperature, air flow, heat sink and board thermal mode. Operating environment affects static power consumption. Different operating environments will affect the FPGA chip temperature and static power consumption. Air flow affects the thermal performance of the chip.The heat sink is used for the heat dissipation of the specified chip through the auxiliary device;The circuit board thermal mode is used for the heat dissipation of the specified chip through the board.

Junction temperature is determined by external temperature, chip power consumption, and thermal impedance. Please refer to Appendix A Calculation Principle for Junction Temperature for calculation principle of junction temperature. Details of Environment configuration parameters are as follows:

- Ambient Temperature: The unit is ℃. The range is to from minus 40 ℃ ~ 150 ℃, and the default is 25.000 ℃;
- Custom Theta JA: The user specifies the thermal impedance θ_{JA} between the chip and environment. The unit is ℃ / W. The range is from 0.001 ℃/W ~ 100 ℃ / W, and the default is 25.000 ℃ / W;
- Heat Sink: Heat Sink includes 5 modes: None, Low Profile, Medium Profile, High Profile and Custom. "None" indicates heat sink is unused, and only thermal impedance θ_{JA} influences junction temperature; Custom indicates that the user specifies the thermal impedance θ_{SA} from the heat sink to the environment; Low Profile, Medium Profile and High Profile modes represent θ_{JA} is automatically calculated by the power analyzer.
- Air Flow: The unit is LFM or m/s. The unit displayed in the user interface is LFM. There are four selection modes, including 0LFM, 100LFM (0.5 m/s), 200 LFM (1.0 m/s), 400 LFM (2.0 m/s);The larger the Air Flow is, the smaller the thermal impedance from the case to the Air is, and the smaller the junction temperature is.
- Custom Theta JA: thermal impedance θ_{SA} between Heat Sink and environment. The unit is ℃ / W. The range is from 0.001 ℃/W ~ 100 ℃ / W, and the default is 25.000 ℃ / W;
- Board Thermal Model: Heat dissipation mode of development board. Thermal impedance model of the development board is the path that dissipating heat from the development board to outside, which

includes three modes: None, Custom, and Typical. None means board thermal is not to be considered; Custom indicates the user specifies thermal impedance $\theta_{JB}$from device to development board; Typical indicates $\theta_{JB}$is automatically determined by chip package.

- Board Temperature: Board temperature
- CustomTheta JB: Thermal impedance θ_{JB} from junction to board. The user can specify only if selecting Custom from Board Thermal Model.

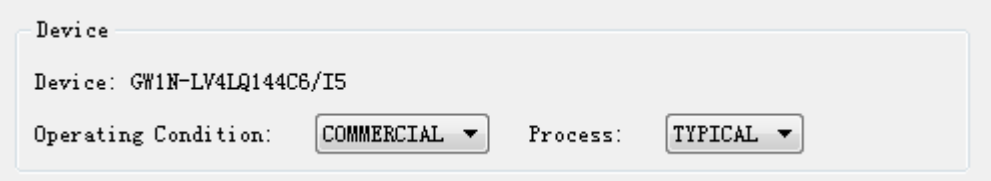
3. Voltage
   - VCC: core voltage. The unit is V, and for the voltage range of each series device, you can see the pinout manuals at our website:
   - VCCX: auxiliary voltage; The unit is V, and for the voltage range of each series device, you can see the pinout manuals at our website:

Device Configuration

The Device configuration includes package and speed of the chip, as well as set the temperature level and process of the chip, as shown in Figure 3-6 .

1. Set Operating Condition:
   Click "Operating Condition" and select COMMERCIAL, INDUSTRIAL or AUTOMOTIVE in drop-down list;
2. Set Process;
   Click "Process" and select TYPICAL or WORST in the drop-down list.

Figure 3-6 Device Configuration



Environment Configuration

1. Set ambient temperature.
   Set ambient temperature by entering environment temperature in Ambient Temperature, or adding and reducing the temperature value through the upper and lower buttons on the right side of text box or sliding mouse wheel.
2. Set thermal impedance if there is no heat sink in chip.
   Thermal impedance θ_{JA} can be specified by the user or determined by package and air flow if there is no heat sink.
   a). Custom Theta JA Check "Custom Theta JA" and enter the specified thermal impedance value in text box, adding and reducing the thermal impedance values, as shown in Figure 3-7.

Note!

You can also add and reduce the thermal impedance value using the upper and lower buttons on the right side of text box or by sliding mouse wheel.

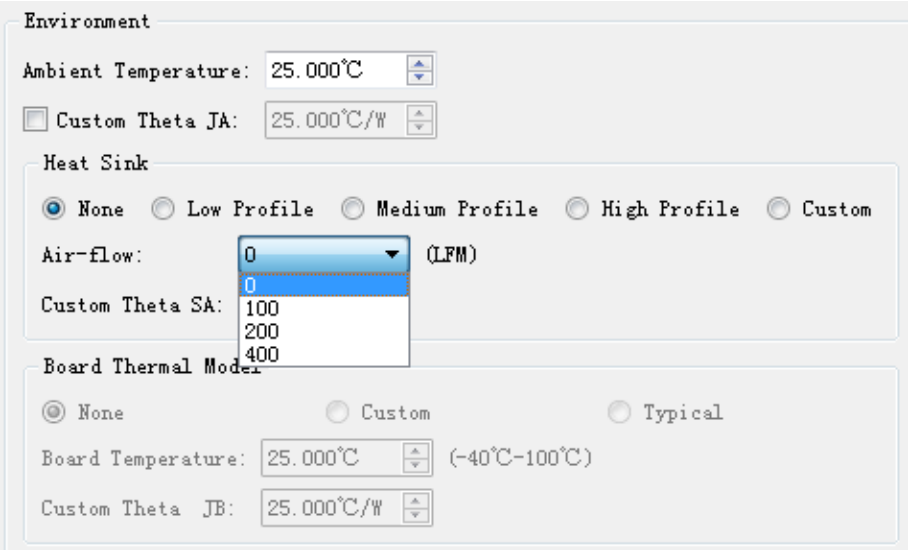
Figure 3-7 Specify Thermal Impedance θ_{JA}

Note!

Custom Theta JA has a higher priority than that specified by package and air flow. If Thermal impedance is specified, Heat Sink and the Board Thermal Model is grayed out and not available;

b). Thermal Impedance θ_{JA} is determined by package and air flow. In the Heat Sink configuration area, click "None" and choose not to use the Heat Sink mode. Click "air-flow" and select Air flow 0, 100, 200, or 400 from the drop-down list, as shown in Figure 3-8.

Figure 3-8 Thermal Impedance θ_{JA} Determined by Package and Air Flow



Note!

If there is no heat sink, Board Thermal Model is not available.

3. If there is heat sink, but board thermal is not considered, you can set the thermal impedance.
   If there is heat sink and board thermal is not considered, thermal impedance θ_{JA} can be specified by user or determined by heat sink

mode. User specifies. User can specify the thermal impedance in following two ways:

a). Check "Custom Theta JA″ and enter the specified thermal impedance value in text box, adding and reducing the thermal impedance values, as shown in.

Note!

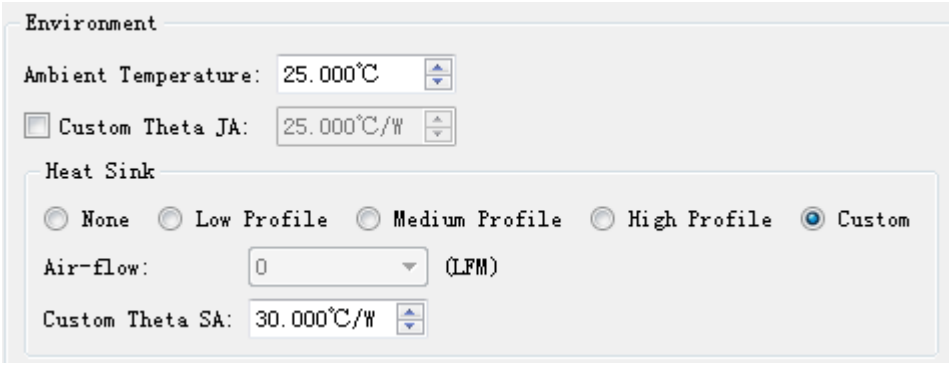
You can also add and reduce the thermal impedance value using the upper and lower buttons on the right side of text box or by sliding mouse wheel.

b). In Heat Sink configuration area, click "Custom"and enter the specified thermal impedance value θ_{SA} in Custom Theta SA, as shown in Figure 3-9 . In "Heat Sink", select "Low Profile", "Medium Profile" and "High Profile" as your required; Click air-flow and select 0, 100, 200, or 400 in drop-down list. As shown in Figure 3-8, select "None" in "Board Thermal Model" without regard to board thermal.

Note!

You can also add and reduce the thermal impedance value using the upper and lower buttons on the right side of text box or by sliding mouse wheel.

Figure 3-9 User Specifies Thermal Impedance θ_{SA}



Note!

- Specify θ_{SA} only when Custom Theta JA is not selected and Custom is selected in Heat Sink;
- When specifying thermal impedance θ_{SA}, air flow has an impact on θ_{SA}. Air-flow box will be grayed out and not available.

4. Set thermal impedance if there is heat sink and board thermal is considered.
If there is heat sink, thermal impedance θ_{JA} can be specified by user or be determined by heat sink mode; thermal impedance θ_{JB} can be specified by user or determined by heat sink mode.

a). Users specify thermal impedance θ_{JA}. Refer to the method b) specified in item 3 for parameter settings. Users specify thermal impedance θ_{JB}. In Board Thermal Model configuration area, click "Custom" and enter the temperature of the device in Board Temperature; Enter the specified thermal impedance value θ_{SA} in Custom Theta JB textbox, as shown in Figure 3-10.

Note!

You can also add and reduce the temperature value or thermal impedance value of development board by the upper and lower buttons on the right side of text box or by sliding mouse wheel.

Figure 3-10 User Specifies Thermal Impedance θ_{JB}

Note!

Specify Board Thermal Model only when Custom Theta JA is unspecified and None is not selected in Heat Sink.

b). Thermal impedance θ_{JA} is determined by heat sink mode. Please refer to item 3 for parameter settings.
Thermal impedance θ_{JB} is determined by board thermal. Click ″Typical″ in Board Thermal Model; Enter temperature in text box, adding and reducing the temperature value or thermal impedance value, and as shown in Figure 3-11

Figure 3-11 Thermal Impedance θ_{JB} Determined by Board Thermal

Note!

- You can also add and reduce the thermal impedance value of development board by the upper and lower buttons on the right side of text box or by sliding mouse wheel.
- If the thermal impedance θ_{JB} is specified by users, Custom Theta JB text box is greyed out and not available.
- Specify Board Thermal Model only when Custom Theta JA is not specified and None is not selected in Heat Sink.

Voltage Configuration

- V_{CC}: Enter core voltage in V_{CC}, and you can add and reduce the voltage value;

  Note!

  You can also add and reduce voltage value by using the upper and lower buttons on the right side of the text box or by sliding mouse wheel.

- V_{CCX}: Enter auxiliary voltage in V_{CCX}, and you can add and reduce the voltage value;

  Note!

  You can also add and reduce voltage value by using the upper and lower buttons on the right side of the text box or by sliding mouse wheel.

3.2.2 Signal Toggle Rate Configuration

Rate Setting is used for configuring signal toggle rate. You can set toggle rate of IO or Net or use default toggle rate.

As shown in Figure 3-12, Rate Setting view displays Net Rate, VCD File and Default Rate Setting.

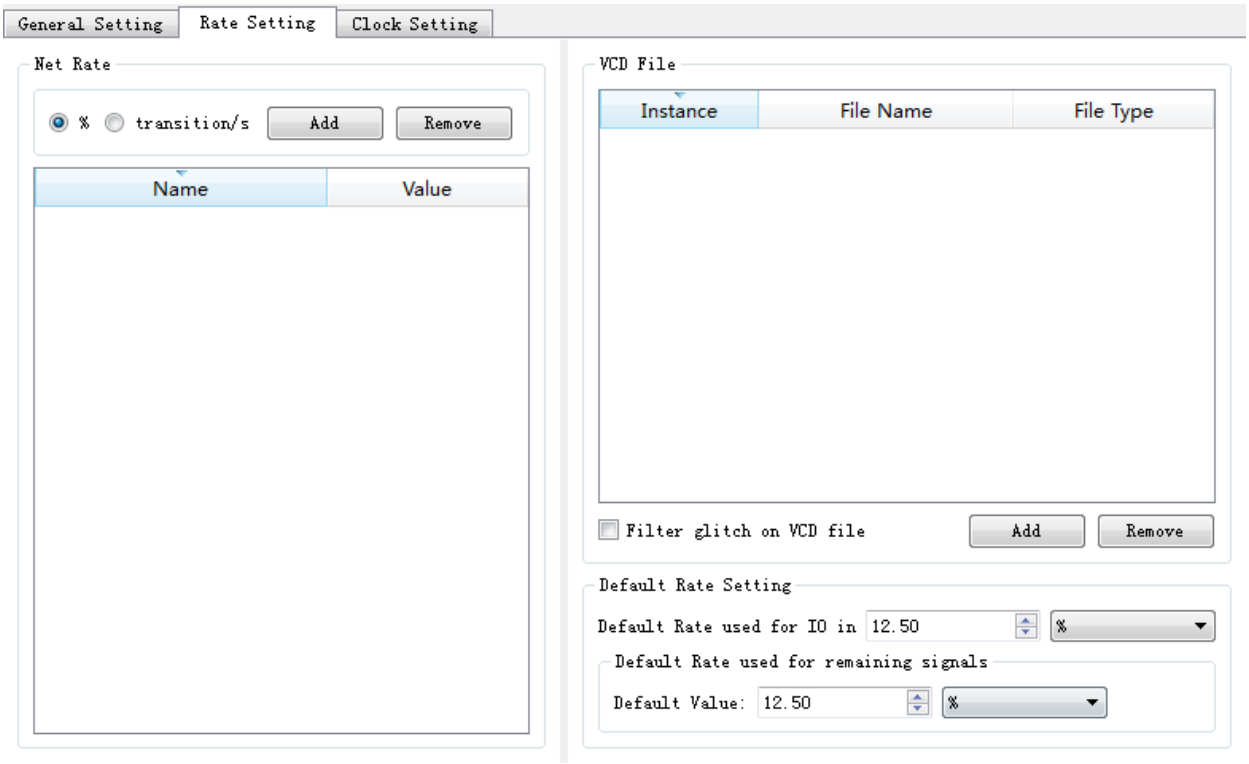
The description of each configuration is as follows:

- Net Rate is used to configure specified net toggle rate;
- VCD File is used to load waveform files generated by simulation;
- Default Rate Setting is used to configure general default toggle rate for IO and Net.

Note!

Net and IO toggle rate specified by users is of the highest priority, and the default IO and Net toggle rate is of the lowset priority.

Figure 3-12 Rate Setting View

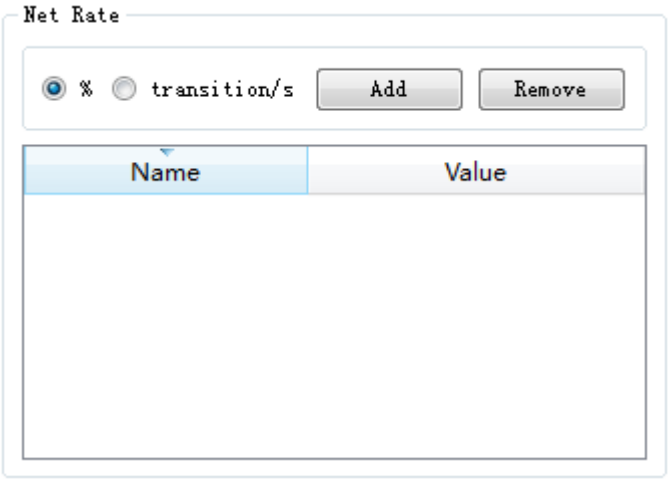


Specified Net Toggle Rate Configuration

Net Rate is used to set net signal toggle rate specified by users, as shown in Figure 3-13. Net toggle rate includes TOGGLE RATE mode and SIGNAL RATE mode.

Click "%" to select TOGGLE RATE mode; Or click "transition/s" to select SIGNAL RATE mode.

Figure 3-13 Net Rate Configuration



Note!

- TOGGLE RATE mode: The ratio of signal toggle rate to clock rate, and the unit is %;
- SIGNAL RATE mode: The signal toggle rate, and the unit is transition/s.

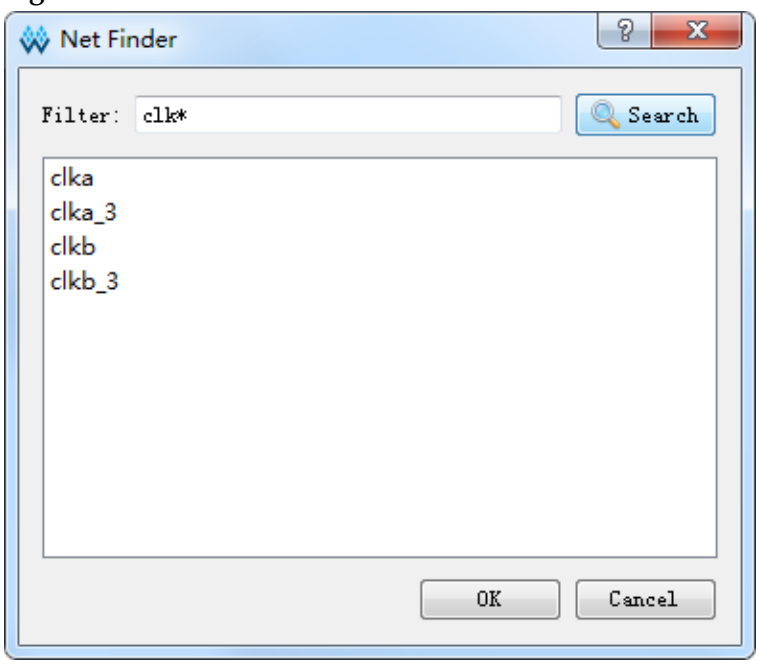
Select Net signal. The steps are as follows:

1. Click "Add" , and "Net Finder" dialog box pops up, as shown in Figure 3-14;
2. Enter net name in Filter, click "Search ";
3. Select the specified net in list;
4. Click ″OK″ to finish selecting net signal.

Note!

You can also right click in editing area and select "Add" in the pop-up menu.

Figure 3-14 Net Finder

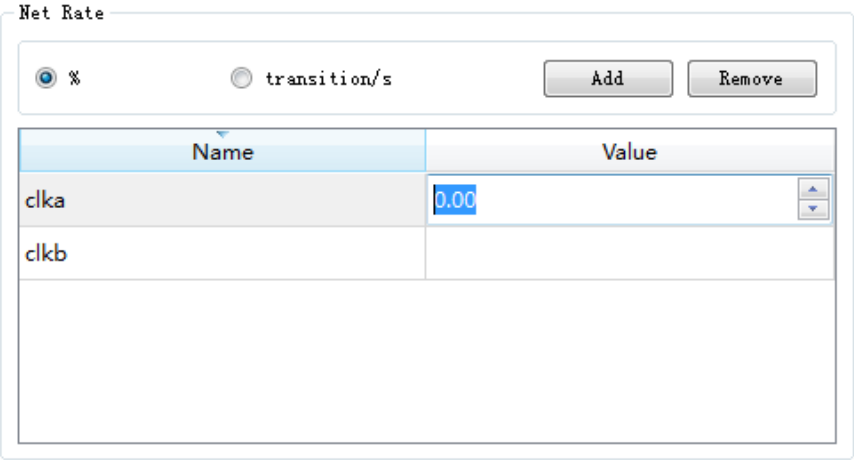


Note!

- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

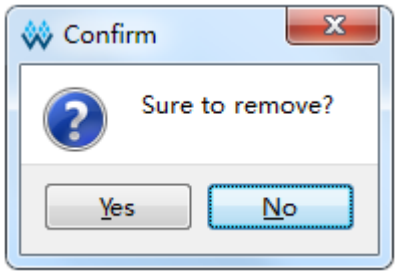
5. See Net signals in Net Rate table, and double-click the corresponding value column and enter signal toggle rate, as shown in Figure 3-15.

Figure 3-15 Set Net Toggle Rate



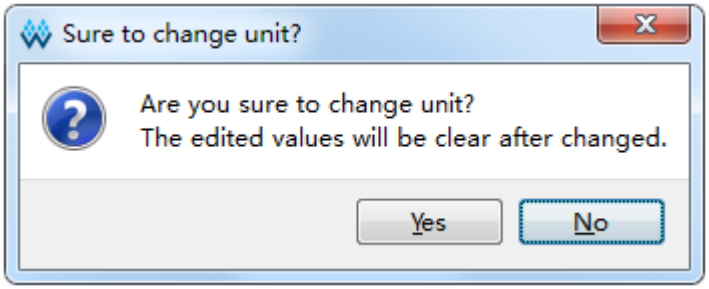
6. Select the row to be deleted in the editing area, and click "Remove" or right-click to select "Remove" in the pop-up menu. The "Confirm" dialog box will pop up, click "Yes" to delete the net toggle rate, as shown in Figure 3-16.

Figure 3-16 Delete Toggle Rate



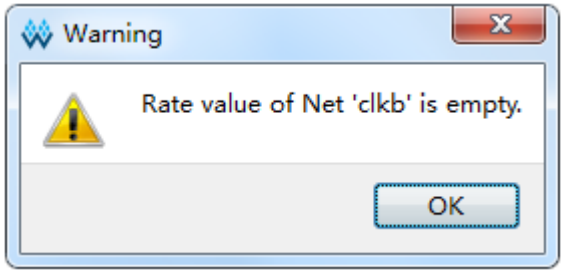
7. For the net toggle rate that has been set, the shift between TOGGLE RATE and SIGNAL RATE is not supported. If one of settings is selected, "Sure to change the unit" will pop up, as shown in Figure 3-17.

Figure 3-17 The Prompt



8. For the net added in the editing table, value should be set, or when clicking "save", a "Warning" dialog box will pop up, as shown in Figure 3-18.

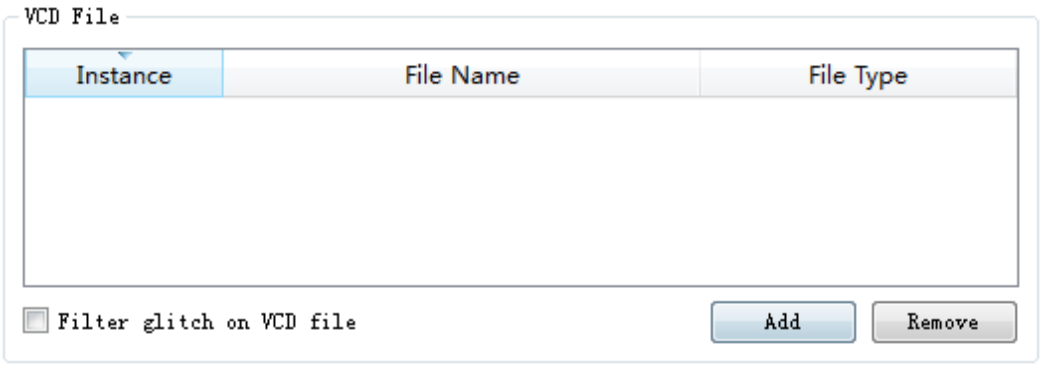
Figure 3-18 The Prompt



Load Waveform File Generated by Simulation

VCD File is used to load waveform files generated by simulation, as shown in Figure 3-19 . Waveform files are the basis for calculating IO and NET toggle rate. Two types of waveform files generated by VCS or modelsim simulation tools are supported: VCD (Value Change Dump) and SAIF (Switching Activity Interchange) files.

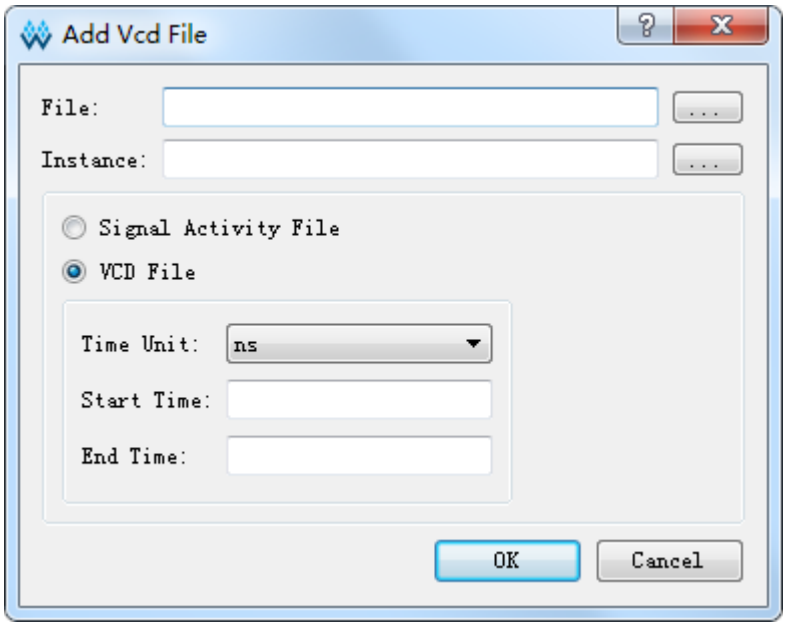
Figure 3-19 VCD File Configuration



The steps of loading the waveform files are as follows:

1. Click "Add", and "Add Vcd File" dialog box pops up, as shown in Figure 3-20;

Figure 3-20 Add Vcd File Dialog Box



Note!

You can also right-click in editing table and select "Add Input File" in the pop-up menu.

2. Click the "..." button on the right of "File", and the "Select VCD File" dialog box pops up, as shown in Figure 3-21 ; Select the *.vcd or *.saif file to be loaded and click "OK" to finish.
3. Click the "..." button on the right of "Instance", and the "Select Instance" dialog box pops up, as shown in Figure 3-22. Select the Instance to be loaded, and click the "OK".
4. If "File" loads *.saif file, select "Signal Activity File"; If "File" loads *.vcd file, select "VCD File";
5. When "VCD File" is selected, the time configuration is highlighted, and part of the time in the VCD File can be set as the basis for power analysis. Click the drop-down box at Time Unit and select s, ms, us, ns or ps in the drop-down list, as shown in Figure 3-23. Enter the start Time in the "Start Time" text box and the end time in the "End Time" text box.
6. Click the "OK" to complete the loading the waveform file. The configured Instance name, waveform File name, and File type are displayed in the VCD File configuration zone.
7. As shown in Figure 3-19, check the check box before "Filter glitch on VCD file" to filter out the glitches in the loaded waveform file.

Figure 3-21 Select VCD File Dialog Box

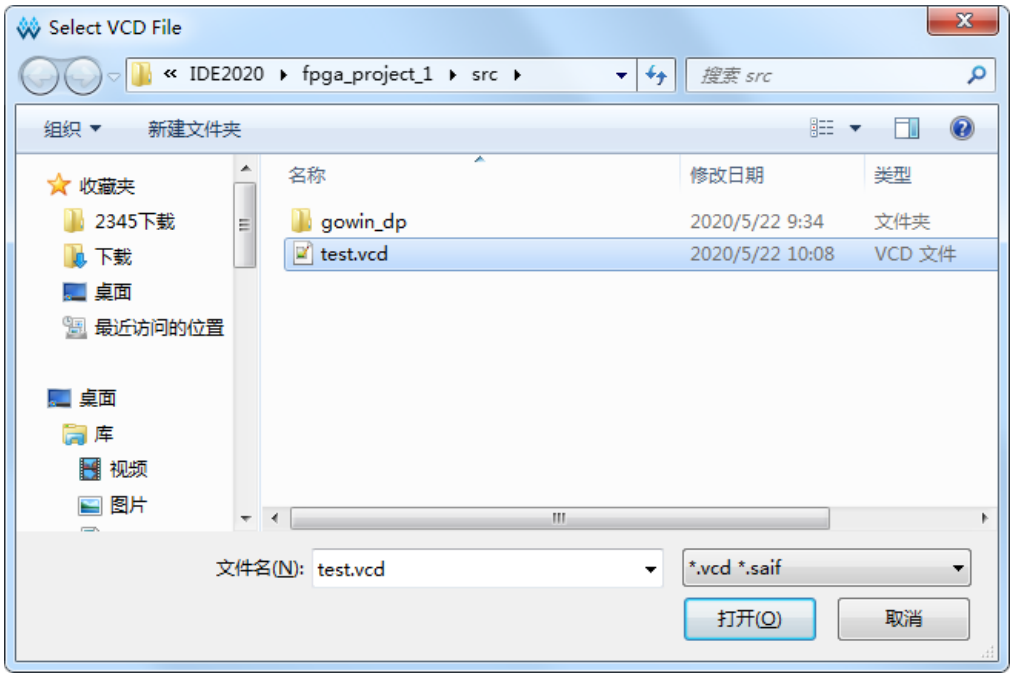


Figure 3-22 Select Instance Dialog Box

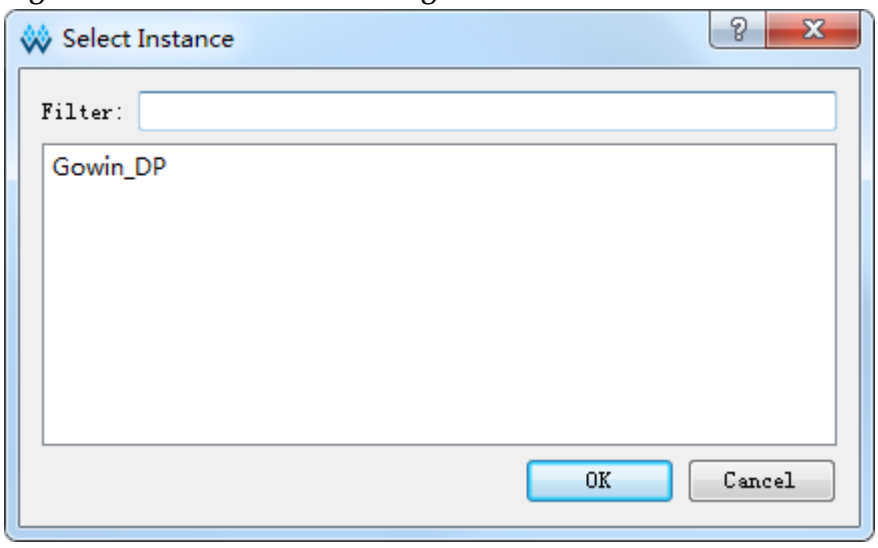
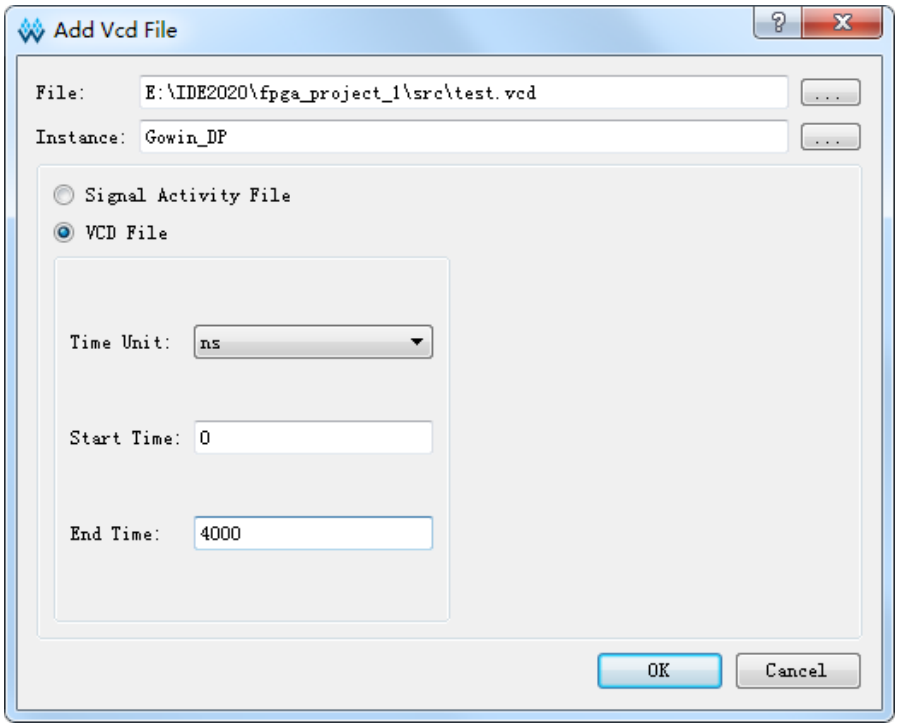


Figure 3-23 Set the Start and End Time of the Waveform File

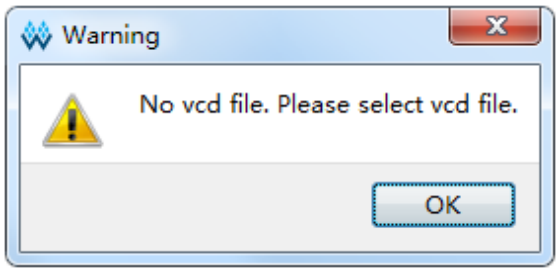


Note!

- "Signal Activity File" and "VCD File" are used for the specified type of loaded file, which should be consistent with the type of loaded waveform.
- When clicking the "Signal Activity File" button, the time unit and the start and end time is greyed.

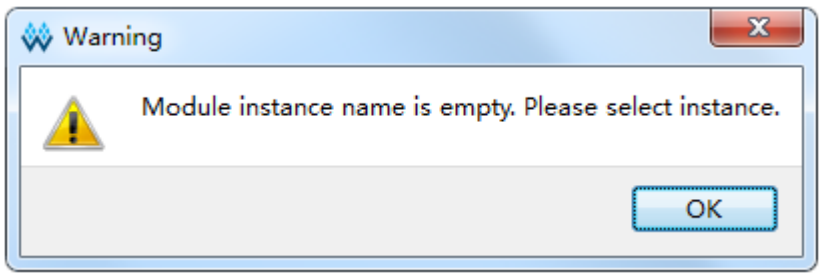
In the "Add Vcd File" dialog box, if the "File" configuration is empty, click the "OK" to pop up a prompt, as shown in Figure 3-24.

Figure 3-24 Prompt



In the "Add Vcd File" dialog box, if the "Instance" configuration is empty, click the "OK" to pop up a prompt, as shown in Figure 3-25.

Figure 3-25 Prompt



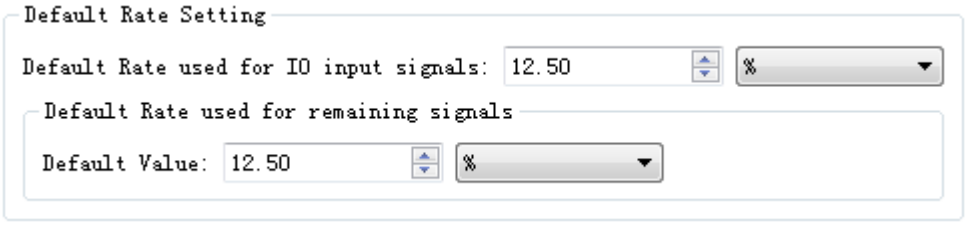
Global Default Toggle Rate Configuration

Default Rate Setting is used to set global default toggle rate of IO and Net signals, as shown in Figure 3-26.

Enter toggle rate in Default Rate used for IO input signals text box. Click the drop-down box on the right side and select the toggle rate unit "%" (TOGGLE RATE mode) or "transition/s" (SIGNAL RATE mode) in drop-down list.

Enter IO (except IO input signal) and unspecified net toggle rate in Default Rate used for remaining signals > Default Value text box, click the drop-down list on the right side and select toggle rate unit "%" (TOGGLE RATE mode) or "transition/s" (SIGNAL RATE mode).

Figure 3-26 Default Rate Setting Configuration



Note!

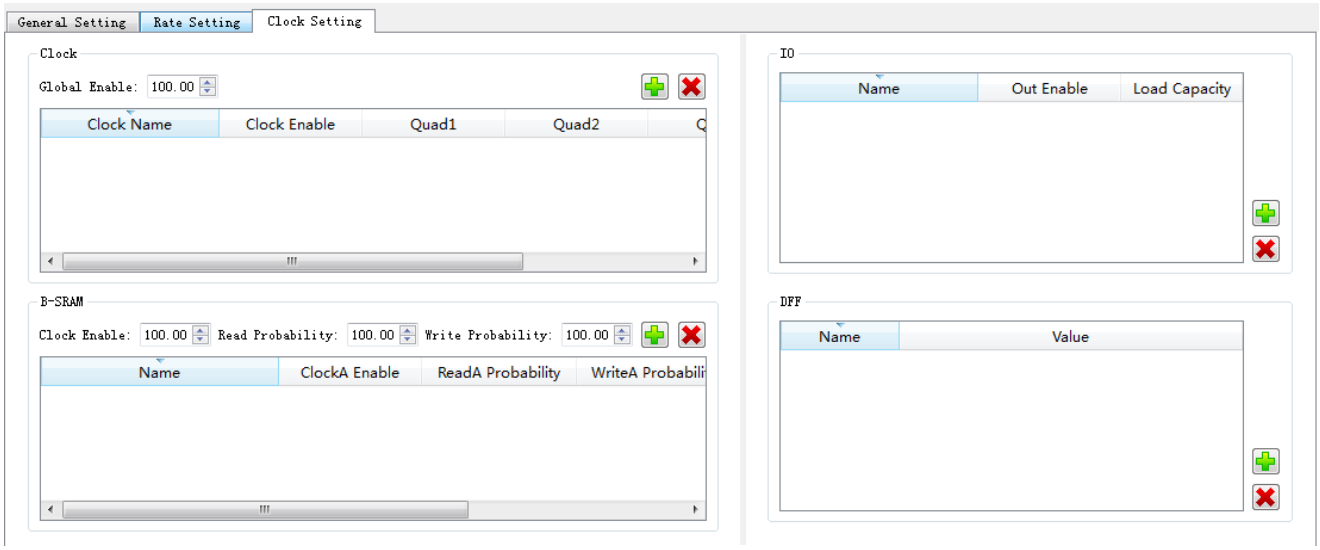
- TOGGLE RATE mode: The ratio of signal toggle rate to clock rate, unit: %;
- SIGNAL RATE mode: Toggle rate of signal, unit: transition/s;
- In other cases, toggle rate of IO and net is determined according to the priority in each configuration area.

3.2.3 Clock Enable Configuration

"Clock Setting" is used to configure clock and enable of B-SRAM, IO and DFF.

As shown in Figure 3-27, "Clock Setting" includes Clock, B-SRAM, IO and DFF.

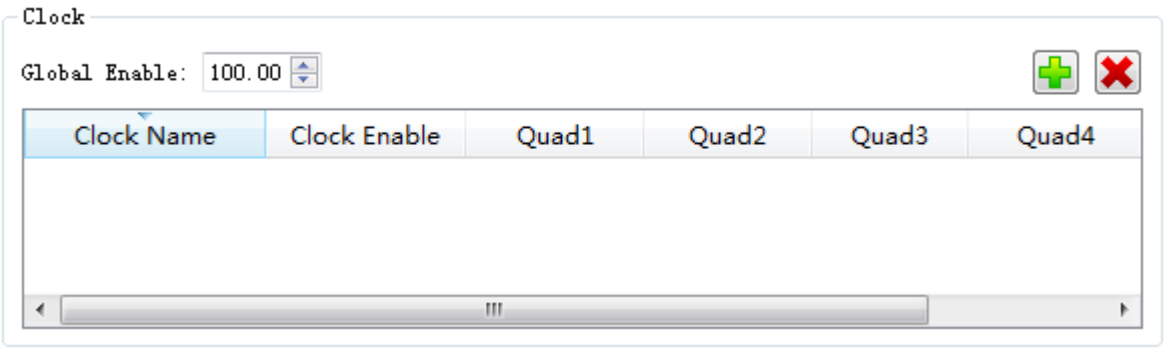
Figure 3-27 Clock Setting View



Clock Enable Configuration

"Clock" is used to configure clock enable, as shown in Figure 3-28. Clock is specified from SDC timing constraints file. Users can enable all clocks or the specified clock, or the clock in quadrant. The priority of settings is quadrant, specified clock, and clock global enable.

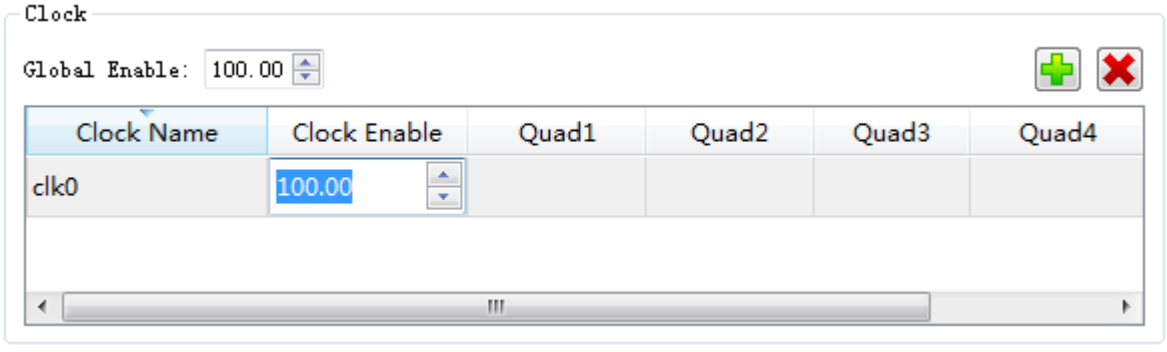
Figure 3-28 Clock Configuration



The steps are as follows:

1. Enter rate of global enable time percentage for all clocks in "Global Enable";
2. Click "  " to add a editable row, as shown in Figure 3-29;
3. Specify a row, double-click cell corresponding to "Clock Name" and enter clock Name;
4. Double-click the cell corresponding to "Clock Enable", enter rate of clock enable time;
5. Double click cells corresponding to "Quad1", "Quad2", "Quad3" and "Quad4", and set enable time rate of clock in 4 quadrants.

Figure 3-29 Clock Enable Configuration

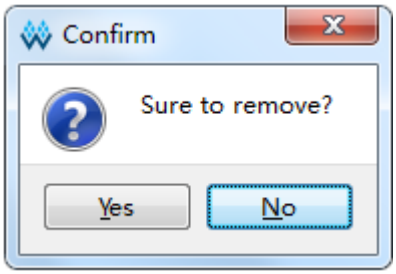


Note!

- You can also add an editable row by right clicking in the blank and selecting "Add" in menu.
- Clock Name should be consistent with the Name in SDC timing constraints file.

6. Select the row needed to be removed in editing area, click "  ", and "Confirm" dialog will pop up, as shown in Figure 3-30. Click "Yes" to remove.

Figure 3-30 Remove Clock Enable



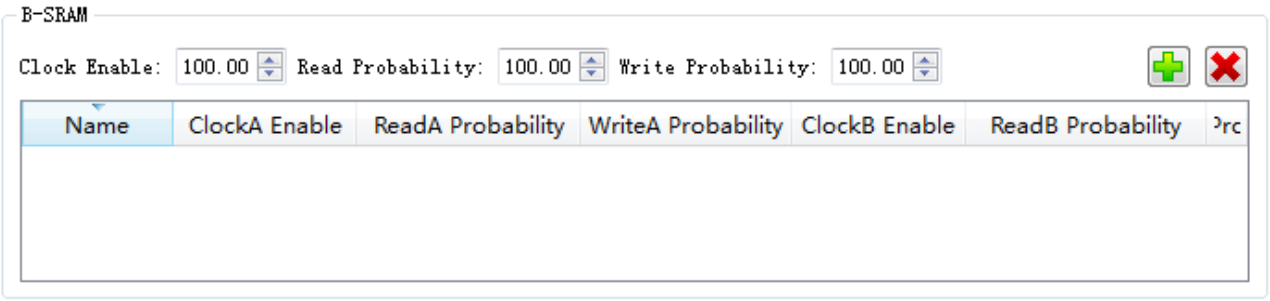
Note!

Right click and select "Remove" in menu, and "Confirm" pops up.

B-SRAM Enable Configuration

B-SRAM is used to set enable of B-SRAM clock and Read-Write, as shown in Figure 3-31. You can set global enable for all B-SRAM clocks and read-write, or for a specified B-SRAM. A single B-SRAM enable takes priority over all B-SRAM global enable setting.

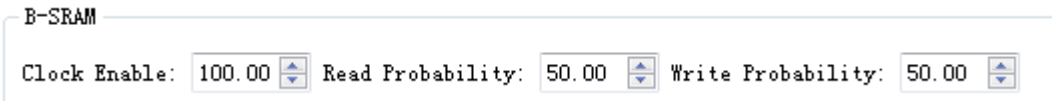
Figure 3-31 B-SRAM Configurtation



As shown in Figure 3-32, the relevant settings are as follows:

1. Enter rate of B-SRAM clock enable time in "Clock Enable";
2. Enter rate of B-SRAM read data time in "Read Probability";
3. Enter rate of B-SRAM write data time in "Write Probability".

Figure 3-32 Clock Enable for All B-SRAMs



Note!

- Clock Enable,Read Probability, and Write Probability parameters are valid for all B-SRAMs in design file;
- If B-SRAM has no read function, ignore Read Probability parameter; if no write function exists, ignore Write Probability parameter.

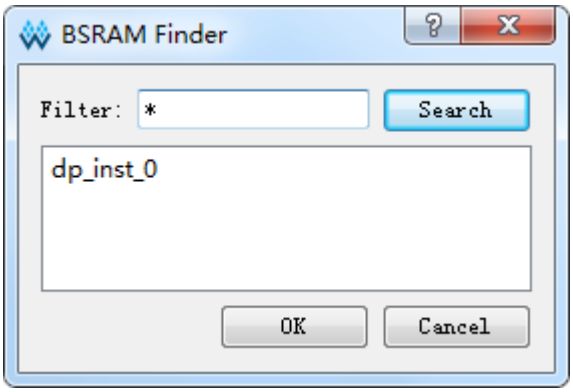
Set enable for the specified B-SRAM after adding.

Add B-SRAM

Click "  " and "BSRAM Finder" dialog will pop up, as shown in Figure 3-33; Enter the instance name of B-SRAM in Filter, and click "Search"; Select the specified B-SRAM in list, and click "OK" to finish adding

B-SRAM.

Figure 3-33 BSRAM Finder Enable



Note!

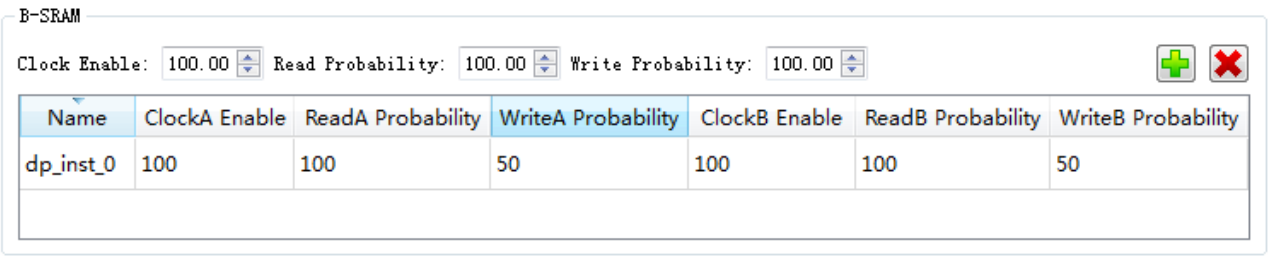
- You can also right-click in the blank of table and select "Add" in menu, and "BSRAM Finder" will pop up.
- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

B-SRAM Enable Configuration

See the instance name of added B-SRAM in B-SRAM table, as shown in Figure 3-34, and the steps are as follows:

1. Select a row, double-click cell corresponding to "ClockA Enable", enter the time percentage of B-SRAM CLKA enable;
2. Double-click the cell corresponding to "ReadA Probability", enter rate of B-SRAM CLKA read data time;
3. Double-click the cell corresponding to "WriteA Probability", enter rate of B-SRAM CLKA write data time;
4. Double-click the cell corresponding to "ClockB Enable", enter rate of B-SRAM CLKB enable time;
5. Double-click the cell corresponding to "ReadB Probability", enter rate of B-SRAM CLKB read data time;
6. Double-click the cell corresponding to "WriteB Probability", enter rate of B-SRAM CLKB write data time.

Figure 3-34 Specified B-SRAM Clock Enable



Note!

- If the specified B-SRAM has no read function of port A , ReadA Probability can not be edited. If there is no write function of port A, WriteA Probability can not be edited.

- If specified B-SRAM has no CLKB, the ClockB Enable can not be edited; if there is no read enable of B port, the ReadB Probability can not be edited; if there is no write enable of B port, the ReadB Probability can not be edited.

Remove B-SRAM Enable

1. Select the row needed to be removed in editing table, click "  ", and the "Confirm" dialog box will pop up, as shown in Figure 3-30;
2. Click "Yes" to remove B-SRAM Enable Setting.

Note!

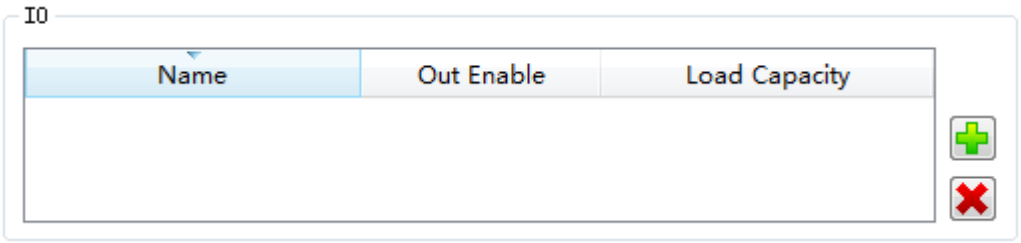
Right click to select "Remove" in menu, and "Confirm" pops up.

I/O Enable Configuration

"IO" is used to configure OEN enable and output load of I/O, as shown in Figure 3-35.

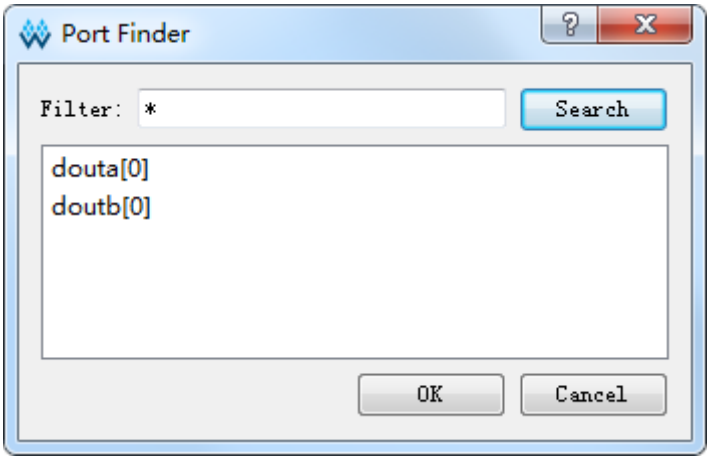
You can set OEN enable rate for PORT of single and differential IOBUF in design file to calculate I/O power consumption. If not specified, take the fault value "50%"; You can set BUF load capacitance value of TLVDS (pF) in the design file for calculating output power consumption, if not specified, take default value "5pF".

Figure 3-35 I/O Configuration



1. Click "  ", and "Port Finder" dialog box will pop up, as shown in Figure 3-36;
   a). Enter Port name in Filter and click "Search";
   b). Select the specified port in list, click "OK" to finish adding Port.

Figure 3-36 Port Finder



Note!

- You can also right click in the blank of table and select "Add" in menu. "Port Finder" dialog will pop up;
- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

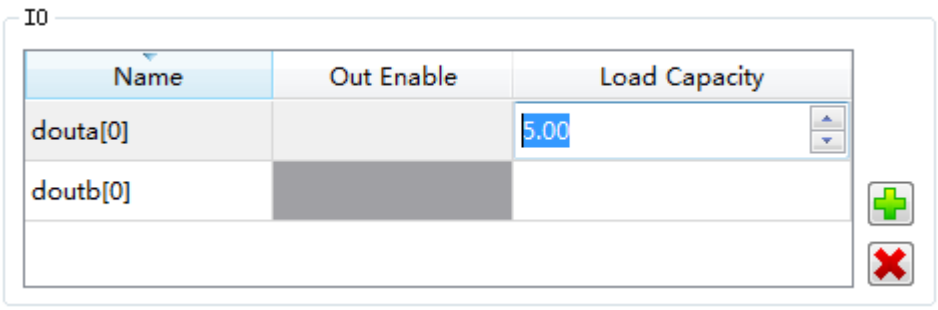
2. Specified I/O Enable Configuration

   a). See the added ports in table of I/O, as shown in Figure 3-37;

   b). Specify a row, double-click cell corresponding to "Out Enable", and enter rate of OEN enable time;

   c). Double-click cell corresponding to "Load Capacity", and enter load capacitance value.

Figure 3-37 Specified I/O Enable Configuration



Note!

If there is no OEN function for the specified BUF, "Out Enable" is not available.

3. Remove I/O Enable Setting

   a). Select the row needed to be removed in editing table, click "  ". "Confirm" dialog will pop up, as shown in Figure 3-30;

   b). Click "Yes" to remove I/O enable setting.

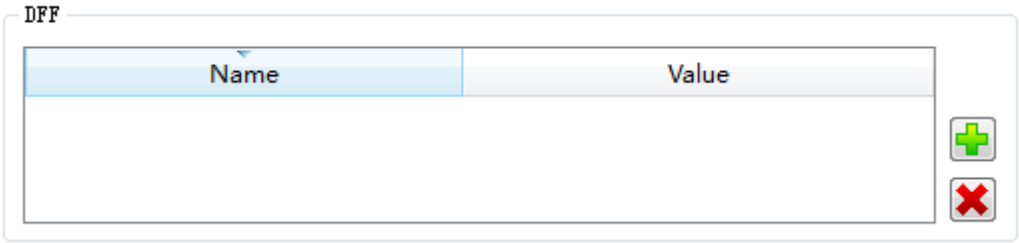
   Note!

You can also right click to select "Remove" in menu, and the "Confirm" dialog box will pop up.

DFF Enable Configuration

"DFF" is used to configure DFF clock enable, as shown in Figure 3-38.

Figure 3-38 DFF Configuration



1. Add DFF

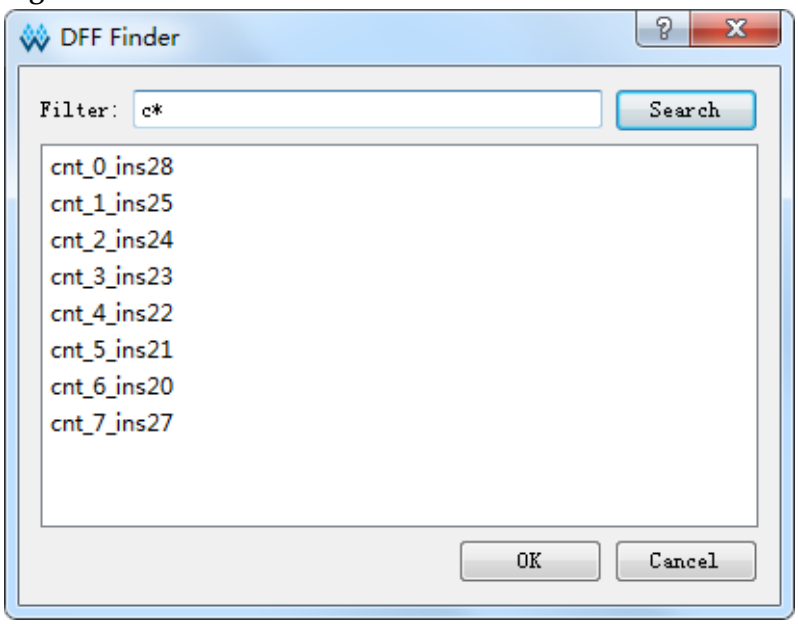
   a). Click "  " and "DFF Finder" dialog will pop up, as shown in Figure

3-39;

b). Enter instance name of DFF in Filter and click "Search";

c). Select the specified DFF in list and click "OK" to finish adding DFF.

Figure 3-39 DFF Finder



Note!

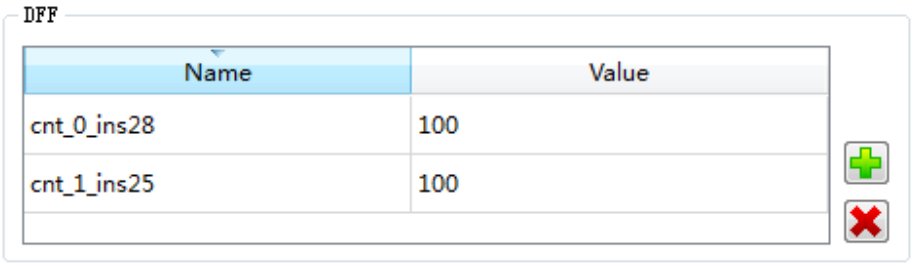
- You can also right-click in the blank of table, select "Add" in menu. "DFF Finder" dialog will pop-up;
- "Filter" supports wildcard screening;
- The list supports options of left-click, Shift + left, and Ctrl + left.

2. Specified DFF Enable Configuration

a). See instance name of the added DFF in DFF table, as shown in Figure 3-40;

b). Specify a row, double-click cell corresponding to "Value", and enter rate of DFF clock enable time.

Figure 3-40 Specified DFF Enable Configuration



3. Remove DFF clock enable setting

a). Select the row needed to be removed in editing table, click "  ", and the "Confirm" dialog box will pop up, as shown in Figure 3-30;

b). Click "Yes" to remove DFF clock enable.

Note!

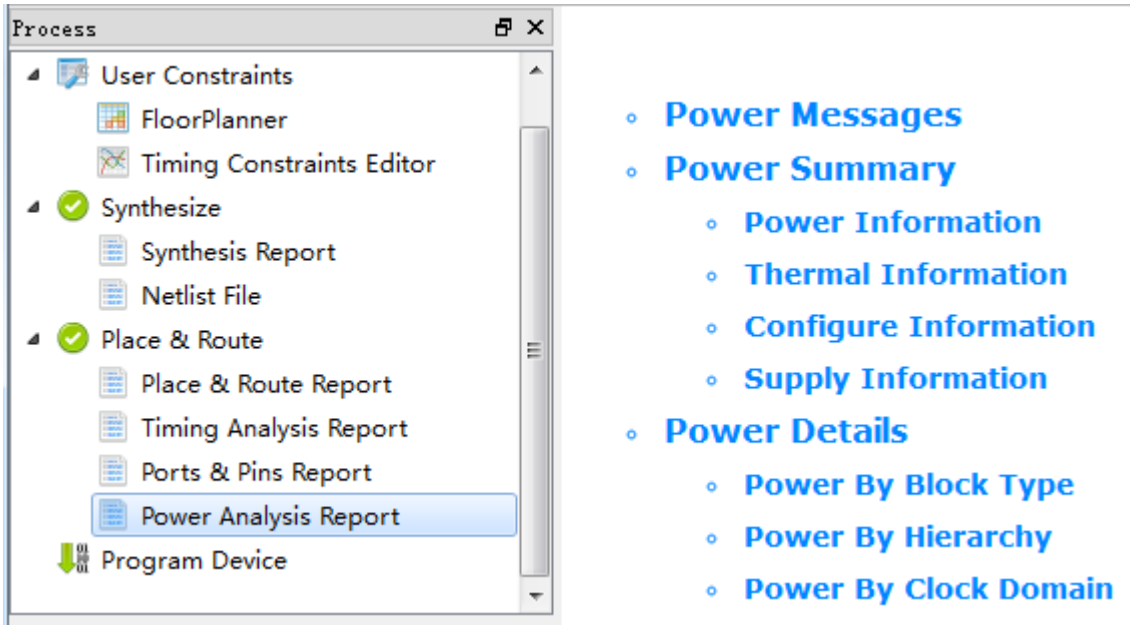
Right clicking and select "Remove" in menu, and "Confirm" pops up.

3.3 GPA Power Analysis Report

After configuring GPA, click "  " to save. Double-click "Place&Route" in Process to perform the place&route to generate GPA report.

Double-click "Place & Route > Power Analysis Report" in Process, GPA Report will pop up in main window, as shown in Figure 3-41.

Figure 3-41 Open GPA Report



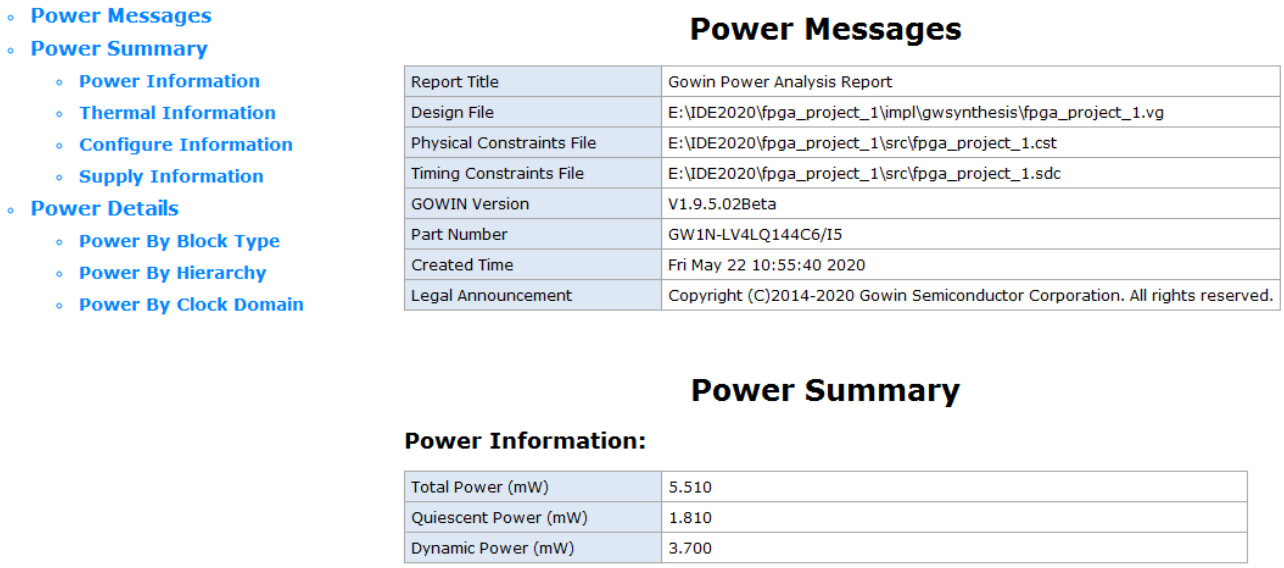
4 Power Analysis Report

GPA report shows the estimated result of power consumption calculated by the user-defined parameters, which helps users more easily to analyze and design power consumption.

GPA report includes two parts: Navigation tree and content, as shown in Figure 4-1. The navigation tree is used to hierarchically display report titles using hyperlinks with content, which helps users to find the required content more easily.

Power Analysis Report content is divided into three parts: Power Message, Power Summary and Power Details. Power Messages mainly introduces the device and design files; Power Summary mainly introduces parameters set by the user and power consumption. Power Detail mainly introduces the power consumption of Block type, design hierarchy, and clock domain.

Figure 4-1 GPA Report



4.1 Power Message

Power Message includes title, tool version, device type, package, speed, temperature range, process, user design name, design file, constraints file, power report file and created time, command line and legal announcement, as shown in Figure 4-2.

Figure 4-2 Power Message

Power Messages

Report Title	Gowin Power Analysis Report	(1)
Design File	E:\IDE2020\fpga_project_1\impl\gwsynthesis\fpga_project_1.vg	(2)
Physical Constraints File	E:\IDE2020\fpga_project_1\src\fpga_project_1.cst	(3)
Timing Constraints File	E:\IDE2020\fpga_project_1\src\fpga_project_1.sdc	(4)
GOWIN Version	V1.9.5.02Beta	(5)
Part Number	GW1N-LV4LQ144C6/I5	(6)
Created Time	Fri May 22 10:55:40 2020	(7)
Legal Announcement	Copyright (C)2014-2020 Gowin Semiconductor Corporation. All rights reserved.	(8)

（1）Report Title
（2）Design File
（3）Physical Constraints File
（4）Timing Constraints File
（5）Gowin version
（6）Part Number
（7）Created Time
（8）Legal Announcement

4.2 Power Summary

Power Summary includes Power Information, Thermal Information, Configure Information configuring, and Supply Information.

4.2.1 Power Information

Power Information is used to report total power consumption, total static power consumption, and total dynamic power consumption, as shown in Figure 4-3.

Figure 4-3 Power Information

Power Summary

Power Information:

Total Power (mW)	5.510
Quiescent Power (mW)	1.810
Dynamic Power (mW)	3.700

4.2.2 Thermal Information

Thermal Information is used to report junction temperature, Theta $\theta_{JA,}$

θ JB and allowed max. ambient temperature, as shown in Figure 4-4.

Figure 4-4 Thermal Information

Thermal Information:

Junction Temperature	25.031	(1)
Theta JA	7.250	(2)
Theta JB	25.000	(3)
Max Allowed Ambient Temperature	84.960	(4)

（1）Junction Temperature （2）θJA

（3）θJB （4）Max Allowed Ambient Temperature

Note!

- Junction Temperature: Operating temperature of die;
- Theta JA: thermal resistance θ_{JA}, dissipate heat from case to outside;
- When the ambient temperature set by the user is greater than the max. allowed ambient temperature, the junction temperature is marked red.

4.2.3 Configure Information

Configure Information is used for reporting default I/O toggle rate, default remain toggle rate, vectorless estimation, filter glitches, customized thermal θ_{JA}, air flow, heat sink, customized thermal θ_{SA}, board thermal model, customized thermal θ_{JB} and ambient temperature, as shown in Figure 4-5.

Figure 4-5 Configure Information

Configure Information:

Default IO Signal Rate	12.500	(1)
Default Remain Toggle Rate	0.125	(2)
Use Vectorless Estimation	false	(3)
Filter Glitches	false	(4)
Related Vcd File	E:\IDE2020\fpga_project_1\src\test.vcd	(5)
Related Saif File		(6)
Use Custom Theta JA	false	(7)
Air Flow	LFM_0	(8)
Heat Sink	Low Profile	(9)
Use Custom Theta SA	false	(10)
Board Thermal Model	None	(11)
Use Custom Theta JB	false	(12)
Ambient Temperature	25.000	(13)

（1）Default I/O signal toggle rate （2）Default Remain toggle rate

（3）Use *Vectorless* Estimation （4）Filter Glitches

（5）Related vcd files
（6）Related saif files
（7）Use Custom Thermal θ_{JA}
（8）Air Flow
（9）Heat Sink
（10）Use Custom Thermal θ_{SA}
（11）Board Thermal Model
（12）Use Custom Thermal θ_{JB}
（13）Ambient Temperature

4.2.4 Supply Information

Supply Information is used for reporting the voltage, dynamic current, static current and power consumption of core, reporting auxiliary voltage, dynamic current,static current and its power consumption, and reporting voltage, dynamic current, static current and power consumption of device output, as shown in Figure 4-6.

Figure 4-6 Supply Information

Supply Information:

Voltage Source	Voltage	Dynamic Current(mA)	Quiescent Current(mA)	Power(mW)
VCC	1.000	1.054	1.602	2.655
VCCX	3.300	0.182	0.088	0.890
VCCO18	1.800	0.181	0.087	0.483

4.3 Power Details

Power Details include Power By Block Type, Power By Hierarchy and Power By Clock Domain.

4.3.1 Power By Block Type

Power By Block Type reports total power consumption of Blocks, static power, and average toggle rate included in file according to Block, as shown in Figure 4-7. Block includes Logic, I/O, B-SRAM, DSP, PLL, DLL, DQS, DLLDLY and so on.

Figure 4-7 Power By Block Type

Power Details

Power By Block Type:

Block Type	Total Power(mW)	Static Power(mW)	Average Toggle Rate(millions of transitions/sec)
IO	1.624	0.296	23.438
BSRAM	2.033	NA	NA

Note!

NA indicates that the parameter is not considered.

4.3.2 Power By Hierarchy

Power By Hierarchy is used for reporting total power consumption, dynamic power consumption and route resources power consumption generated from top to bottom module in design file, as shown in Figure 4-8.

Figure 4-8 Power By Hierarchy

Power By Hierarchy:

Hierarchy Entity	Total Power(mW)	Block Dynamic Power(mW)	Routing Dynamic Power(mW)
top	2.235	1.830(1.830)	0.406(0.034)
top/dp_inst1/	1.864	1.830(0.000)	0.034(0.000)

4.3.3 Power By Clock Domain

Power By Clock Domain is used for reporting the name, frequency, and dynamic power consumption of clock based on Clock Domain, as shown in Figure 4-9.

Figure 4-9 Power By Clock Domain

Power By Clock Domain:

Clock Domain	Clock Frequency(Mhz)	Total Dynamic Power(mW)
DEFAULT_CLK	100.000	2.373

Appendix A Calculation Principle for Junction Temperature

Junction temperature (TJ) refers to the operating temperature of die, which is determined by ambient temperature (TA), power consumption (P) and heat sink features of chip and outside. The temperature of die is balanced by heat sink and ambient environment. Heat sink includes two types: heat sink and 0 no heat sink.

- No heat sink

The model mainly dissipates heat 0 through development board and CASE. Thermal impedance (θ_{JA}) means rising temperature corresponding to power consumption (℃ / W), which is influenced by air flow; In no heat sink mode, The relationships between power P and thermal impedance θ_{JA}, TJ, TA are shown in Formula 1.

$$P = (TJ - TA) / \theta_{JA} \text{ (Formula 1)}$$

- Heat Sink

Chip dissipates heat by heat sink , and the total thermal impedance of it is called θ_{JA}. Chip dissipates heat by board thermal, and the thermal impedance of it is called θ JB.

θ_{JA} consists of three parts: thermal impedance theta θ_{JC} from chip to case, thermal impedance θ_{CS} from case to heat sink, and thermal impedance θ_{SA} from heat sink to ambient environment. The calculation formula is as follow:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \text{ (Formula 2)}$$

The relationship between power P and thermal impedance θ_{JA}, TJ, TA, TB (board temperature) is shown in formula 3:

$$P = (TJ - TA) / \theta_{JA} + (TJ - TB) / \theta_{JB} \text{ (Formula 3)}$$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