Gowin Software

User Guide

SUG100-2.4E,09/01/2020

Disclaimer

Revision History

Date	Version	Description
11/08/2019	2.0E	● Synplify Pro configuration options added; ● Synplify Pro attributes and the value of directives added.
11/28/2019	2.1E	● General option added in Place & Route: Promote Physical Constraint Warning to Error, Report Auto-Placed IO Information, Place Option, Route Option; ● Resource information display added in Hierarchy view; ● Three "Find" options supported in netlist file in Process view; ● Function of adding and removing comments supported in IDE built-in editor.
03/09/2020	2.2E	● VHDL is supported in Hierarchy view; ● GowinSynthesis supports the synthesis of VHDL and the mixed language of Verilog and VHDL. ● Pop-up reminder added when the unsaved project is performed synthesis or PnR process. ● The introduction to tcl command usage added in Output view. ● The description of Synthesize PnR configuration options added. ● The introduction to the editor of User Flash initialization file added.
05/13/2020	2.3E	● Unused Pin configuration added; ● Encryption function added in Hierarchy view.
09/01/2020	2.4E	● Schematic Viewer added; ● Hierarchy window updated; ● Enable Daisy Chain Bypass added.

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1 About This Guide

1.1 Purpose

This manual describes Gowin software installation and operation and is designed to help users be familiar with the flow and improve design efficiency. The software screenshots and the supported products listed in this manual are based on 1.9.7Beta. As the software is subject to change without notice, some information may not remain relevant and may need to be adjusted according to the software that is in use.

1.2 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS100, GW1N series of FPGA Products Data Sheet
2. DS117, GW1NR series of FPGA Products Data Sheet
3. DS821, GW1NR series of FPGA Products Data Sheet
4. DS102, GW2A series of FPGA Products Data Sheet
5. DS226, GW2AR series of FPGA Products Data Sheet
6. DS841, GW1NR series of FPGA Products Data Sheet
7. DS861, GW1NR series of FPGA Products Data Sheet
8. DS871, GW1NSE series of FPGA Products Data Sheet
9. DS891, GW1NR series of FPGA Products Data Sheet
10. SUG940, Gowin Design Timing Constraints User Guide
11. SUG935, Gowin Design Physical Constraints User Guide
12. SUG113, Gowin FPGA Design Guide
13. SUG114, Gowin Analyzer Oscilloscope User Guide
14. SUG282, Gowin Power Analyzer User Guide
15. UG285, Gowin BSRAM & SSRAM User Guide

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
CRC	Cyclic Redundancy Check
FPGA	Field Programmable Gate Array
GowinSynthesis	GowinSynthesis
IP Core	Intellectual Property Core
PnR	Place & Route
GAO	Gowin Analyzer Oscilloscope
GPA	Power analyzer

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail：support@gowinsemi.com

2 General Description

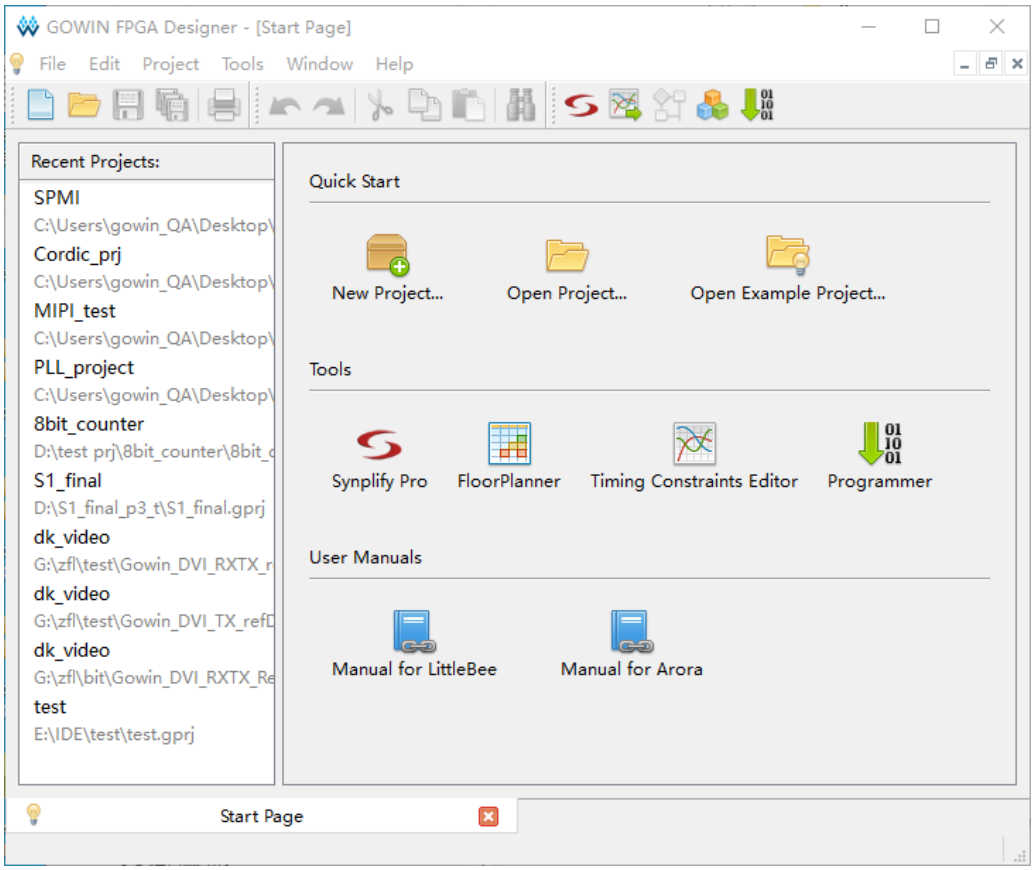
2.1 Introduction

Gowin software is an integrated circuit design and implementation tool for Gowin FPGA chip. It provides a complete FPGA design and verification environment based on GUI, integrating the design tools from the HDL to the FPGA bit stream (bitstream) download. It is easy to use with rich functions and the excellent performance.

Gowin software supports all functions of Gowin FPGA chips and has optimized for Gowin devices. The built-in Synplify Pro supports high-performance logic design and synthesis. The software supports VHDL, Verilog and system verilog, resource analysis and optimization, hierarchical and flatten input and output. The software supports to generate timing constraints, physical constraints and power analysis reports.

To meet the different requirements of users, you can choose either command line mode or GUI mode. Using script design, any single module can be designed flexibly without affecting the whole design flow. Moreover, Gowin Software integrates IP Core Generator for quickly implementation of complex designs and Gowin Analysis Oscilloscope for debugging. The software supports Linux and Windows. It can quickly start the FPGA download tool to download the bit stream file to the chip, and realize the function of user design. It is a complete EDA tool chain. Gowin Software interface is as shown in Figure 2-1.

Figure 2-1 GUI



2.2 Supported Devices

Gowin software supports the LittleBee family and Arora family chips. For the chip type, resources and package, etc., you can visit Gowin official website.

- LittleBee® family: www.gowinsemi.com/en
- Arora family: www.gowinsemi.com/en

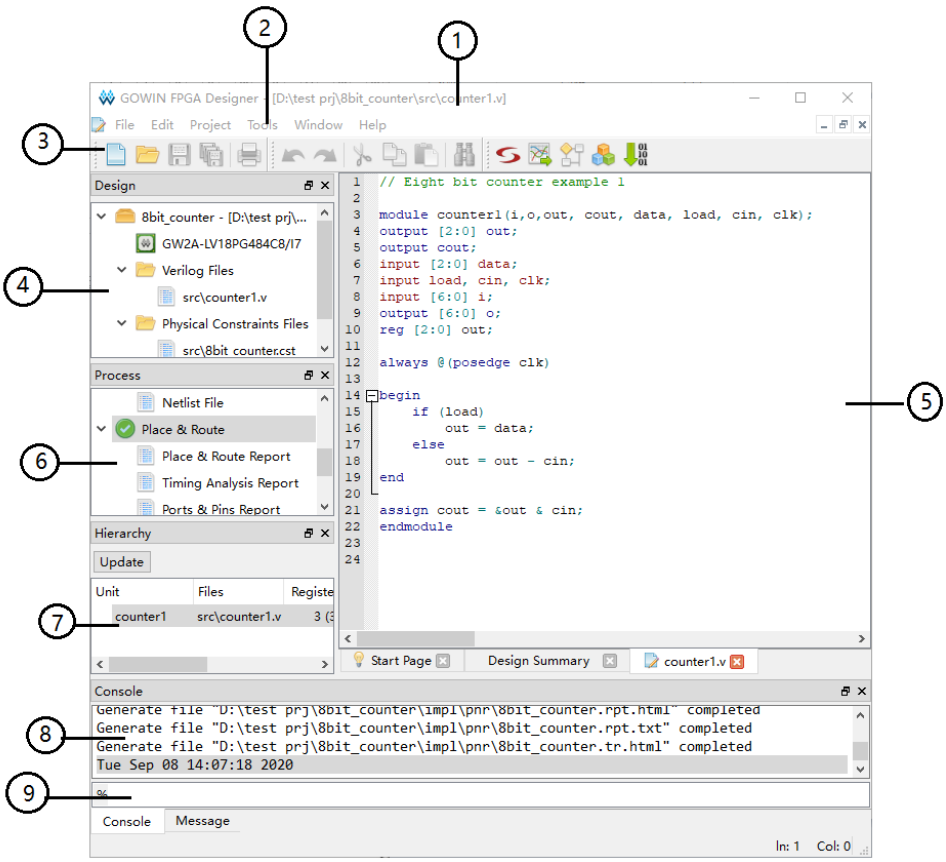
Note!

The supported devices may vary according to the software version in use. Please refer to the software you use for more detailed device information.

3 Gowin Software GUI

Gowin software GUI is as shown in Figure 3-1. It consists of the title bar, menu bar, tool bar, project area (Design View), process area (Process View), source file editing area, hierarchy area, information output area and TCL command editing area.

Figure 3-1 GUI



① Title Bar
② Menu Bar
③ Tool Bar
④ Project Area
⑤ Source File Editing Area
⑥ Process Area
⑦ Hierarchy Area
⑧ Information Output area
⑨ TCL Command Editing Area

3.1 Title Bar

Title bar shows the current project path, name, and the files opened.

3.2 Menu Bar

The menu bar contains links to the tools and functionality that are commonly used in projects, including the File, Edit, Project, Tools, Window, and Help options. See the following for details.

3.2.1 File

- New: Create a new file and project;
- Open: Open a new file and project;
- Save: Save the project files;
- Save As…: Save as the project files;
- Save All: Save all the project files;
- Close: Close projects or the file and page in project;
- Close All: Close all project files and pages;
- Close Project: Close the current project;
- Print Preview: Print preview;
- Print: Print
- Recent Files: Show the files opened. Users can click on the names of these files to re-open;
- Recent Projects: Show the projects opened. The user can click on the names of these projects to re-open;
- Exit: Exit and close Gowin software.

3.2.2 Edit

- Undo: Undo your last operation;
- Redo: Redo your last operation;
- Cut: Cut;
- Copy: Copy;
- Paste: Paste;
- Select All: Select all;
- Find: Find or repalce key words;
- Toggle Comment Selection: Add comments to the selected;
- Macros: Macros.

3.2.3 Project

- Archive Project: Archive project;
- Restore Archived Project: Restore archived project;
- Set Incremental: Set incremental;
- Set Device: Set device of current project;

- Configuration: Open configuration interface;
- Design Summary: Show details of current project.

3.2.4 Tools

- Start Page: Start page;
- Synplify Pro: Front-end synthesis software;
- Gowin Analyzer Oscilloscope: Gowin Analyzer Oscilloscope;
- Schematic Viewer: View schematic
- IP Core Generator: IP Core Generator;
- Programmer: FPGA programmer;
- FloorPlanner: FloorPlanner;
- Timing Constraints Editor: Timing Constraints Editor;
- Options: Open the required tools, set IDE parameters or set Synplify Pro path.

Note!

For the Synplify Pro options in "Options" view, if "Custom" is selected, the local defined Synplify Pro will be used whether the software will be updated or not; if "Default" is selected, the SynplifyPro in the current software path will be used.

3.2.5 Window

- Full Screen: Full screen;
- Tile: Tile display;
- Cascade: Cascade display;
- Reset Layout: Restore initial settings;
- Panels: Select whether to display GUI models or not;
- Start Page: Display start page in source file editing;
- Design Summary: Display design page in source file editing.

3.2.6 Help

- View Help: View help documents;
- Contact Us: Click to contact us;
- Manage License: Manage license;
- About: Show software version and copyright information.

3.3 Tool Bar

It provides quick access to some commonly used functions and the buttons from left to right are:

- "  ": New File or Project
- "  ": Open File or Project
- "  ": Save the file.
- "  ": Save all the project files

- "  ": Print
- "  ": Undo your last operation
- "  ": Redo your last operation
- "  ": Cut
- "  ": Copy
- "  ": Paste
- "  ": Find
- "  ": Synplify Pro
- "  ": Gowin Analyzer Oscilloscope
- "  ": Schematic Viewer
- "  ": IP Core Generator
- "  ": Programmer

3.4 Project Area (Design)

The project area shows projects and the related files. Users can check or change the project device information, user design files, user constraints files, configuration files, etc.

3.5 Process Area (Process)

The process provides FPGA design flow, including synthesis, place & route, and download bitstream files (program device). Users can also double-click timing constraints editor and physical constraints editor to edit the constraints files.

3.6 Hierarchical Area (Hierarchy)

After loading the design files, software will parse the design files first. The hierarchy window shows the hierarchy of current project. The Unit column shows module hierarchy of the design files. The Files column shows the file where the module definition is. Hierarchy has supported Verilog, VHDL and System Verilog. Functions supported in the right-click list in the Hierarchy window are as follows:

- Goto Module Instantiation: Go to the instance module in the source file and open it with the editor built in Gowin software.
- Goto Module Instantiation With…: Go to the instance module in the source file and open it with a third-party editor;
- Goto Module Definition: Go to the module in the source file and open it with the editor built in Gowin software.
- Goto Module Definition With…: Go to the module in the source file and open it with a third-party editor;
- Pack User Design: Pack the module and its sub-module.

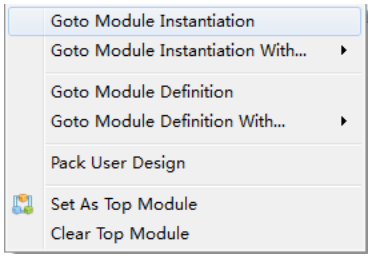
- Set As Top Module: Set the module to top module;
- Clear Top Module: Clear the top module setting.

If there is an error in hierarchy parse of the project file, the options of "Hierarchy panel error" marked in red will be displayed at the top right of the hierarchy window.

The Hierarchy view allows you to locate the definition and instance of a module in a design file. You can also set a module to top module.

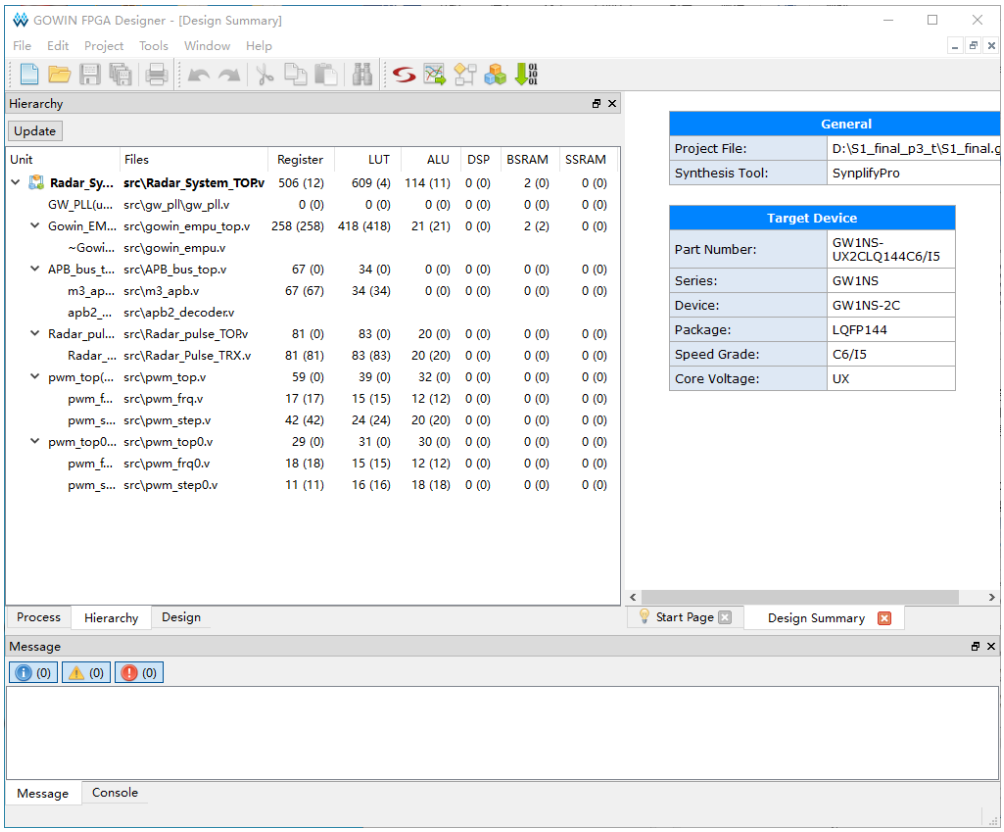
- Click one module. You can locate the module definition and instance in the design file by "Goto Module Instantiation" and "Goto Module Definition" in the right-click menu.
- When locating a module in a design file, you can open it with the default editor or with a third-party editor. The third-party editor is in the list and you can add external editor by "Add External Editor" option, as shown in Figure 3-2. If you select "Add External Editor", the "External Editor" GUI pops up. If "Always Use External Editor" is checked, you can double-click the design file in Hierarchy view to open it with a third-party editor by default.
- In the hierarchy view, every module supports "Set As Top Module" by right-clicking. The module set as the top will be marked "  " to indicate that the current module is the top module, and the original hierarchy remains unchanged.

Figure 3-2 Right-click of Hierarchy



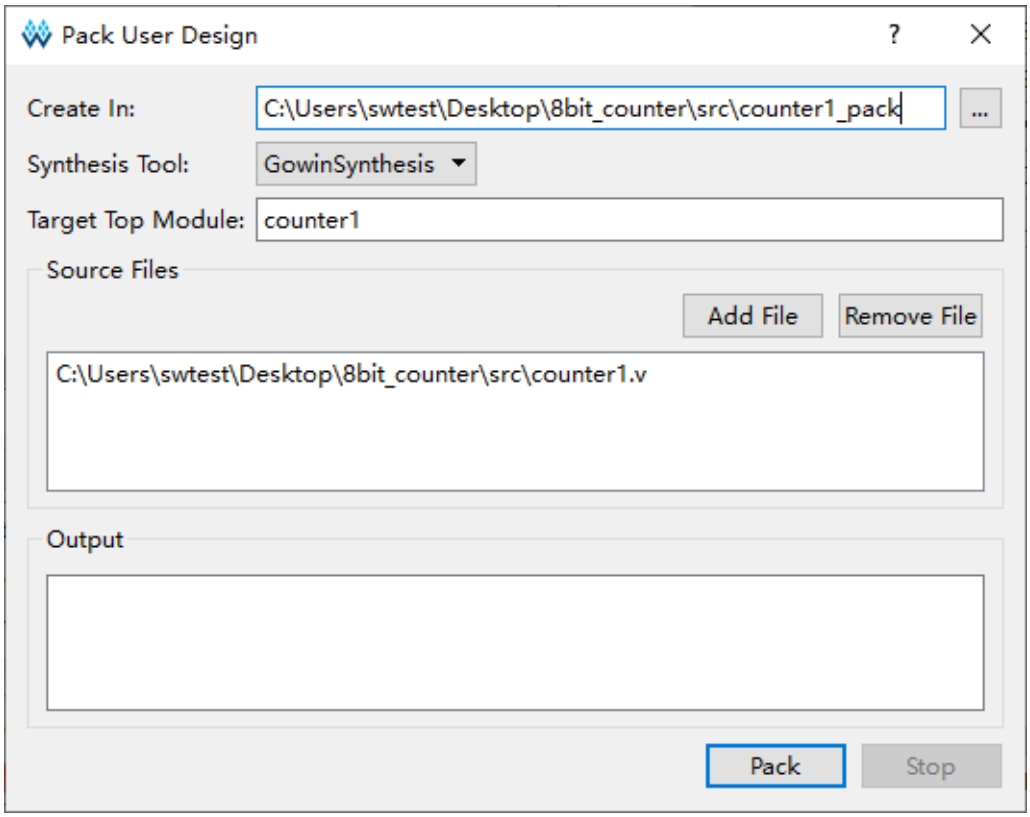
The Hierarchy view will automatically display the resources of the current project after synthesis, as shown in Figure 3-3. If a module is defined as a pack module in the design, its resource is not displayed, and its resource will be counted in its upper module. The resources used by each module wil be displayed in two data. As shown in Figure 3-3, the number of register is 506 (12), where 12 is the number of register used by the module itself and 506 is the total number of register used by the module and its sub-modules.

Figure 3-3 Resources Display in Hierarchy View



When you open the project, you can generate a pack file after synthesis for the source file of the selected top module and sub module in Hierarchy. Right-click the module to be packed in the Hierarchy view, and you can select "Pack User Design" to open the view, as shown in Figure 3-4.

Figure 3-4 Pack User Design View



The configuration options are as follows:

- Create In: The path of the generating packed files. The default path is \src\<topmodule_name>_pack.
- Synthesis Tool: Select a synthesis tool. The drop-down list supports GowinSynthesis and Synplify_pro. The default is GowinSynthesis.
- Target Top Module: Top module to pack. The default is the module selected in the Hierarchy view. You can modify it.
- Source Files: List the source files of module and sub module selected in the Hierarchy view.
- Add File: Add file
- Remove File: Remove file
- Output window: Output information
- Pack button: Pack
- Stop: Stop pack

Information will be printed in the Output window, as shown in Figure 3-5. When pack starts, if there is an error, the error will be displayed in the Output window, and the information of pack failure will be printed, as shown in Figure 3-6.

Figure 3-5 Output Information in Pack User Design View

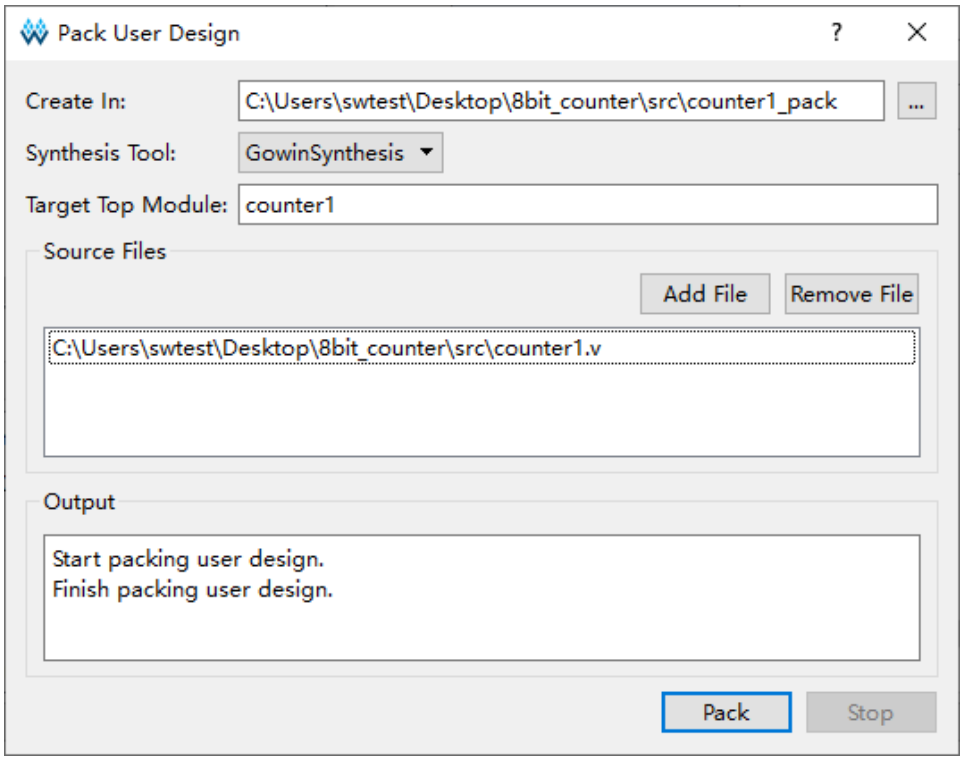
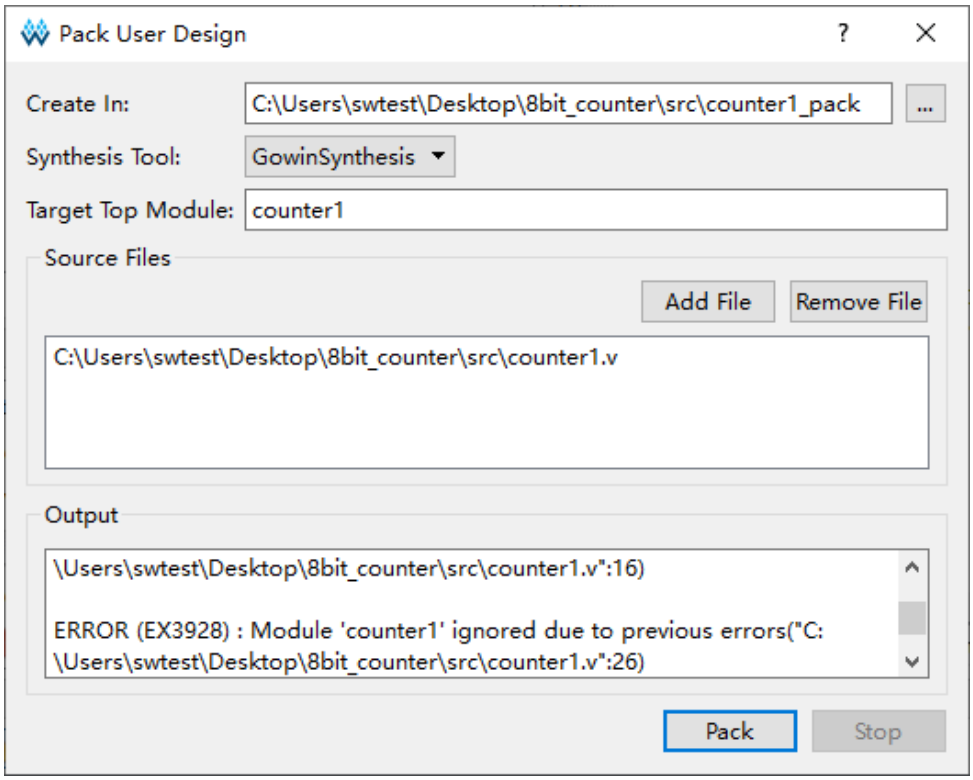


Figure 3-6 Error Prompt



After pack, two files are generated under the target path: <topmodule_name>_gowin.vp and <topmodule_name>_sim.v. <topmodule_name>_gowin.vp is a pack file and can be used by others. <topmodule_name>_sim.v is a plain netlist that can be used for internal

simulation.

3.7 Source File Editing Area

Users can view, edit and highlight source files in the source file editing area.

The source file editing area shows different files, including new files or opened files, the generated files after synthesis or Place & Route, the "Start Page" and "Design Summary".

If the file currently displayed is modified, "File Changed" will pop up in the file editing area. Select "Reload" to reload the file.

To close the file currently displayed, click "File > Close", or click on the icon " " in the file editing area.

To close all the files in the file editing area, click "File > Close All".

Open the generated netlist file, and you can open "Find & Replace" view by shortcut ctrl+f or clicking "Find" in the toolbar. There are three options in "Find All": Current File, Open Files and Current Project, as shown in Figure 3-7. After clicking "Find All", "Search Result" view will pop up in software and the search content will be highlighted, as shown in Figure 3-8.

Figure 3-7 Find & Replace

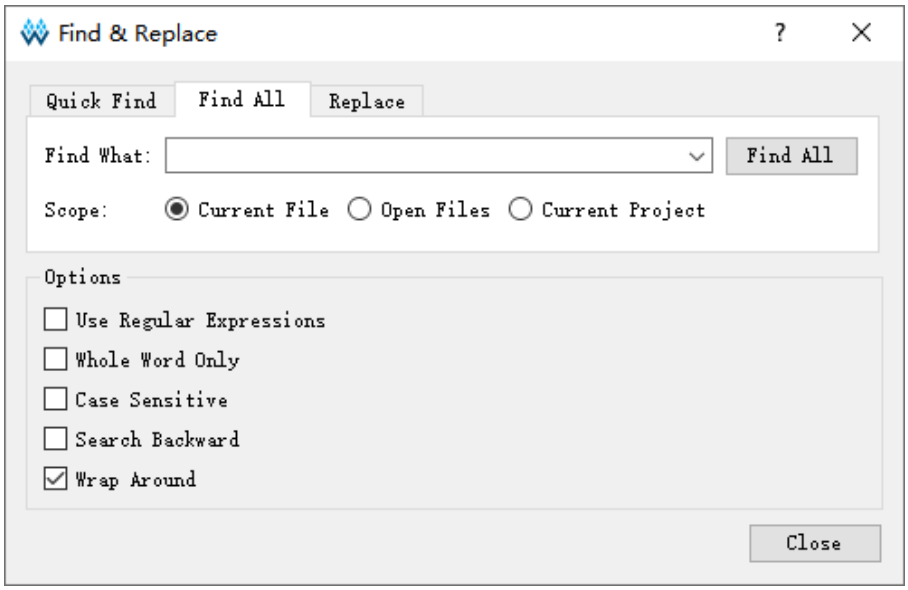
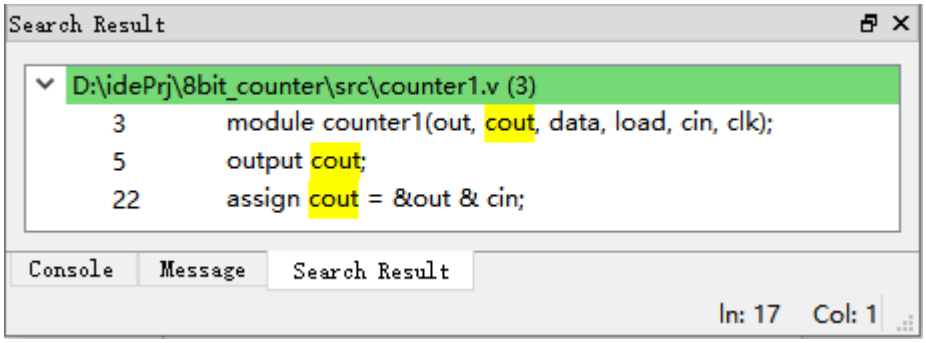


Figure 3-8 Search Result



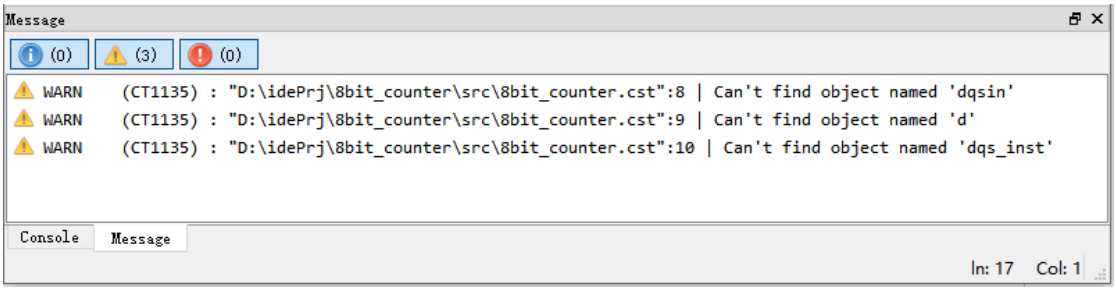
3.8 Information Output area

The information output area displays the processing information when the software is running. Users can view different outputs by manually switching between the tabs:

- Console page includes tcl commands, warnings, errors , etc.;
- Message page includes notes, warnings, errors.

In Console page, right-click and select "Clear" to clear all the information in the tab. Message page includes notes, warnings, errors. Users can configure the message page to display notes only, warnings only or errors only. The number of notes, warnings and errors will be recorded and shown on each of the corresponding tabs, as shown in Figure 3-9. Right-click and select "Clear" on "Message" page to clear the page information.

Figure 3-9 Information Output area



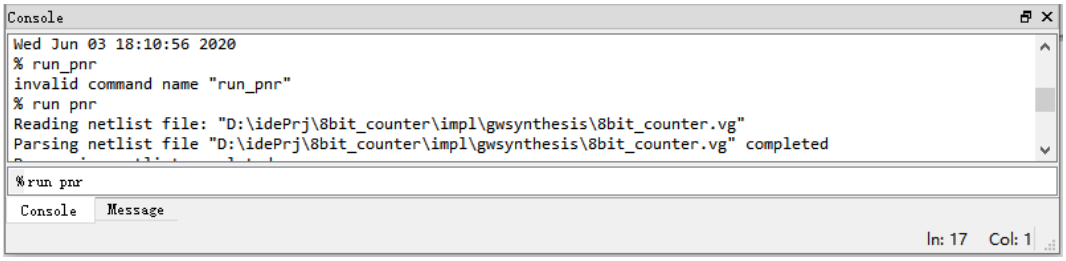
After selecting certain Error or Warning message reported by PnR, right-click and select "Help" or press the shortcut key "F1", the "GOWIN Help" of this error or warning will pop up, and the help information of this error or message will be described in details in the document. Some common warnings or errors are shown in Table 3-1, and help document can be viewed by clicking "Help > View Help", which supports Chinese and English versions.

Table 3-1 Common Warnings and Errors

Name	Code	Description
Warning	WARN (PA1002): <file>:<line> | Invalid parameterized value <value>(<parameter>) specified for instance <instanceName>	The specified instance set invalid parameters.
	WARN (PA1008): <file>:<line> | Object <name> is already defined	The line or port has already defined.
	WARN (PA1001) : Dangling net <netName>(source:<instanceName>) in module <moduleName> has no destination	The net in the specified module has no destination.
	WARN (CT1098) : <file>:<line> | Group name <name> is already defined	The constraints group name has alredy defined.
	WARN (CT1101) : <file>:<line> | Location column <number> is out of chip range(<maxColumn>)	The location column is out of chip range.
Error	ERROR (PA2000): <file>:<line> | Syntax error near token <name>	There is an error near token,
	ERROR (PA2001): <file>:<line> | Module <moduleName> is already defined	The module name has already defined.
	ERROR (PA2017): The number(<value>) of <instType> in the design exceeds the resource limit(<maxValue>) of current device	The number of the devices in the design file exceeds the resource limit.
	ERROR (PA2025): No <instType> resource in current device	There are resource that are not supported by the chip in the design.
	ERROR (PA2054): <file>:<line> | <name> is already declared	The name has already declared.

The TCL editing window locates at the bottom of theConsole page. You can enter tcl commands in the window and press the Enter key to execute, as shown in Figure 3-10. For the details of tcl, please refer to Appendix A Tcl Command.

Figure 3-10 Tcl Commit Window



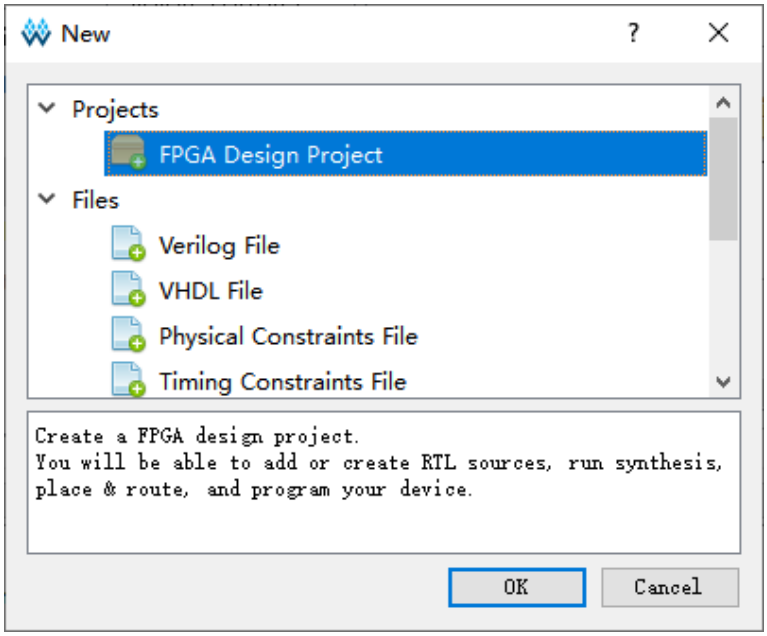
4 Gowin Software Usage

Gowin software supports interface mode and command line. Command line mode can be referenced Appendix A Tcl Command in this document. Take Windows10 and GUI as an example to introduce how to use the software.

4.1 Create a New Project

1. From the File menu, choose "File> New…" to open the "New" dialog, as shown in Figure 4-1.

Figure 4-1 Create New Project



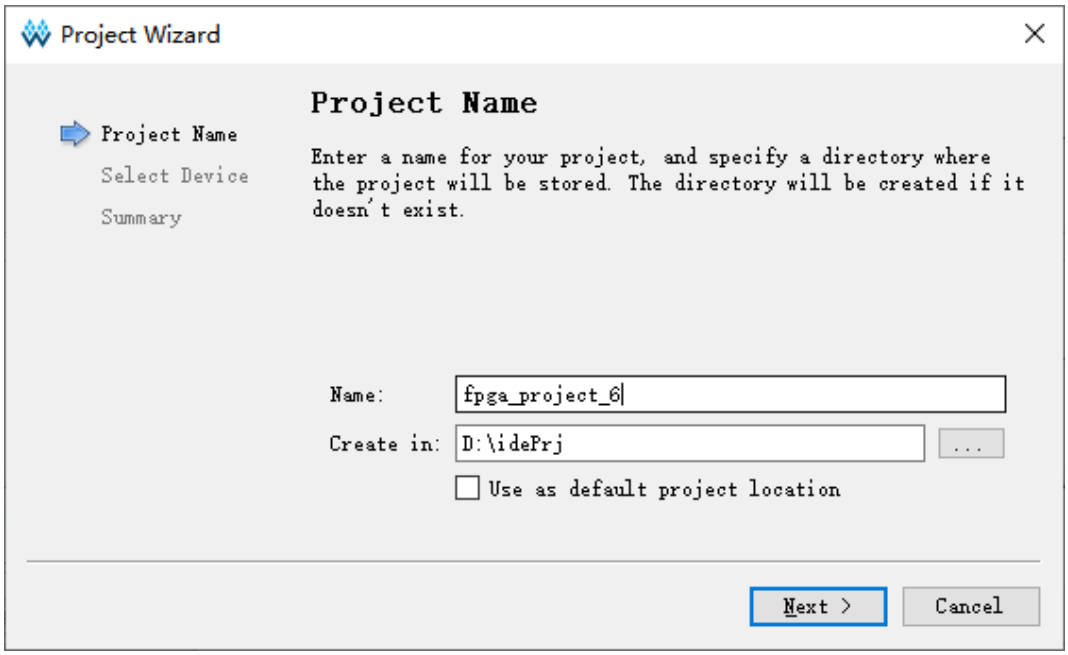
Note!

There are different ways to open a "New" dialog:

- Using the "Ctrl+N" short cut;
- Clicking on the "New File or Project" icon in the toolbar;
- By selecting "Quick Start>New Project" on the Start Page.

2. Select "FPGA Design Project" , and then click "OK" to open "Project Wizard", as shown in Figure 4-2.

Figure 4-2 Create New Project



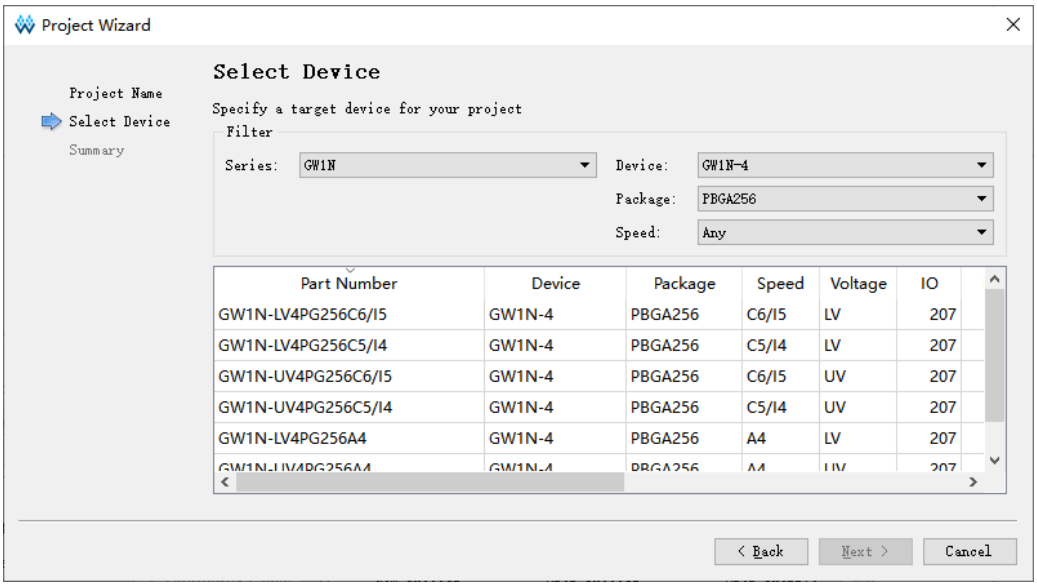
3. Create the project "Name" and "Create in", as shown in Figure 4-2;
   a) Enter the project name in the "Name" field;
   b) Click on the "..." icon to choose the project path.

Note!

- The file path length is limited in both Windows and Linux. You cannot delete or copy the files with the length going over the limits;
- The path separator is "\" in Windows; for example, E:\Gowin\ide;
- If users select "Use as default project location", the project location will be set as the default location, and all later projects you create will be saved to this location.

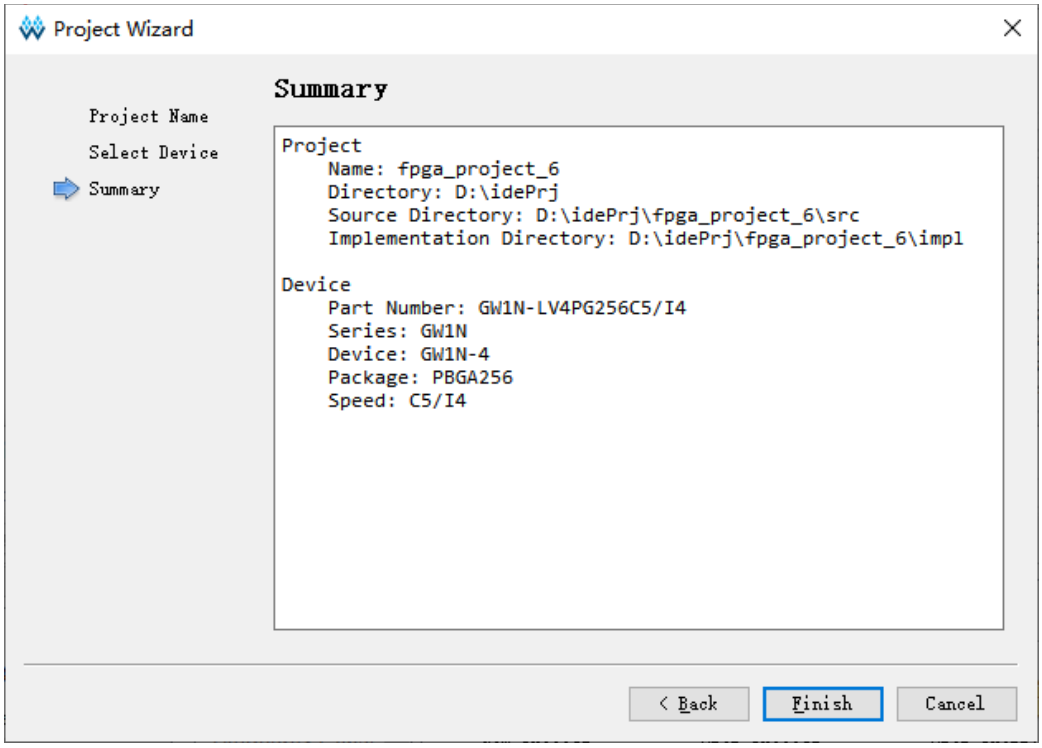
4. Click "Next" to select the device, as shown in Figure 4-3:
   - Users can select the target device series, package, and speed.
   - Choose package type from the "Package" drop-down list;
   - Choose speed grade from the "Speed" drop-down list;
   - Choose the detailed part number from the "Part Number" sub-window. It displays the detailed resource information related to the selected device.

Figure 4-3 Select Device



5. Click "Next" to open the project information summary window, as shown in Figure 4-4.

Figure 4-4 Project Information Summary



6. Click "Finish". The project now is created.

4.2 Open an Project

Use one of the following four methods to open an existing project:

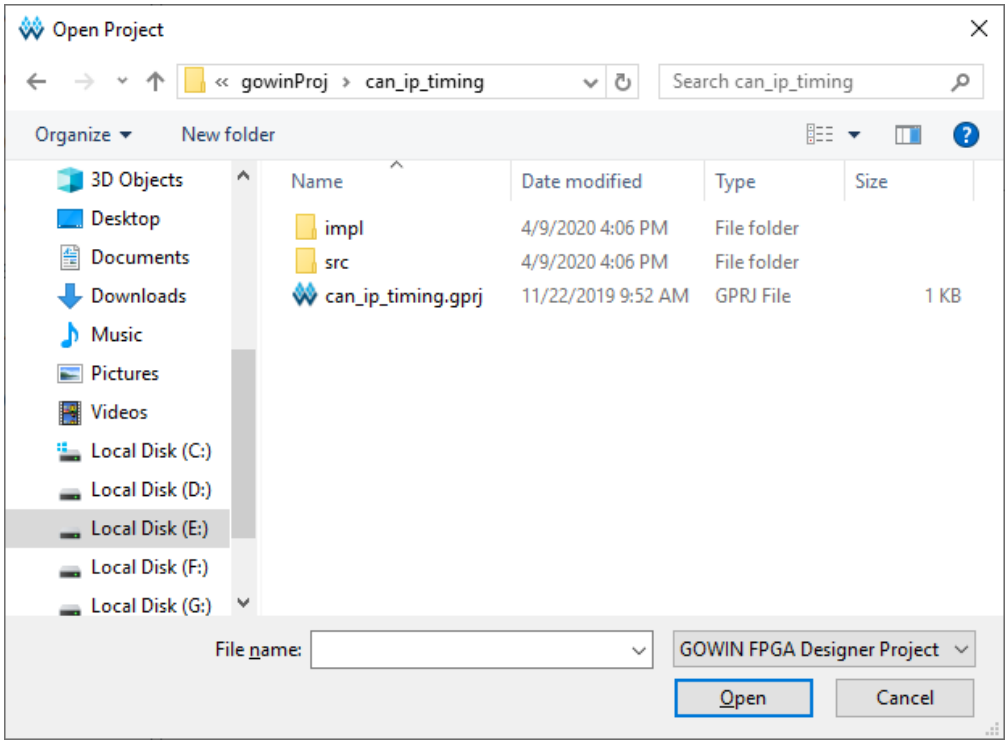
Open From Menu

1. From the File menu, select "File> Open …" to open the "Open File" dialog box, as shown in Figure 4-5.

Note!

Users can also click on the "  " icon in the tool bar to open the "Open File" dialog box.

Figure 4-5 Open an Existing Project



2. Choose the project file (*.gprj) and click "Open" to open the existing project.

Open Form Start Page

1. On the start page, click "  " to open "Open Project" dialog box.
2. Click "Open" to open the project.

Open Form Recent Projects

From the File menu, click "File> Recent Projects", to open your required project.

Note!

- Users can also open recent projects from the projects list that is displayed on the left side of the start page.
- Recent Projects shows the recently opened projects. Users can click on the names of the files to re-open them;
- If the project was deleted, the "Open Project" dialog box will pop up.

Open Form Project File

Find the project you established and find the *.gprj file. Doule-click *.gprj file to open the project automatically.

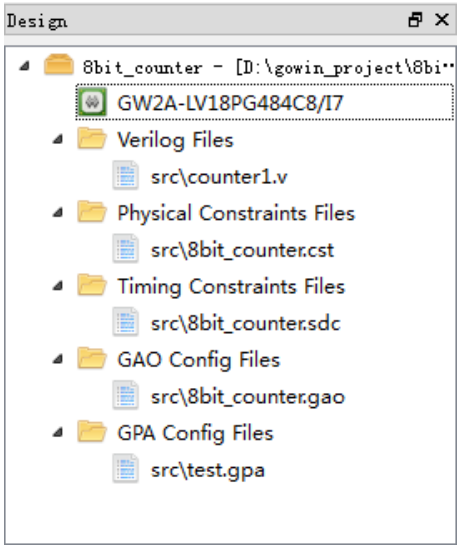
4.3 Edit a Project

After creating or opening a project, users can edit the device information and the related files in the project design area, as shown in Figure 4-6.

The Project Design Area contains the following:

- The project path;
- Chip info: Chip type, package type, and speed;
- The current project files, including user design files, physical constraints files (.cst.), timing constraints files (.sdc), GAO config files (.gao), and GPA config files (.gpa), etc.

Figure 4-6 Project Design Area



4.3.1 Modify Project Device

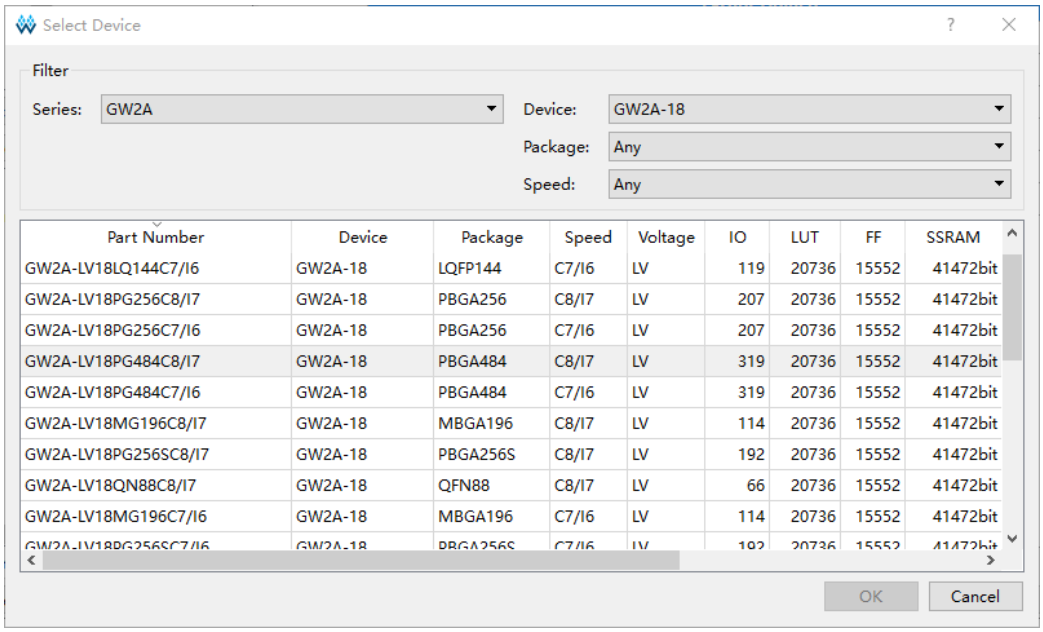
The chip information used in the current FPGA project can be modified in the project design view.

1. As shown in Figure 4-6, double-click ″GW2A-LV18PG484C8/I7″ to open the "Select Device" view, as shown in Figure 4-7;
2. In the "Select Device" view, select "Series" and "Device", select "Package" from the package drop-down list and select "Speed" from the speed drop-down list, and then select the detailed part number from the "Part Number" sub-window. Click "OK".

Note!

The "Part Number" displays the detailed resource information related to the selected device.

Figure 4-7 Project Device Info



4.3.2 Edit a Project File

Files that need to be added in projects include design files (Source Files), constraints files, and configuration files. Constraints files contain the Physical Constraints File and Timing Constraints File; configuration files contain the GAO Config File and GPA Config File.

Refer to the following sections to edit the project files.

Create a New Project Design File

1. As shown in , right-click on a blank area of the project design area, select "New File…" to open the "New" dialog box, and "Verilog File" is selected by default, as shown in ;
2. As shown Figure 4-8, select the file type and click "OK" to create a new file.

Figure 4-8 Right-click Menu

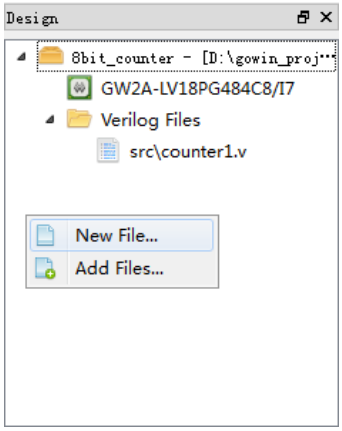
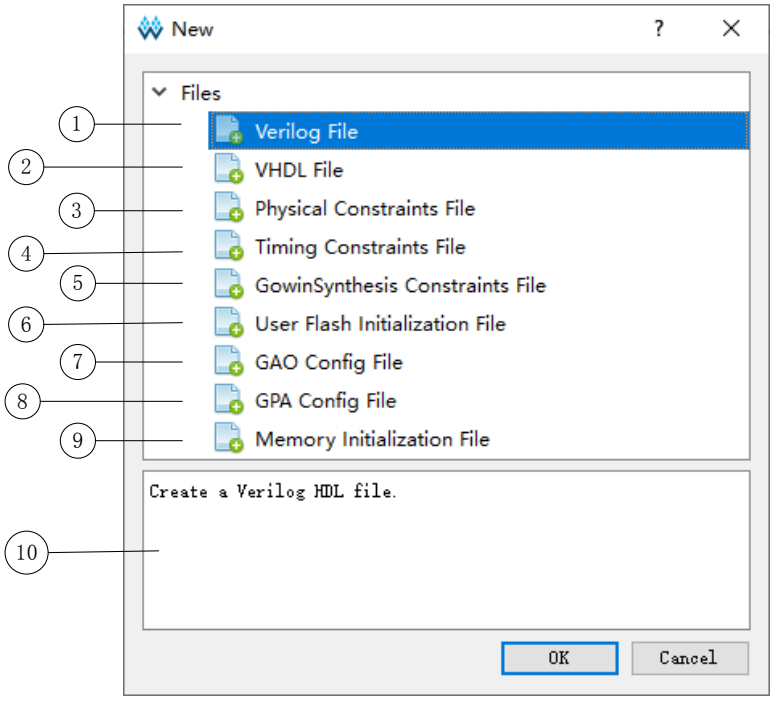


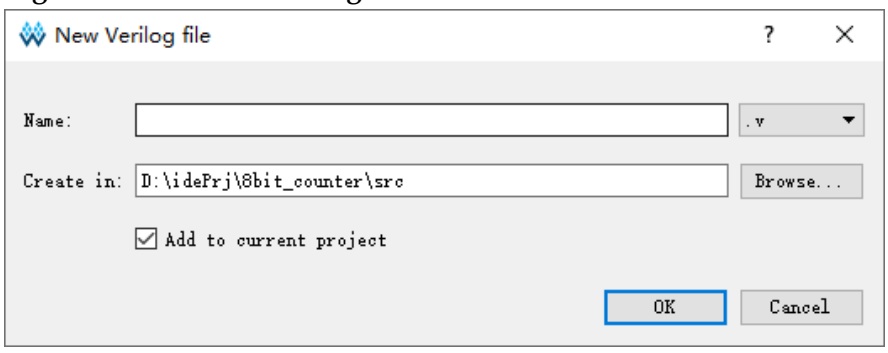
Figure 4-9 Create a New File



① Verilog File
② VHDL File
③ Physical Constraints File
④ Timing Constraints File
⑤ GowinSynthesis Constraints File
⑥ User Flash Initialization file
⑦ GAO Config File
⑧ GPA Config File
⑨ Memory Initialization File
⑩ File Description

3. Take creating a Verilog File, for instance. Select "Verilog File" and click "OK" to open the Verilog File view, as shown in Figure 4-10.

Figure 4-10 Create a Verilog File



4. Enter the file name and click "OK".

Note!

- Users can select file extensions from the drop-down list. "Add to current project" is selected by default.
- User can open and edit the newly created blank file in the source file editing area.

Create a Configuration File

1. As shown in Figure 4-8, right-click on a blank area of the project design area, select "New File…" to open the "New" dialog box, as shown in ;
2. As shown in Figure 4-9, select the file type and click "OK" to create a new file. Take creating a GPA Config File, for instance. Select "GPA Config File" and click "OK" to open the GPA Config File view, as shown in Figure 4-11.
3. The created Config File will not be directly opened in the source file editing area directly. Users need to double-click the Config File in the project Design area to open and edit the blank Config File, as shown in Figure 4-12. The created GPA config file will be added to the design view automatically.

Figure 4-11 Create a Config File

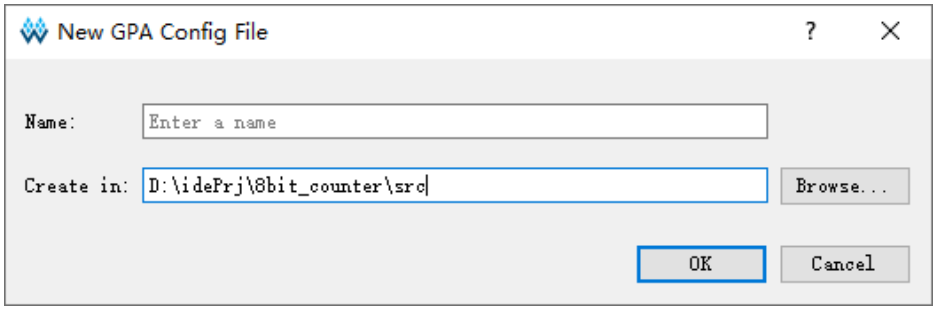
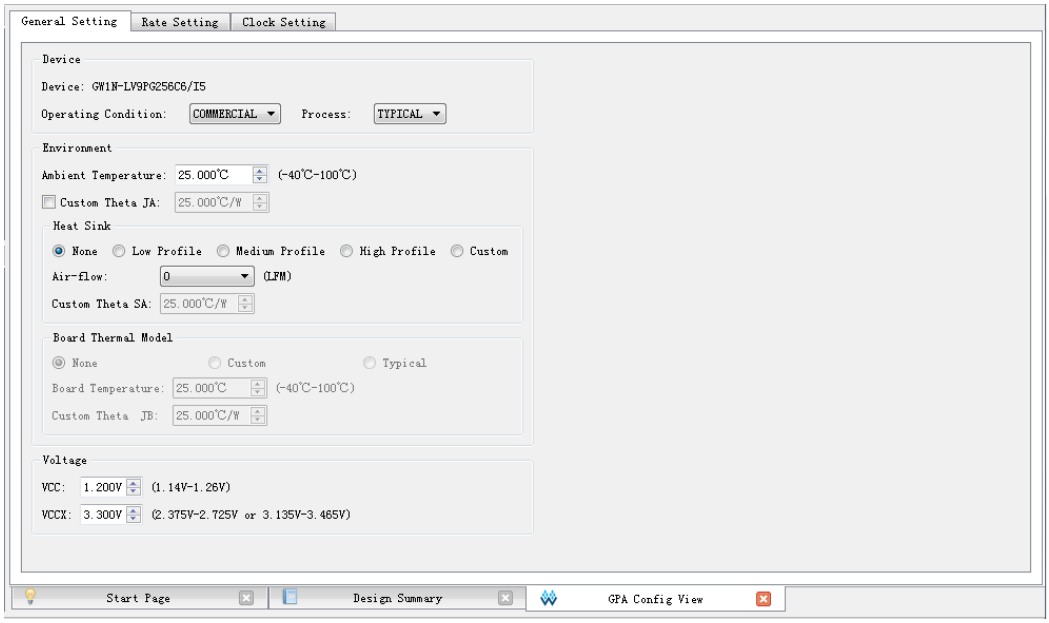


Figure 4-12 GPA Config File



Note!

If a user creates a new design file, constraint file, or configuration file with a duplicate name of an existing file, the user cannot create a new file and a prompt pops up in the window.

Add Project Files

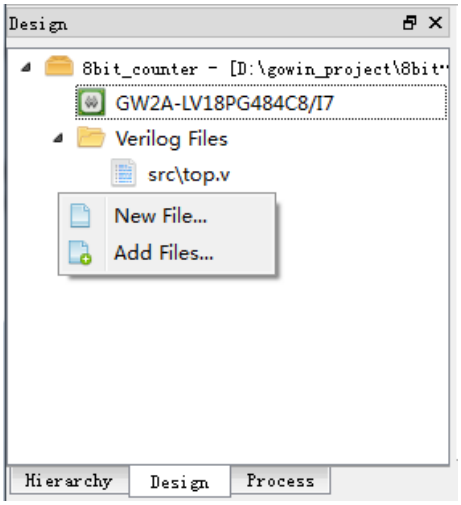
1. As shown in Figure 4-13, right-click in the blank of the project design area, select "Add Files…" to open the "Select Files" dialog box;

2. Select single or multiple project files to add.

Note!

- If the added files are not the project files, a prompt will pop up to confirm whether the user needs to copy them into the project source directory.
- If the users add RTL files and constraints files at the same time, Gowin will automatically classify the files in the project design area;
- If the added files are neither RTL design files and netlist file nor constraints files, GPA,/GAO configuration files, "Other Files" will be added in the project design area.

Figure 4-13 Right-click of Design

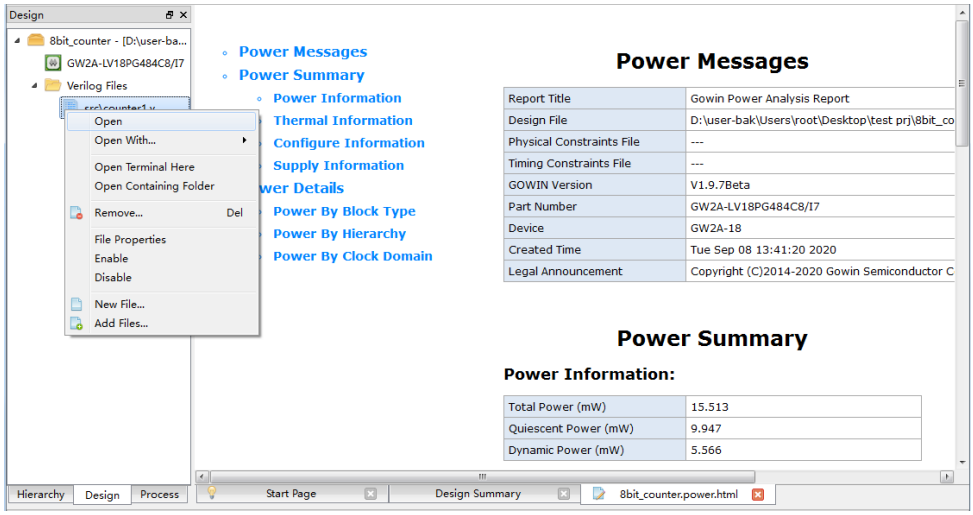


Modify Project Files

Use the following two methods to open and modify the project files, as shown in Figure 4-14:

1. Double-click any file in the project design area; the file will open in the source file editing area;
2. Right-click on the name of the file that is to be modified and select "Open".

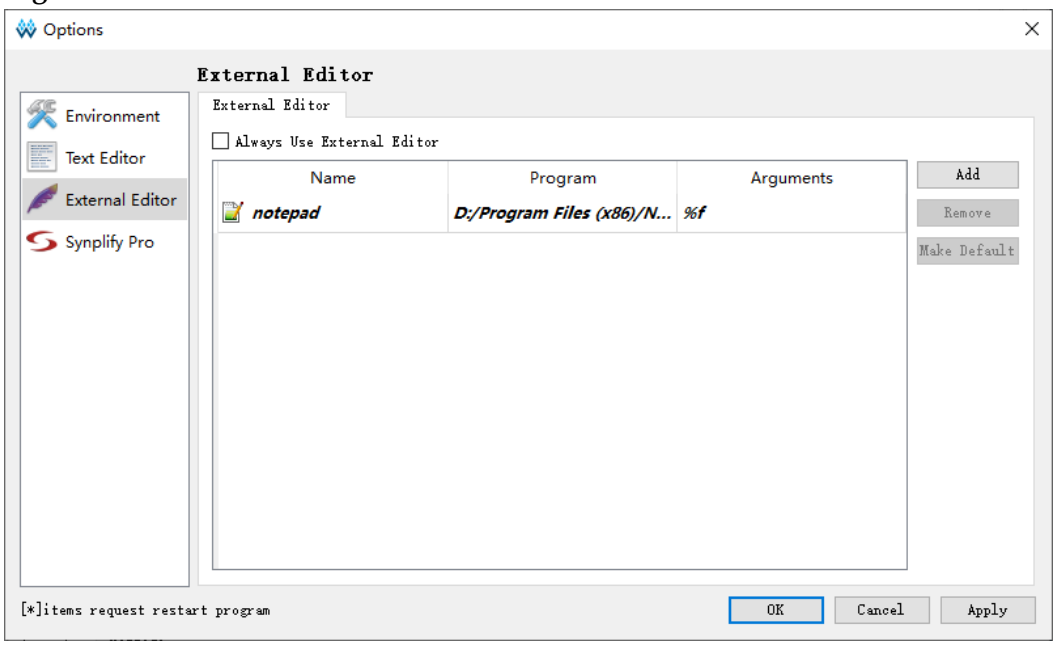
Figure 4-14 Project Files Editing Actions



Note!

- If the user has configured the third-party text editor by "Tools > Options", select "Open With…" to open the design file with the third-party text editor. As shown in Figure 4-15, you can add external editor as required. If "Always Use External Editor" is checked, it will always use external editor to open files.
- Select "Open Containing Folder" to open the file folder;
- Select "Open Terminal Here" to open the command line window. Command liine mode can be used;
- If users modify and save a file that has been opened in Gowin software by an external editor, Gowin software will generate a change notice.
- The user closes the unsaved file after editing, Gowin software will pop up the project file save notice.

Figure 4-15 External Editor



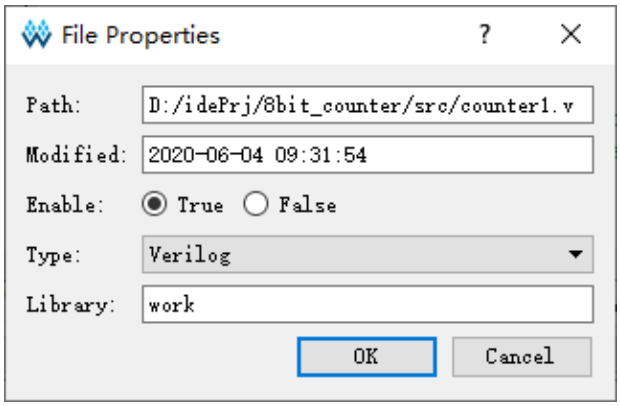
Delete Project Files

1. Select the file in the project design area;
2. Right-click and select "Remove", or directly press the Delete key to open the "Delete File" dialog box. If you select the "Delete Permanently" check box, the file is deleted from the current project and on disk. Otherwise, the file is deleted only from the current project. If the file that is open in the editing area is deleted, the delete notice will pop up.

View File Properties

Rigut-click any file in the project management, select File Properties from the right menu list, and "File Properties" dialog box pops up, as shown in Figure 4-16. The path, modified time, Enable, Type, and Library information are displayed in the dialog. The file type can be modified in the Type drop-down menu. After clicking OK, the file will automatically move to the selected type in the Design window. Library is used to specify the library used when Synplify Pro synthesizes VHDL files. The default is work.

Figure 4-16 File Properties



Enable/Disable Options

Users can see the "Enable" and "Disable" options by righting click on any files in the project design area, as shown in Figure 4-14. After setting Enable / Disable, Synthesize and Place & Route can read the enable file.

1. Set Enable / Disable by right-clicking actions, including single file setting and setting of batch files;
2. If multiple design files (Reference Design Files or Netlist Files) are selected, "Enable" and "Disable" are all available;
3. If multiple constraints files or configuration files are selected, "Enable" is disabled, and "Disable" is enabled, as shown in Figure 4-17.
4. For multiple constraints files or configuration files, only one file can be in "Enable" state. When you create or add a new file of same type, the previous one will be disabled; when multiple files with different types are selected, both "Enable" and "Disable" are disabled, as shown in Figure 4-18.

Figure 4-17 Right-clicking Actions of Selecting Same Type Files

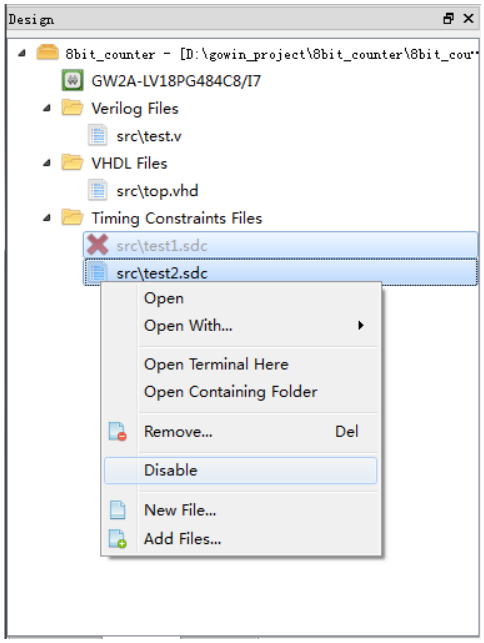
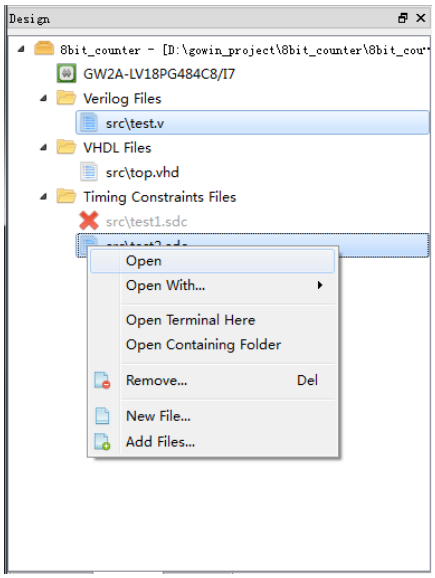


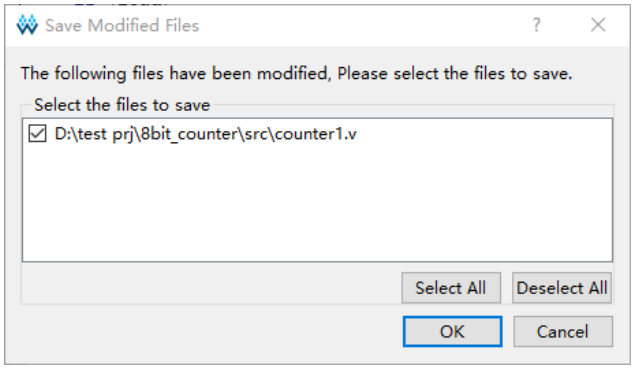
Figure 4-18 Right-clicking Actions of Selecting Different Type Files



"Save Modified Files" Prompt

After project files are modified, if you run Synthesize or Place&Route before saving these files, the "Save Modified Files" prompt dialog box will pop up, as shown in Figure 4-19.

Figure 4-19 The Prompt

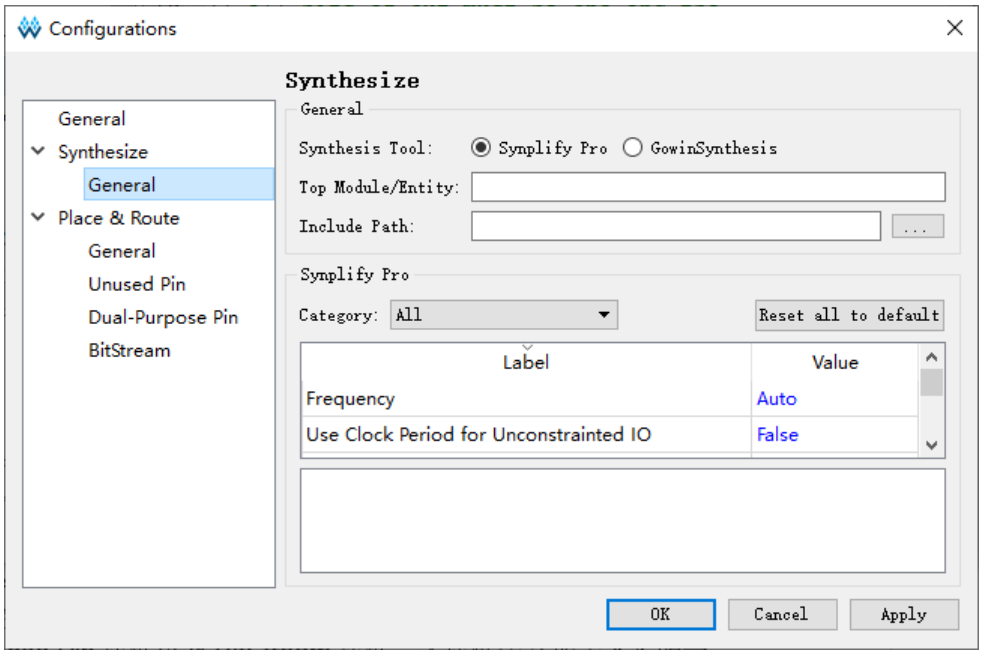


Click "OK". The files will be saved and the process needs to be performed will pop up directly. If "Cancel" is clicked, the files will not be saved and Synthesize or Place&Route will not be performed.

4.3.3 Modify Project Configuration

Right click "Synthesize" or "Place & Route" in the Project Design area. Select "Configuration" to open the project configuration view, as shown in Figure 4-20.

Figure 4-20 Project Configuration View



As shown in Figure 4-20, the project configuration contains the Synthesis configuration and Place & Route configuration, and among them, Place & Route configuration includes General, Unused Pin, Dual-Purpose Pin, and BitStream configuration, as shown in Table 4-1.

Table 4-1 Description of Configuration

Option	Description
Synthesize	Configure the parameters for optimizing user design with synthesis tool;
General	Configure the parameters for place and route;
Unused Pin	Set different IO types and properties for unused pin (except for unused pins of the dual-purpose pins);
Dual-Purpose Pin	Configure dual-purpsose pin;
Bitstream	Configure download speed and CRC check, compress, etc.

The further details of the options are as follows:

Synthesize

Select Synthesize in project configuration view. You can select synthesis tool in General tab: Synplify Pro or GowinSynthesis.

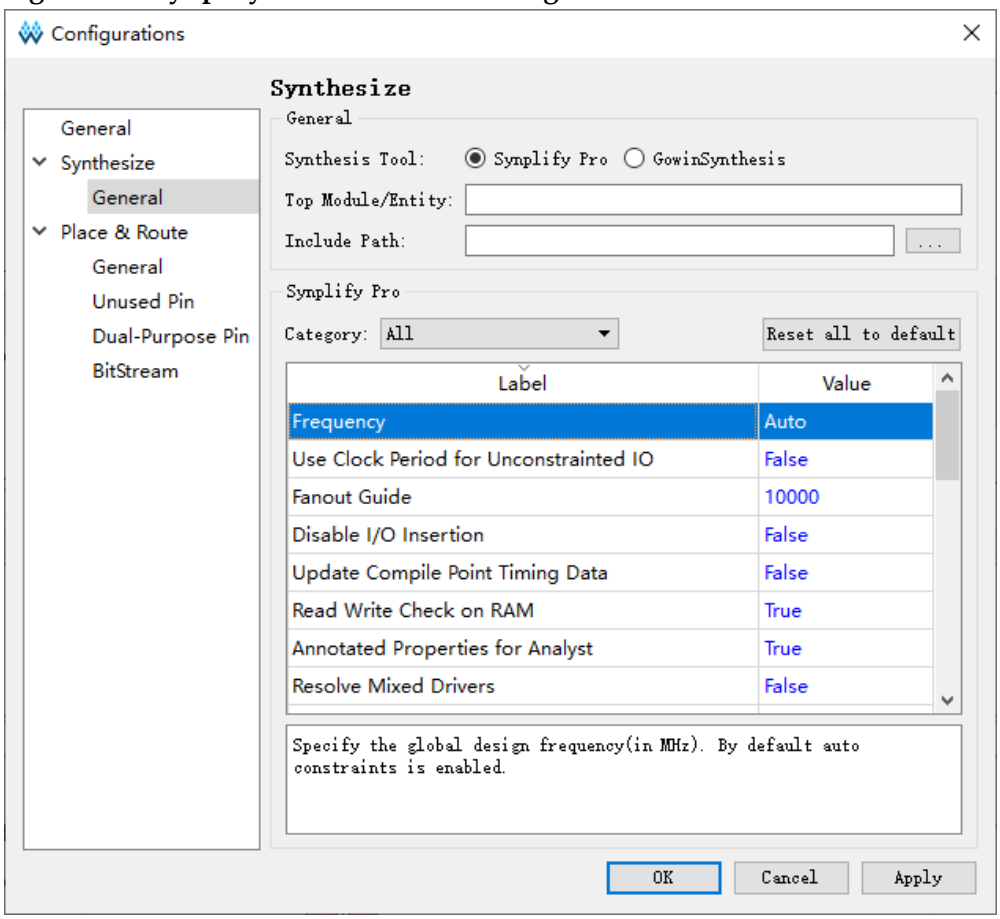
- If Synplify Pro is selected as the Synthesis Tool,
  - Top Module/Entity and Include Path can be configured;
  - Select the parameters options from the "Category" drop-down list. The default value is "All";
  - Select the parameter that needs to be configured in "Lable". The corresponding description shows at the bottom of "Configuration" view, as shown in Figure 4-21.

- Double-click the corresponding value and configure based on your requirements. Click "Apply" to put the current configuration into effect. Click "OK" to complete the configuration.

Note!

- For further details about Synplify Pro, please refer to and the SynplifyPro manuals in the Gowin installation directory: installPath\SynplifyPro\doc;
- Reset all to default: Reset all configuration on this page to default values; "Reset" will pop up when you click it.

Figure 4-21 Synplify Pro Parameters Configuration

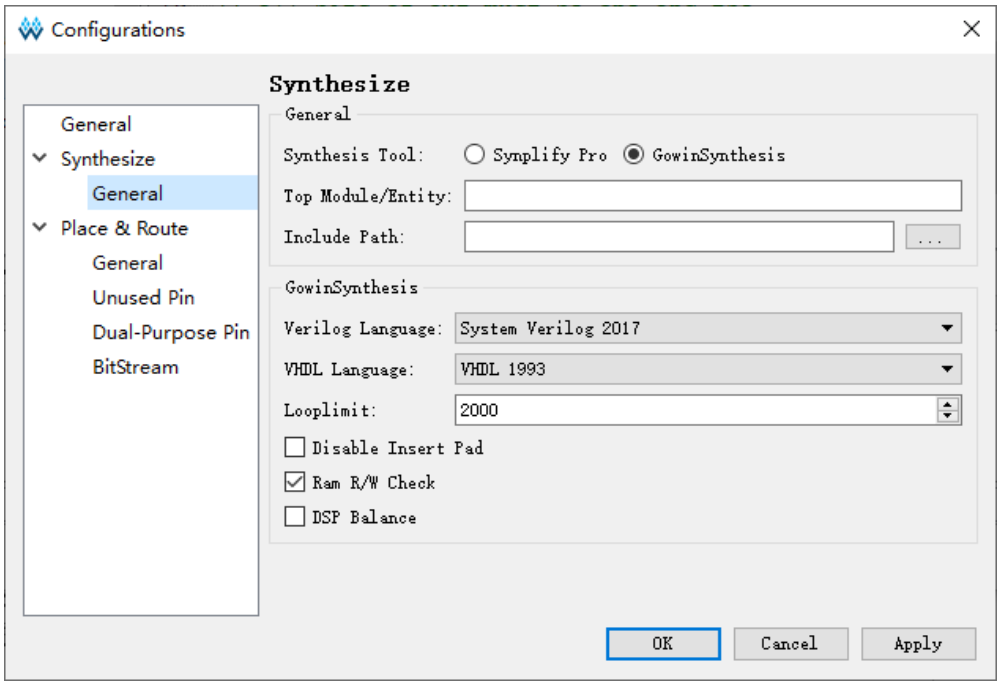


Note!

For further detailed description of the parameters in Figure 4-21, please refer to the file in the software Installation directory: path/x.x.xBeta/ SynplifyPro/doc/ fpga_command_reference.pdf.

- If GowinSynthesis is selected as the Synthesis Tool, Top Module/Entity, Include Path, Verilog Language, VHDL Language, and Looplimit can be configured.
  - There are three options for Verilog Language: System Verilog 2017, Verilog 2001 and Verilog 95；
  - VHDL Language supports VHDL 1993 and VHDL 2008.
  - Select the check boxes to select Disable Insert Pad, Raw R/W Check and DSP Balance, as shown in Figure 4-22.

Figure 4-22 GowinSynthesis Parameters Configuration



The description of parameters in Figure 4-22 is as follows:

- Looplimit: Set the loop limit value of the default editor in RTL. The default Value is 2000;
- Disable Insert Pad: Whether to insert I/O BUF to the netlist after synthesis;
- Ram R/W Check: If RAM has read or write conflicts, check this option and bypass logic will be inserted around RAM to prevent emulation mismatches. Disabling this option does not generate bypass logic. Checked by default.
- DSP Balance: If the DSP resource exceeds the limit when the design is synthesized, if it is checked, the DSP resource will be synthesized to registers.

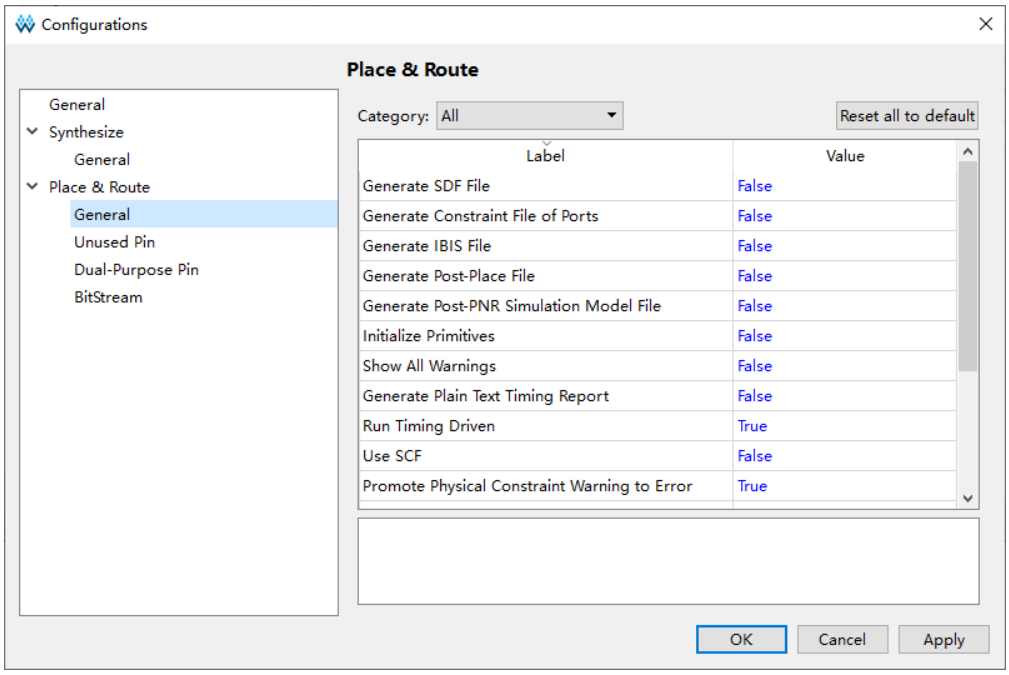
Note!

For the details, see SUG550, GowinSynthesis User Guide

Place & Route

"General" configuration in Place & Route, which was independently designed by Gowin, is compatible with Gowin software. Users can modify the value configuration, as shown in Figure 4-23.

Figure 4-23 Place&Route Configuration



Note!

Reset all to default: Resets all configurations on the page to the default values.

The description of parameters in Figure 4-23 is as follows:

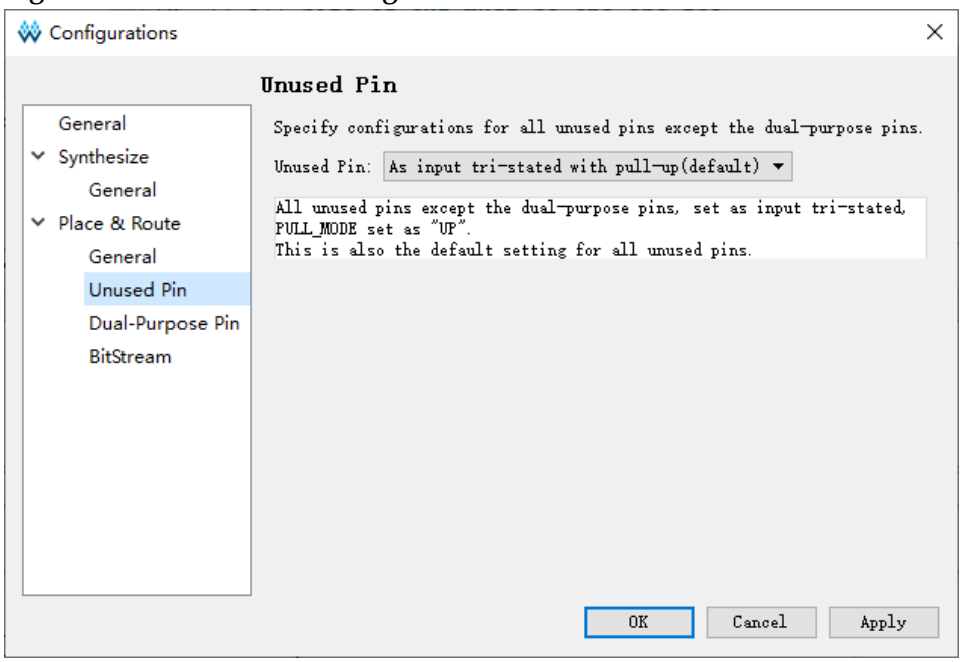
- Generate SDF File: Generate the Standard Delay Format file, named as *.sdf. The default Value is False;
- Generate Constraint File of Ports: Generate the constraints file of ports, named as *.io.cst. The default Value is False; This file allows you to view the place location of the port or load it to FloorPlanner.
- Generate IBIS File: Generate the Input/Output Buffer Information Specification file, named as *.ibs. The default Value is False;
- Generate Post-Place File: Generate the device place file, named as *.posp. The default Value is False; The generated*.posp file only contains BSRAM placement.
- Generate Post-PNR Simulation Model File: Generate the Post-PNR Simulation Model file, named as *.vo. The default Value is False;
- Initialize Primitives: Add the default initial value to the instance of the generated post-PNR simulation model File. The default Value is False;
- Show All Warnings: Output all warning information when pnr is running. The default Value is False;
- Generate Plain Text Timing Report: Generate plain text timing report, named as *.tr. The default Value is False;
- Run Timing Driven: When this option is checked, timing driven optimization of the placement and routing is performed. The default Value is True;
- Use SCF: Use Synplify Pro to generte the *.scf file, used as the additional timing constraint files. The default Value is False;

- Promote Physical Constraint Warning to error: The default Value is True.
- Report Auto-Placed IO Information: The default Value is False.
- Place Option: Layout algorithm options. The options are 0 and 1. When the value is 0, the default place algorithm is used; when the value is 1, the algorithm 1 is used. Algorithm 1 is based on algorithm 0 to try to find better optimization.
- Route Option: The options are 0, 1, 2. When the value is 0, the default route algorithm is used according tocongestion. When the value is 1, the algorithm 1 is used according to timing. With algorithm 2, the speed will be faster. If the algorithm 0 is not effective, it is recommended to try algorithm 1 or algorithm 2. The default Value is 0;
- Place input register to IOB: Input registers are placed to IOB when this option is checked. The default value is True;
- Place output register to IOB: Output registers are placed to IOB when this option is checked. The default value is True;
- Place inout register to IOB: Inout registers are placed to IOB when this option is checked. The default value is True;

Unused Pin

The Unused Pin configuration can set different IO types and attribute values for unused pins (except for the dual-purpose pins). There are two configuration options: As input tri-stated with pull-up (default) and As open drain driving ground, as shown in Figure 4-24.

Figure 4-24 Unused Pin Configuration



- As input tri-stated with pull-up (default): All pins that are not used by the user (except for the dual-purpose pin) are configured according to the IO attribute of input LVCMOS18, and PULL_MODE is set to UP.

- As open drain driving ground: All pins that are not used by the user except for the dual-purpose pin) are configured according to the IO attributes of output LVCMOS18, and OPEN_DRAIN is set to ON.

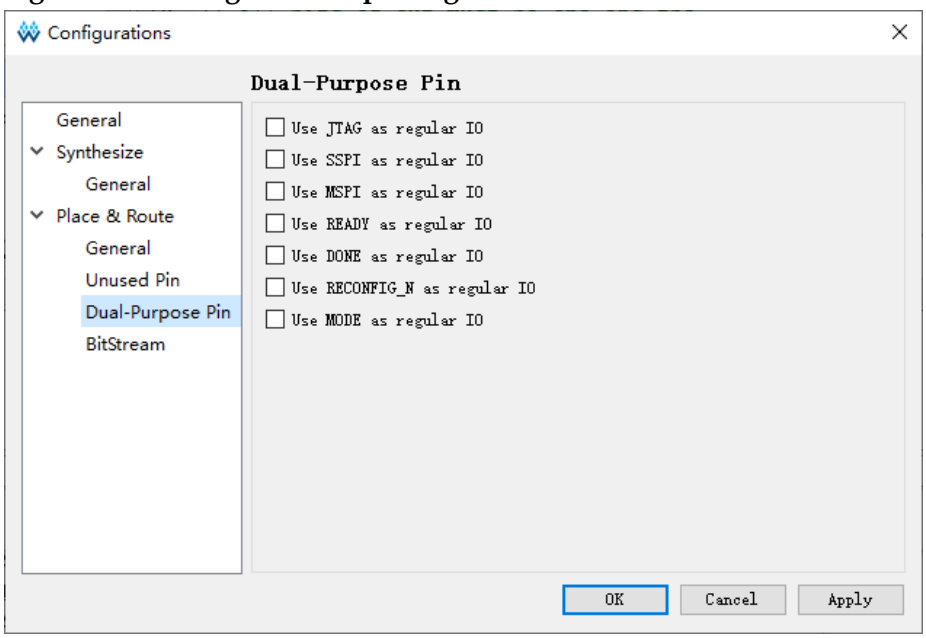
Note!

The dual-purpose pin is not affected by the unused pin setting.

Dual-Purpose Pin

In the Dual-Purpose Pin tab, users can configure the multiplexing pins in different modes for the selected device; see Figure 4-25 for the detailed configuration options.

Figure 4-25 Configure Multiplexing Pins



The dual-purpose pins in Figure 4-25 are described as follows:

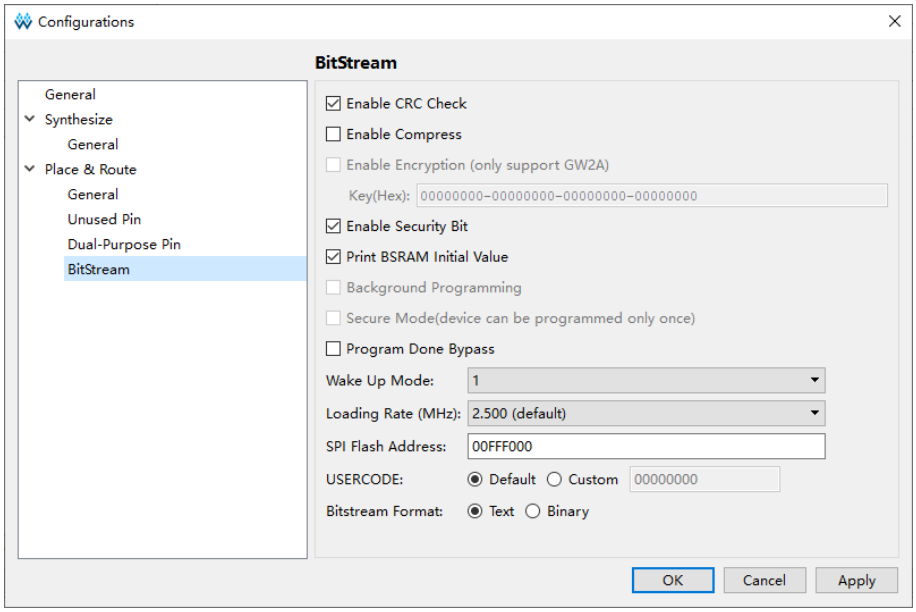
- Use JTAG as regular IO: Use the JTAG related pins as regular IO. JTAG related pins are TCK, TMS, TDI, and TDO;
- Use SSPI as regular IO: Use SSPI as regular IO. SSPI related pins are SI, SO, SSPI_CS_N.
- Use MSPI as regular IO: Use MSPI as regular IO. MSPI related pins are ASTRD_N, MCLK, MCS_N and MI、MO.
- Use READY as regular IO: Use READY as regular IO. READR related pin is READY.
- Use DONE as regular IO: Use DONE as regular IO. DONE related pin is DONE.
- Use RECONFIG_N as regular IO: Use RECONFIG_N as regular IO. RECONFIG_N related pin is RECONFIG_N.
- Use MODE as regular IO: Use MODE related pins as regular IO. MODE related pins are MODE0, MODE1, and MODE2;

Bitstream

Users can configure the bitstream files format or frequency, etc. See

Figure 4-26 for the detailed options.

Figure 4-26 Configure Bitstream File



The description for each parameter in Figure 4-26 is as follows:

- Enable CRC Check: Enable CRC Check, checked by default.
- Enable Compress: Compress the generated bit file, not checked by default.
- Enable Encryption（only support GW2A）: Encrypt bit files, supporting GW2A series only, not checked by default.
- Key(Hex): Key(Hex) can be configured only "Enable Encryption（only support GW2A" is selected.This enables the user to customize the secret key. The default is 0.
- Enable Security Bit: Checked by default.
- Print BSRAM Initial Value: Print BSRAM initial value to bit file, checked by default.
- Background Programming: Remote Upgrade. You can program Flash without interrupting the current FPGA running, supported by GW1N-4B, GW1NR-4B, GW1N-4C, GW1NR-4C, GW1N-9, GW1NR-9, GW1N-9C, GW1NR-9C and GW1NZ-1, not checked by default. For GW1NS-2, GW1NSR-2, GW1NSE-2C, GW1NSR-2C, the hardware configuration support this function for these devices, supported by default.

Note!

The Background Programming cannot be configured when there is User Flash in the design, otherwise the Error prompt will be reported.

- Secure Mode (device can be programmed only once): Enable secure mode. Use JTAG pin as GPIO, and device can be programmed only once. This feature only supported by GW1NSE-2C and GW1NSER-4C. It’s unchecked by checked.

- Program Done Bypass: When the Done Final signal takes effect, the external Done Pin keeps low, so that the bitstream can be forwarded after the bitstream is loaded.
- Wake Up Mode: Enable or disable wake up mode. Options are 0 and 1.

  The default value is 0; When wake up mode is "0", DONE pin can be pulled up or down. When wake up is "1", if the DONE pin is pulled up, device can download and run normally. If the done pin is pulled down during downloading, device can download normally, but to wake up, DONE pin needs to be pulled up and keep TCK connected to the pulse signal.
- Loading Rate: In AutoBoot mode and MSPI mode, the rate of loading bitstream data from flash to sram is 2.500MHz by default. For the details, see UG290, Gowin FPGA Products Programming and Configuration Guide. The lading rate of different devices and the calculation methods are shown below.
  - For GW1NZ-1/GW1NSER-4C/GW1NS-4/GW1NSR-4/ GW1NS-4C/GW1NSR-4C/GW1N-4B/GW1NR-4B/ GW1N-4C/GW1NR-4C/GW1NRF-4B/ GW1N-4/GW1NR-4/GW1N-9/GW1N-9C/GW1NR-9/ GW1NR-9C/GW2A-18/GW2A-18C/GW2AR-18/GW2AR-18C/ GW2ANR-18C/GW2A-55/GW2A-55C, see Table 4-2.

Table 4-2 Loading Rate Value and Formula

Loading Rate (MHz)	Fraction
2.500 (default)	250 / 100
5.435	250 / 46
5.682	250 / 44
5.952	250 / 42
6.250	250 / 40
6.579	250 / 38
6.944	250 / 36
7.353	250 / 34
7.812	250 / 32
8.333	250 / 30
8.929	250 / 28
9.615	250 / 26
10.417	250 / 24
11.364	250 / 22
12.500	250 / 20
13.889	250 / 18
15.625	250 / 16
17.857	250 / 14
20.833	250 / 12
25.000	250 / 10

Loading Rate (MHz)	Fraction
31.250	250 / 8
41.667	250 / 6
62.500	250 / 4

- For GW1N-1/GW1N-1S/GW1NS-2/GW1NSR-2/GW1NS-2C/GW1NSR-2C/ GW1NSE-2C, see Table 4-3.

Table 4-3 Loading Rate Value and Formula

Loading Rate (MHz)	Fraction
2.500 (default)	240 / 96
2.553	240 / 94
2.609	240 / 92
2.667	240 / 90
2.727	240 / 88
2.791	250 / 86
2.857	240 / 84
2.927	240 / 82
3.000	240 / 80
3.077	240 / 78
3.158	240 / 76
3.243	240 / 74
3.333	240 / 72
3.429	240 / 70
3.529	240 / 68
3.636	240 / 66
3.750	240 / 64
3.871	240 / 62
4.000	240 / 60
4.138	240 / 58
4.286	240 / 56
4.444	240 / 54
4.615	240 / 52
4.800	240 / 50
5.000	240 / 48
5.217	240 / 46
5.455	240 / 44
5.714	240 / 42
6.000	240 / 40
6.316	240 / 38

Loading Rate (MHz)	Fraction
6.667	240 / 36
7.059	240 / 34
7.500	240 / 32
8.000	240 / 30
8.571	240 / 28
9.231	240 / 26
10.000	240 / 24
10.909	240 / 22
12.000	240 / 20
13.333	240 / 18
15.000	240 / 16
17.143	240 / 14
20.000	240 / 12
24.000	240 / 10
30.000	240 / 8
40.000	240 / 6
60.000	240 / 4

- SPI Flash Address: Specify SPI Flash Address. The SPI Flash address refers to the initial address to which the bitstream will be loaded for the next multiboot. The default is 00000000. For further details, see SUG502, Gowin Programmer User Guide.
- USERCODE: Users can custom User Code. The default Value is Default (00000000);
- Bitstream Format: Used to specify the bitstream file format, Text and Binary. The default value is Text. When the Text option is selected, the *.fs file in plain text format is generated. A bitstream file in the *.fs, *.bin, and *.binx formats is generated when the Binary option is selected. *.bin and *.binx are bit tream files in binary format, *.binx file contains header annotation information, and *.bin does not have header annotation information.

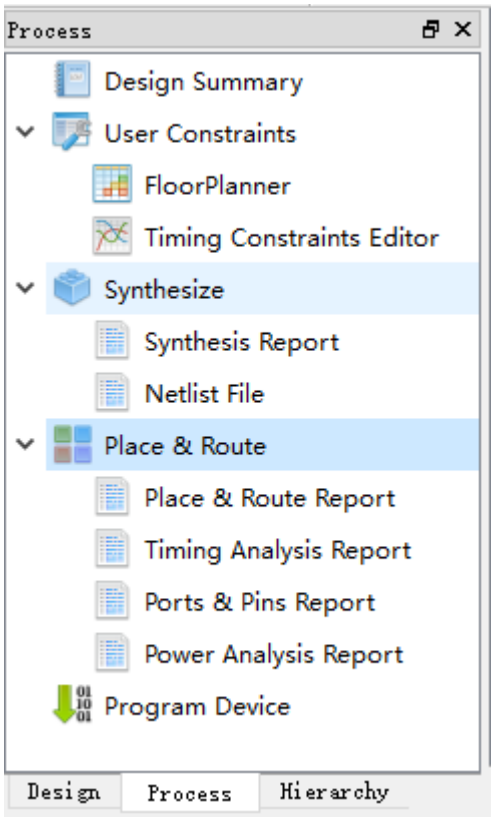
4.4 Manage a Project

The Process view provides a system-level overview of the FGPA design flow, as shown in Figure 4-27. The Process View incorporates the following actions:

- View design summary;
- Start FloorPlanner;
- Start timing constraints editor;
- Implement Synthesis;
- View post Place & Route report;

- Implement Place & Route;
- Check the report generated after Place & Route;
- Start GOWINSEMI FPGA programmer, etc.

Figure 4-27 Project Process View



4.4.1 Design Summary

Creating new project, the software will analyze the project and provide a report of Design Summary, which will include the project file path, synthesis information and device information, as shown in Figure 4-28. There are following three ways to open the Design Summary:

- From the menu bar, select "Window > Design Summary";
- In the Process View, double-click "Design Summary";
- In the Process View, right- click in the "Design Summary", and select "Open".

Figure 4-28 Project Summary

General	
Project File:	D:\gowin_project\1.9.0\fpga_project_1\fpga_project_1.gprj
Synthesis Tool:	SynplifyPro

Target Device	
Part Number:	GW1N-LV4PG256C6/I5
Series:	GW1N
Device:	GW1N-4
Package:	PBGA256
Speed Grade:	C6/I5
Core Voltage:	LV

4.4.2 User Constraints

User constraints provide quick access to and creation of constraints files, which includes the FloorPlanner and Timing Constraints Editor.For the details, please refer to SUG940, Gowin Design Timing Constraint User Guide.

FloorPlanner

1. Double-click "FloorPlanner" or select "Run" from the right-clicking list. If the project has not been synthesized, the prompt dialog box will pop up. After synthesis, double-click "FloorPlanner" or select "Run" from the right-clicking list to open the Physical Constraints Editor;
2. If the physical constraints file already exists in the project, the editor will read it directly when the editor is opened.
3. If the existing physical constraints file (.cst) is modified and saved, click on the "  " icon in the Physical Constraints Editor to reload the Physical modified constraints file;
4. If the project does not include the corresponding constraints file, and when users double-click FloorPlanner after synthesis, a prompt will pop up;
5. If the project does not include a physical constraints file, but a constraints file with the same name exists in the source file directory, a warning dialoge box will appear and ask whether you want to override it or not.

Note!

Users can open the Floor Planner and Timing Constraints Editor directly by selecting "Tools > Floor Planner/Timing Constraints Editor".

Timing Constraints Editor

1. Double-click "Timing Constraints Editor" or select "Run" from the right-clicking list. If the project has not been synthesized, the prompt dialog box will pop up. After synthesis, double-click "Timing Constraints Editor" or select "Run" from the right-clicking menu to open the Physical Constraints Editor;
2. If the timing constraints file (.sdc) exists in the project, the editor will read it directly when the editor is opened.
3. If the project does not include the corresponding constraints file, Gowin will prompt users to create a constraints file;
4. If the project does not include a physical constraints file, but a constraints file with the same name exists in the source file directory, a warning dialog box will appear and ask whether you want to override it or not.

4.4.3 Synthesize

Gowin software offers two synthesis tools: Synplify Pro and GowinSynthesis. If users do not selected, the default synthesis tool is GowinSynthesis.

Right-click "Synthesize" and select "Configuration" in the Project

Design area to open the configuration view, as shown in Figure 4-20. Synthesis is the Pro FPGA synthesis software customized by Synopsys for GOWINSEMI. It supports GOWINSEMI library files and their implementation, VHDL, and Verilog, etc.

GowinSynthesis is the sythesis tool developed by Gowin. It supports GOWINSEMI library files and their implementations. It supports System Verilog 2017, Verilog 2001, Verilog 95, and VHDL 2008.

Synthesize provides functions of running synthesis, setting synthesis parameters, and managing Netlist File and Synthesis Report.

Refer to the following steps to run Synthesize:

1. Configure synthesis attributes. Users can select Synplify Pro or GowinSynthesis as the synthesis tool;
2. For the Synthesis configuration attributes, please refer to 4.3.3 Modify Project Configuration;
3. Run Synthesize;
4. In Process View, double click "Synthesize" or right-click "Synthesize > Run" to start synthesis of source files. If succeed, the status icon " " appears before Synthesize; if not, the status icon " " appears.
5. After synthesis has been completed successfully, double click "Netlist Report" or right-click and select "Open" to view the Netlist Report. The netlist file name is the same as the project name. If users select Synplify Pro, the generated integrated netlist file is *.vm. If users select GowinSynthesis, the generated integrated netlist file is *.vg.

Note!

- If the Synthesize icon is " " before synthesis, double click ″Netlist File″ or right click to select "Open" to synthesize first, and the netlist file opens after successful synthesis;
- If the synthesize icon is " " before synthesis, double-click ″Synthesis Report″ or right-click and select "Open" to synthesize first. The Synthesis Report will open after successful synthesis.

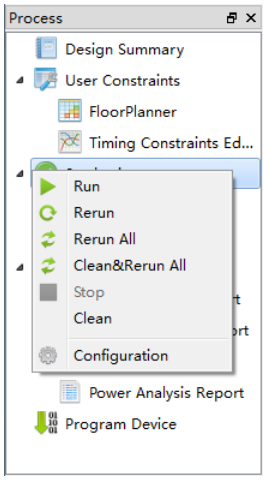
Right-clicking actions of Synthesize, as shown in Figure 4-29:

- Run: only when the icon before Synthesize is " ", " ", or " ", you can select Run to start synthesis of source files;
- Rerun: no matter what Synthesize status is, you can select Rerun to restart synthesis of source files;
- Rerun All: If selecting this option, no matter what status of "Place&Route" and "Synthesize" is, the source file will be synthesized and placed & routed again.
- Clean& Rerun All: Clean the generated files after synthesis, and synthesize and place & route the source files again.
- Stop: Stop Synthesize;
- Clean: Clean all the generated files. Click it and a prompt will pop up.
- Configuration: Configure Synthesis parameters.

Note！

The files name generated by Synplify Pro is synthesize and the one generated by GowinSynthesis is gwsynthesis.

Figure 4-29 Right-clicking Synthesize



4.4.4 Place & Route

Place and route includes the functionality required to run Place & Route, set the place and route parameters, and manage the post-P&R report.

Note!

Place & Route will be implemented after Synthesize runs.

Refer to the following steps to run Place & Route:

1. Configure Place & Route attributes;
2. To configure the Place & Route attributes, please refer to 4.3.3 Modify Project Configuration;
3. Run Place & Route;
4. Double-click "Place&Route", right-click and select "Place & Route > Run " to generate bitstream files and related reports. If running successfully, the "✔" icon will appear before Place & Route. Otherwise, the "❗" will appear;
5. After Place & Route has been run successfully, double-click on "View Post PnR Report" or right-click and select "Open" to view the report.
6. Users can view four kinds of files: Place & Route Report, Timing Analysis Report, Ports & Pins Report, and Power Analysis Report. These reports can not be edited.

Note!

- If the report is already opened and is regenerated by implementing Place & Route, Gowin will ask the users whether they would like the report to be updated.;
- Before implementing Place & Route, if the status icon before Place & Route is " ", double click the report or right-click and select "Open" to run Place & Route first. The report will open after Place & Route has been successfully.

The options of Place & Route right-clicking:

- Run: Users can only select "Run" to start Place & Route only when the icon before Place&Route is " ", " ", or " ";

- Rerun: Regardless of the Place&Route status, you can select Rerun to rerun Place&Route;
- Rerun All: If this option selected, regardless of the status of "Place&Route" and "Synthesize", the source file will be synthesized and placed & routed again.
- Clean& Rerun All: Clean the generated files after PnR and rerun the source files.
- Stop: Stop Place & Route;
- Clean: Clean all the generated files after PnR; A prompt will pop up when clicking this option.
- Configuration: Configure Place & Route parameters.

4.4.5 Program Device

Bitstream files will be generated after Gowin software has run placement and routing. Start Gowin FPGA programmer to download the bitstream files to the chip to realize user-required functions.

Note!

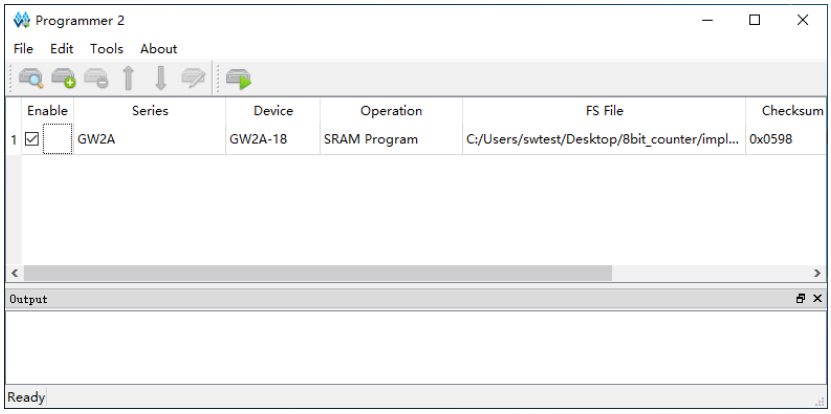
Program Device will be implemented after running Synthesize and Place & Route. If you do not run synthesize and Place & Route first, warnings will pop up.

Double-click "Program Device" or right click and select "Run" to open the Gowin FPGA Programmer, as shown in Figure 4-30.

Note!

The programmer in the Linux installation package is available for Red Hat 5.10. If you need the Red Hat 6/7 programmer, please download it from the Gowin website, rename it as "Programmer", and replace the programmer in the Gowin software installation package.

Figure 4-30 Gowin Programmer



For detailed instructions on how to use the Gowin programmer, please refer to SUG502, Gowin Programmer User Guude.

4.5 Archive and Restore Project

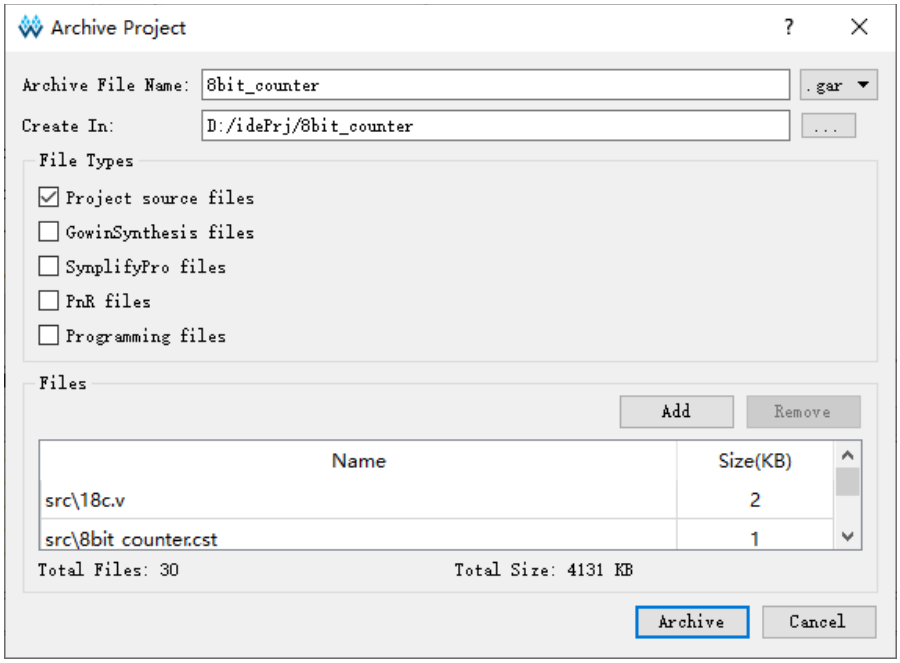
Gowin software supports to archive project and restore archived project. Use the "Archive Project" and "Restore Archived Project" under "Project" in the menu bar to archive or restore archived project.

4.5.1 Archive Project

A dialogue will pop up when clicking Project>Archive Project, as shown in Figure 4-31 .

- File Name is the archived file name. The default name is the same as the current archived project name with .gar suffix.
- Create In" is the path for the archived file, and the default is the current project path
- The File Types includes Project source files (checked by default), GowinSynthesis files, SynplifyPro files, PnR files and Programming files.
- When a file type is checked, the source file, path and size of the current project are displayed below.
- Add and Remove can be used to add and remove archived files.
- After clicking Archive, a prompt box will pop up if the files in the project are not saved.
- A prompt will pop up, indicating whether archived successfully or not.
- When the archive is completed, two files are generated under the "Create In path: the archive project *.gar and the archived file *.garlog. The file with gar suffix compresses and stores all the archived files. The log file with *.garlog suffix is used for checking which files are archived and whether the archive is successful.

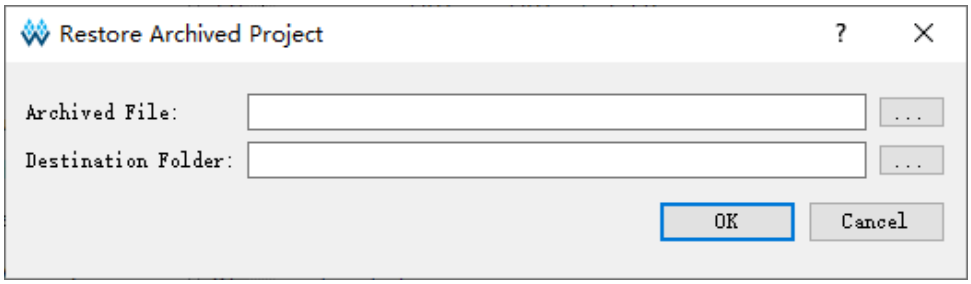
Figure 4-31 Archive Project View



4.5.2 Restore Archived Project

Restore Archived Project dialog will pop up when clicking Project in the menu bar, as shown in Figure 4-32.

Figure 4-32 Restore Archived Project

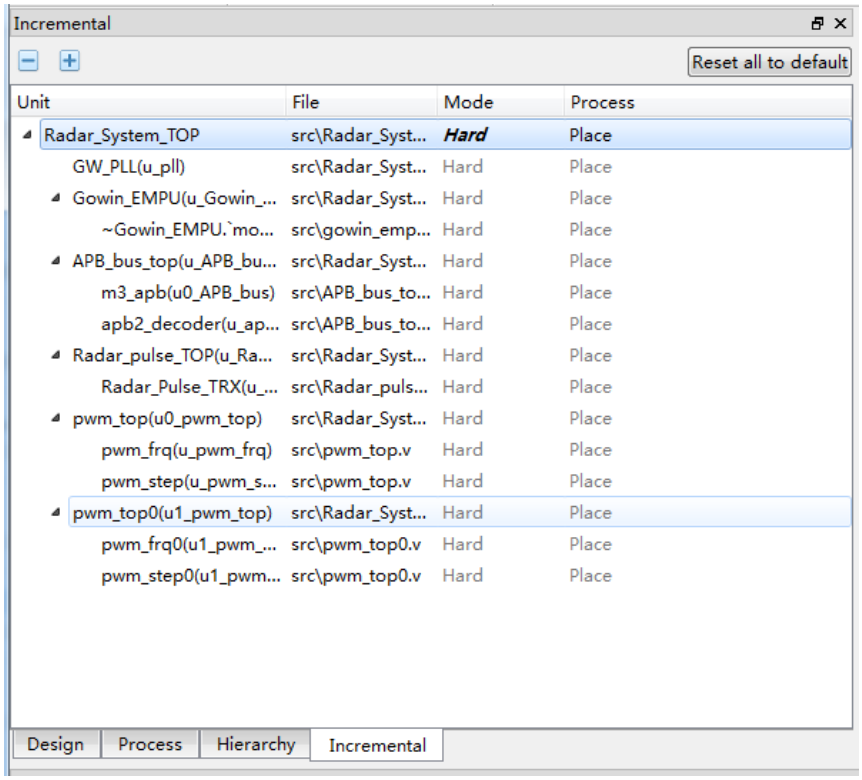


Click the button on the right side of Archived File to select the archive file to restore. After selecting, "Destination Folder" is automatically updated to the path where the archive file is. Click OK and a dialog box will pop up.

4.6 Set Incremental

Gowin incremental currently supports to retain the previous place to reduce runtime. Click "Project > Set Incremental" to open GUI, as shown in Figure 4-33.

Figure 4-33 Incremental GUI



The "Unit" displays the module hierarchy of the design file. The "File" displays the files defined by the module. The "Mode" displays incremental mode, and the "Process" specifies a valid process. Clicking "" and "  " in the upper left corner can collapse and expand all levels in the design. Click "Reset all to default" in the upper right corner to reset all configurations to the default.

The incremental mode can be configured by double-clicking the left key

and currently supports the following three modes:

- Unset: Unset an unspecified incremental;
- Ignore: Ignore the previous synthesis and PnR and rerun;
- Hard: Use previous place.

Process currently only supports Place, indicating that the previous synthesis and place are used, and the process requires the db file that is generated when in place.

The incremental mode defaults to Ignore. When Unset or Ignore selected, Process displays empty. When Hard selected, Process displays Place. Currently, only top mode supports mode, and the corresponding value of sub module is updated synchronously with the top module configuration.

4.7 Exit IDE

There are two ways to exit Gowin software:

1. Select "File > Exit" from the File menu;
2. Click the "  " icon on the upper right of the IDE.

Note!

- If files are not saved, IDE will prompt you to save the files first;
- Save, Save All, and Save As…are only available for text editing;
- Project configuration modification and project files addition and deletion will not be saved to project configuration files in time; They will be saved automatically when the user close the software;
- If the software is running, users cannot exit software by clicking the icon.

5 Tools in Gowin Software

5.1 Synplify Pro

Synthesis is the Pro FPGA synthesis software customized by Synopsys for GOWINSEMI. It supports GOWINSEMI library files implementation, VHDL, and Verilog, etc.

For more details about Synplify Pro, you can refer to the manuals in the Help drop-down list.

5.2 FloorPlanner

Gowin FloorPlanner is designed in-house by Gowin and used for Place, physical constraints and timing optimization. It supports the read and write of I/O, Primitive, block (B-SRAM and DSP), and Group, etc. It also supports the generation of new place and constraints files according to users configuration. The files defines I/ The O attributes, primitives and locations, etc. Gowin FloorPlanner provides a editing way to improve design efficiency and also supports timing optimization, and it supports Gowin all FPGA products.

FloorPlanner can be started using two methods:

1. If no FPGA project is created, users can select "Tools > FloorPlanner" directly from the menu bar. You will need to add netlist files and devices information by selecting "File > New";
2. If an FPGA project is already created, run Synthesize, and then double-click "FloorPlanner" directly in the Process View. The Floorplanner will then load the project files directly before displaying them. The FloorPlanner contains Chip Array and Package View, as shown in Figure 5-1and Figure 5-2.

Note!

- For more details, see SUG935, Gowin Design Physical Constraints User Guide
- The FloorPlanner also supports timing optimization.

Figure 5-1 Chip Array View

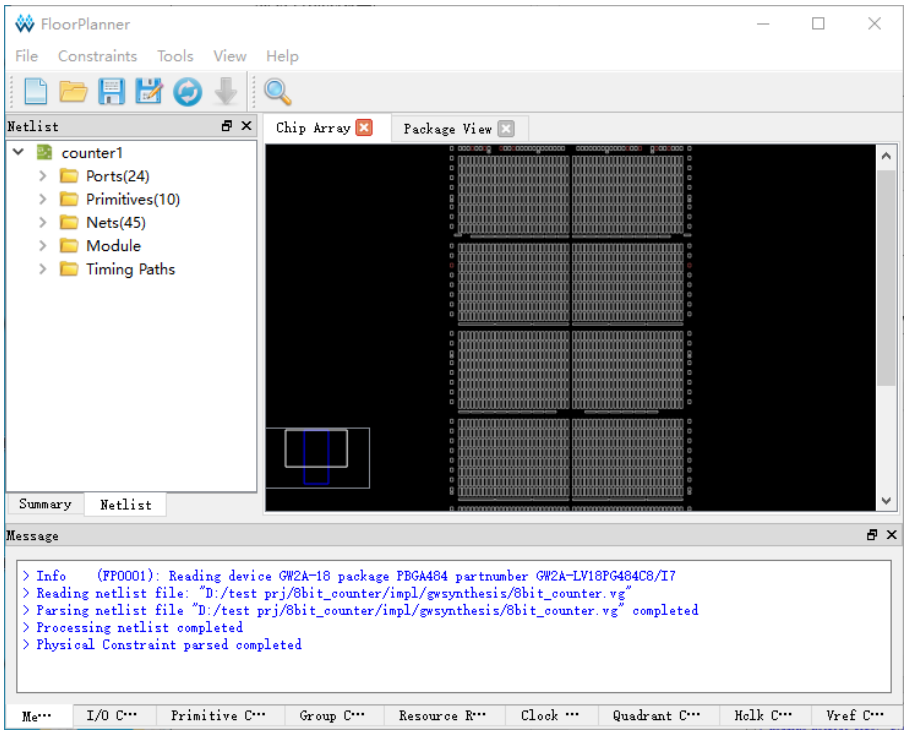
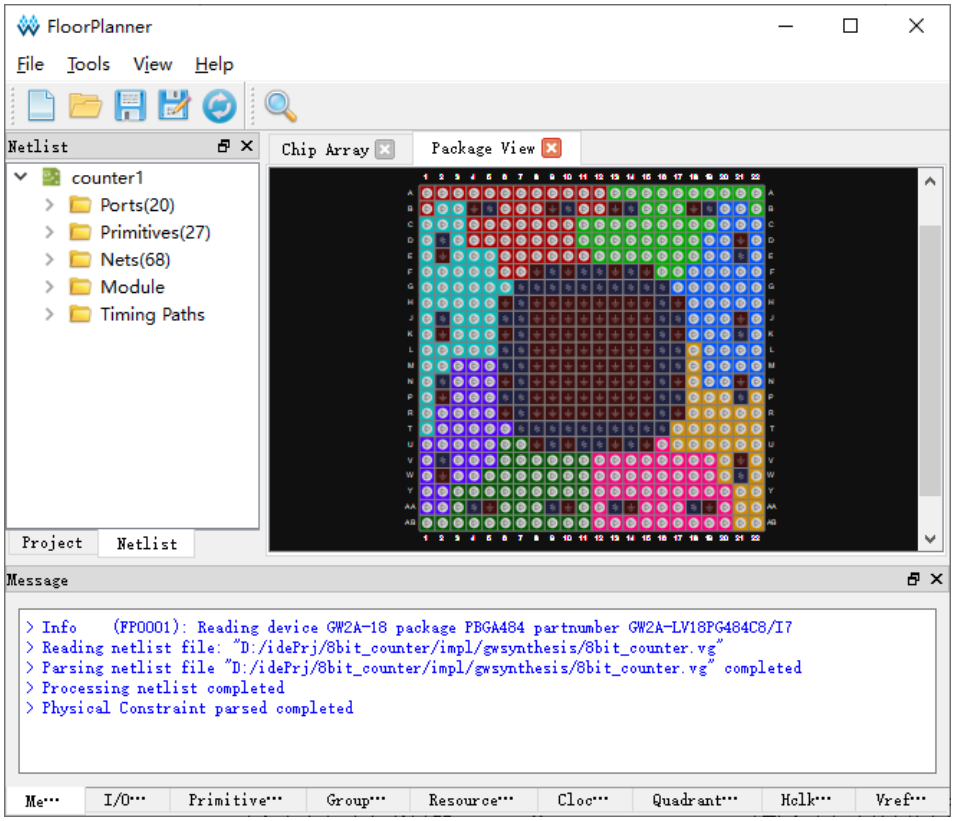


Figure 5-2 Package View



5.3 Timing Constraint Editor

The Gowin Timing Constraints Editor supports multiple timing constraints commands editing, including clock constraints, I/O constraints,

path constraints, and clock report constraints. The Timing Constraints Editor allows an easy and quick timing constraints editing. It supports all GOWINSEMI FPGA devices.

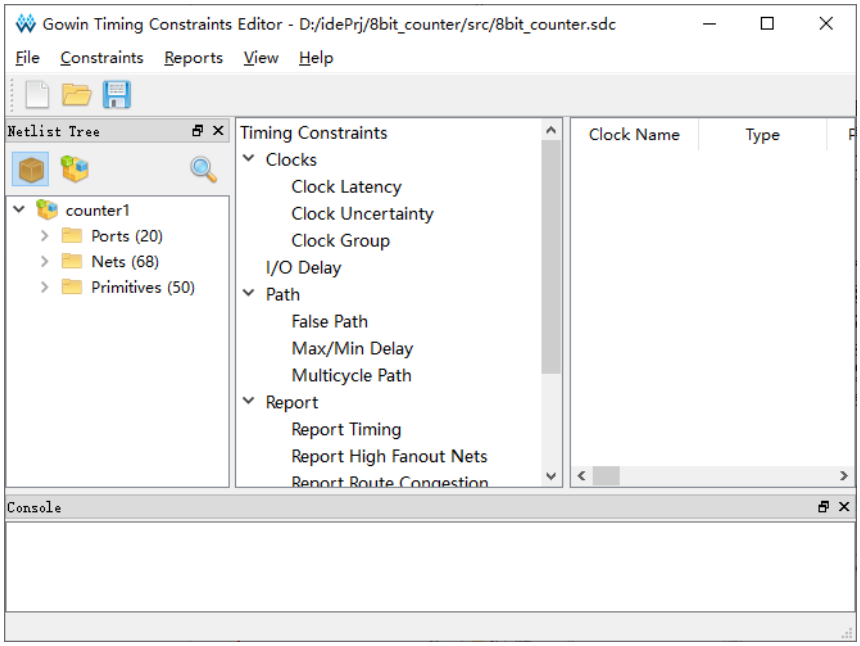
Timing Constraints Editor can be started using two methods:

1. If no FPGA project is created, users can select "Tools > Timing Constraints Editor" from the menu bar. Add netlist files by selecting "File > New";
2. If an FPGA project is already created, Run Synthesize, double-click "Timing Constraints Editor", and the Timing Constraints Editor will load project files directly and display them, as shown in Figure 5-3 .

Note!

For the detailed operation, please refer to SUG940, Gowin Design Timing Constraint User Guide.

Figure 5-3 Create Timing Constraints

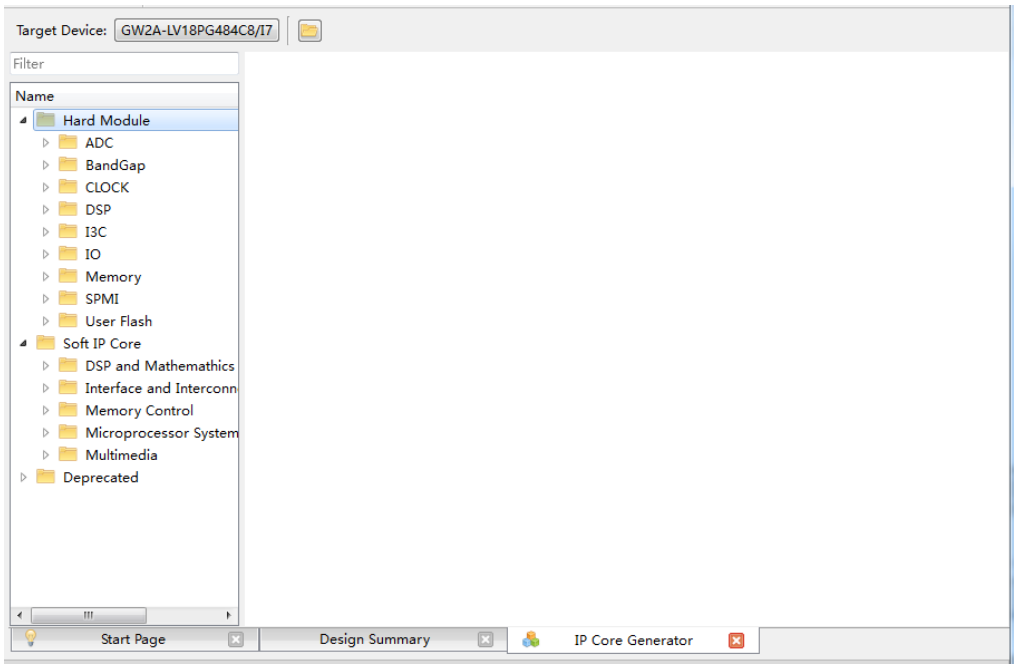


5.4 IP Core Generator

The IP Core Generator in Gowin software is mainly used to generate instantiation components and IPs, which the users can call to implement the required functions. As such, they provide users with a convenient method of creating complex designs. The IP Core Generator includes the modules associated with primitives and the IP Cores associated with reference designs, as shown in Figure 5-4.

Start the IP Core Generator by selecting "IP Core Generator" from the Tools menu.

Figure 5-4 IP Core Generator View



Note!

Current device does as not support the Module and IP Cores which are displayed as grey of.

5.5 Gowin Analyzer Oscilloscope

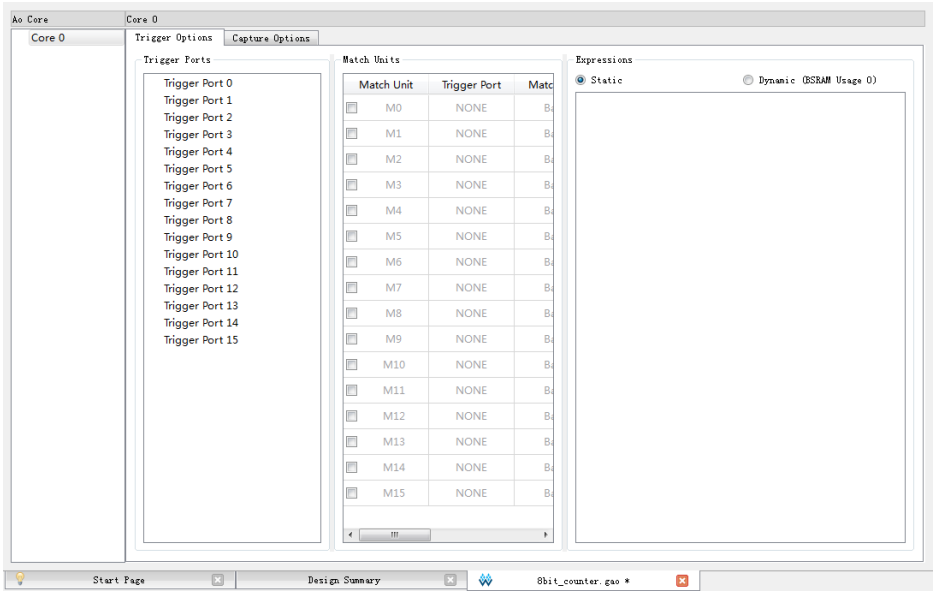
The Gowin Analyzer Oscilloscope (GAO) is a digital signal analyzer that is independently designed by Gowin. It helps users to analyze signal timing in design more easily, and quickly perform system analysis and fault locating, thereby improving design efficiency.

GAO supports RTL-level signal capture and netlist-level after synthesis signal capture, and provides standard version (Standard) and simplified version (Lite) of GAO. Standard GAO can support up to 16 AOs, each of which can be configured with one or more trigger ports, supporting multi-level static or dynamic trigger expressions. Lite GAO is easy to configure, and you do not need to set trigger conditions. Lite GAO can also capture the initial value of the signal, which is convenient for users to analyze the state of power-on. After signal capture, the waveform can be exported, supporting *.csv, *.vcd and *.prn file formats. *.csv and *.prn files can be directly used in matlab and other third-party simulation tools.

The GAO includes the Gowin GAO and the Gowin Analyzer Oscilloscope. The Gowin GAO is mainly used to insert position information into the design, which is predominantly based on the sampling clock, trigger unit, and trigger expression. The Gowin Analyzer Oscilloscope connects software and target hardware through the JTAG interface, and visually displays the data for the sampled signal set by GAO Config File with waveform.

Before starting the GAO, create the GAO config file gao in the Project View to open the GAO configuration view, taking standard version as an example, as shown in Figure 5-5.

Figure 5-5 GAO Configuration View

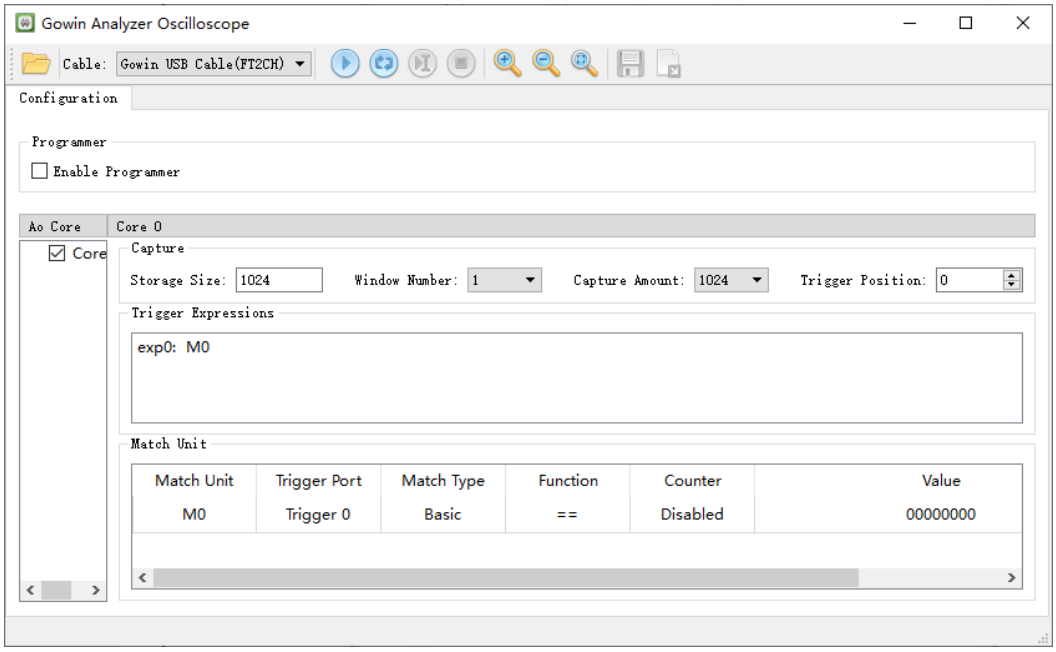


After the configuration file has been created, select "Tools > Gowin Analyzer Oscilloscope" from the menu bar to open the Gowin Analyzer Oscilloscope, as shown in Figure 5-6.

Note!

For further details about how to use the Gowin Analyzer Oscilloscope, please refer to the *SUG114,* Gowin Analyzer Oscilloscope User Guide.

Figure 5-6 GAO



5.6 Power analyzer

The Gowin Power Analyzer (GPA) estimates the power dissipation for your design and provides rich user configuration options. It should be configured per the actual design. The closer the configuration is to the actual design, the more accurate the power dissipation analysis will be.

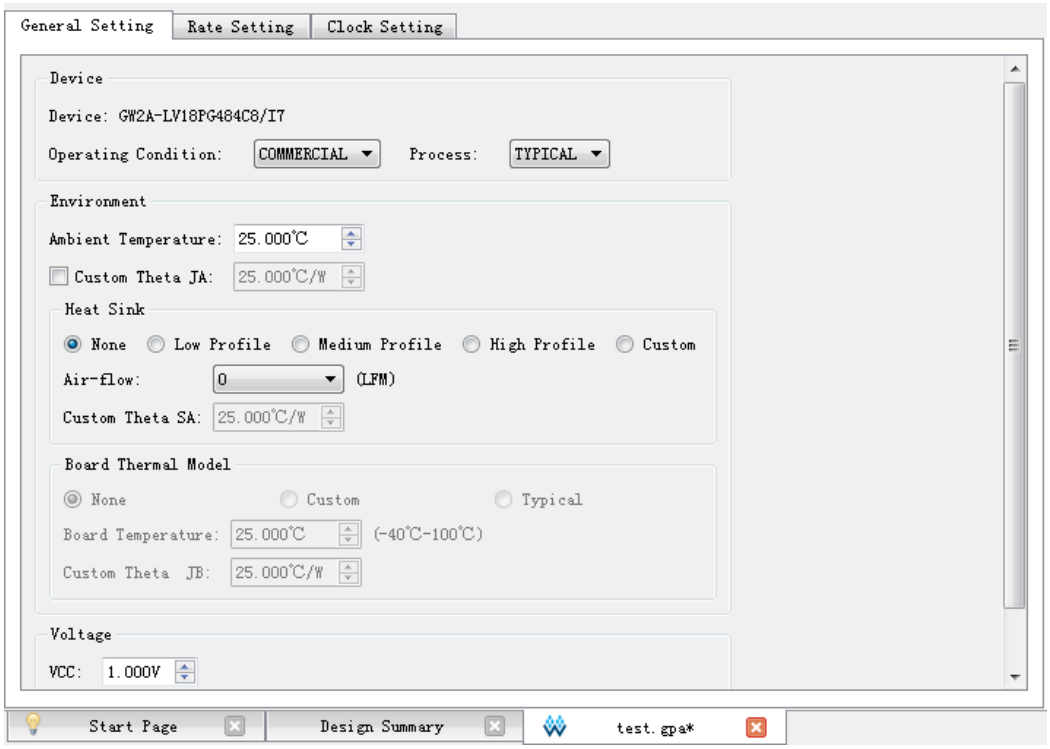
Based on the new configuration file (.gpa), follow the steps outlined below to start the GPA:

1. In the File menu, select "File> New…" to open a "New" dialog box;
2. Select "GPA Config File" and enter "Name" in the pop-up "New GPA Config File" ;
3. Click "OK", and the new GPA config file will be displayed in the Project Design View;
4. Double click on the file name to open the GPA Config view, as shown in Figure 5-7.

Note!

For further details about how to use GPA, please refer to SUG282, Gowin Power Analysis User Guide.

Figure 5-7 GPA Config View



5.7 Memory Initialization File Editor

The Memory Initialization File is an ASCII file with an .mi suffix. You can generate the corresponding Initialization File according to your design to specify the initial value for the memory of each address. The Memory Initialization File editor can be used to open and edit the existed .mi file.

Each line in the Memory Initialization File correlates with one memory. The number of lines is the number of memories and also the memory address depth. The number of columns represents each memory bit; that is, the memory data width. The address decreases from top to bottom with the most significant bit first for each line.

The Gowin block memory initialization file is based on .mi file and supports the Bin File, Hex File, and Hex File with address formats. For the details, see UG285, Gowin B-SRAM & S-SRAM) User Guide. The steps to

use are as follows:

1. In the File menu, select "File> New…" to open the "New" dialog box;
2. Select "Memory Initialization File", as shown in Figure 5-8. Click "OK" and enter the initialization file name in the pop-up "New File" window, and then click "OK". The Initialization File Configuration View is as shown in Figure 5-9;
3. Start the file initialization view as shown in Figure 5-10. Enter the initial value on the left side and configure the initialization file format and depth/width and view on the right side;
4. On the right side, configure the depth and width for the initialization file and the format for the address and initial values in the left table.
   - The depth and width values should be same as the Block Memory or Shadow Memory address depth and data width set in the IP Core Generator. If the address depth and data width in the initialization file are greater than the values set in the IP Core Generator, the IP Core Generator will display the error message. If the depth and width values are less than the BSRAM address depth and data width set in the IP Core Generator, the value of the unassigned address will be initialized to 0 by default. Click "Update" after configuration.
   - The display format of address and numbers on the left can be configured as binary, hexadecimal, and address- hexadecimal, etc.
5. Enter the initial value on the left table, and set the view layout.
   - Right-click on the table header to configure the column number which can be displayed as 1, 8, or16, as shown in Figure 5-11.
   - Double-click and enter the initial value, or right-click to set the value. "Fill with 0" means the initial value is 0, "Fill with 1" means each bit of the initial value is 1, and "Custom Fill" means you can write according to your needs or batch setting, as shown in Figure 5-12.
6. Save the file.

Figure 5-8 New Memory Initialization File

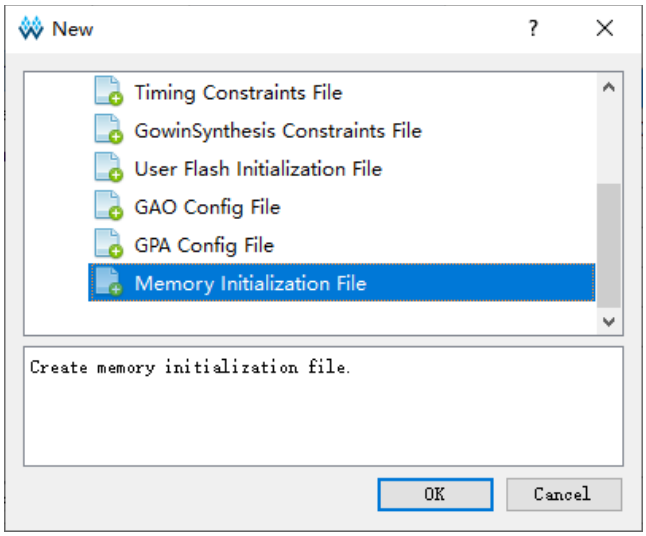


Figure 5-9 New File

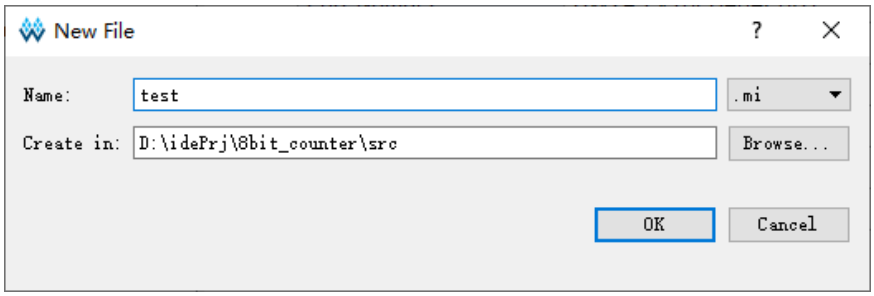


Figure 5-10 Initialization File Configuration

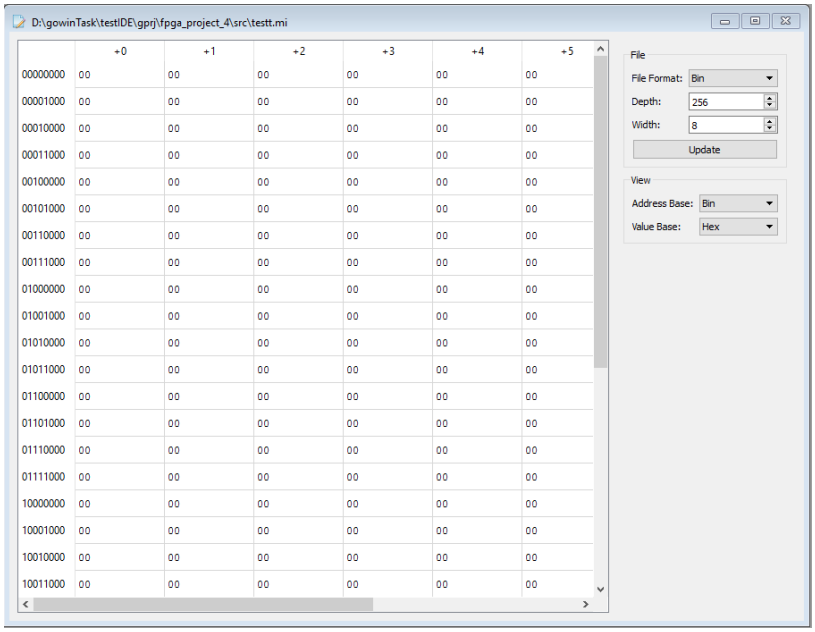


Figure 5-11 Column Setting

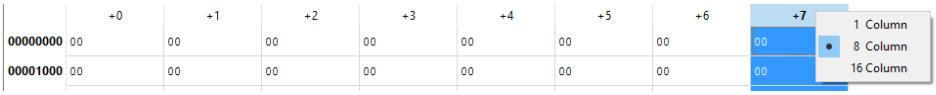
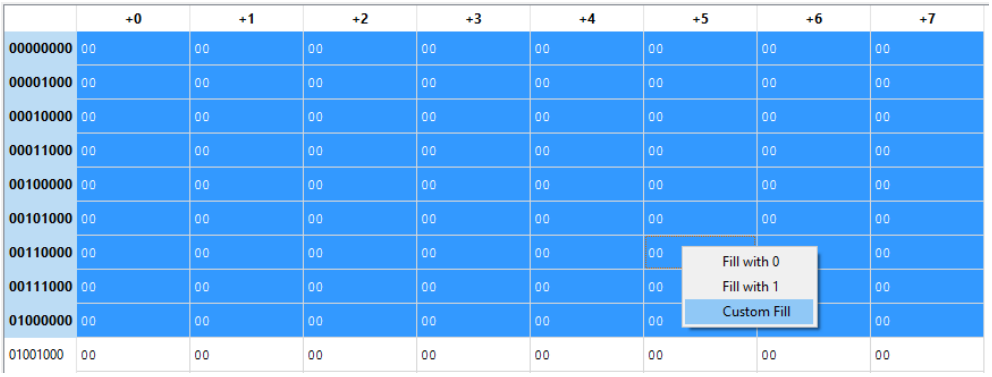


Figure 5-12 Batch Setting



5.8 User Flash Initialization File Editor

User Flash Initialization file is an ASCII file with an . fi suffix. You can generate the corresponding Initialization File according to your design to

specify the initial value for the User Flash of each address. The User Flash Initialization File editor can be used to open and edit the existed . fi file.

The name of User Flash initialization file is *.fi(file_name.fi). Each line in the Memory Initialization File correlates with one memory. The number of lines is the number of memories that needs to be initialized. The contents in the header bracket represent the ordinate address and the abscissa address respectively, separated by a semicolon. The contents after the brackets in each line represent the data initialized by the memory. The data supports binary and hexadecimal, MSB first.

The Gowin User Flash Initialization File supports the binary and hexadecimal formats. The following are examples of the .fi file format.

5.8.1 Bin File

Bin file is a text file that consists of the 0 and 1 binary numbers.

```
//Copyright (C) 2014-2020 Gowin Semiconductor Corporation.
//All rights reserved.
//File Title: User Flash Initialization File
//GOWIN Version: V1.9.6Beta
//Part Number: GW1N-LV4QN32C6/I5
//Device-package: GW1N-4-QFN32-6
//Flash Type: FLASH256K
//File Format: Bin
//Created Time: 5/14/2020 1:07:11 PM
[1:0] 00000001000000010000000100000000
[2:1] 00000000000000010001000100000001
[3:1] 00010000000100010000000100000001
[3:2] 00000001000000010000000100000001
[5:1] 00010001000000000001000000000000
[6:3] 00010000000100010000000100000001
```

5.8.2 Hex File

The Hex file is similar to the Bin file. It consists of hexadecimal numbers 0~F. Copyright (C)2014-2020 Gowin Semiconductor Corporation.

```
//All rights reserved.
//File Title: User Flash Initialization File
//GOWIN Version: V1.9.6Beta
//Part Number: GW1N-LV4QN32C6/I5
//Device-package: GW1N-4-QFN32-6
//Flash Type: FLASH256K
//File Format: Hex
//Created Time: 5/14/2020 1:15:17 PM
[0:1] ff156fa2
```

[0:2] 00111111

[0:4] 03fa21bc

[2:1] e22efffa

[3:2] 0011def2

[3:3] 000e2bc3

Based on the new configuration file (. fi), refer to the following steps to use the initialization file editor:

1. In the File menu, select "File> New…" to open the "New" dialog box;
2. Select "User Flash Initialization File", as shown in Figure 5-13. Click "OK" and enter the initialization file name in the pop-up "New File" window, and then click "OK", as shown in . The Initialization File Configuration View is as shown in Figure 5-14; The devices supported by User Flash Initialization File Editor is the same as the devices supported by User Flash Primitive. If the device you selected does not support User Flash, "Current device do not support flash" will appear at the bottom of "New File" dialog box after you click "OK".

Figure 5-13 New Memory Initialization File

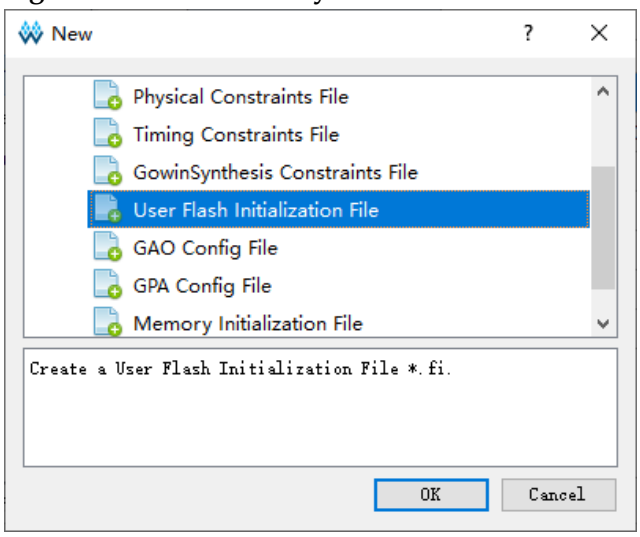
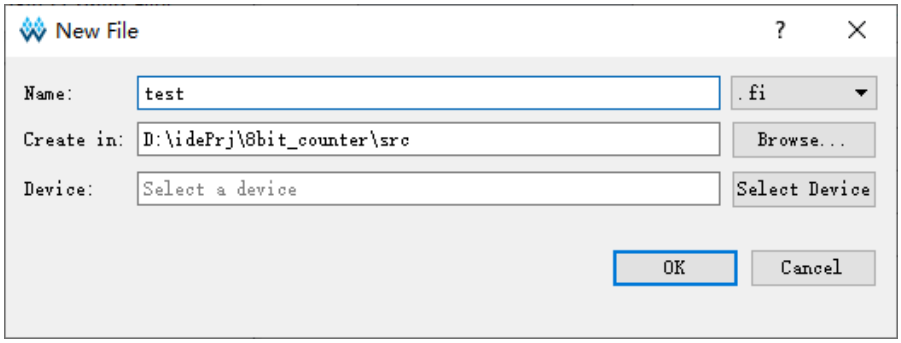
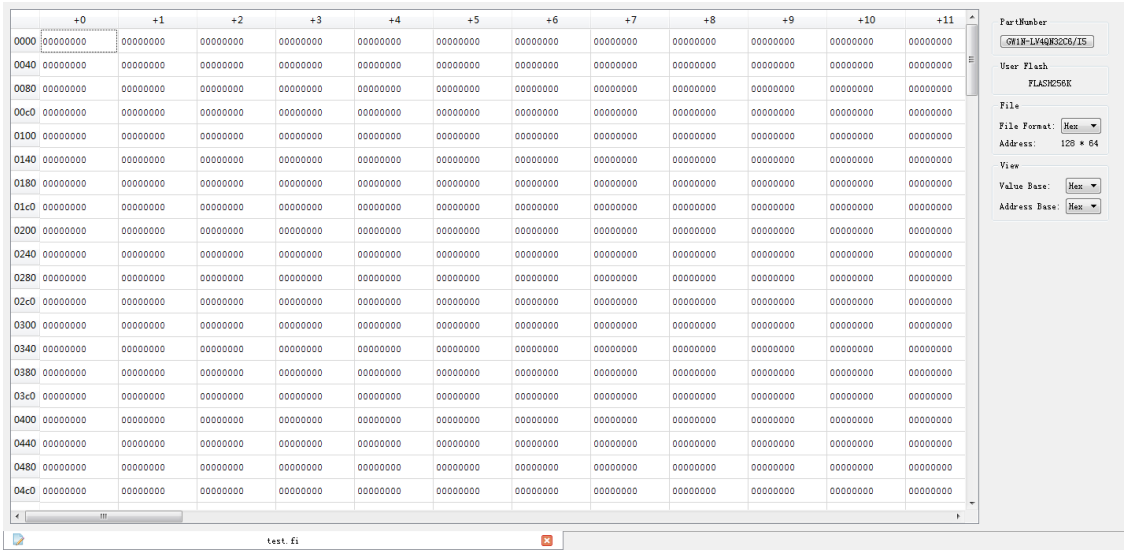


Figure 5-14 New File



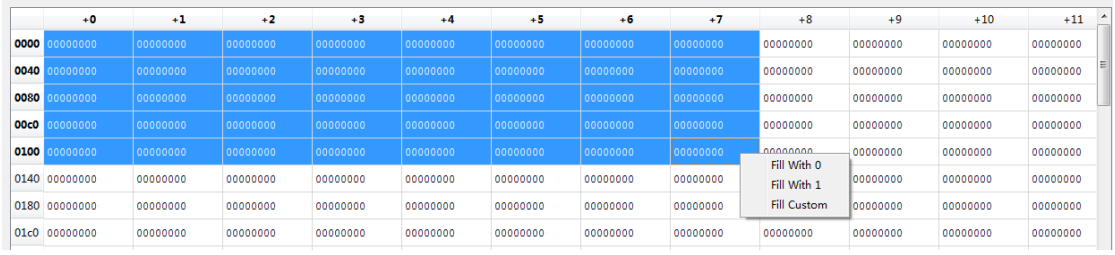
3. Start the file initialization view as shown in Figure 5-15. Enter the initial value on the left side and configure the initialization file format and view on the right side; PartNumber and User Flash also displayed on the right.

Figure 5-15 Initialization File Configuration



4. On the right side, configure Part Number, file format, initial value base and address base.
   - Click "Part Number" and "Select Device" dialog box will pop up. Users can select the other device.
   - The display format of address and numbers on the left can be configured as binary, octal, decimal, hexadecimal, etc.
5. Enter the initial value on the left table, and set the view layout. Double-click and enter the initial value, or right-click to set the value. "Fill with 0" means the initial value is 0, "Fill with 1" means each bit of the initial value is 1, and "Fill Custom" means you can write according to your needs or batch setting, as shown in Figure 5-16.

Figure 5-16 Batch Setting

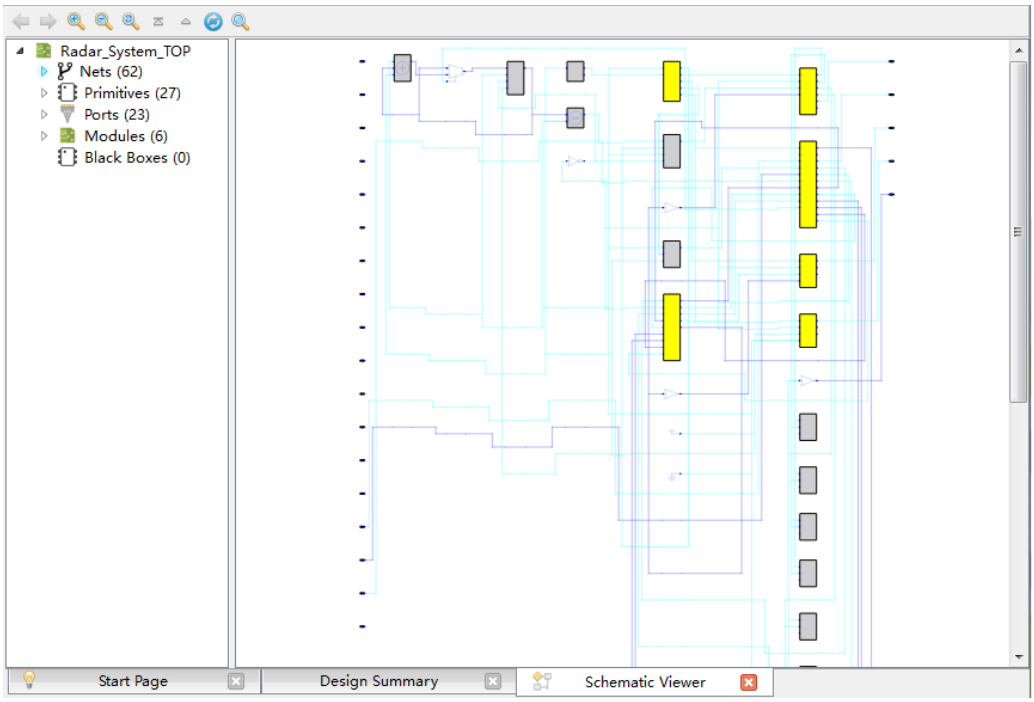


6. Save the file.

5.9 Schematic Viewer

You can click "Tools > Schematic Viewer" to open GUI, as shown in Figure 5-17.

Figure 5-17 Schematic Viewer



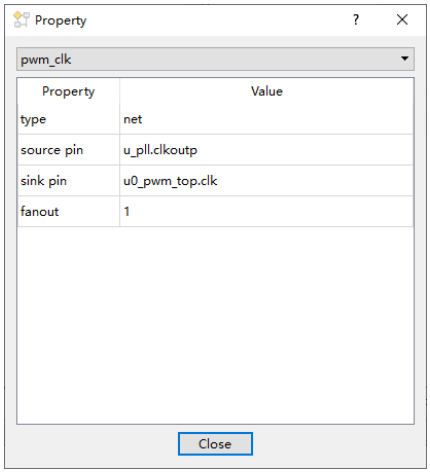
You can understand the design logic by Schematic Viewer, which is helpful to the later modification. Schematic Viewer uses common component symbols to build circuits, including adders, multipliers, registers, and gates, non-gates, and inverters.

Schematic Viewer interface displays backward "", forward "", zoom in "", zoom out "", zoom "," top view "", upper level view "", reload "", and search "". The deisgn hierarchy is displayed on the left side, including module, port, net, primitive, blackbox, and name.

Select a net and right-click to pop up the right-click list. The options include Expand Net and Property:

- Expand Net: Select the net and its associated primitive/module/port in the schematic;
- Property: The net property as shown in Figure 5-18.

Figure 5-18 Net Property



Select a primitive and right-click to pop up the right-click list. The options in the right-click list include Filter and Property. Click "Filter" to display the current primitive in the schematic. Click "Property" to pop up the properties view.

Expand Port, Filter, and Property are displayed in the right-click list after a port is selected. Click "Expand Port" to select the port and its associated primitive/module/port in the schematic.

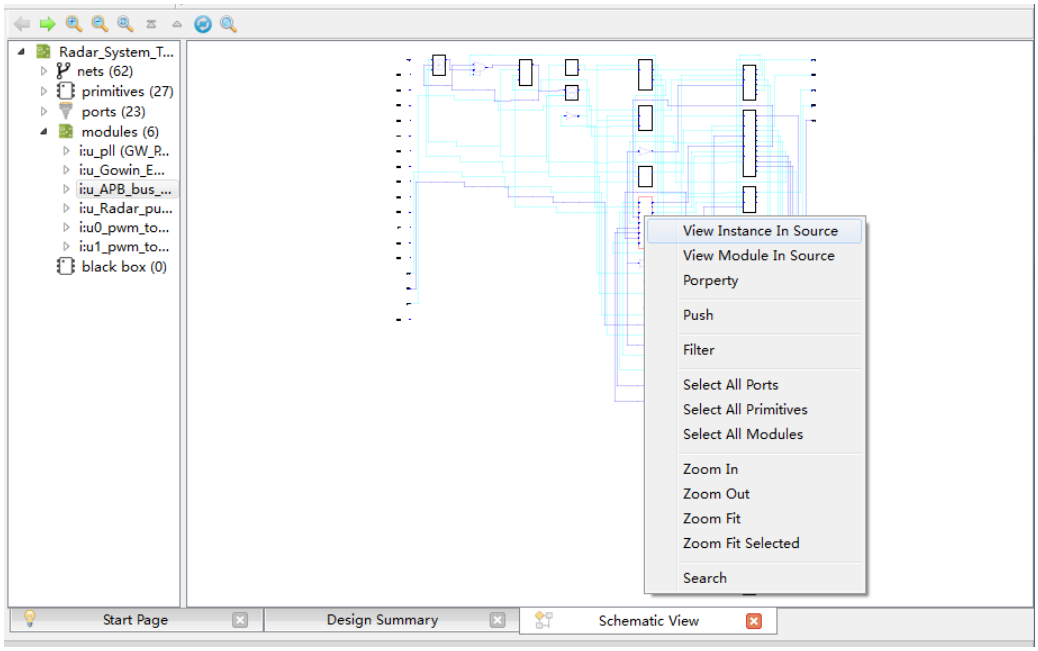
Push, Filter, and Property are displayed in the right-click list after a module is selected. Click "Push" to view the schematic.

In the schematic, right-click to pop up a right-click list, including following options:

- Sellect All Ports: Select all ports;
- Sellect All Primitives: Select all primitives;
- Sellect All Modules: Select all modules;
- Zoom In: Zoom in schematic;
- Zoom Out: Zoom out schematic;
- Zoom Fit: Zoom fit schematic;
- Search: Search.

Select a module in the schematic and right-click to pop up the right-click list, as shown in Figure 5-19. Click "View Instance In Source" to jump to the instantiation, and click "View Module In Source" to jump to the definition.

Figure 5-19 Right-click List of Module



6 Description of Output Files

In the process of FPGA design, Gowin software generates bitstream files, and pin constraints location files (io.cst), and also generates multiple reports depending on different parameters. The reports include the place&route report, timing report, and power analysis report. In addition, you can right-click on Place & Route to modify the configuration and attributes to generate pins constraints, simulation files, etc.

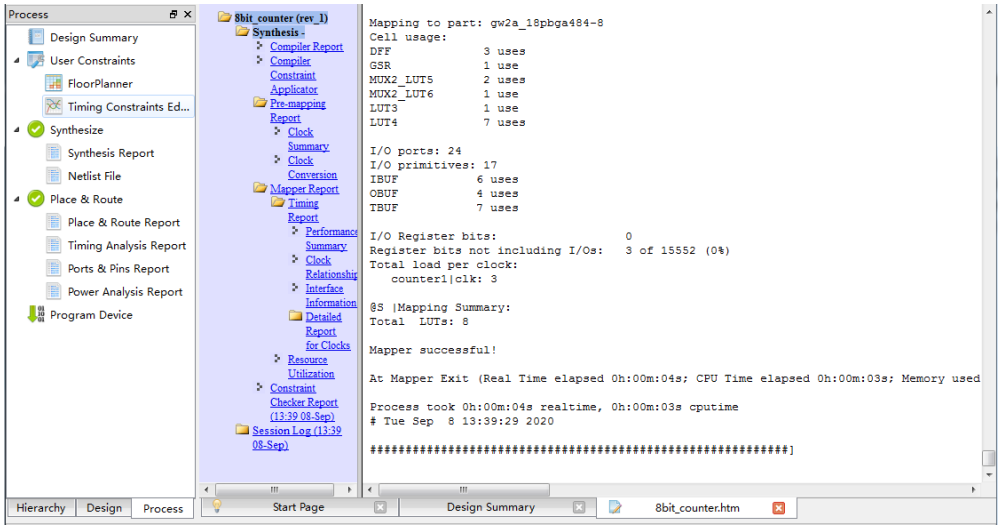
6.1 Synthesis Report

After the synthesis, the corresponding synthesis reports and netlist files are generated, including synplifyPro and GowinSynthesis.

6.1.1 Synplify Pro Report

If selecting Synplify Pro, the synthesis report will be generated. Synplify Proreport includes various resources, including device, synthesis and timing, etc. Double click ″Synthesis Report″ in the Process View to open the project corresponding synthesis report, as shown in Figure 6-1.

Figure 6-1 Synplify Pro Report

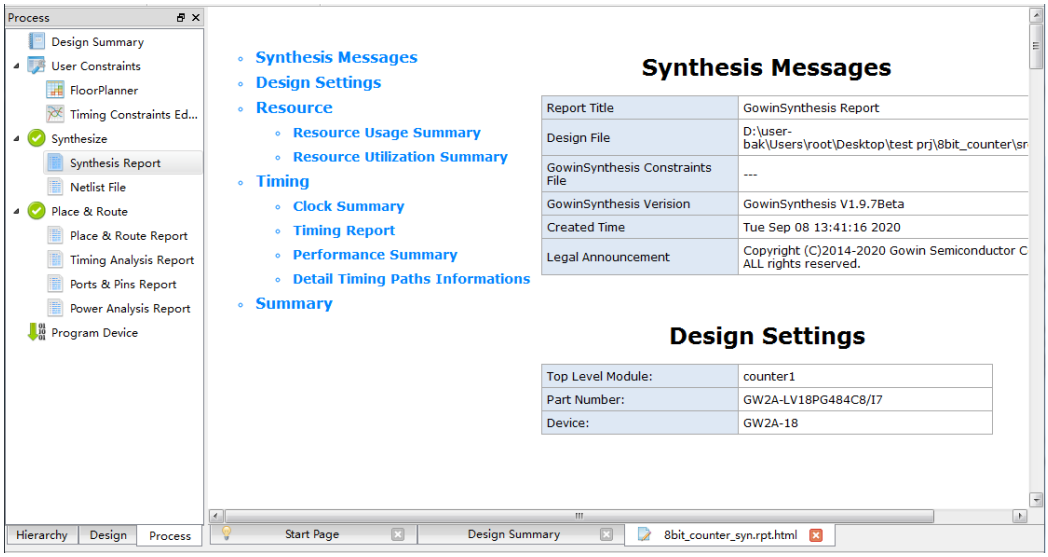


6.1.2 GowinSynthesis Report

If selecting GowinSynthesis, a report named *_syn.rpt.html is

generated, including Synthesis Message, Design Settings, Resource, Timing, Message and Summary, as shown in Figure 6-2.

Figure 6-2 GowinSynthesis Report



The details are as follows:

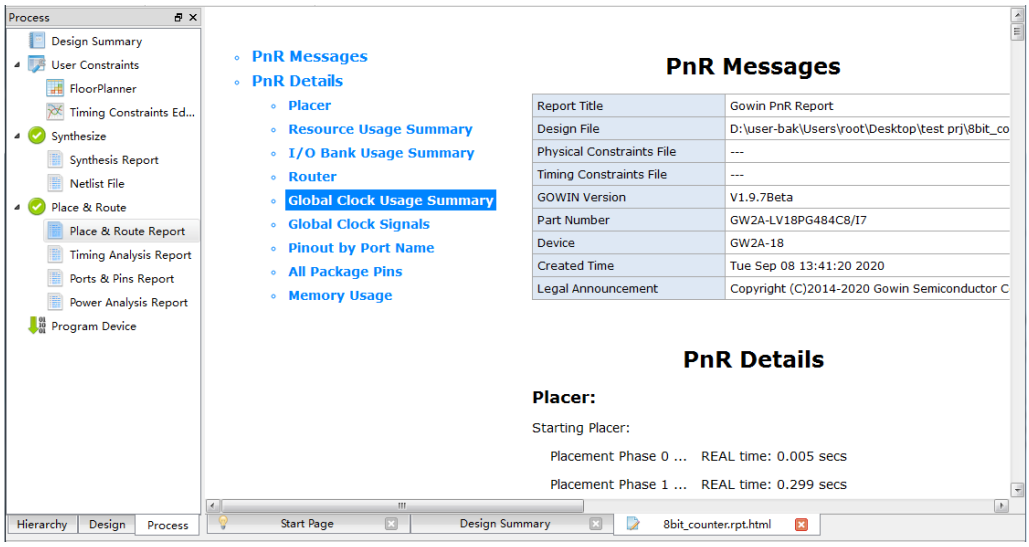
- Synthesis Message: It includes design file, the GowinSynthesis version, running time, etc.
- Design Settings: Configuration information, including the top-level module of the design file and the specified chip type;
- Resource: It includes resource statistics and chip utilization statistics;
- Timing: It includes Clock Summary, Timing Report, Performance Summary and Detail Timing Paths Informations.
- Summary: The number of warnings, errorsin the output information, and the synthesis actual running time and CPU running time, as well as the memory peak.

6.2 Place&Route Report

The Place&Route Report describes the resource, memory consumption, time consumption, etc. occupied by the user design, with the file suffix .rpt.html. Check the *.rpt.html file for further details.

Double-click "Place & Route Report" in the Process View to open the project that corresponds to the Place&Route report, as shown in Figure 6-3.

Figure 6-3 Place & Route Report



The details are as follows:

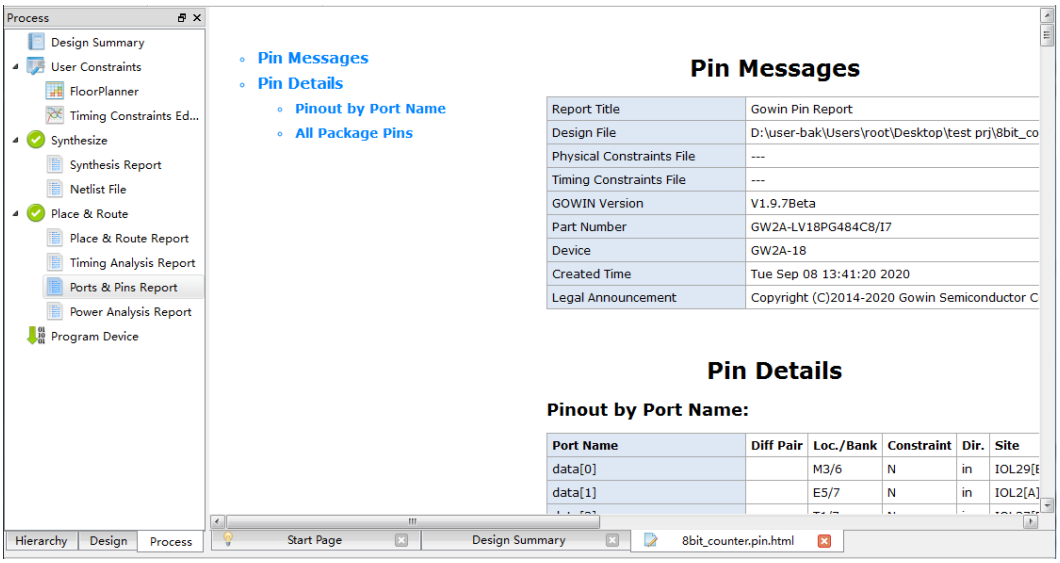
- PnR Messages: Overview of the report, including report name, path and name of design case, physical constraints file, timing constraints file, software, device information, report creation time and declaration;
- Placer: Time spent at each stage and total time spent;
- Resource Usage Summary: Chip resources utilization in user design;
- I/O BANK0 Usage Summary: I/O BANK0 in user design;
- Router: Time spent at each stage and total time spent;
- Global Clock Usage Summary: Global clock used;
- Global Clock Signals: Clock signals used in the user design;
- Pinout by Port Name: Pinout by port in user design;
- All Package Pins: Details of all the pins in the device package;
- Memory Usage: Memory utilization for PnR.

6.3 Ports and Pins Report

The Ports and Pins Report is the ports and pins files after placement. It includes ports type, attributes, and locations, etc. The generated file is saved with the .pin.html suffix. Check the .pin.html file for further details.

Double-click "Ports & Pins Report" in the Process View to open the report corresponding to the project, as shown in Figure 6-4.

Figure 6-4 Ports & Pins Report



The details are as follows:

- Pin Messages: Overview of the report, including report name, path and name of design case, physical constraints file, timing constraints file, software, device information, report creation time and declaration;
- Pinout by Port Name: Pinout by port in user design;
- All Package Pins: Details of all the pins in the device package;

6.4 Timing Report

The timing report is available in web format and text format. The default is web format.

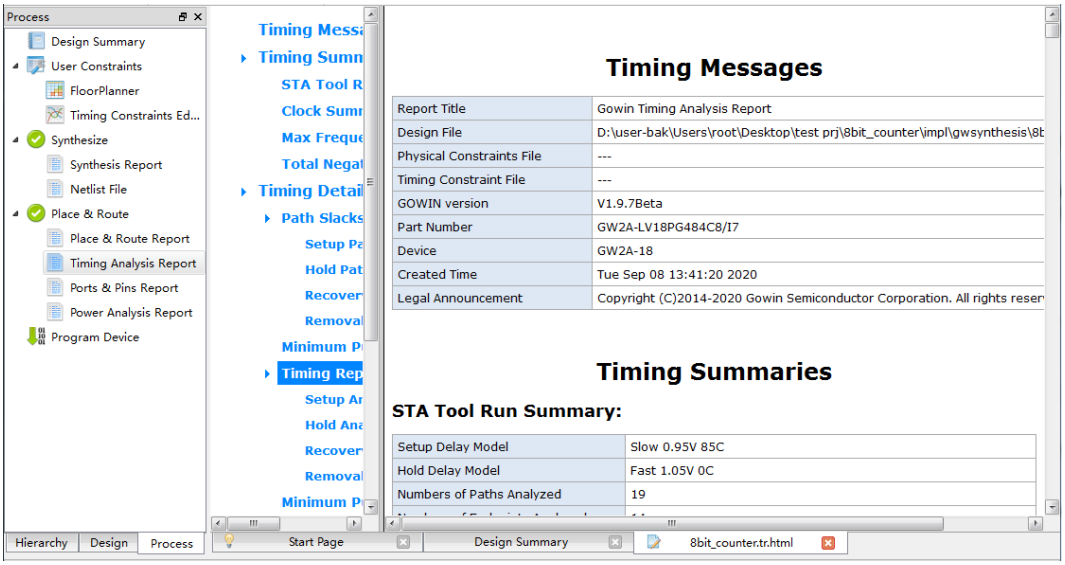
The Timing report includes set-up time check, hold-time check, restoring time check, removal time check, Min. clock pulse check, max. fan out path, Place&Route congestion report, etc. by default. The timing report also includes the Max. frequency report.

Double-click ″Timing Analysis Report″ in the Process View to open the timing analysis report for the project, as shown in .

Note!

For the details, please refer to SUG940, Gowin Design Timing Constraints User Guide.

Figure 6-5 Timing Report



6.5 Power Analysis Report

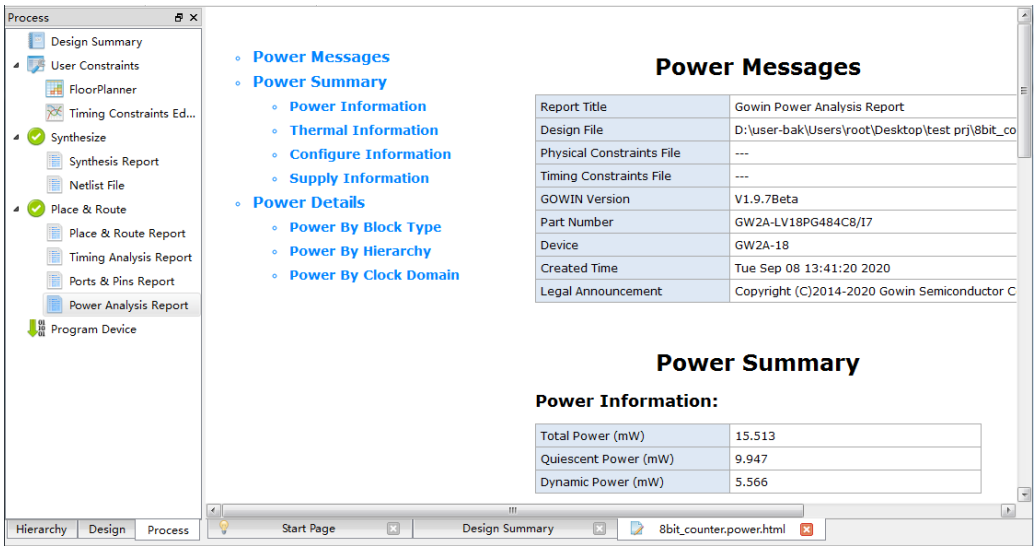
The Power Analysis Report mainly includes the power dissipation estimation for your design. It is designed to help you evaluate the basic power consumption of your design.

Double-click "Power Analysis Report" in the Process View to open the analysis report that corresponds to the project, as shown in Figure 6-6.

Note!

For the details, pleaserefer to *SUG282*, Gowin Power Analysis User Guide

Figure 6-6 Power Analysis Report



Appendix A Tcl Command

Gowin software supports command line mode in addition to interface mode. In the following description, the content in <> must be specified, and the content in [] is optional.

A.1 Command Line Mode

A.1.1 gw_sh.exe

Syntax

Command: Under the installation directory \x.x\IDE\bin\gw_sh.exe

Parameter:

[script file]

Parameter is null: Enter the command line console mode directly;

script file: Execute a specified script file, optional

Application Example:

```
# Start Command Line mode
gw_sh.exe
#Execute script file
gw_sh.exe script_file
```

A.2 Command Introduction

A.2.1 add_file

add_file [options] <file...>

Add design file

Parameter:

<File...> : The file to be added. You can specify more than one design file to add and the files are separated by spaces.

Options:

- The -type add_file command automatically determines the file type based on the file suffix, or can be used to specify the file type. The supported file types are verilog, vhdl, netlist, cst, sdc, fdc, gao, gpa, gsc.

- -disable: Disable the added file. The disabled file is added to the file list and is not used in the flow implementation. Relevant command: Set_file_enable.
- -h, --help: Display help information.

For example:

add_file abc.v

add_file –type vhdl 1.vhd 2.vhdl 3.vhd

A.2.2 rm_file

rm_file [options] <files...>

Remove design file

Parameter:

<File...> : The file to be removed. You can specify more than one design file to remove.

Option:

-h, --help: Display help information.

For example:

rm_file a.v

rm_file a.v b.v c.v

A.2.3 set_device

set_device [options] <part number>

Set device

Parameter:

The device part number, such as GW1N-UV4LQ144C6/I5.

Options:

- -name <name>: Specify the name of the device, such as GW1N-4. In most cases, the device can be selected by Part Number, and the -name is optional. However, some different devices may have the same Part Number, in which case the device name must be specified by the -name.
- -h, --help: Display help information.

For example:

set_device GW1N-LV1CS30C6/I5

set_device -name GW1N-4 GW1N-UV4LQ144C6/I5

A.2.4 set_file_prop

set_file_prop [options] <file...>

Set file property

Parameter:

<File...>: The file to be set. You can specify more than one file and the files are separated by spaces.

Options:

- -lib <name>: Set library name It is only valid for VHDL file.
- -h, --help: Display help information.

For example:

set_file_prop -lib work abc.vhd

A.2.5 run

run [options] <process>

Run the whole process or a process.

Parameter:

<process>: Specify the process name, such as syn and pnr. It can also specify all, indicating running the whole process.

Options:

-h, --help: Display help information.

For example:

run pnr

run all

A.2.6 set_file_enable

set_file_enable [options] <file> <true|false>

Set the file as true or false

Parameter:

- <file> : The file to be set.
- <true|false>: It can set as true or false.

Options:

-h, --help: Display help information.

For example:

set_file_enable abc.v fasle

A.2.7 saveto

saveto [options] <file>

Save the current project to tcl, including the device, file and process, etc.

Parameter:

<file> : The file to be exported.

Options:

- -all_options saveto: Save only the modified, which is different from the default value. You can save all information by -all_options.
- -h, --help: Display help information.

For example:

saveto project.tcl

saveto -all_options project.tcl

A.2.8 set_option

set_option [options]

Set options

Options:

- -output_base_name <name>

  Specify the output files. This option specifies the base name of the file, and different processes use the appropriate extension based on the type of output file. For example, if -output_base_name abc, the netlist file generated by gowinsynthesis is named abc.vg.

- -synthesis_tool <tool>

  Specify gowinsynthesis or synplify_pro.

- -top_module <name>

  Specify Top Module/Entity

- -include_path <path or path list>

  Specify include path When multiple include paths are specified, they need to be separated by a semicolon and the path is contained by a pair of braces {}, such as -include_path {/path1;/path2;/path3}. When a relative path is specified, the result is the path returned by the relative pwd command.

- -in <incremental.cfg >

  Specify incremental.cfg.

Synthesis Configuration

- -verilog_std <v1995|v2001|sysv2017>

Specify verilog standard, such as Verilog 95 / Verilog 2001 / System Verilog, and the default is System Verilog.

- -vhdl_std <vhd1993|vhd2008|vhd2019>

  Specify VHDL standard: VHDL 1993 / VHDL 2008 / VHDL2019

- -dsp_balance <0|1>

Specify whether to run DSP Balance automatically when synthesizing. It is only valid for GowinSynthesis and the default value is 0.

0: DSP Balance will not be performed automatically.

1: DSP Balance will be performed automatically.

- -allow_duplicate_modules <0|1>

For Verilog, duplicate module names are allowed after this option is enabled, and the software uses the last definition of the module and ignores any previous definitions, and the default value is 0.

0: Duplicate names are not allowed.

1: Duplicate names are allowed.

- -auto_constraint_io <0|1>

  Whether to use the default constraint for I/O ports without user-defined constraints.

  0: Default constraint will not be used for I/O ports without user-defined constraints;

  1: Default constraint will be used for I/O ports without user-defined constraints.

- -compiler_compatible <0|1>

  Whether to allow cross-process/ boundary to synthesize three states.

  0: Allow cross-process/boundary to synthesize three states.

  1: Not allow cross-process/boundary to synthesize three states.

- -default_enum_encoding <default|onehot|gray|sequential>

  Set the default enum type encoding mode (VHDL only).

- -disable_io_insertion <0|1>

  Enable or disable I/O insertion, 0 by default.

  0: Disable I/O insertion.

  1: Enable I/O insertion.

- -fix_gated_and_generated_clocks <0|1>

  Strobe and generated clock optimized when this option is enabled, 0 by default.

  0: Disable optimization.

  1: Enable optimization.

- -frequency <value>

  Specify the global frequency.

- -looplimit <value>

  Set the loop limit value of the default editor in RTL. The default value is 2000;

- -maxfan <value>

  Set fanout valuefor an input port, net, or register output, 10000 by default.

- -multi_file_compilation_unit <0|1>

  When this option is enabled, the Verilog compiler uses the compilation unit in multiple file-defined modules, 1 by default.

  0: Disable.

  1: Enable

- -num_critical_paths <value>

  Specify the number of the key paths in the report.

- -num_startend_points <value>

  Specify the number of start and end points of a path with the worst slack in a timing report.

- -pipe <0|1>

Run faster by creating a pipeline, 1 by default.

0: Disable.

1: Enable.

- -resolve_multiple_driver <0|1>

When the network is driven by a VCC or GND, enabling this option to connect the network to the driver of the VCC or GND, and the default value is 0.

0: Disable.

1: Enable.

- -resource_sharing <0|1>

Whether to enable resource sharing, 1 by default.

0: Disable.

1: Enable.

- -retiming <0|1>

When this option is enabled, registers can be moved to the combined logic to improve performance, and the default value is 0.

0: Disable.

1: Enable.

- -run_prop_extract <0|1>

Enable/disable comments for some properties associated with clocks and extensions on the RTL view.

0: Disable.

1: Enable.

- -rw_check_on_ram <0|1>

Enable this option to automatically insert bypass logic to prevent simulation mismatches when read during write, 1 by default.

0: Disable.

1: Enable.

- -supporttypedflt <0|1>

When this option is enabled, the compiler passes the init value to the mapper through the syn_init.

0: Disable.

1: Enable.

- -symbolic_fsm_compiler <0|1>

Enbale /disable FSM compiler, 1 by default.

0: Disable.

1: Enable.

- -synthesis_onoff_pragma <0|1>

Whether to ignore the synthesis on/off code.

0: Disable.

1: Enable.

- -update_models_cp <0|1>

Whether to update a complier point (or top level) because of updating within a compiler point.

0: Disable.

1: Enable.

- -write_apr_constraint <0|1>

Write to vendor-specific constraints files, 1 by default.

0: Disable.

1: Enable.

Note!

For further details about the configuration methods, please refer to the the SynplifyPro manual fpga_command_reference.pdf in the Gowin installation directory: installPath\SynplifyPro\doc;

Place & Route Configuration

- -gen_sdf <0|1>

Specify whether Place & Route to generate an SDF file, 0 by default.

0: Disable.

1: Enable.

- -gen_io_cst <0|1>

Specify whether Place & Route to generate port physical constraints file named as *.io.cst. The default value is 0.

0: Disable.

1: Enable.

- -gen_ibis <0|1>

Specify whether Place & Route to generate the input/output buffer specification file named as *.ibs. The default is 0.

0: Disable.

1: Enable.

- -gen_posp <0|1>

Specify whether Place & Route to generate place file named as *.posp. The default is 0.

0: Disable.

1: Enable.

- -gen_text_timing_rpt <0|1>

Specify whether Place & Route to generate plain text timing report named as *.tr. The default is 0.

0: Disable.

1: Enable.

- -gen_sim_netlist <0|1>

Specify whether Place & Route to generate simulation file named as

*.vo. The default is 0.

0: Disable.

1: Enable.

- -show_init_in_vo <0|1>

  Add the default initial value to the instance of the generated post-PnR simulation model file. The default is 0.

  0: Disable.

  1: Enable.

- -show_all_warn <0|1>

  Output all warnings when -PnR is running. The default is 0.

  0: Disable.

  1: Enable.

- -timing_driven <0|1>

  Timing driven optimization of the placement and routing is performed. The default is 1.

  0: Disable.

  1: Enable.

- -use_scf <0|1>

  Use *.scf files generated by Synplify Pro as the additional timing constraint files. The default is 0.

  0: Disable.

  1: Enable.

- -cst_warn_to_error <0|1>

  Change the Physical Constraint Warning to Error. The default is 1.

  0: Disable.

  1: Enable.

- -rpt_auto_place_io_info <0|1>

  Report auto-placed IO. The default is 0.

  0: Disable.

  1: Enable.

- -place_option <0|1>

  Place algorithm option, and the default is 0.

  0: Use default algorithm.

  1: Use algorithm 1.

- -route_option <0|1|2>

  Route algorithm option, and the default is 0.

  0: Use default algorithm.

  1: Use algorithm 1.

  2: Use algorithm 2.

- -ireg_in_iob <0|1>

Place input register to IOB, 1 by default.

0: Disable.

1: Enable.

- -oreg_in_iob <0|1>

  Place output register to IOB, 1 by default.

  0: Disable.

  1: Enable.

- -ioreg_in_iob <0|1>

  Place in/out register to IOB, 1 by default.

  0: Disable.

  1: Enable.

Note!

For more details of Place&Route options, refer to 4.3.3Place & Routein this document.

Dual-purpose Pins Configuration

- -use_jtag_as_gpio <0|1>

  Use JTAG as general IO. JTAG related pins are TCK, TMS, TDI, and TDO. The default is 0.

  0: JTAG.

  1: General IO.

- -use_sspi_as_gpio <0|1>

  Use SSPI as general IO. SSPI related pins are SI/D2, SO/D1, and SSPI_CS_N/D0. The default is 0.

  0: SSPI.

  1: General IO.

- -use_mspi_as_gpio <0|1>

  Use MSPI as general IO. MSPI related pins are FASTRD_N/D3, MCLK/D4, MCS_N/D5, MI/D7, and MO/D6. The default is 0.

  0: MSPI.

  1: General IO.

- -use_ready_as_gpio <0|1>

  Use READY as general IO. READY related pin is READY. The default is 0.

  0: READY.

  1: General IO.

- -use_done_as_gpio <0|1>

  Use DONE as general IO. DONE related pin is DONE. The default is 0.

  0: DONE.

  1: General IO.

- -use_reconfign_as_gpio <0|1>

  Use RECONFIG_N as general IO. RECONFIG_N related pin is

RECONFIG_N. The default is 0.

0: RECONFIG_N.

1: General IO.

- -use_mode_as_gpio <0|1>

Use MODE as general IO. MODE related pins are MODE0, MODE1, and MODE2. The default is 0.

0: MODE

1: General IO.

BitStream Configuration

- -bit_format <txt|bin>

Specify the bitstream file format.

- -bit_crc_check <0|1>

Enable CRC check.

0: Disable.

1: Enable.

- -bit_compress <0|1>

Compress the generated bitstream file.

0: Disable.

1: Enable.

- -bit_encrypt <0|1>

Encrypt the bitstream file, only GW2A series supported.

0: Disable.

1: Enable.

- -bit_encrypt_key <key>

Combined with "-bit_encrypt", it allows the user to customize the encrypted key.

- -bit_security <0|1>

Enable security bit.

0: Disable.

1: Enable.

- -bit_incl_bsram_init <0|1>

Print BSRAM Initial Value to Bitstream file.

0: Disable.

1: Enable.

- -bg_programming <0|1>

Program Flash without interrupting the current FPGA running.

0: Disable.

1: Enable.

- -secure_mode <0|1>

Enable secure mode. Use JTAG pin as GPIO, and device can be programmed only once.

0: Disable.

1: Enable.

- -loading_rate <value>

In AutoBoot mode and MSPI mode, the rate of loading bitstream data from flash to sram is 2.500MHz by default.

- -spi_flash_addr <value>

Specify SPI Flash address.

- -program_done_bypass <0|1>

After this option is configured, when the Done Final internal signal takes effect, the external Done Pin remains low so that new bitstream can be forwarded after the bitstream is loaded. The default is 0.

0: Disable.

1: Enable.

- -wakeup_mode <0|1>

Enable wake up mode.

0: Disable.

1: Enable.

- -user_code <default|value>

User can customize user code.

Note!

For more details of Bitstream options, refer to 4.3.3 BitStream in this document.

Unused Pin Configuration

-unused_pin <default|open_drain>

Set IO types and attribute values for unused pins (except multiplexing pins).

Note!

For more details of Unused Pin option, refer to 4.3.3 Unused Pin.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