GW1N-4 FPGA Download DUALBOOT Program

Overview

To realize the functional requirements of the DUALBOOT module of GW1N-4 FPGA devices, a few external circuits are loaded based on the chip download circuit. Two types of circuits are provided, and their usage varies according to the power design employed. The DUALBOOT download demand can be met via circuit simulation and board-level verification.

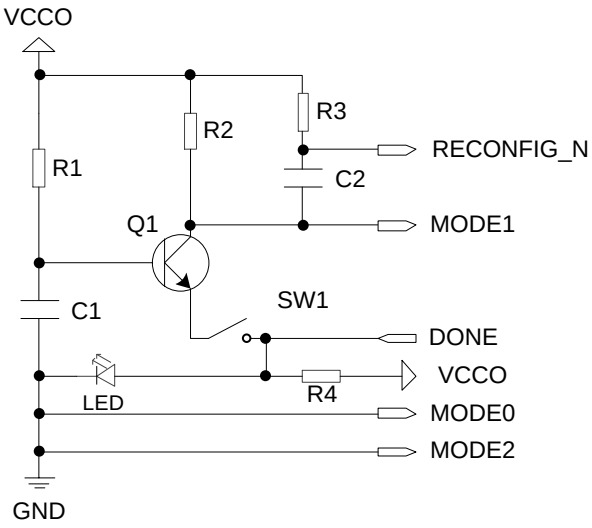
Technical Protocol

Operations

1. External flash download: The initial MODE1 is a high level, and the MODE[2:0] value sampled by the READY signal is "010"; i.e., MSPI download mode. FPGA will load the program from an external flash to SRAM. If the DONE signal changes from a low level to a high level, this indicates that the program has been successfully loaded from the external flash.
2. Internal flash download: If the R1 and C1 circuits meet the condition of triode conduction but the external flash is still not loaded successfully, the DONE signal will remain low. MODE1 will also change from a high level to a low level. Concurrently, RECONFIG_N will produce a low pulse to trigger FPGA and load the program from the internal flash. The MODE[2:0] value sampled by the READY signal is "000"; i.e., the AUTOBOOT download mode. If the DONE signal changes from a low level to a high level, the program has successfully loaded from the external flash.

Circuit Diagram

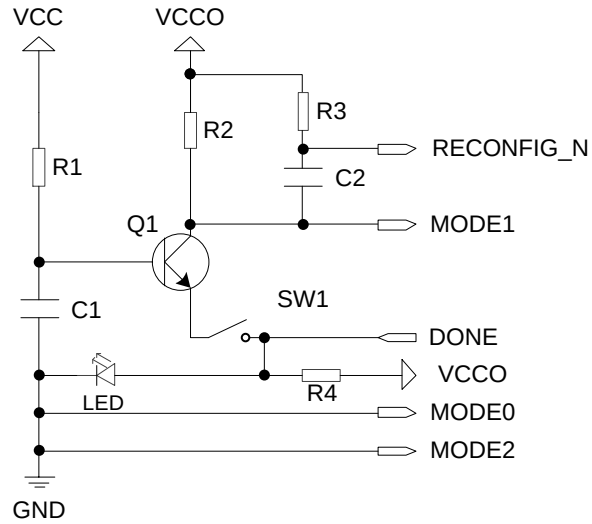
Figure 1: DUALBOOT Circuit Diagram 1



Notes:

- This circuit diagram applies if VCC powers up after VCCO.
- R1=100 KΩ; R2=10 KΩ; R3=20 KΩ; R4=4.7 KΩ; C1=10 μF; C2=4.7 μF; Q1=BC847A-235; VCCO=3.3 V; Download Speed=25 MHz.
- SW1 switch: SW1 must be disconnected when an internal flash is downloading; SW1 must be connected when the DUALBOOT function is running.

Figure 2: DUALBOOT Circuit Diagram 2



Notes:

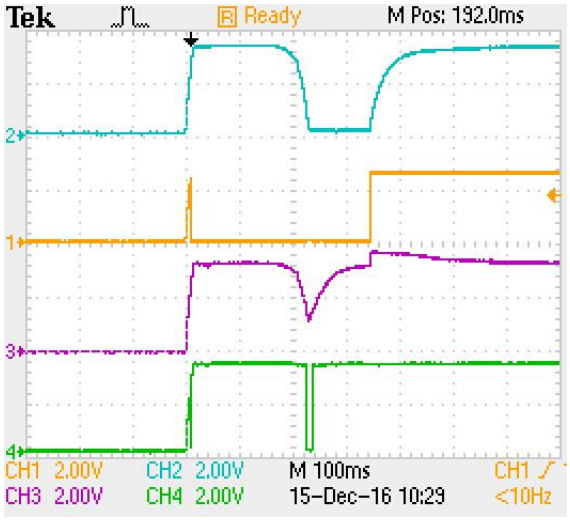
- This circuit diagram applies if VCC powers up after VCCO.
- R1=100 KΩ; R2=100 KΩ; R3=100 KΩ; R4=4.7 KΩ; C1=2.2 μF; C2=4.7 μF; Q1=BC847A-235; VCCO=3.3 V, VCC=1.2 V; Download Speed=25 MHz.
- SW1 switch: SW1 must be disconnected when an internal Flash is downloading; SW1 must be connected when the DUALBOOT function is running.

Board Level Validation

DUALBOOT function verification was carried out based on the DK-ENTRY-GW1N4 development board. The validation steps are as follows:

1. Connect a USB cable to the PC from a development board and open the Programmer.
2. Disconnect SW1. Download the bitstream file for the internal flash after powering up.
3. After downloading successfully, connect SW1 and restart the development board power supply. Observe the DUALBOOT method that loads from the internal flash.
4. After loading from the internal flash successfully, load and verify the external flash DUALBOOT.
5. Disconnect SW1, download the bitstream file for the external flash using the Programmer (exFlash Program in bscan) after powering up.
6. After downloading successfully, connect SW1 and restart the power supply of the development board. Observe the DUALBOOT method that loads from the external Flash.
7. Finish verifying if the load is successful from both the internal flash and the external flash using the DUALBOOT method.

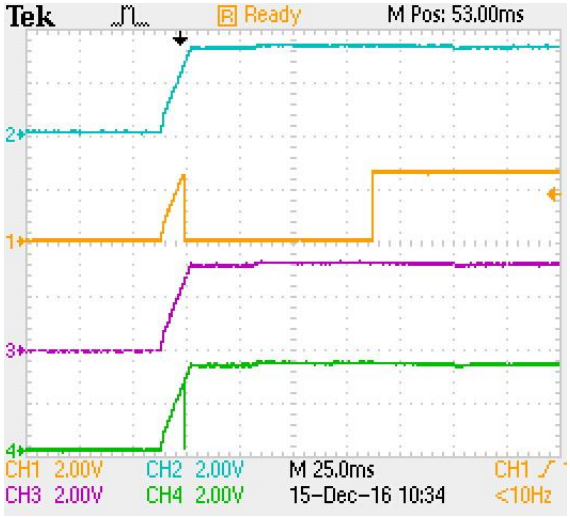
Figure 3: FPGA Successfully Loads From Internal Flash After Powering On



Notes:

- Channel 1 is DONE signal.
- Channel 2 is MODE1 signal.
- Channel 3 is RECONFIG_N signal.
- Channel 4 is READY signal.
- MSPI download clock rate is 25 MHz.

Figure 4: FPGA Successfully Loads From External Flash After Powering On



Notes:

- Channel 1 is DONE signal.
- Channel 2 is MODE1 signal.
- Channel 3 is RECONFIG_N signal.
- Channel 4 is READY signal.
- MSPI download clock rate is 25 MHz.

Notes

1. The R and C values in the DUALBOOT circuit can be adjusted according to the MSPI download speed and specific hardware platform.
2. A power supply of about 10 msIt is recommended.
3. The READY tube increates 4.7 K resistance to VCCO.

Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

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Revision History

Date	Version	Description
12/16/2016	1.0E	Initial version published.

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