Gowin Software Quick Start Guide

SUG918-1.1E,2020-09-07

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Revision History

Date	Version	Description
05/07/2020	1.0E	Initial version published.
09/07/2020	1.1E	● RTL schematic added; ● File encryption added; ● Tcl command added.

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1 About This Guide

1.1 Purpose

This manual uses MIPI as an example to introduce Gowin Software and aims to help users get familiar with the usage and improve the design efficiency.

1.2 Related Documents

You can find the related documents at www.gowinsemi.com:

- SUG100, Gowin Software User Guide
- SUG935, Gowin Design Physical Constraints User Guide
- SUG101, Gowin Design Timing Constraints User Guide
- SUG114, Gowin Analyzer Oscilloscope User Guide
- SUG282, Gowin Power Analyzer User Guide
- SUG502, Gowin Programmer User Guide.

1.3 Terminology and Abbreviations

Table 1-1 shows the abbreviations and terminology used in this manual.

Table 1-1 Terminology and Abbreviations

Terminology and Abbreviations	Meaning
PnR	Place & Route
GAO	Gowin Analyzer Oscilloscope
GPA	Power analyzer

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly by the following ways.

Website: www.gowinsemi.com

E-mail： support@gowinsemi.com

2 Introduction

2.1 Design Flow

Gowin software is available in Windows and Linux. It supports GUI running mode and commands running mode. Take the GUI running mode in Windows 10 and MIPI design as an instance to introduce quick start of Gowin software.

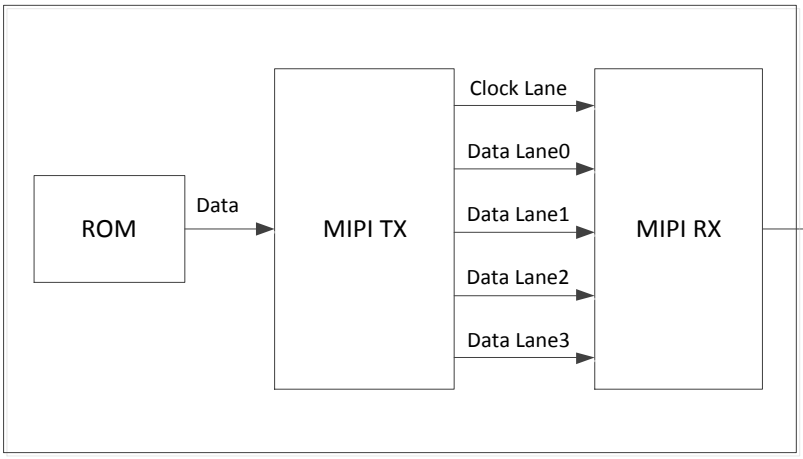
The design uses Synplify Pro to synthesize, FloorPlanner to add physical constraints, Timing Constraints Editor to add timing constraints, GAO to add GAO config file and to capture data, GPA to add GPA config file and Programmer to download bitstream.

2.2 Design Diagram

Gowin MIPI D-PHY TX RX IP applies to the serial display interface and serial camera interface for receiving or transmitting the image or video data. MIPI D-PHY provides its physical definition.

The design integrates MIPI RX IP and MIPI TX IP. ROM provides data for MIPI TX. MIPI TX transmits data and MIPI RX receives data. GAO captures the data received by MIPI RX to verify MIPI RX and MIPI TX. The design diagram is as shown in Figure 2-1 .

Figure 2-1 MIPI Design Diagram



3 Quick Start

3.1 Create a New Project

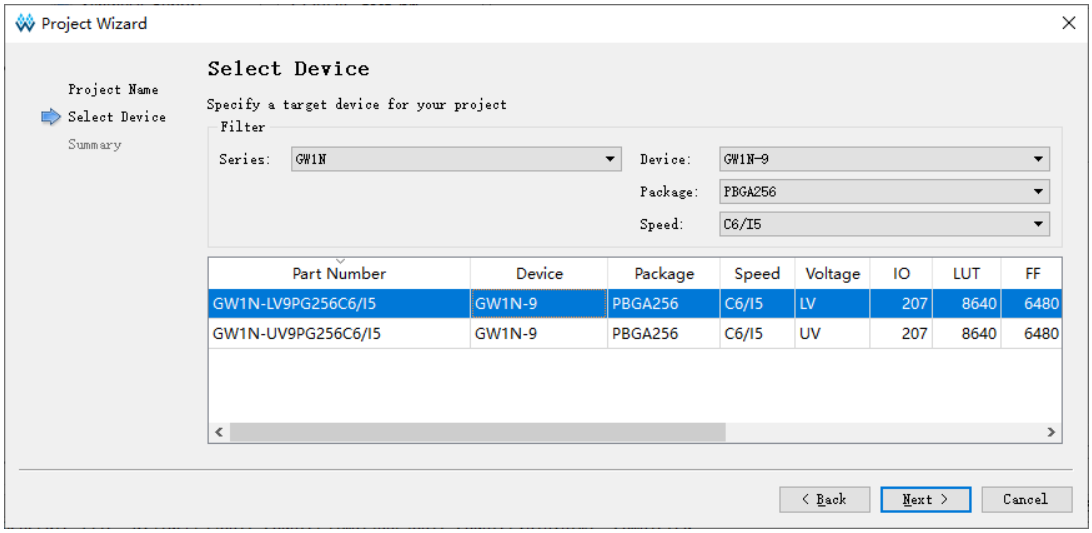
3.1.1 Create a New Project

Open Gowin software and click "Start Page > Quick Start > New Project" to create a new project named as MIPI_RX_TX. The device selection is as shown in Figure 3-1.

- Series: GW1N
- Device: GW1N-9
- Package: PBGA256
- Speed: C6/I5
- Part Number: GW1N-LV9PG256C6/I5

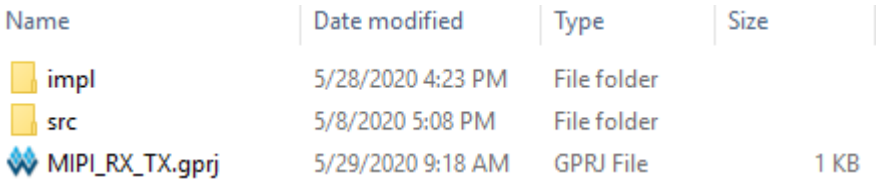
Click "Next" until the project creation completed. For the details, please refer to SUG100, Gowin Software User Guide.

Figure 3-1 Create a New Project



After the project is created, the impl and src folders are generated under the project creation path, as shown in Figure 3-2. impl contains synthesis and PnR files and src contains the source files.

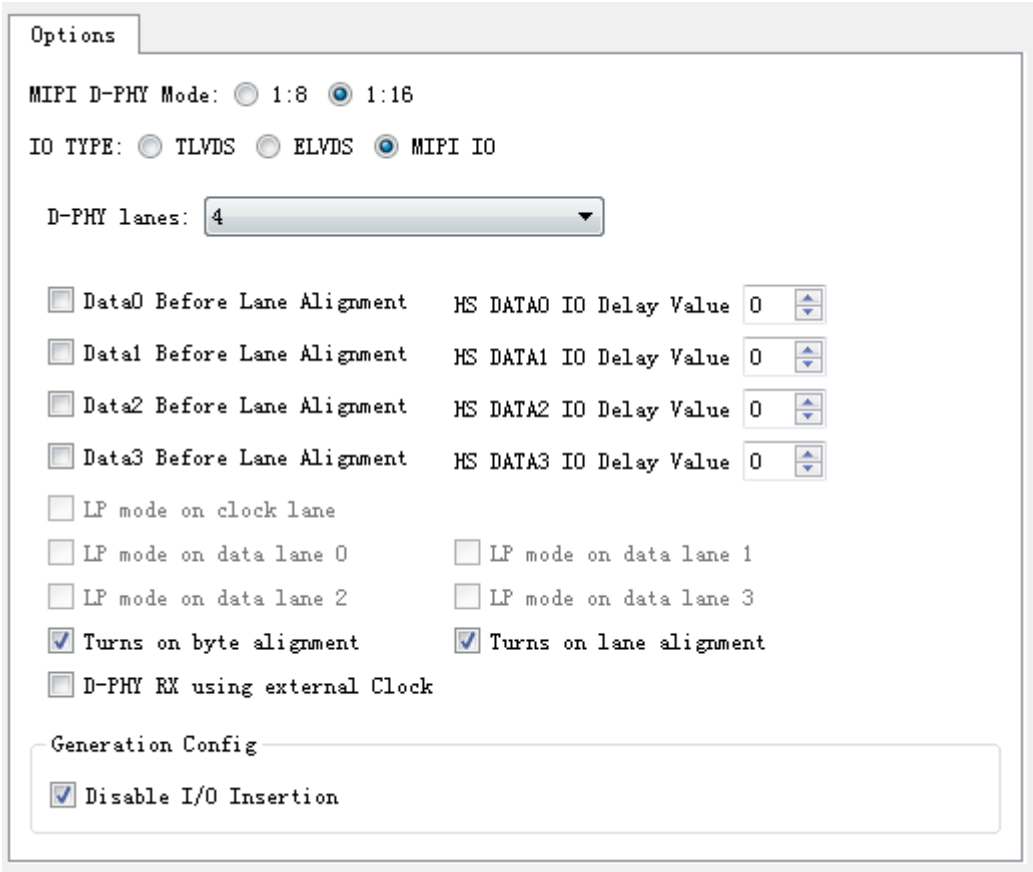
Figure 3-2 Project Directory



3.1.2 Generate MIPI D-PHY IP

Click "Tools > IP Core Generator" to open the IP Core Generator interface. Double-clicking on "Interface and Interconnect > MIPI RX" to open the IP Customization interface to configure as required. The MIPI RX configuration in this design is shown in Figure 3-3. Then click "OK" to generate MIPI RX IP.

Figure 3-3 MIPI RX Configuration



After generation, IP design files and simulation files are generated under IP creation path, as shown in Figure 3-4.

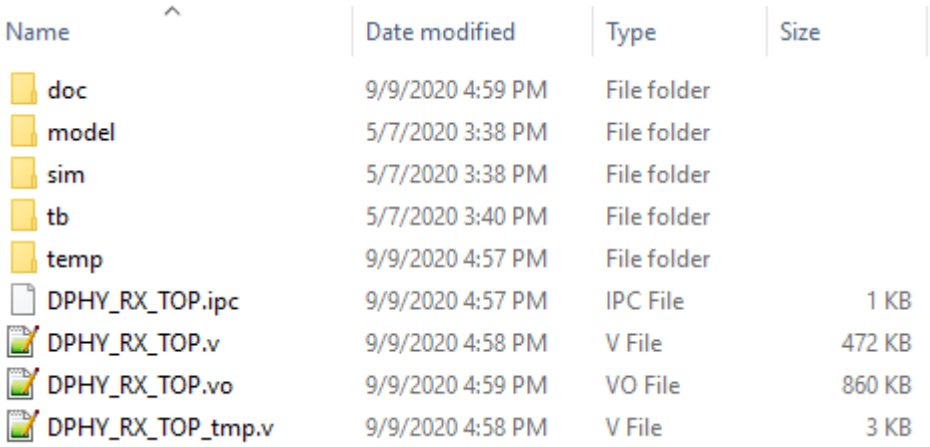
- .v file is IP design file, encrypted;
- _tmp.v is IP design template file;
- .vo file is IP simulation model file, unencrypted;
- .ipc file is IP configuration file. The user can load the file to modify the configuration.
- temp contains the files required to generate the IP.

- The doc, model, sim, and tb contain the simulation files: readme text, simulation model, simulation script, and testbench.

Note!

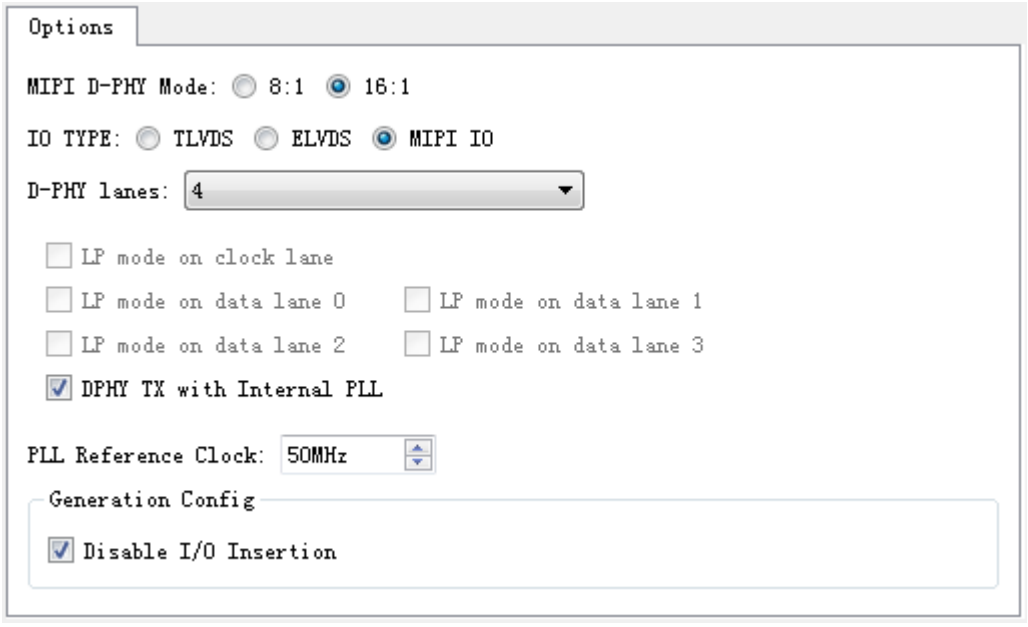
At present, Gowin software has not provided simulation files for some IPs. IP directory is subject to IP Core Generator in use.

Figure 3-4 MIPI RX IP Directory



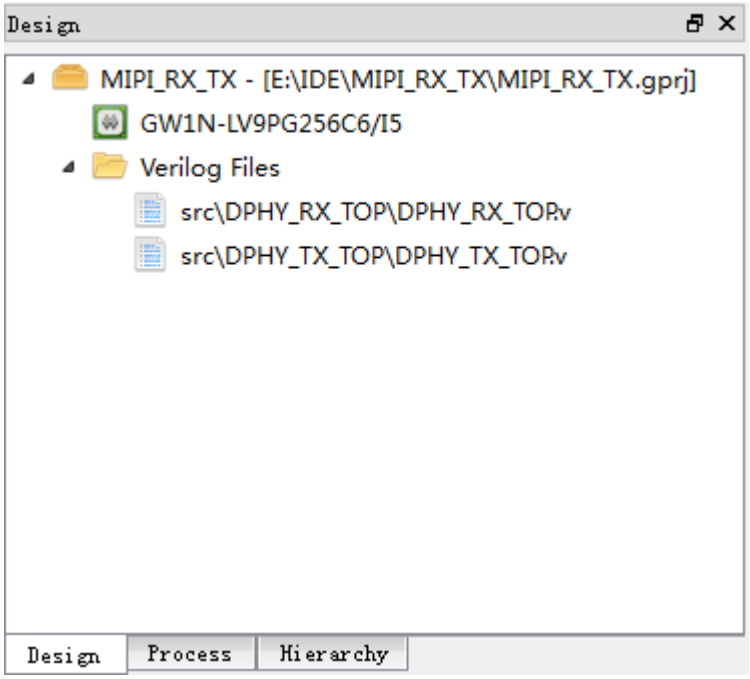
Double-click MIPI TX to open the IP Customization interface to configure as required. The MIPI TX configuration in this design is shown in Figure 3-5. Then click "OK" to generate MIPI TX IP.

Figure 3-5 MIPI TX Configuration



After MIPI RX and MIPI TX IPs generated, the Design window is as shown in Figure 3-6.

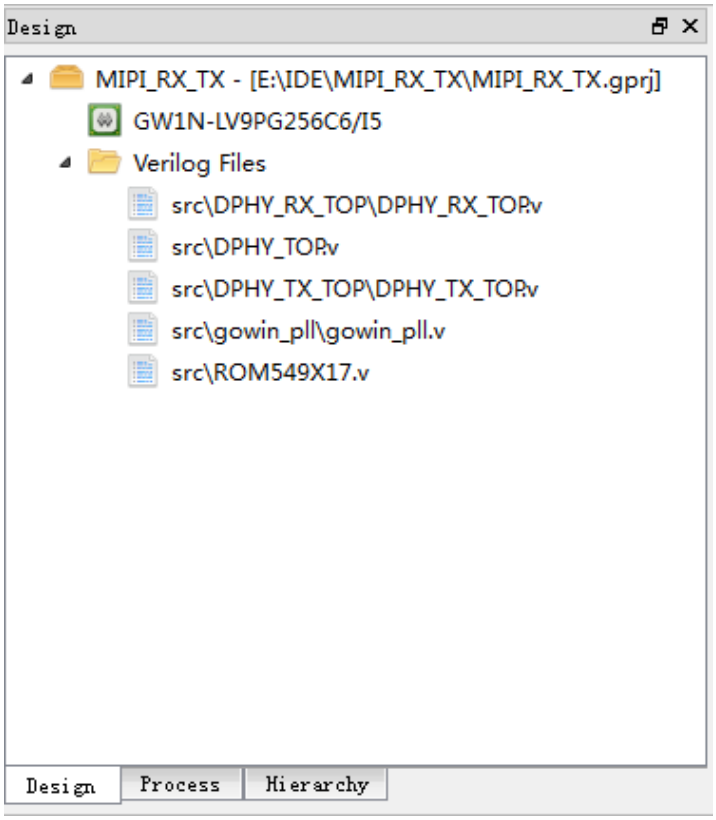
Figure 3-6 Design Window



3.1.3 Load File

In order to test MIPI RX and MIPI TX, it needs to create or load some design files, as shown in Figure 3-7.

Figure 3-7 Load Files



3.1.4 RTL Schematic

After the source file is loaded, you can view the design schematic by

clicking "Tools > Schemetic Viewer" to help you better understand the logic. For details, see SUG100, Gowin Software User Guide.

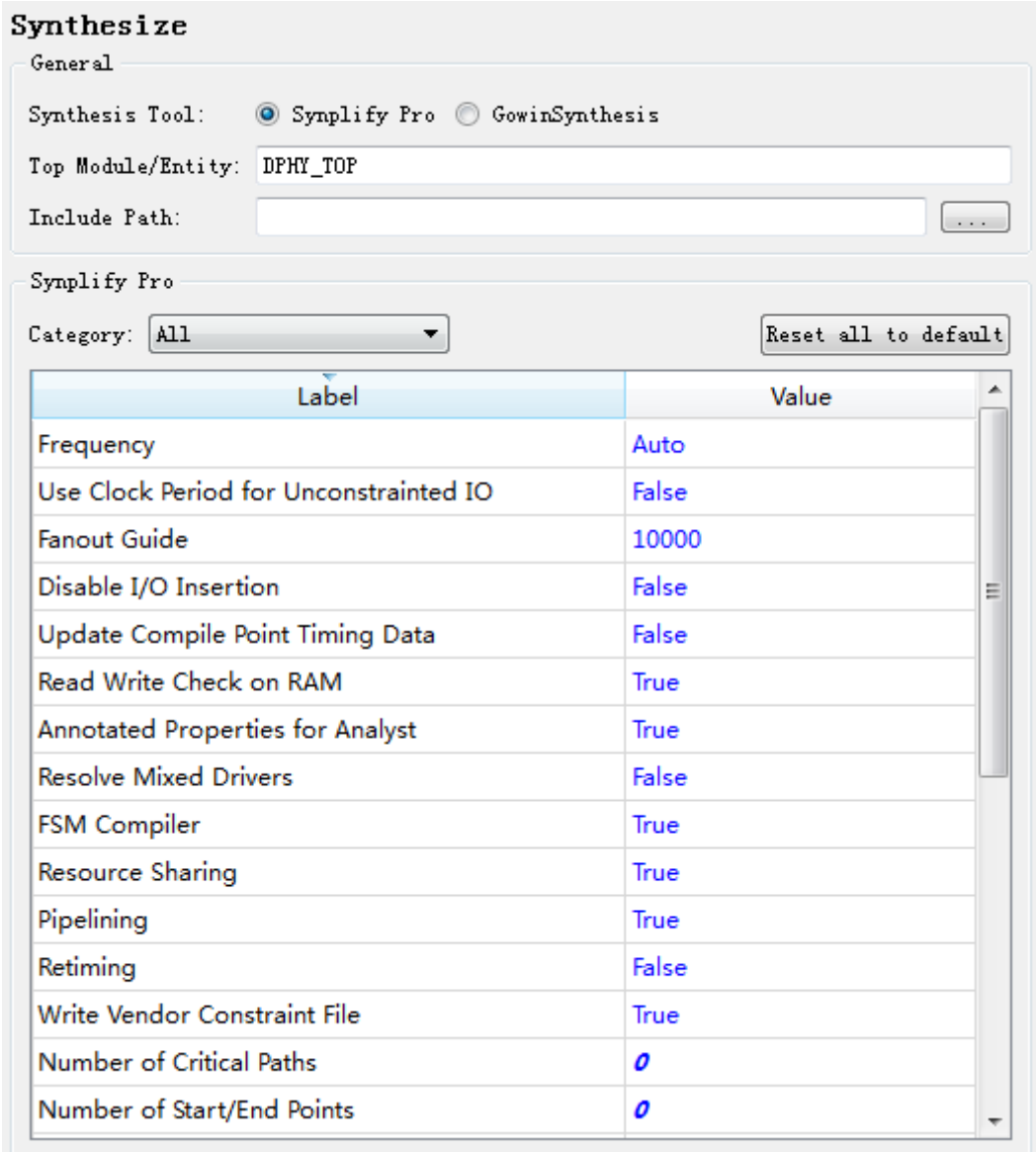
3.2 Synplify Pro for Synthesis

3.2.1 Parameter Configuration

Select "Process > Synthesize > Configuration" to open Configurations to configure parameters. For further details about the configuration, refer to the SynplifyPro documents under the Gowin installation directory: installPath\SynplifyPro\doc.

This design uses Synplify Pro to synthesize. Top module/entity is DPHY_TOP. Number of Critical Paths and Number of Start/End Points are both set to 0, as shown in Figure 3-8.

Figure 3-8 Synthesis Parameters Configuration



In addition, you can add some attributes and instructions to the source file to control synthesis. For the details, see the SynplifyPro documents

under the Gowin software installation directory and the path is installPath\SynplifyPro\doc. As shown in Figure 3-9, in this design, a specific net is retained without optimization during the synthesis by using the/* synthesis syn_keep=1 */ attribute

Figure 3-9 Attributes and Instructions of Synplify Pro

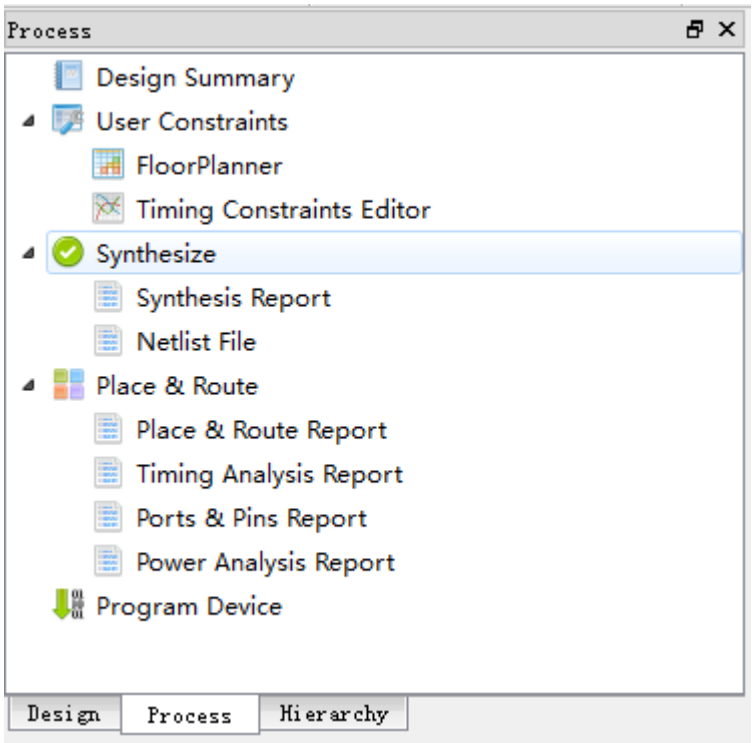
```
417  `ifdef GEN_MIPI_RX_16
418     reg  [63:0] data_in;
419     reg  [15:0]  data0, data1, data2, data3;
420     reg  [15:0] dout, dout1;
421     reg  [15:0] data_cntr;
422     reg  hactive_flag_RX;
423
424     wire [1:0] lp_clk_out,lp_data0_out;
425     wire [1:0] lp_data1_out,lp_data2_out,lp_data3_out;
426
427     wire [15:0] data_out3, data_out2, data_out1, data_out0;
428     wire  D0_delay,D1_delay,D2_delay,D3_delay;
429     reg  [63:0] data_out_reg;
430     wire clk_byte_out/* synthesis syn_keep=1 */;
431     wire sclk_tx ;
432  `endif
```

3.2.2 Synthesize

After parameters configuration, it can synthesize.

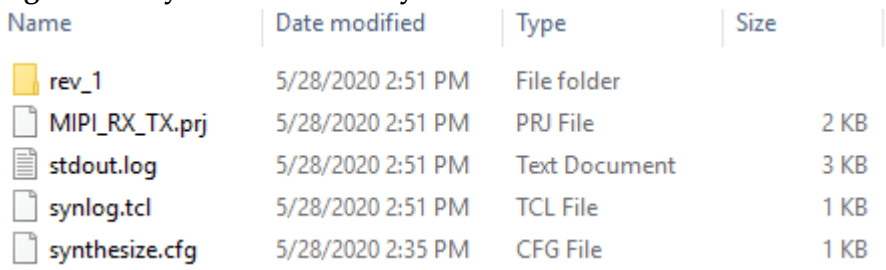
Double-click "Synthesize" in Process window to synthesize as shown in Figure 3-10. When the icon changes to " ", you can double-click Synthesis Report to view the report and double-click Netlist File to view the netlist file.

Figure 3-10 Synthesize Completed



After synthesis, synthesize folder is generated under \impl path. The folder contains all the files and folders generated in synthesis, as shown in Figure 3-11. The netlist file and report are placed in the rev_1 folder.

Figure 3-11 Synthesize Directory



Note!

If you use GowinSynthesis to synthesize, gwsynthesis folder is generated under \impl path. This folder contains all the files generated in synthesis.

3.3 Physical Constraints

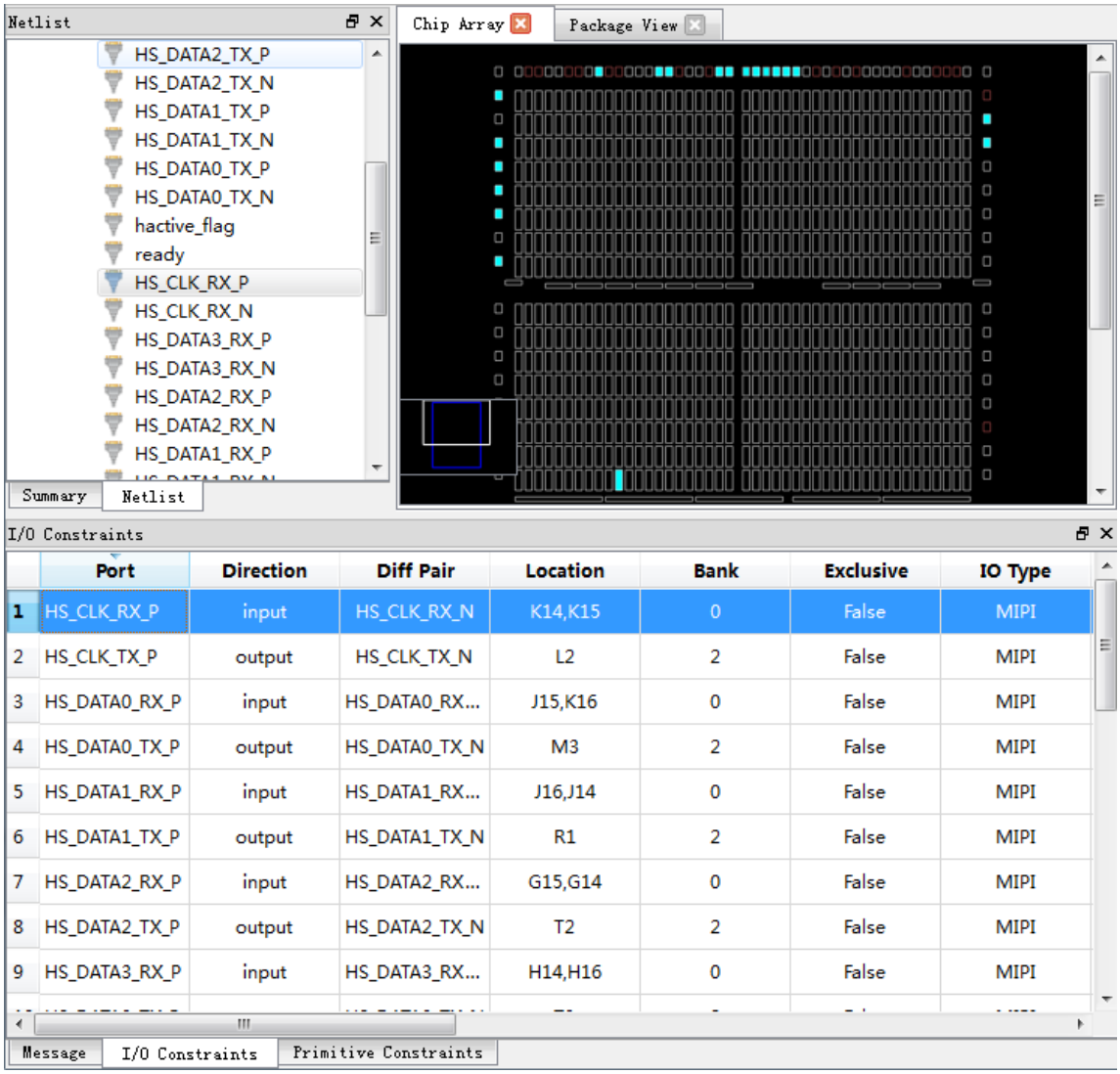
After synthesis, you can use FloorPlanner or write manually to add physical constraints. In this design, FloorPlanner is selected. For more details, please refer to the SUG935, Gowin Design Physical Constraints User Guide

3.3.1 Create New Physical Constraints

Click "Process > User Constraints > FloorPlanner" to open FloorPlanner, which supports I/O, Primitive, Group physical constraints. This design only adds I/O constraints and uses it as an instance.

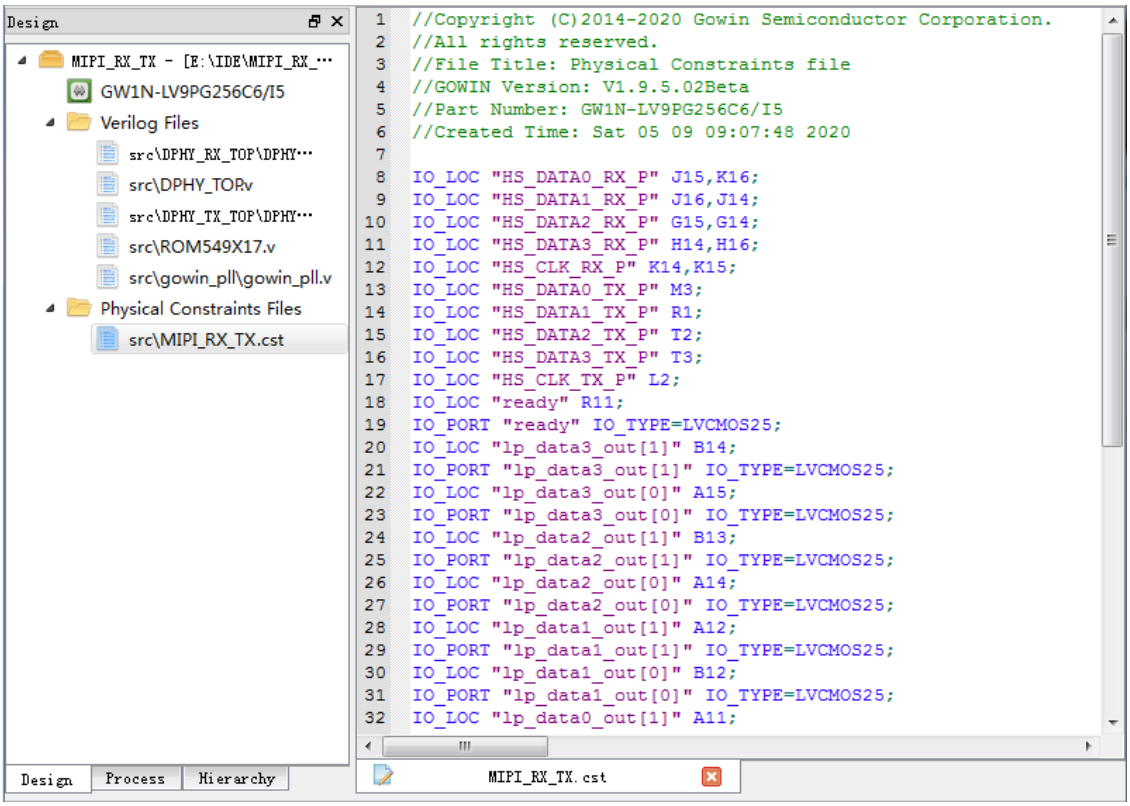
You can create I/O constraints in I/O Constraints window. Drag the port row to be constrained in the Netlist or I/O Constraints window to a specific location in the Package View or Chip Array view. After finished, the port location displays in the IOB, as shown in Figure 3-12.

Figure 3-12 I/O Constraints



After constraints finished, click "Save" to generate physical constraints files as shown in Figure 3-13.

Figure 3-13 Physical Constraints Display



In PnR, if there is no physical constraints file, the PnR will be automatically generated. If there is a physical constraint file, the PnR will be generated according to the physical constraints file.

3.3.2 Modify Physical Constraints

After physical constraints files generated, you can modify the constraints by FloorPlanner. Click "Save"to finish.

3.4 Timing Constraint

After synthesis, you can use Timing Constraints Editor or write manually to add timing constraints. In this design, Timing Constraints Editor is selected. For more details, please refer to SUG101, Gowin Design Timing Constraints Guide.

3.4.1 Create New Timing Constraints

Click "Process > User Constraints > Timing Constrains Editor" to open Timing Constrains Editor, which supports clock, I/O and timing report constraints. This design adds clock and timing report constraints and uses them as instances.

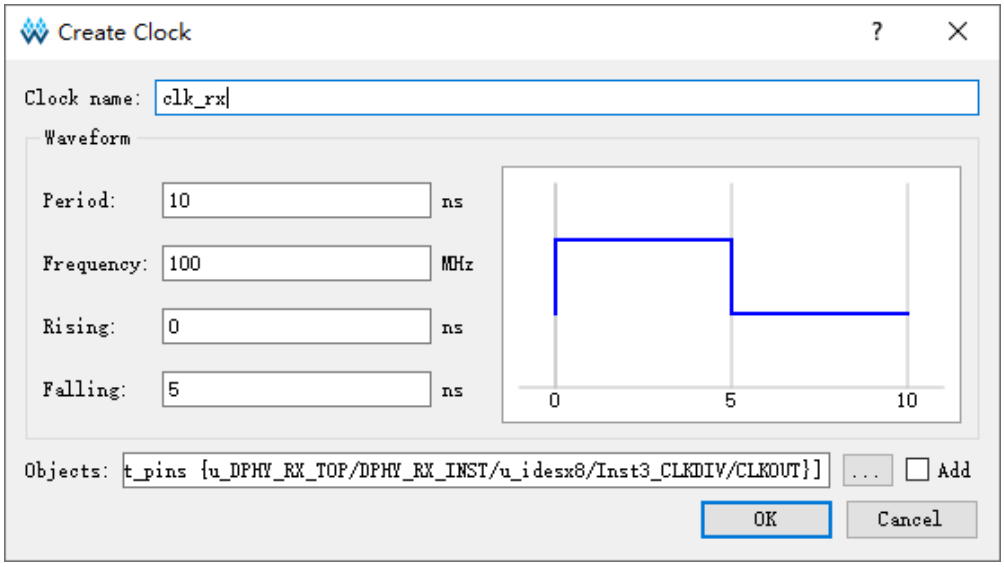
Clock Constraints

Select "Timing Constraints > Clocks" and right-click to select "Create Clock" as shown in Figure 3-14. The constraints are as follows:

- Clock name：clk_rx

- Period：10
- Rising：0
- Falling：5
- Source Object：get_pins {u_DPHY_RX_TOP/DPHY_RX_INST/u_idesx8/Inst3_CLKDIV/CLKOUT}

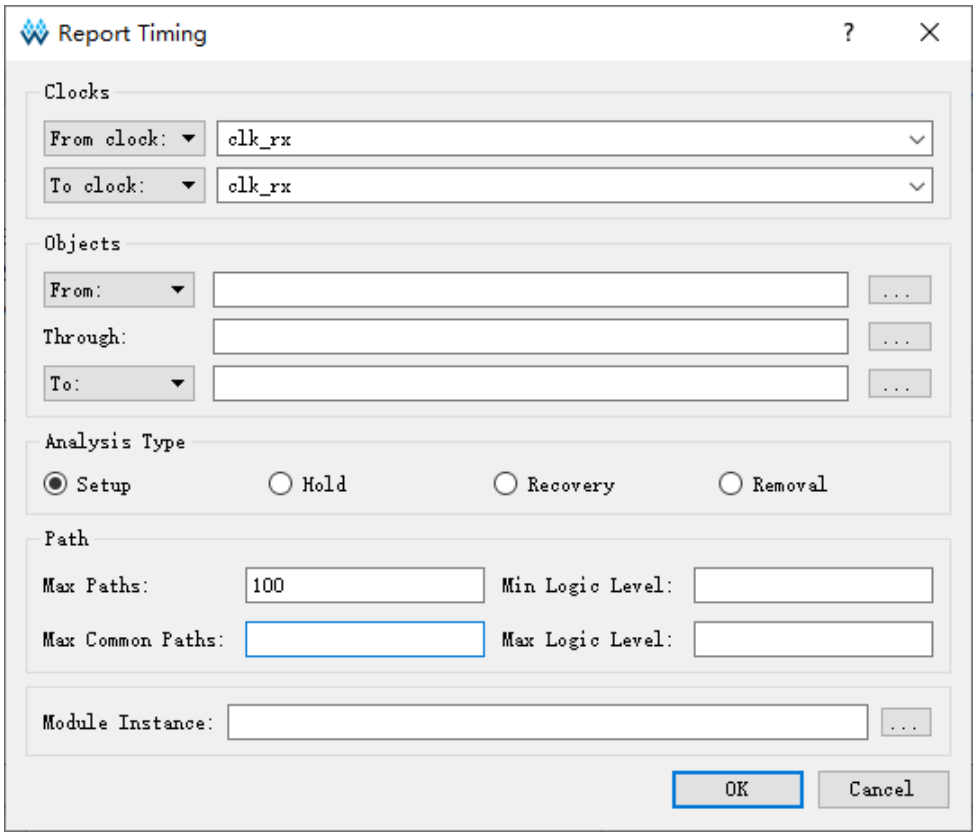
Figure 3-14 Clock Constraints



Timing Report Constraint

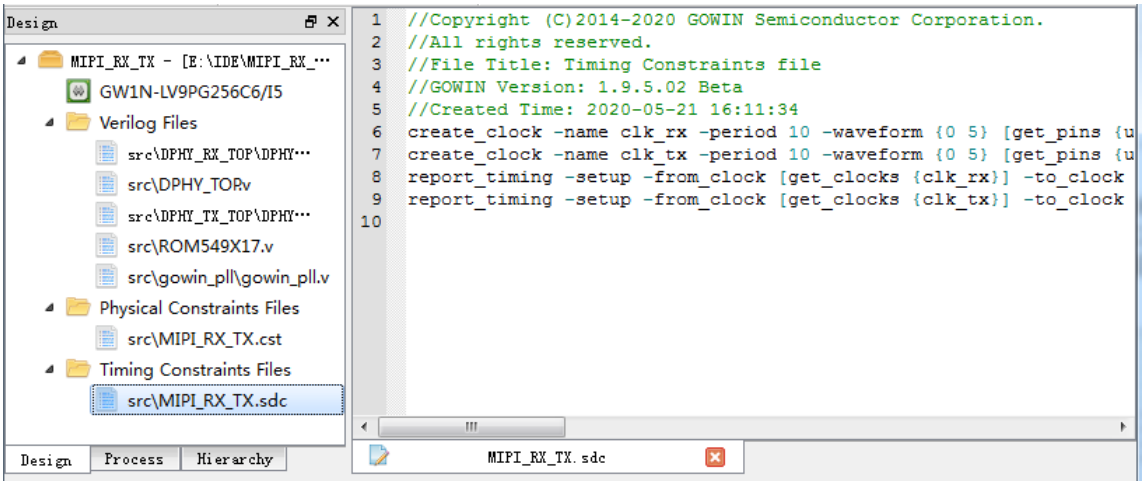
Select "Timing Constraints > Report > Report Timing" and right-click to select "Create Report". You can configure parameters in Report Timing dialog box. The setup max. path is 100 as shown in Figure 3-15.

Figure 3-15 Timing Report Constraints



After constraints finished, click "Save" to generate timing constraints as shown in Figure 3-16.

Figure 3-16 Timing Constraints Display



In PnR, if there is no timing constraints file, the PnR will be automatically generated. If there is a timing constraint file, the PnR will be generated according to the timing constraints file.

3.4.2 Modify Timing Constraints

After timing constraints files generated, you can modify the constraints by Timing Constrains Editor. Click "Save" to finish.

3.5 GAO Configuration

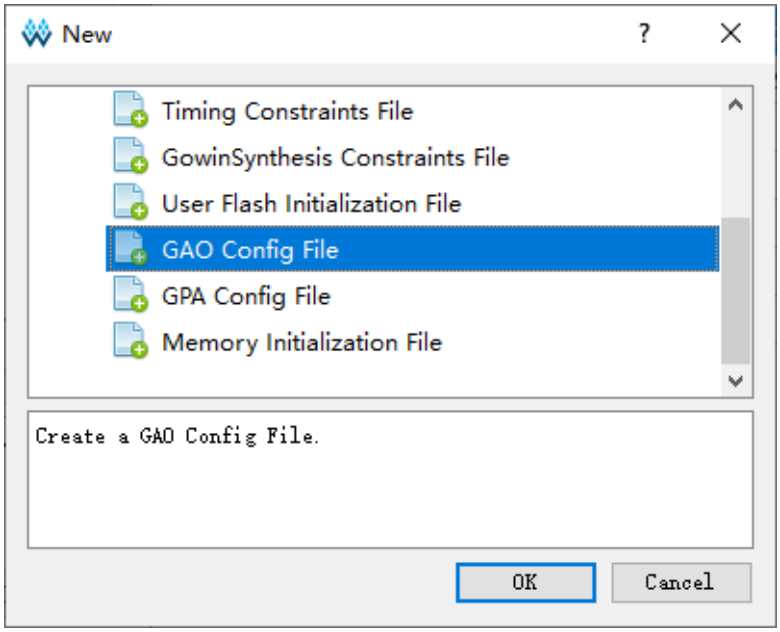
After synthesis, you can create GAO config file to capture data and verify the design. Gowin software provides Standard Mode GAO and Lite Mode GAO. For the usage, see SUG114, Gowin Analyzer Oscilloscope User Guide.

This design uses Standard Mode GAO and takes it as an instance.

3.5.1 Create Standard Mode GAO Config File

Select "Design > Design > New File…" to open "New" dialog box, and select "GAO Config File" in "New" as shown in Figure 3-17. Click "OK". Select For Post-Synthesis Netlist in Type, Standard in Mode. Click "Next". The file name is MIPI_RX_TX. Then click "Next" until finished.

Figure 3-17 Create GAO Config File



3.5.2 Configure Standard Mode GAO

After file created, you can configure AO, trigger options and capture options. The trigger options include match unit, trigger port, match type and expressions; The capture options include sample clock, capture, capture utilization and capture signals. In this design the AO is 1 and the trigger options and capture options configuration are shown in Figure 3-18 and Figure 3-19.

Figure 3-18 Trigger Options Configuration

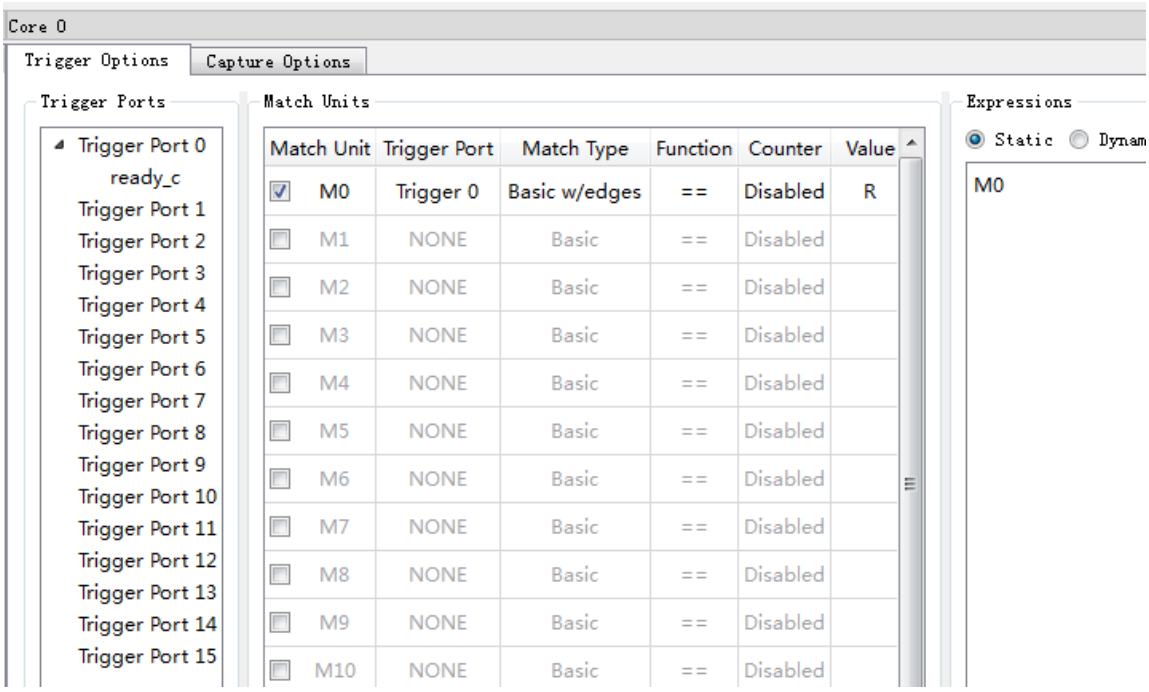
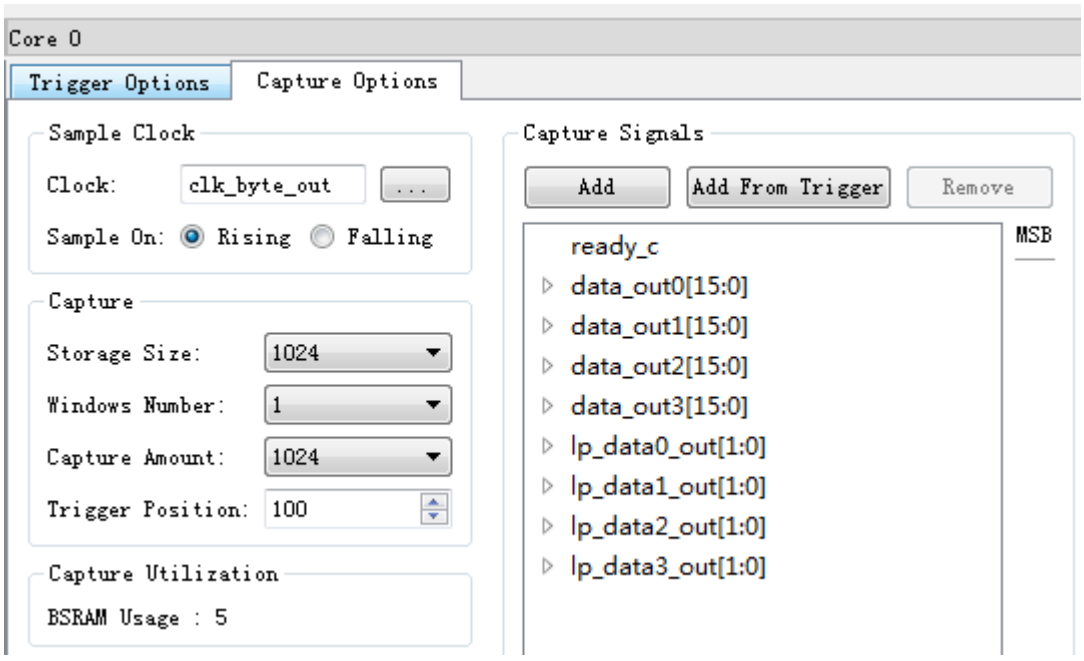
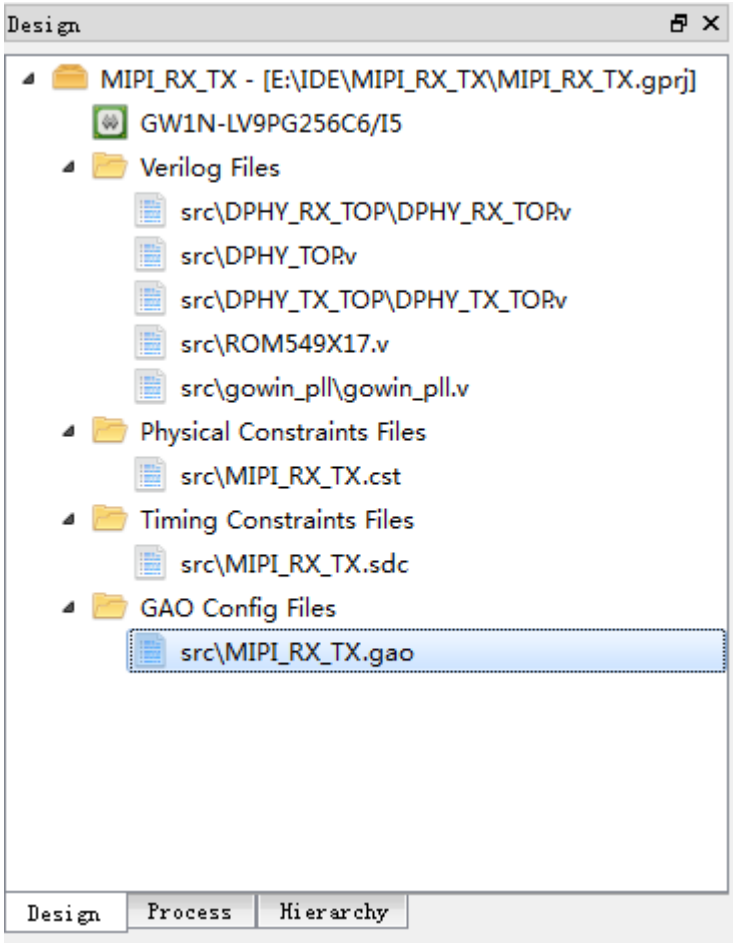


Figure 3-19 Capture Options Configuration



After configuration, click "Save" to finish and the design window is as shown in Figure 3-20.

Figure 3-20 GAO Config File Display



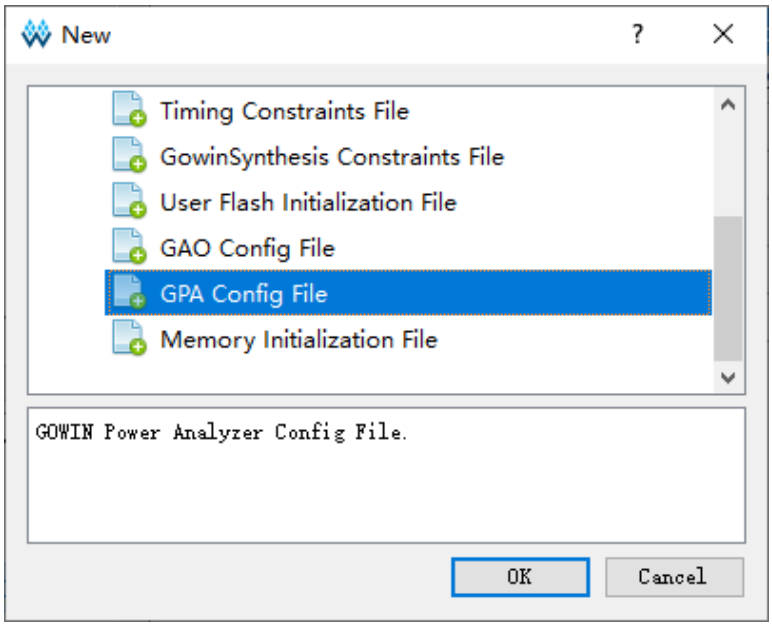
3.6 GPA Configuration

After synthesis, you can create GPA config file to analyze power. For the usage, please refer to SUG282 Gowin Power Analyzer User Guide.

3.6.1 Create GPA Config File

Select "Design > Design > New File…" to open "New" dialog box, and select "GPA Config File" in "New" as shown in Figure 3-21. Click "OK". The file name is MIPI_RX_TX, and the file is under src by default. Then click "OK" to finish.

Figure 3-21 Create GPA Config File



3.6.2 Configure GPA

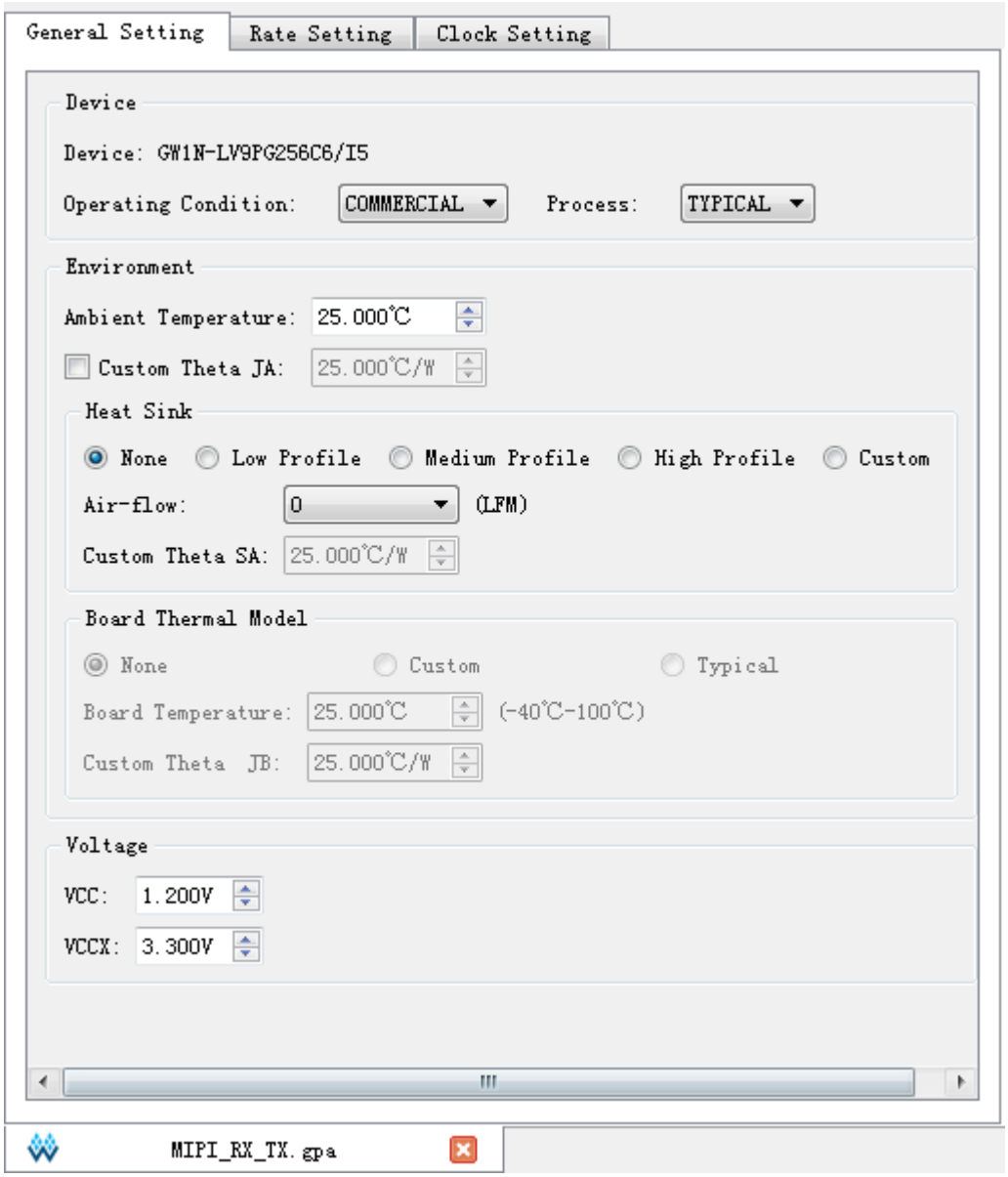
After GPA config file created, configure General Setting, Rate Setting and Clock Setting.

- General Setting includes the parameters of chip, package, speed grade, temperature grade, thermal impedance, and voltage;
- Rate Setting is used to configure signal transition rate. You can set transition rate of IO or Net, or use the default value;
- Clock Setting is used to configure clock and enable features of B-SRAM, I/O and DFF.

General Setting

In this design, the general setting is configured as follows: commercial temperature, 25 ℃ ambient temperature, no heat sink, VCCX 3.3V and VCC 1.2V, as shown in Figure 3-22.

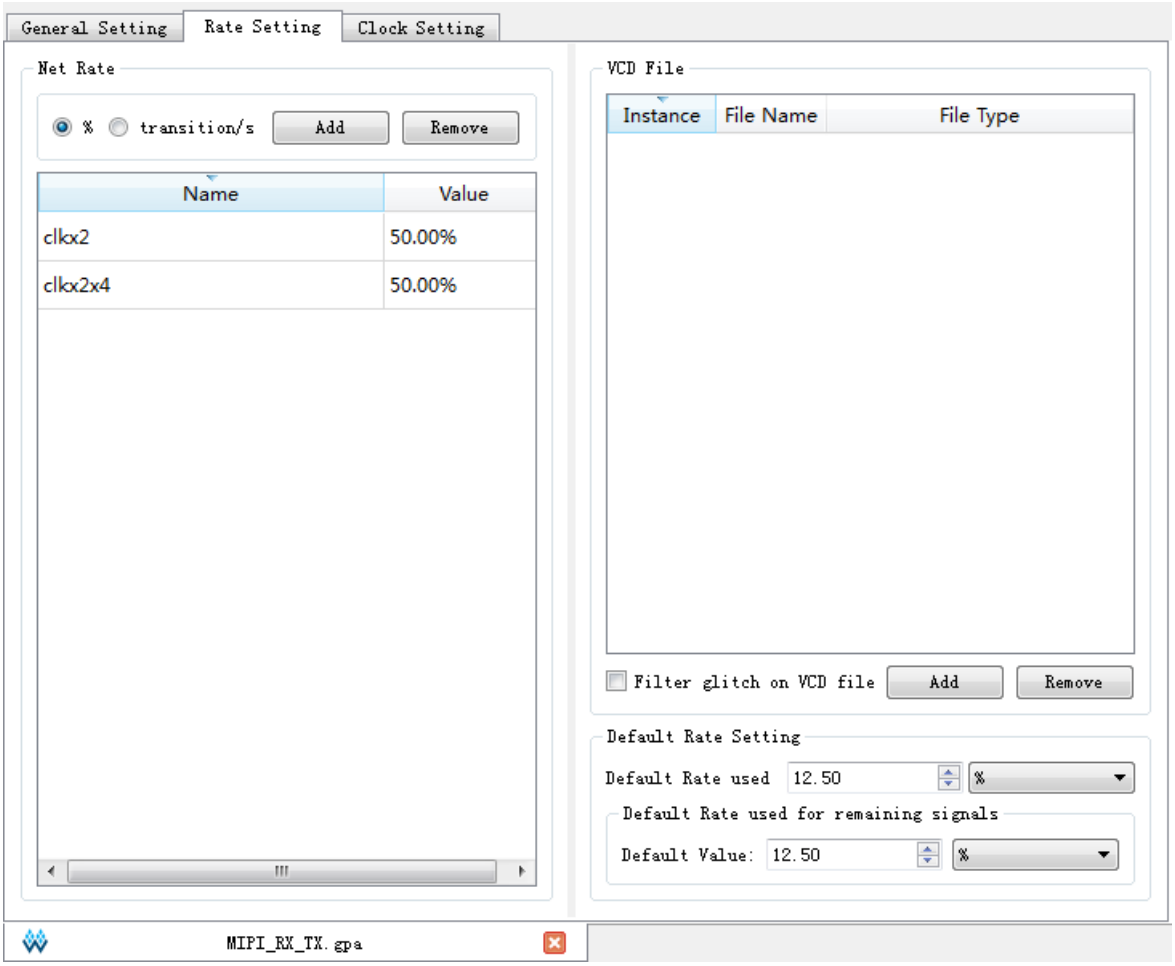
Figure 3-22 General Setting Configuration



Rate Setting

In this design, the transition rate of clkx2 and clkx2x4 is 50% and the remaining signals use the default value, as shown in Figure 3-23.

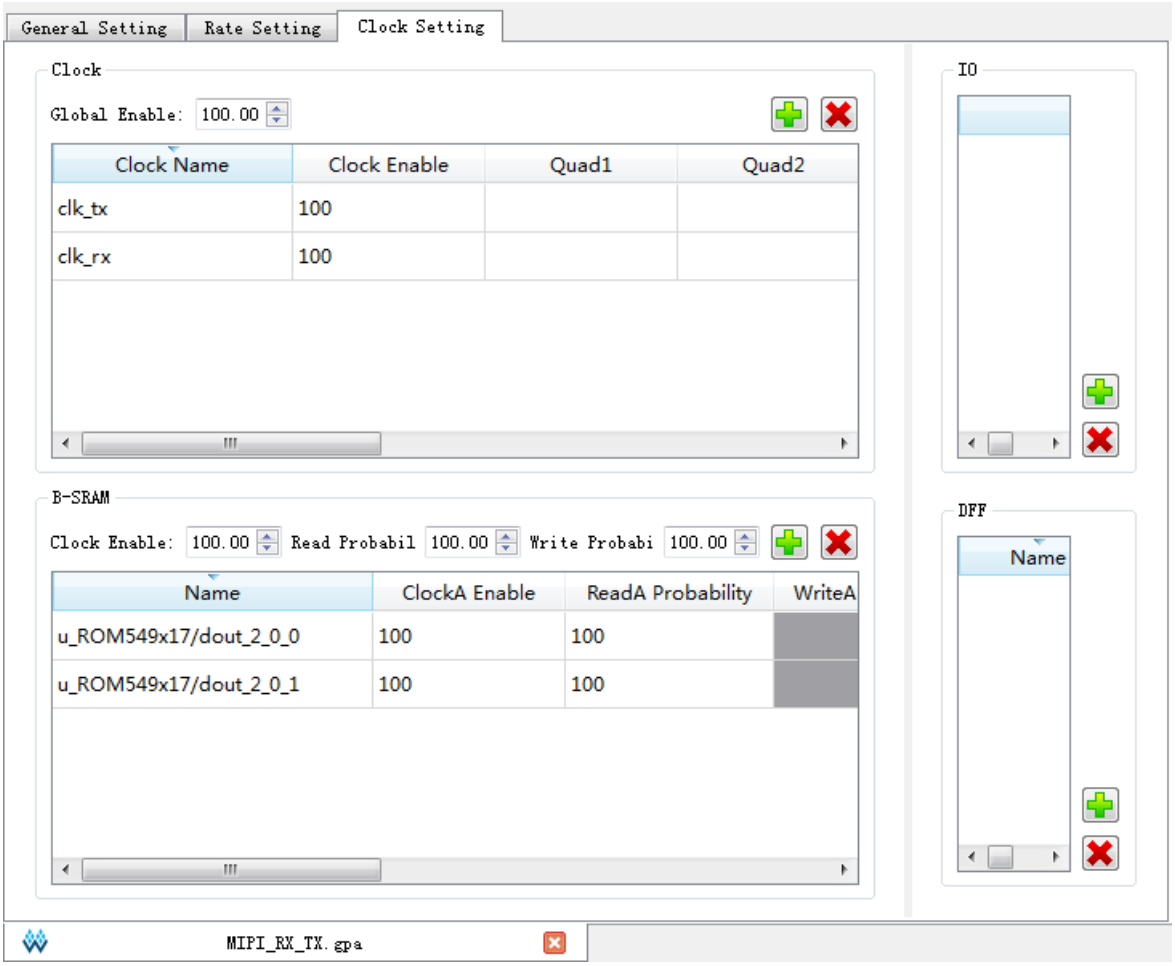
Figure 3-23 Rate Setting Configuration



Clock Setting

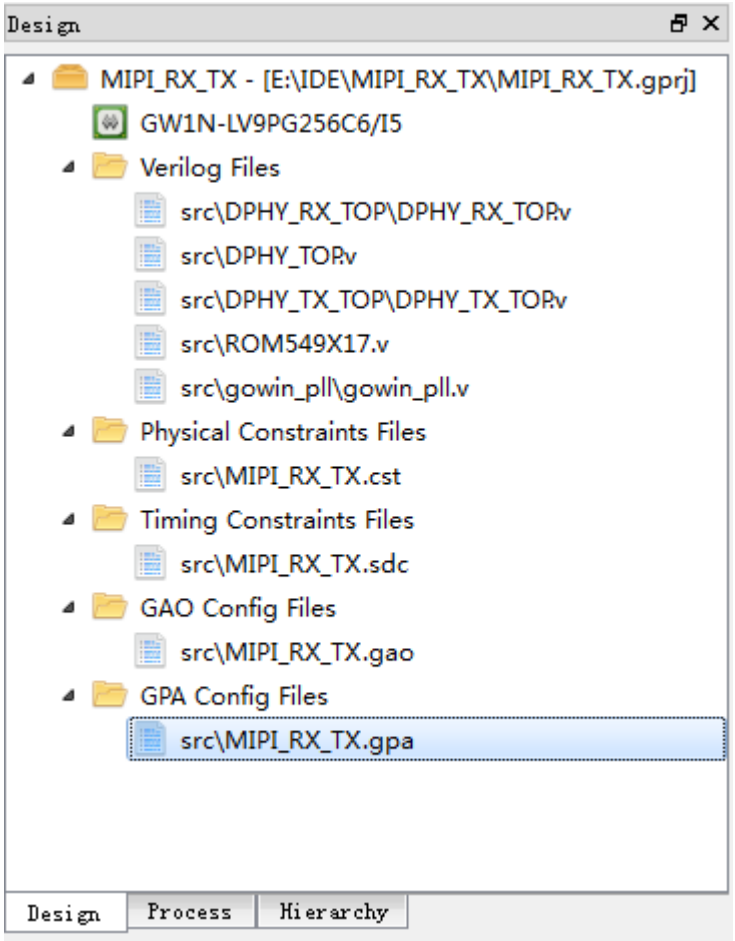
In this design, the clock is created in the timing analysis. The clock enable and read/write enable of pROM used in this design is specified by B-SRAM. The rest are not set, as shown in Figure 3-24.

Figure 3-24 Clock Setting Configuration



After configuration, click "Save" to finish and the design window display is as shown in Figure 3-25.

Figure 3-25 GPA Config File Display



In PnR, if there is no GPA config files, the PnR will be automatically generated. If there is a GPA config file, the PnR will be generated according to the GPA config file.

3.7 Place & Route

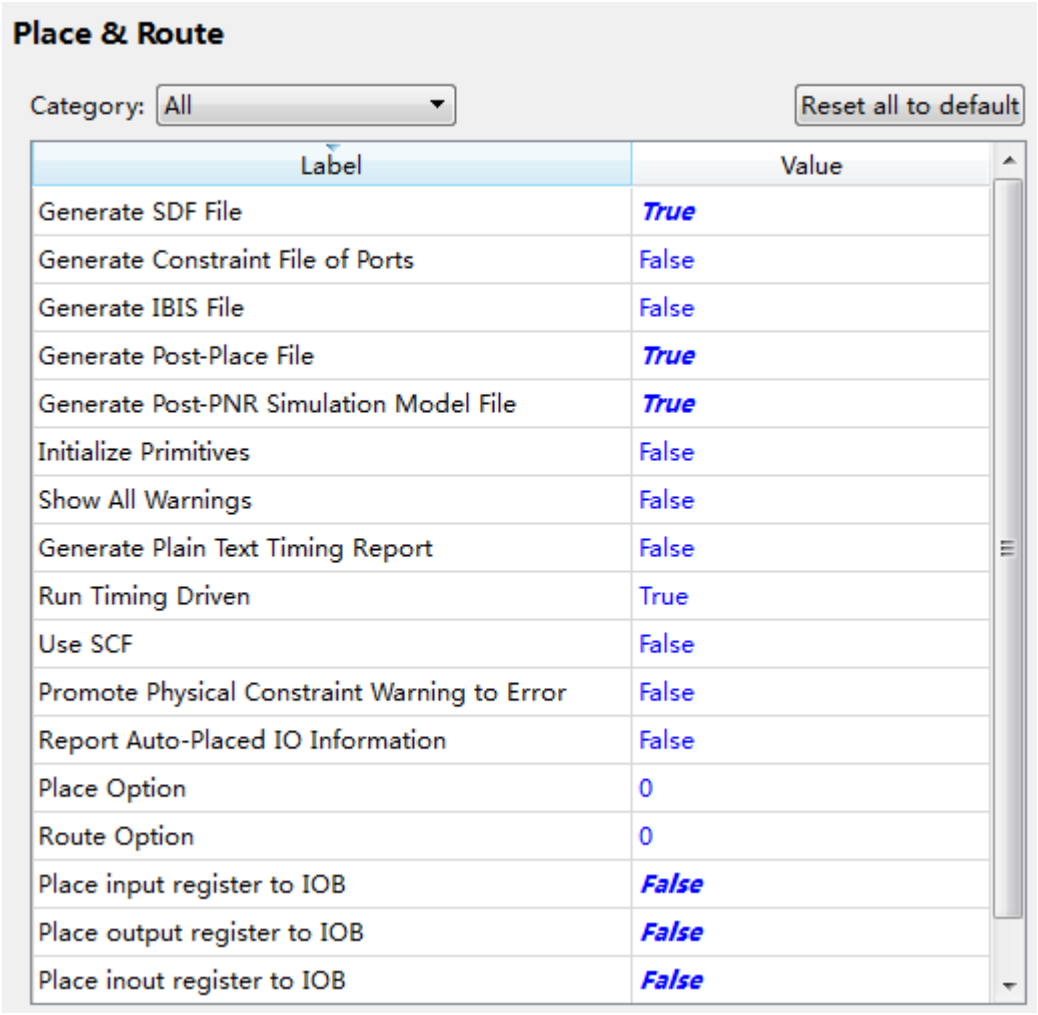
After synthesis and the creation of physical constraints files, timing constraints file, GAO config file, GPA config file as required, you can start PnR.

3.7.1 Parameters Configuration

Select "Process > Place & Route > Configuration" to open Configurations to configure General, Dual-Purpose and Bitstream. For the details, see SUG100, Gowin Software User Guide.

In this design, Generate SDF File, Generate Post-Place File and Generate Post-PNR Simulation Model File are configured to True. Place input register to IOB, Place output register to IOB and Place inout register to IOB are configured to False. The rest use default value, as shown in Figure 3-26.

Figure 3-26 Parameters Configuration

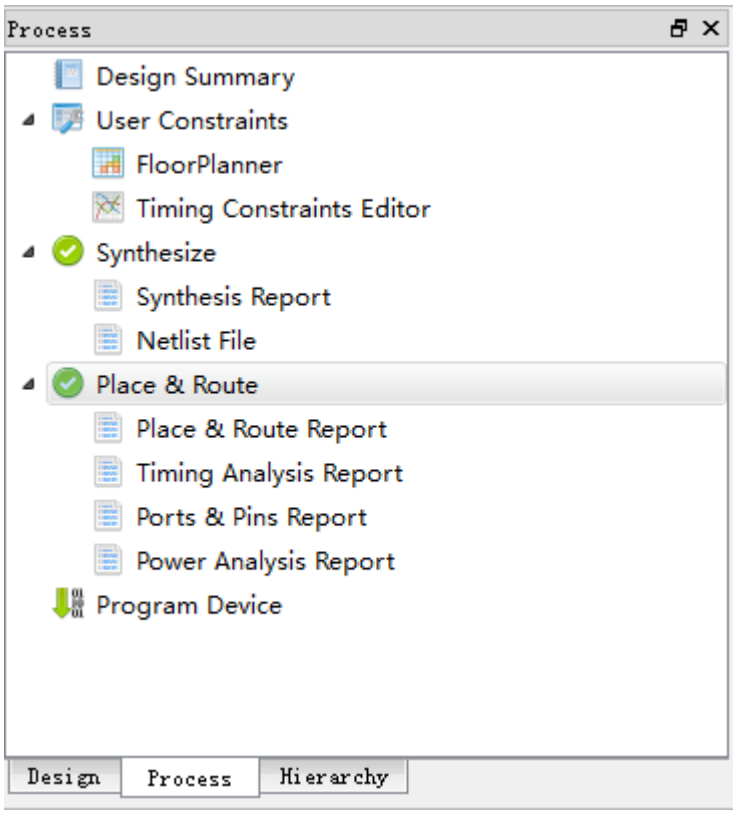


3.7.2 Run PnR

After parameters configuration, it can run PnR.

Double-click Place & Route in Process window to start PnR based on physical constraints, timing constraints, GAO config, GPA config. After PnR, the icon before the Place & Route changes to "", as shown in Figure 3-27.

Figure 3-27 Place & Route Completed



After PnR, the pnr folder is generated under the project creation path \impl, as shown in Figure 3-28. The folder contains all the files generated in PnR, including the bitstream file, the netlist file after PnR, and the output reports. For the details, refer to 3.11 Output Files.

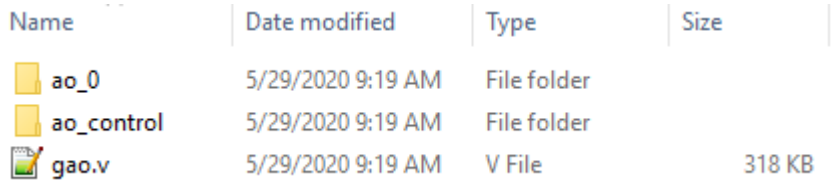
Figure 3-28 PnR Directory

Name	Date modified	Type	Size
ao_0.fs	9/9/2020 5:06 PM	FS File	3,476 KB
cmd.do	9/9/2020 5:05 PM	DO File	1 KB
device.cfg	9/9/2020 5:05 PM	CFG File	1 KB
MIPI_RX_TX.db	9/9/2020 5:06 PM	Data Base File	42 KB
MIPI_RX_TX.log	9/9/2020 5:06 PM	Text Document	3 KB
MIPI_RX_TX.pin.html	9/9/2020 5:06 PM	HTML Document	60 KB
MIPI_RX_TX.power.html	9/9/2020 5:06 PM	HTML Document	10 KB
MIPI_RX_TX.rpt.html	9/9/2020 5:06 PM	HTML Document	67 KB
MIPI_RX_TX.rpt.txt	9/9/2020 5:06 PM	Text Document	50 KB
MIPI_RX_TX.sdf	9/9/2020 5:06 PM	SDF File	2,668 KB
MIPI_RX_TX.timing_paths	9/9/2020 5:06 PM	TIMING_PATHS File	39 KB
MIPI_RX_TX.tr.html	9/9/2020 5:06 PM	HTML Document	1 KB
MIPI_RX_TX.vo	9/9/2020 5:06 PM	VO File	1,105 KB
MIPI_RX_TX_tr_cata.html	9/9/2020 5:06 PM	HTML Document	9 KB
MIPI_RX_TX_tr_content.html	9/9/2020 5:06 PM	HTML Document	1,192 KB

If the project contains the GAO config file, after PnR, gao file is generated under the project creation path \impl, as shown in Figure 3-29:

- ao_0 contains the parameter files and synthesis results of AO.
- ao_control contains the parameter files and synthesis results of the control AO.
- gao.v is the netlist file after GAO synthesis, encrypted.

Figure 3-29 GAO Directory



3.8 Timing Optimization

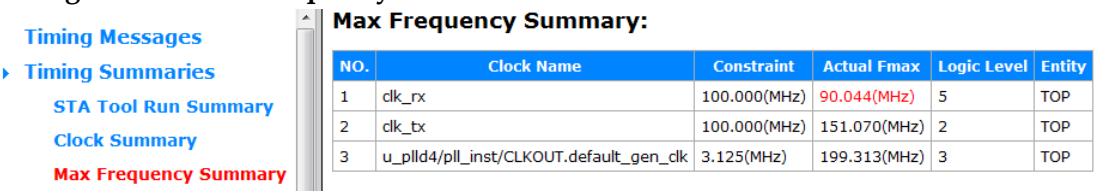
After PnR, you can use FloorPlanner to modify physical constraints and key path to help users realize timing closure to achieve timing optimization. For more details, see SUG935, Gowin Design Physical Constraints User Guide

It needs posp and timing path files for timing optimization when using FloorPlanner, and these two files are automatically generated in PnR.

3.8.1 Timing Analysis

After PnR, timing report will be generated. If the max. frequency does not meet requirements, as shown in Figure 3-30, the timing can be optimized by FloorPlanner.

Figure 3-30 Max. Frequency



3.8.2 Adjust Key Path

Start FloorPlanner and load posp and timing paths files, the setup and hold of timing path in Netlist window is as shown in Figure 3-31. It can highlight a path by changing "Chip Array" to "Show Place View > All Instance" as shown in Figure 3-32.

Figure 3-31 Timing Path

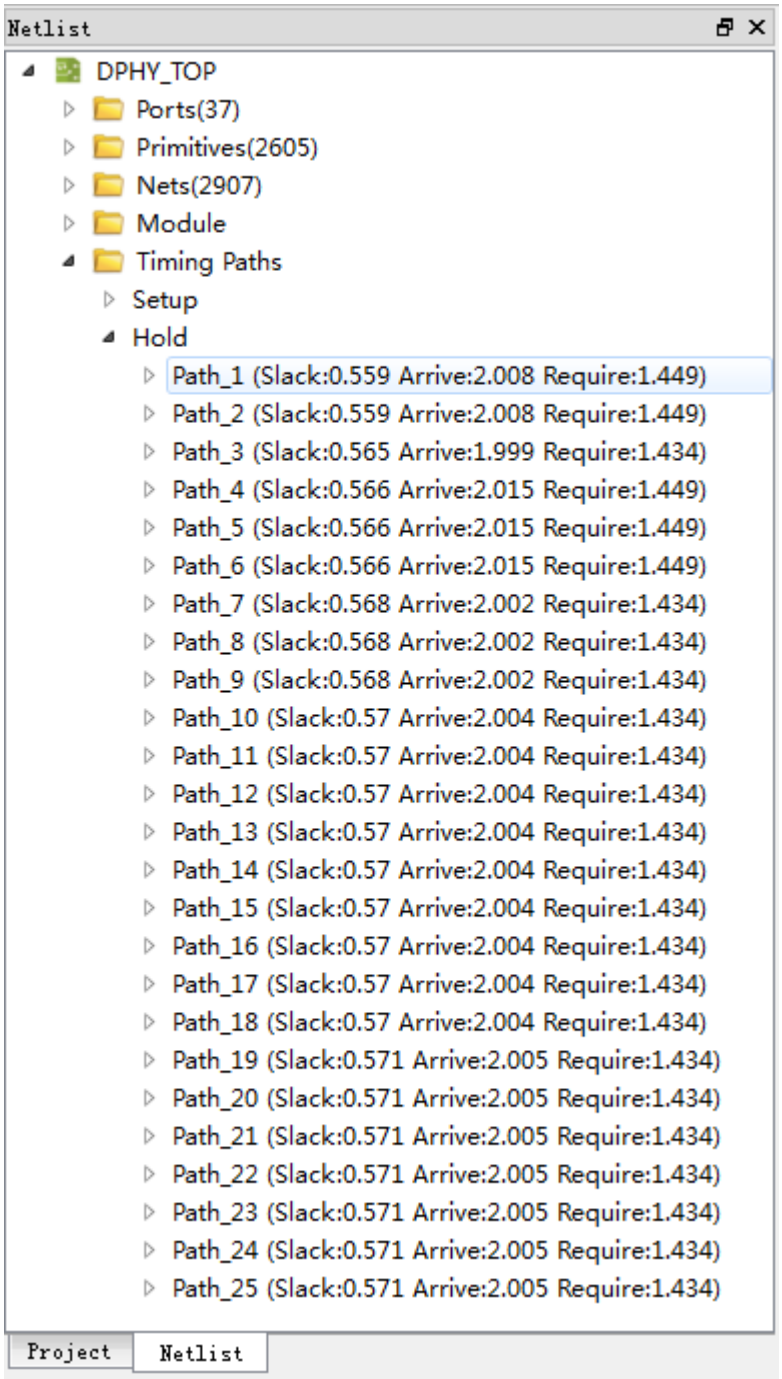
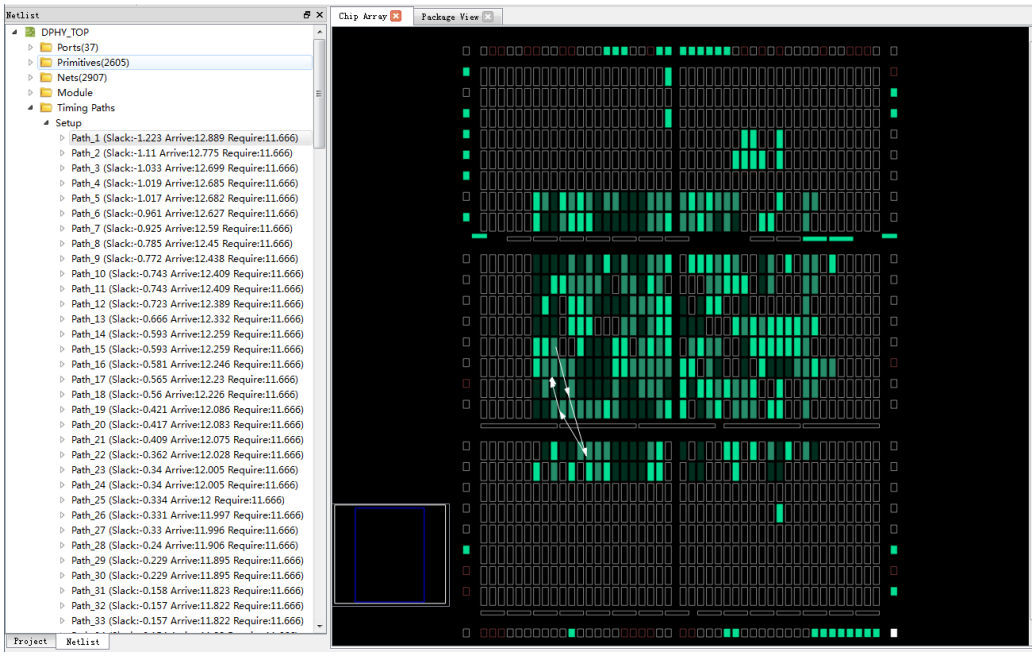


Figure 3-32 Timing Path Highlighted



After adjustment, click "Save" to finish as shown in Figure 3-33. After this adjustment, the timing optimization can be continued if the max. frequency still does not meet the design requirements.

Figure 3-33 Timing Path Adjusted

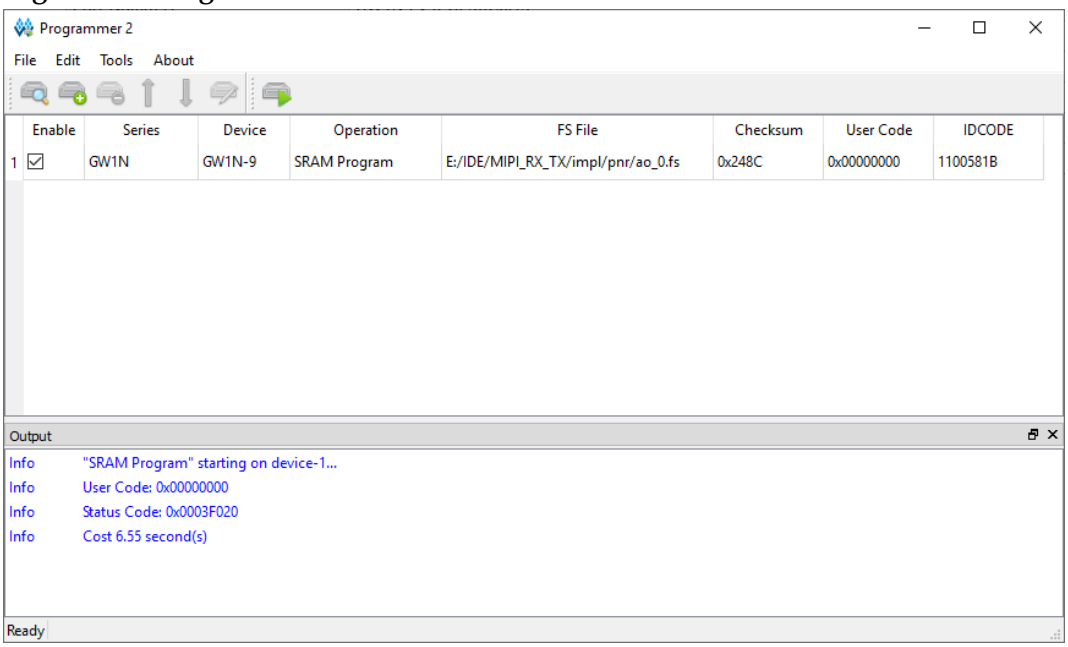
3.9 Download Bitstream

After optimization, the design can meet the timing requirements. Place & route to generate the bitstream file and download with Programmer to verify the design. For the usage, please see SUG502, Gowin Programmer User Guide.

Select "Process > Program Device" to open Programmer, and the

programmer automatically identifies the bitstream file. After the development board ready, click "Program/Configure"to download the bitstream to the development board. It is finished as shown in Figure 3-34.

Figure 3-34 Programmer

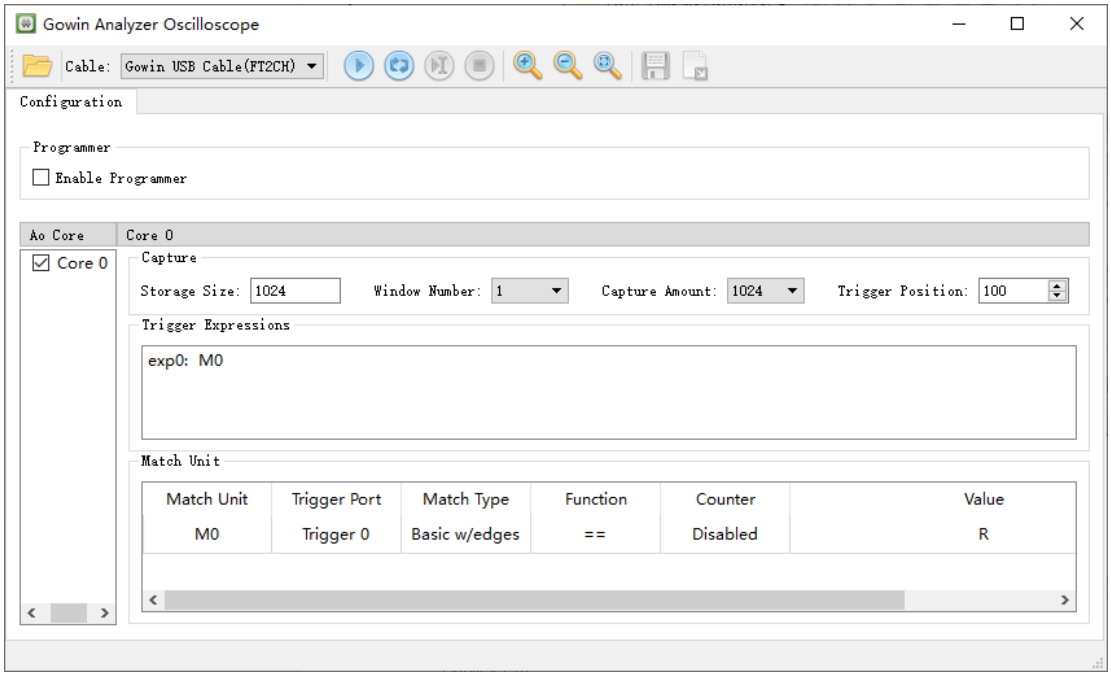


3.10 GAO Captures Data

After the bitstream is downloaded, GAO can verify the design. For the usage, refer to the SUG114, Gowin Analyzer Oscilloscope User Guide.

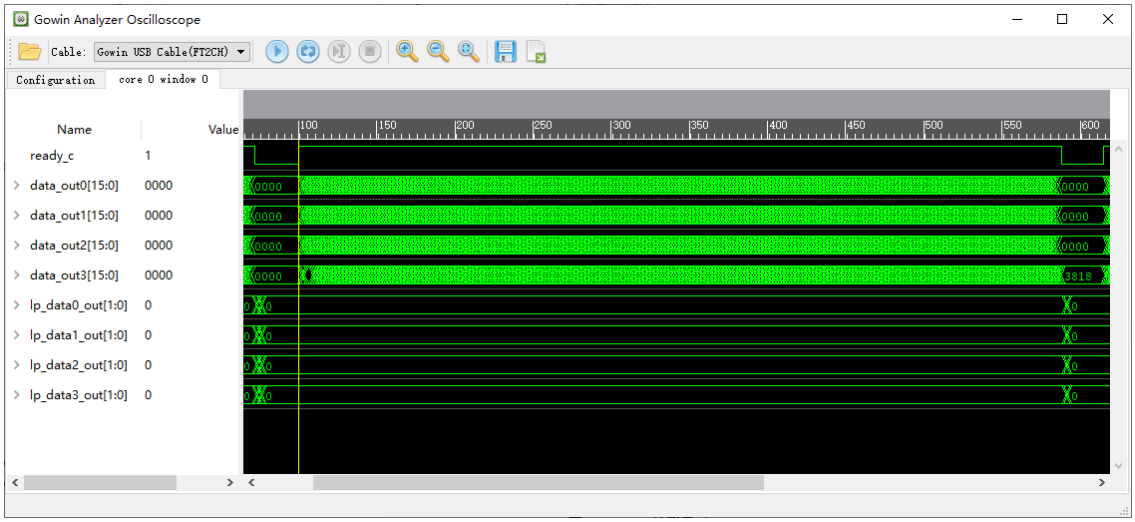
Click the GAO icon in the Gowin Software toolbar to open the GAO interface, which automatically identifies the GAO config file, as shown in Figure 3-35.

Figure 3-35 GAO Interface



Click Start icon in the GAO interface to capture data. After finished, GAO interface generates a window to display the waveform, as shown in Figure 3-36. The window supports cursor, zoom-out and so on, so as to facilitate the user to analyze the data.

Figure 3-36 GAO Waveform Display



3.11 Output Files

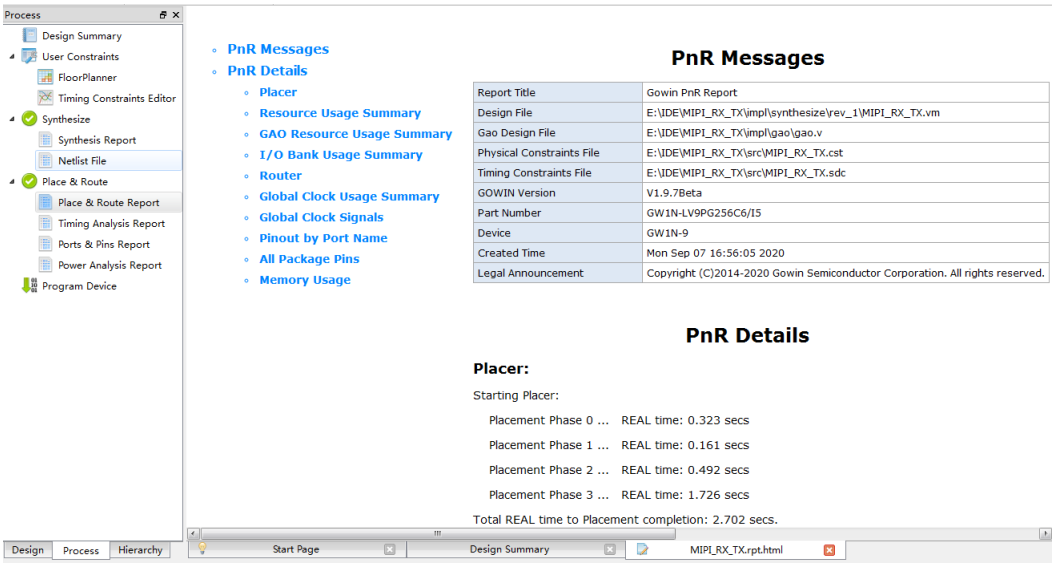
3.11.1 Place&Route Report

The Place&Route Report describes the resource, memory consumption, time consumption, etc. occupied by the user design, with the file suffix .rpt.html. Check the *.rpt.html file for further details.

Double-click "Place & Route Report" in the Process View to open Place & Route report, as shown in Figure 3-37.

For the details, refer to 6.2 Place & Route Report of SUG100 Gowin Software User Guide.

Figure 3-37 Place & Route Report



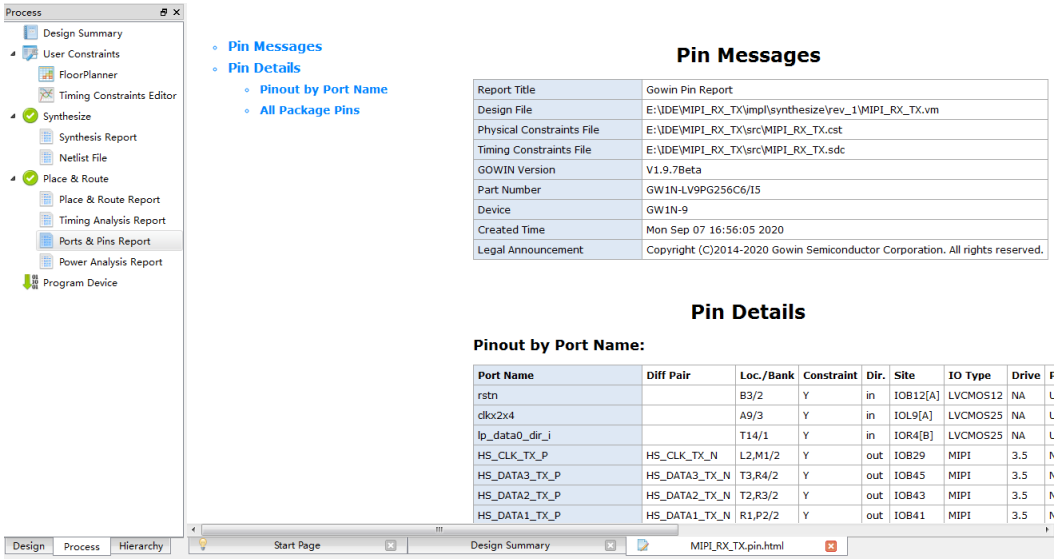
3.11.2 Ports and Pins Report

The Ports and Pins Report is the ports and pins files after placement. It includes ports type, attributes, and locations, etc. The generated file is saved with the .pin.html suffix. Check the .pin.html file for further details.

Double-click Ports & Pins Report in the Process View to open Ports & Pins Report, as shown in Figure 3-38.

For the details, refer to 6.3 Ports & Pins Report of SUG100 Gowin Software User Guide.

Figure 3-38 Ports & Pins Report



3.11.3 Timing Report

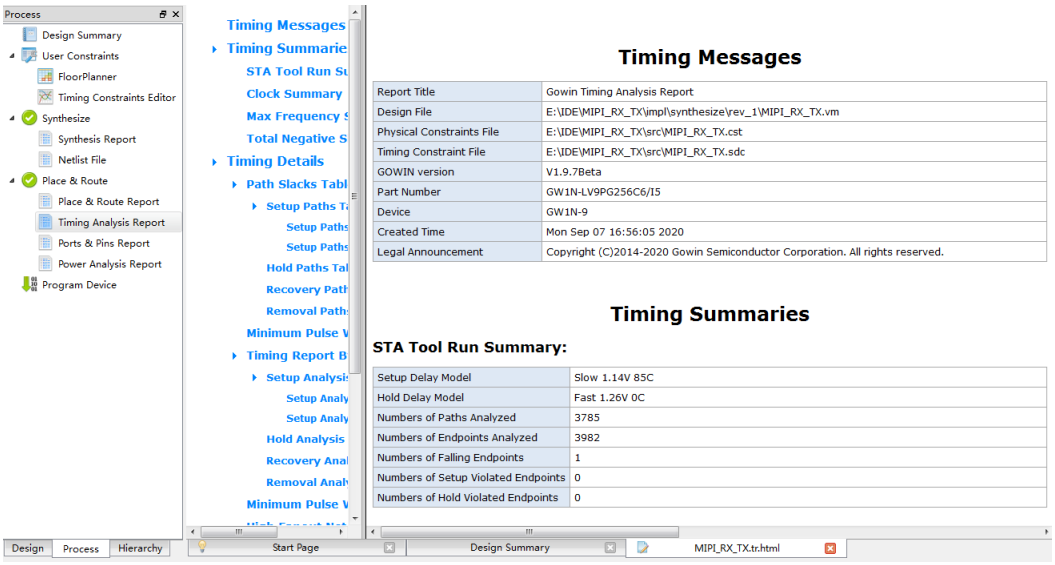
The timing report is available in web format and text format. The default is web format.

The Timing report includes set-up time check, hold-time check, restoring time check, removal time check, min. clock pulse check, max. fan out path, Place & Route congestion report, etc. by default. The timing report also includes the max. frequency report.

Double-click Timing Analysis Report in the Process View to open the timing analysis report for the project, as shown in Figure 3-39.

For the details, please refer to SUG940, Gowin Design Timing Constraints User Guide.

Figure 3-39 Timing Report



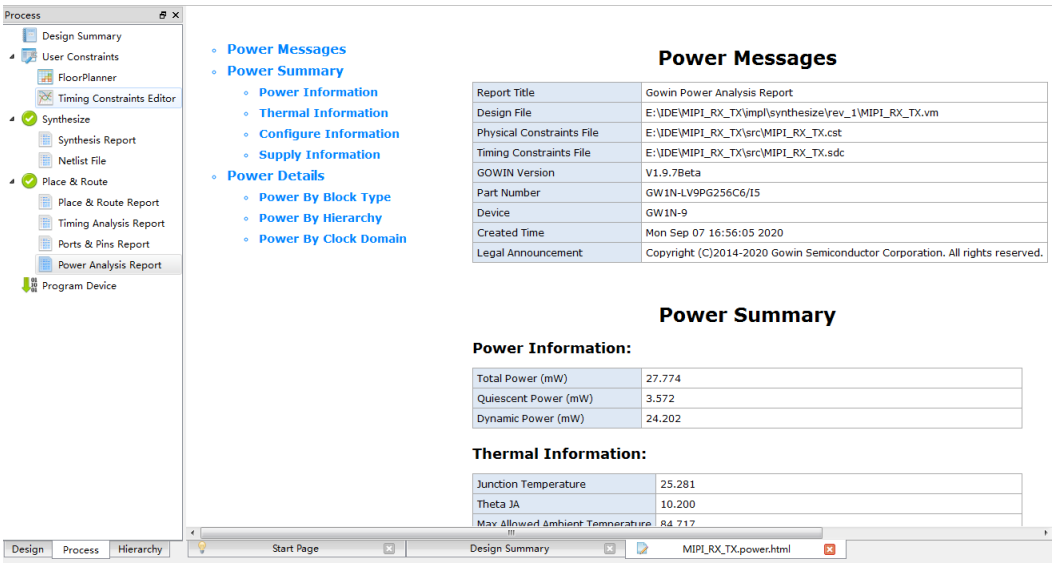
3.11.4 Power Analysis Report

The Power Analysis Report helps you evaluate the basic power consumption of your design.

Double-click Power Analysis Report in the Process View to open the power analysis report as shown in Figure 3-40.

For the details, please refer to chapter 4 Power Analysis Report of SUG282, Gowin Power Analysis User Guide.

Figure 3-40 Power Analysis Report

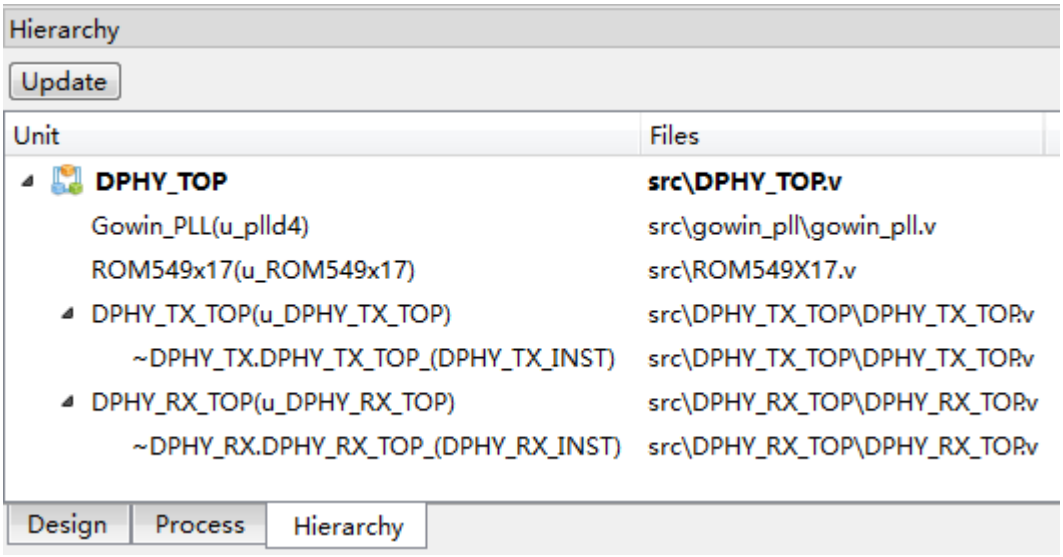


3.12 File Encryption

3.12.1 Source File Encryption

When you need to encrypt and protect source files, you can encrypt the selected module and its sub module through Hierarchy window, as shown in Figure 3-41. For details, see SUG100 Gowin Software User Guide.

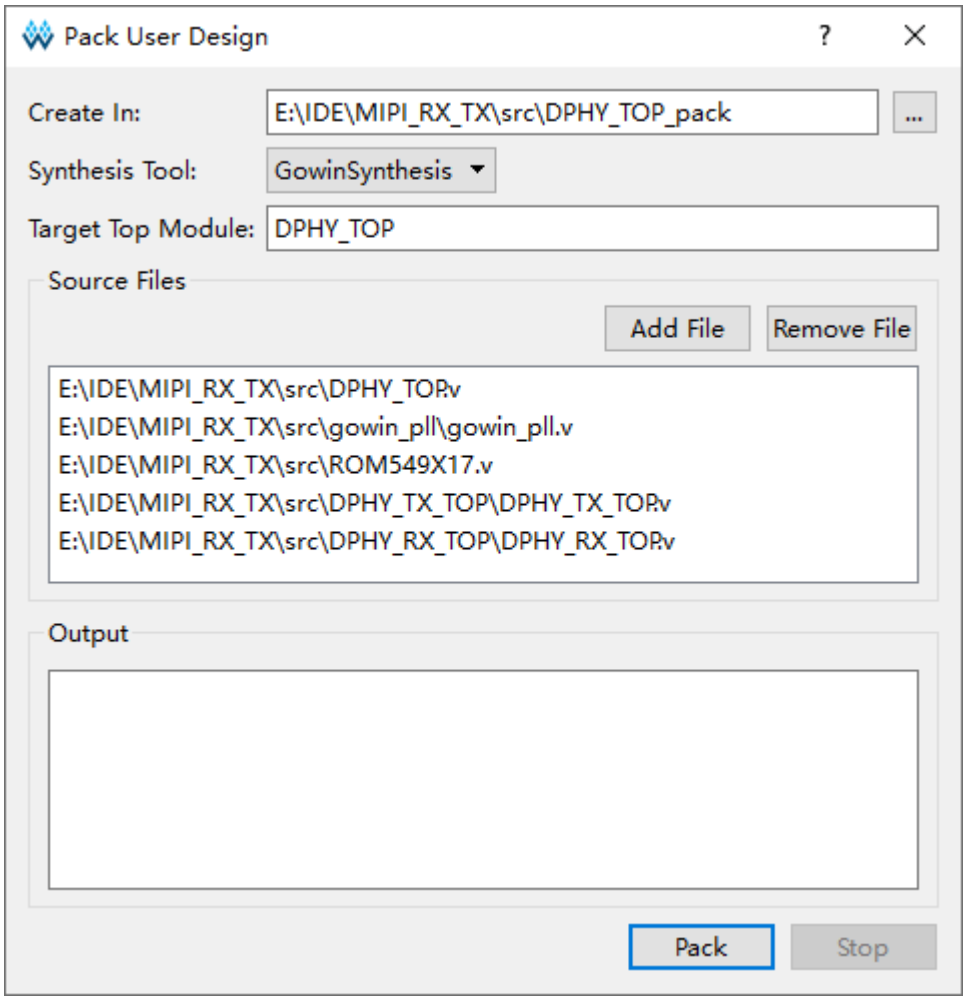
Figure 3-41 Hierarchy Window



Take module DPHY_TOP as an example to introduce the file encryption.

You can right-click DPHY_TOP in the Hierarchy window and select "Pack User Design" in the right-click list to open the window, as shown in Figure 3-42.

Figure 3-42 Pack User Design Window



Select GowinSynthesis and the Target Top Module displays DPHY_TOP. Click "Pack" to start encryption. The relevant information will be printed in the Output window.

After the encryption, two files are generated under the destination path (E:\IDE\MIPI_RX_TX\src\DPHY_TOP_pack): DPHY_TOP_gowin.vp and DPHY_TOP_sim.v.

- DPHY_TOP_gowin.vp: Encrypted files;
- DPHY_TOP_sim.v: flatted synthesized plaintext netlist filethat can be used for simulation.

3.12.2 Simulation File Encryption

The simulation file provided by Gowin is plaintext. In order to protect the simulation file, it can be encrypted by using third-party simulation software, such as Modelsim and vcs. Here it uses DPHY_TOP_sim.v as an example to introduce the encryption.

Encryption by Modelsim

When using modelsim, the steps to encrypt the simulation file are as follows:

1. Add macro `protect and `endprotect before and after the encrypted in the simulation file DPHY_TOP_sim.v;
2. Run command: Vlog +protect DPHY_TOP_sim.v;
3. After running the command, DPHY_TOP_sim.vp is generated in the work library, which is DPHY_TOP_sim.v encrypted file that can be used for modelsim simulation.

Encryption by vcs

When using vcs, the steps to encrypt the simulation file are as follows:

1. Add macro `protect128 and `endprotect128 before and after the encrypted in the simulation file DPHY_TOP_sim.v;
2. Run command: Vcs +v2k -protect128 DPHY_TOP_sim.v;
3. After running the command, DPHY_TOP_sim.vp is generated under the current path, which is DPHY_TOP_sim.v encrypted file that can be used for vcs simulation.

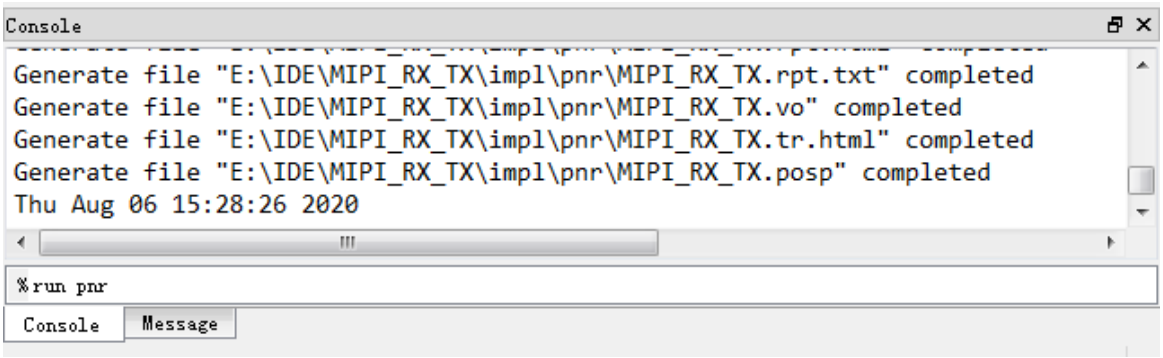
4 Tcl

It has introduced the usage of dsign GUI. The Gowin software also provides tcl for some settings. Taking MIPI design as an example, it introduces the usage of tcl. For the details, see Appendix A of SUG100 Gowin Software User Guide.

4.1 Tcl Edit Window

At the bottom of the Console is the tcl edit window, where you can enter the tcl command and press Enter to run,as shown in Figure 4-1.

Figure 4-1 tcl Edit Window



4.2 Tcl Quick Start

4.2.1 rm_file

rm_file is used to remove files. Here it will introduce tcl to remove the files from the project.

Remove ROM549X17.v and DPHY_TOP.v

rm_file src/ROM549X17.v src/DPHY_TOP.v

After running the command, the Console will display the prompt for removing files, and these two files will not appear in the Design window.

4.2.2 add_file

add_file is used to add files. Here it will introduce tcl to add the remved files to the project.

Add ROM549X17.v and DPHY_TOP.v

add_file src/ROM549X17.v src/DPHY_TOP.v

After running the command, the Console will display the prompt for adding files, and these two files will appear in the Design window.

4.2.3 set_file_enable

set_file_enable is used to set whether a file can be used. Here it will introduce tcl to set DPHY_TOP.v disable/enable.

Modify DPHY_TOP.v to disable

Set_file_enable src/DPHY_TOP.v false

After running the command, the Console will display the prompt for disabling the file and DPHY_TOP.v file is grayed out in Design window.

Modify DPHY_TOP.v to enable

Set_file_enable src/DPHY_TOP.v true

After running the command, the Console will display the prompt for enabling the file and DPHY_TOP.v file is available in Design window.

4.2.4 set_option

set_option is used to set options in the project. Here it will introduce tcl to configure synthesis and PnR parameters.

- Select Synplify Pro

  set_option -synthesis_tool synplify_pro
- Set TOP Module/Entity to DPHY_TOP

  set_option -top_module DPHY_TOP
- Set Number of Critical Paths to 0

  set_option -num_critical_paths 0
- Set Number of Start/End Points to 0

  set_option -num_startend_points 0
- Set Generate SDF File to True

  set_option -gen_sdf 1
- Set Generate Post-Place File to True

  set_option -gen_posp 1
- Set Generate Post-PNR Simulation Model File to True

  set_option -gen_sim_netlist 1
- Set Place input register to IOB to False

  set_option -ireg_in_iob 0
- Set Place output register to IOB to False

  set_option -oreg_in_iob 0
- Set Place inout register to IOB to False

  set_option -ioreg_in_iob 0

4.2.5 run

Run is used to run a flow or all flows. Here it will introduce tcl to run synthesis and PnR flows.

- Run synthesis
  Run syn
- Run PnR
  Run pnr

4.2.6 set_device

set_device is used to set the target device. Here it will introduce tcl to set GW1N-9C, GW1N-LV9PG256C6/I5 as the target device.

Set GW1N-9C, GW1N-LV9PG256C6/I5 as the target device.

Set_device -name GW1N-9C GW1N-LV9PG256C6/I5

After running the command, the Console will display the device.

4.2.7 saveto

saveto is used to save the current data to the tcl script, including device, design files, and flow options. Here it will introduce tcl to save the data.

Save the current data to mipi.tcl

saveto mipi.tcl

After running the command, the mipi.tcl file is generated in the path where the project files are located.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