Gowin HCLK User Guide

Overview

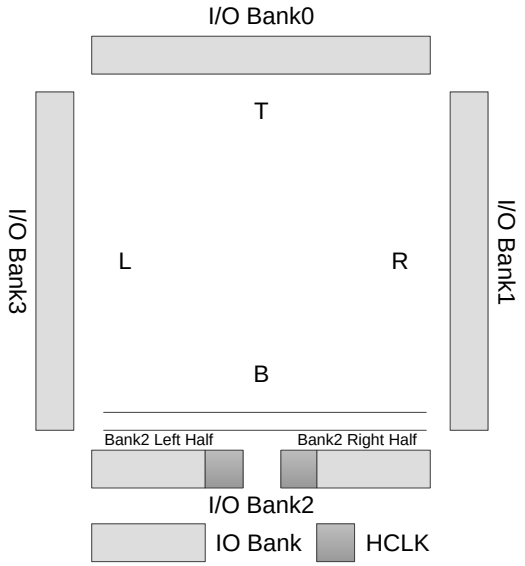
HCLK is the high-speed clock that is incorporated in GOWINSEMI FPGA products. It offers low jitter and low deviation performance, can support high-speed data transfer, and is suitable for source synchronous data transfer protocols. The output of the high-speed clock module is the input clock divided by 2, 3.5, 4, 5, or 8. The high-speed clock module also provides a clock for the I/O logic of IDES4, IVIDEO, IDES8, IDES10, IDES16, OSER4, OVIDEO, OSER8, OSER10, and OSER16.

GW1N-1

GW1N-1 has two HCLKs, which are located in Bank2, with one clock in each half. The HCLK located in the left half of Bank2 is only available for the I/O logic of the left bank, and the HCLK located in the right half of the bank is only available for the I/O logic in the right bank.

HCLK input signals can be sent from any bank to another.

Figure 1: GW1N-1 HCLK Distribution



There is no HCLK in Bank0, Bank1, and Bank3; however, a global clock can also provide the corresponding I/O logic clock.

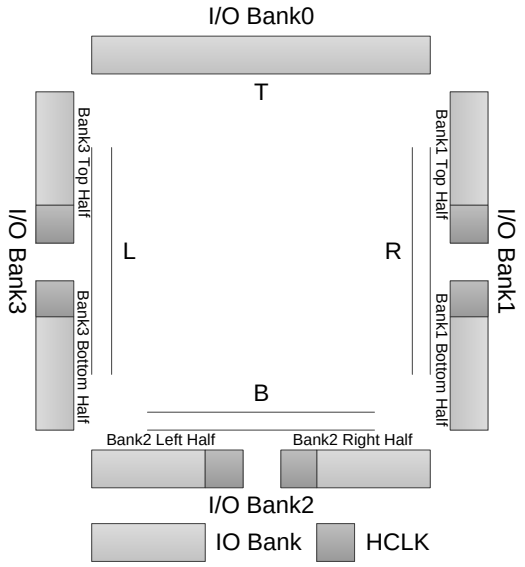
GW1NZ-1

The HCLK distribution and usage are the same as that of GW1N-1.

GW1N-4 / GW1NR-4

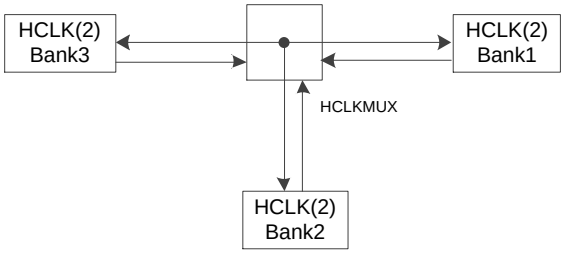
GW1N-4/GW1NR-4 have six HCLKs. Bank1, Bank2, and Bank3 have two HCLKs each. There is one HCLK in the upper half of Bank2 and one HCLK in the lower half. The HCLK that is located in the upper half of the bank is only available for the upper bank I/O logic. The HCLK that is located in the lower half of the bank is only available for the lower bank I/O logic. The HCLK usage of Bank2 and Bank3 is the same as that of Bank1.

Figure 2: GW1N-4/GW1NR-4 HCLK Distribution



GW1N-4 and GW1NR-4 provide HCLKMUX, which is used for HCLK bridging. HCLKMUX can send a HCLK clock input signal from Bank1, Bank2, and Bank3 to any other bank, which makes HCLK more flexible.

Figure 3: GW1N-4/GW1NR-4 HCLKMUX View

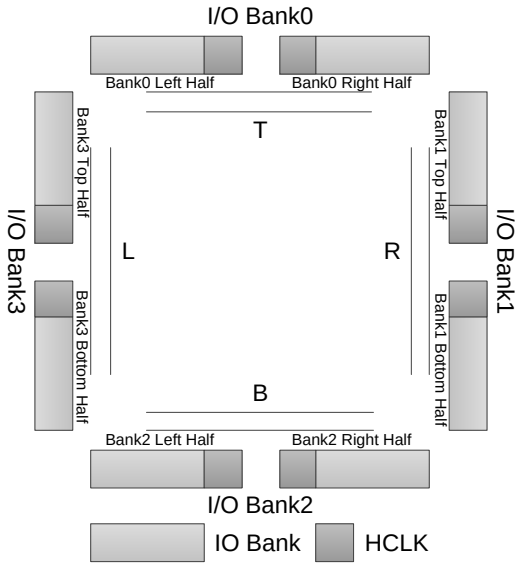


There is no HCLK in Bank0; however, a global clock can also provide the corresponding I/O logic clock.

GW1N-9 / GW1NR-9

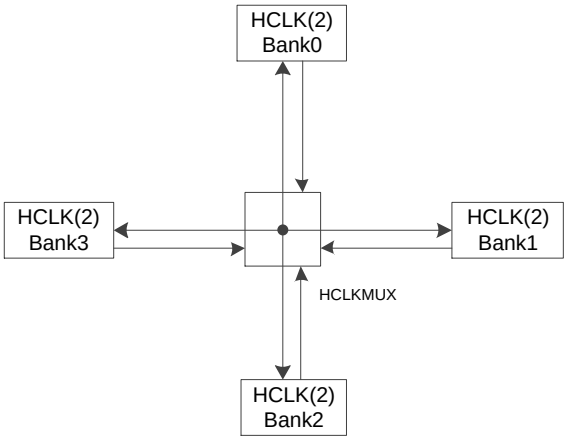
GW1N-9 and GW1NR-9 have eight HCLKs. Bank0, Bank1, Bank2, and Bank3 have two HCLKs each. Bank0 has one clock in each half. The HCLK located in the left half of Bank0 is only available for the I/O logic of the left bank, and the HCLK located in the right half of the bank is only available for the I/O logic in the right bank. The HCLK usage of Bank1, Bank2, and Bank3 is the same as that of Bank0.

Figure 4: GW1N-9/GW1NR-9 HCLK Distribution



GW1N-4 and GW1NR-4 provide HCLKMUX, which is used for HCLK bridging. HCLKMUX can send a HCLK clock input signal from Bank0, Bank1, Bank2, and Bank3 to any other bank, which makes the HCLK more flexible.

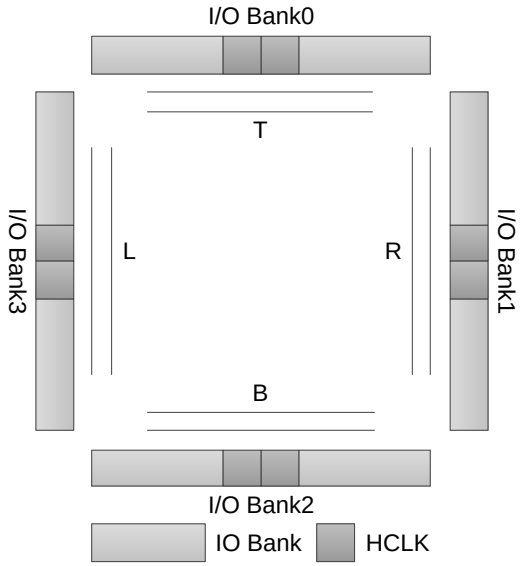
Figure 5: GW1N-9/GW1NR-9 HCLKMUX View



GW1NS-2

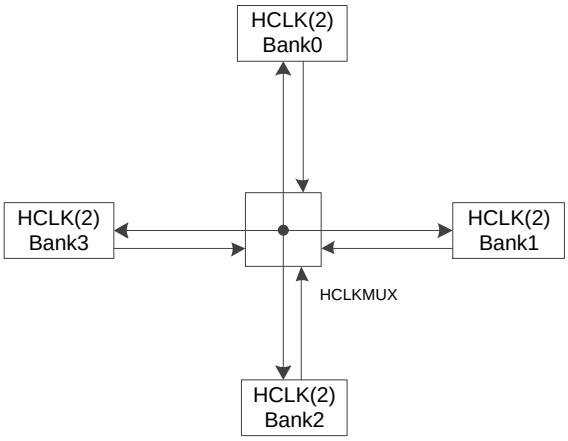
GW1NS-2 has eight HCLKs. Bank0, Bank1, Bank2, and Bank3 have two HCLKs each. The HCLK located in the left half of Bank0 is only available for the I/O logic of the left bank, and the HCLK located in the right half of the bank is only available for the I/O logic in the right bank. The HCLK usage of Bank1, Bank2, and Bank3 is the same as that of Bank0.

Figure 6: GW1NS-2 HCLK Distribution



GW1NS-2 offers HCLKMUX, which is used for HCLK bridging. HCLKMUX can send a HCLK clock input signal from any bank to another, which makes HCLK more flexible.

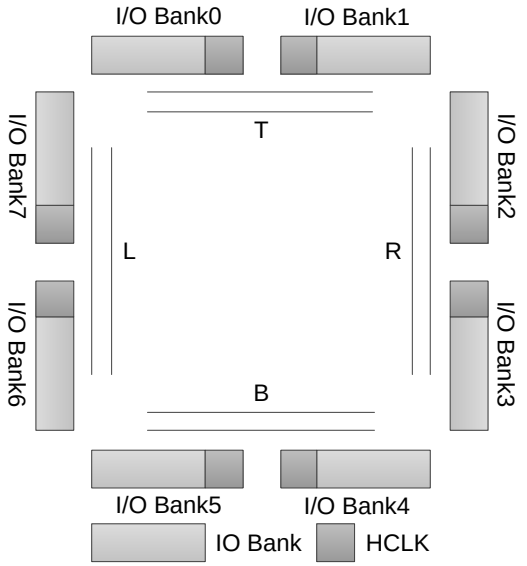
Figure 7: GW1NS-2 HCLKMUX View



GW2A-18 / GW2AR-18

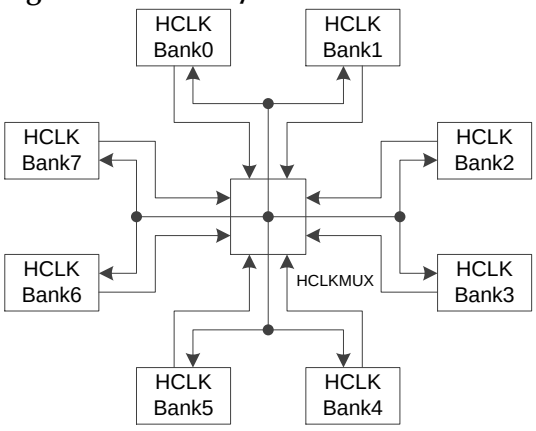
GW2A-18 and GW2AR-18 have eight HCLKs, located in Bank0, Bank1, Bank2, Bank3, Bank4, Bank5, Bank6, and Bank7 respectively. The HCLK located in Bank0 and Bank1 can be shared and are available for the I/O logic in Bank0 and Bank1. The HCLK usage of Bank2 and Bank3, Bank4 and Bank5, Bank6 and Bank7 is the same as that of Bank0 and Bank1.

Figure 8: GW2A-18/GW2AR-18 HCLK Distribution



GW2A-18 and GW2AR-18 offer HCLKMUX, which is used for HCLK bridging. HCLKMUX can send a HCLK clock signal between banks, which makes HCLK more flexible.

Figure 9: GW2A-18/GW2AR-18 HCLK Distribution



GW2A-55

The HCLK distribution and usage of the GW2A-55 are the same as that of GW2A-18.

Left/Right/Top/Bottom HCLK Resources of BANK

Table 1: TOP Left/Right HCLK Resources

Devices	LEFT_start	LEFT _end	RIGHT_start	RIGHT _end
GW1NS-2K	IOT2	IOT10	IOT11	IOT19
GW1N-1K	--	--	--	--
GW1N-4K	--	--	--	--
GW1N-9K	IOT2	IOT28	IOT29	IOT46
GW2A-18K	IOT2	IOT27	IOT30	IOT55
GW2A-55K	IOT2	IOT45	IOT48	IOT91

Table 2: BOTTOM Left/Right HCLK Resources

Devices	LEFT_start	LEFT _end	RIGHT_start	RIGHT _end
GW1NS-2K	IOB7	IOB10	IOB11	IOB19
GW1N-1K	IOB2	IOB10	IOB11	IOB19
GW1N-4K	IOB7	IOB19	IOB20	IOB37
GW1N-9K	IOB2	IOB28	IOB29	IOB46
GW2A-18K	IOB2	IOB27	IOB30	IOB55
GW2A-55K	IOB2	IOB45	IOB48	IOB91

Table 3: LEFT Top/Bottom HCLK Resources

Devices	UP_start	UP _end	DOWN _start	DOWN _end
GW1NS-2K	IOL2	IOL5	IOL7	IOL9
GW1N-1K	--	--	--	--
GW1N-4K	IOL2	IOL9	IOL11	IOL18
GW1N-9K	IOL2	IOL18	IOL20	IOL27
GW2A-18K	IOL2	IOL27	IOL29	IOL54

Devices	UP_start	UP _end	DOWN _start	DOWN _end
GW2A-55K	IOL2	IOL44	IOL46	IOL83

Table 4: RIGHT Top/Bottom HCLK Resources

Devices	UP_start	UP _end	DOWN _start	DOWN _end
GW1NS-2K	IOR2	IOR5	IOR7	IOR9
GW1N-1K	--	--	--	--
GW1N-4K	IOR2	IOR9	IOR11	IOR18
GW1N-9K	IOR2	IOR18	IOR20	IOR27
GW2A-18K	IOR2	IOR27	IOR29	IOR54
GW2A-55K	IOR2	IOR44	IOR46	IOR83

Examples and Explanation

HCLK Primitives

VHDL

```
COMPONENT CLKDIV
    GENERIC(
        DIV_MODE : STRING := "2";
        GSREN : STRING := "false"
    );
    PORT(
        HCLKIN : IN std_logic;
        RESETN : IN std_logic;
        CALIB:   In std_logic;
        CLKOUT : OUT std_logic
    );
end COMPONENT;
```

Verilog

```
module CLKDIV(HCLKIN, RESETN, CALIB, CLKOUT);
input HCLKIN;
input RESETN;
```

```
input CALIB;
output CLKOUT;
parameter DIV_MODE = "2";
parameter GSREN = "false";
endmodule
```

Port

Table 5: CLKDIV Port Signals

Port	Description
HCLKIN	Clock input
RESETN	Reset signal, active low
CALIB:	Dynamic signals adjustment; adjust output clock; used for frequency division of 3.5. The input value is "1".
CLKOUT	Clock output

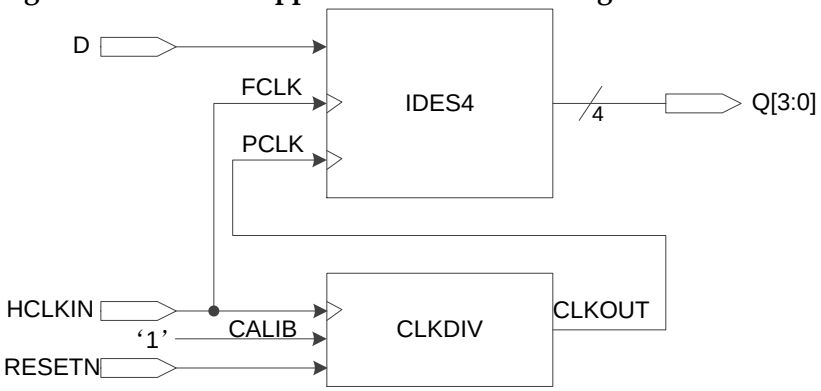
Parameters

Table 6: Description of CLKDIV Parameters

Parameter	Description	Default Value
DIV_MODE	Division factor: 2，3.5，4，5，8	2
GSREN	Global reset enable signal: False, true	false

Application Schematic Diagram

Figure 10: CLKDIV Application Schematic Diagram



Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

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Revision History

Date	Version	Description
01/05/2018	1.0E	Initial version published.
04/20/2018	1.1E	“Left/Right/Top/Bottom HCLK Resources of BANK” section added.

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