Gowin Configurable Function Unit (CFU)

User Manual

UG288-1.08E, 06/12/2018

Disclaimer

Revision History

Date	Version	Description
06/12/2018	1.0E	Initial version.

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1 About This Guide

1.1 Purpose

This guide mainly describes the CFU structure, operation modes, and usage.

1.2 Supported Products

The information in this guide applies to the following products:

1. GW2A series of FPGA products: GW2A-18, GW2A-55;
2. GW1N series of FPGA products: GW1N-1, GW1N-2, GW1N-4, GW1N-6, and GW1N-9;
3. GW2AR series of FPGA products: GW2AR-18.

1.3 Related Documents

The latest user guides are available on the Gowin Website. Refer to the related documents at www.gowinsemi.com:

1. GW2A series of FPGA Products Data Sheet
2. GW1N series of FPGA Products Data Sheet
3. GW2AR series of FPGA Products Data Sheet

1.4 Abbreviation and Terminology

Table 1-1 shows the abbreviations and terminologies used in this guide.

Table 1-1 Abbreviations and Terminologies

Abbreviation and Terminology	Full Name
CFU	Configurable Function Unit
LUT	Look-up Table
CRU	Configurable Routing Unit
RAM	Random Access Memory
ROM	Read Only Memory
CLS	Configurable Logic Slice
REG	Register
MUX2	Multiplexer 2:1

Abbreviation and Terminology	Full Name
ALU	Arithmetic Logic Unit
DFF	D Flip Flop
DL	Data Latch

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using any of the methods listed below.

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E-mail: support@gowinsemi.com

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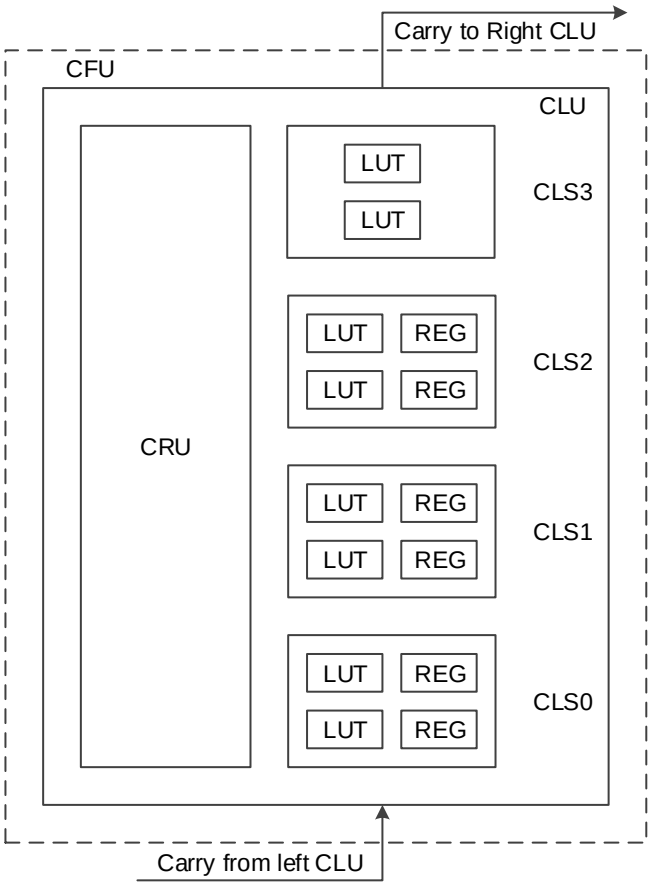
2 Configurable Function Unit

The configurable function unit (CFU) is the base cell for the array featured in GOWINSEMI FPGA products. Each CFU consists of a configurable logic unit (CLU) and its routing resource, the configurable routing unit (CRU). In each CLU, there are four configurable logic slices (CLS), three of which contain two four-input look-up-tables (LUT) and two registers (REG), with the remaining one containing two four-input LUT, as shown in Figure 2-1. The CLS can be configured in basic logic mode, ALU mode, random-access memory mode, and read-only memory mode according to the application scenarios.

Figure 2-1 Configurable Function Unit Structure View



2.1 CLU

The CLU supports three operation modes: Basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

Each LUT can be configured as one four-input LUT (LUT4) in its existing form. A higher input number of LUTs can be formed by combining the LUT4 together.

  - Each CLS can form one five-input LUT (LUT5).
  - 2 CLSs can form one six-input LUT (LUT6).
  - 4 CLSs can form one seven-input LUT (LUT7).
  - 8 CLSs (2 CLUs) can form one eight-input LUT (LUT8).

- ALU Mode

When combined with carry chain logic, LUTs can be configured in ALU mode to implement the following functions.

  - Adder and subtractor
  - Up/down counter
  - Comparator,including greater-than, less-than, and not-equal-to
  - MULT (Multiplier)

- Memory mode

GW1N-6, GW1N-9, GW2A-18, GW2A-55, and GW2AR-18 support this mode. In this mode, a 16 x 4 S-SRAM or ROM can be constructed by using CLSs.

This SRAM can be initialized during the device configuration stage. The initialization data can be generated in the bit stream file provided in the Gowin Yunyuan software.

Register

Each configurable logic slice (CLS) has two registers (REG), as shown in Figure2-2 below.

Figure2-2 Register in CFU

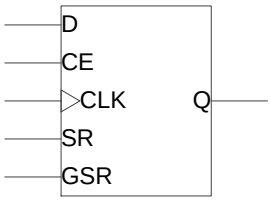


Table 2-1 Register Description in CFU

Signal	I/O	Description
D	I	Data input [1]
CE	I	CLK enable, can be high or low effective [2]
CLK	I	Clock, can be rising edge or falling edge trigging [2]

Signal	I/O	Description
SR	I	Set/Reset, can be configured as [2]: ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSR[3,4]	I	Global Set/Reset, can be configured as[4]: ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Register

Note!

- [1] The source of D can be the output of the LUT, or the input of the CRU, so the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU are independent.
- [3] In the case of GOWINSEMI FPGA products,GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

2.2 CRU

The main functions of the CRU are as following:

- Input selection: select input signals for the CFU.
- Configurable routing: connect the input and output of the CFUs, including inside CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

3CFU Primitives Call and Implementation

3.1 LUT1/LUT2/LUT3/LUT4

LUT1/LUT2/LUT3/LUT4 can be implemented by one four-input LUT4. Figure 3-1 shows the basic structure and signal definition.

Figure 3-1 LUT1/LUT2/LUT3/LUT4 Structure View

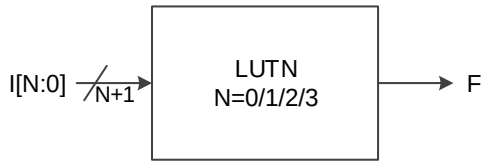


Table 3-1 LUT1/LUT2/LUT3/LUT4 Signal Definition

Signal	Input/Output	Description
I[0:0]/ I[1:0]/ I[2:0]/ I[3:0]	I	Look-up table input
F	O	Look-up table output

INIT can be used to define the corresponding output values of different input combinations, for example:

- LUT1 has two input combinations
- LUT2 has four input combinations
- LUT3 has eight input combinations
- LUT4 has sixteen input combinations

3.2 LUT5/LUT6/LUT7/LUT8

Larger look-up tables can be implemented by using smaller look-up tables and MUX2. Figure 3-2 shows the basic structure and signal definition.

Figure 3-2 LUT5/LUT6/LUT7/LUT8 Structure View

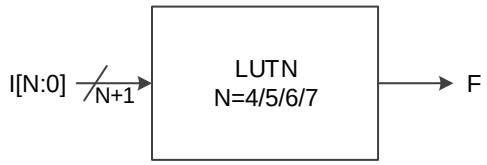


Table 3-2 LUT5/LUT6/LUT7/LUT8 Signal Definition

Signal	Input/Output	Description
I[4:0]/ I[5:0]/ I[6:0]/ I[7:0]	I	Look-up table input
F	O	Look-up table output

INIT can be used to define the corresponding output values of different input combinations, such as:

- LUT5 has 32 input combinations
- LUT6 has 64 input combinations
- LUT7 has 128 input combinations
- LUT8 has 256 input combinations

3.3 DFF

In synchronous circuit design, the clock pulse is used as the control signal. The circuit is triggered only when the clock pulse is received, and the output changes based on the input. Figure 3-3 shows the basic structure and signal definition.

Figure 3-3 DFF Structure View

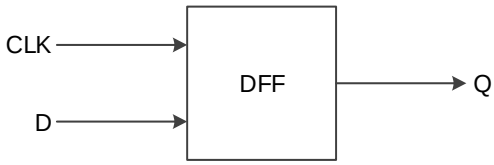


Table 3-3 DFF Signal Definition

Signal	Input/Output	Description
Q	O	Port Q output of DFF
D	I	Port D input of DFF
CLK	I	Clock pulse input

INIT is used to define the DFF output of port Q in the state of power-on reset.

3.4 DL

DL is a kind of memory unit circuit and changes its status under specified input pulse. Figure 3-4 shows the basic structure and signal definition of DL.

Figure 3-4 DL Structure View

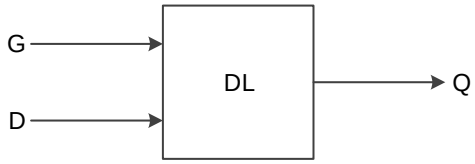


Table 3-4 DL Signal Definition

Signal	Input/Output	Description
Q	O	Port Q output of DL
D	I	Port D input of DL
G	I	Pulse input of DL

INIT is used to define the DL output of port Q in the state of power-on reset.

3.5 ALU

ALU can be used to implement multiple arithmetic and logic operation. Figure 3-5 shows the basic structure and signal definition.

Figure 3-5 ALU Structure View

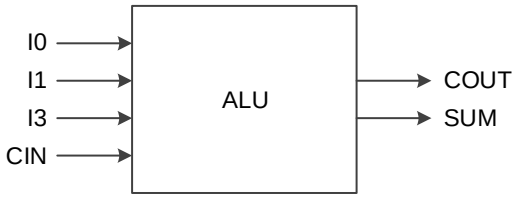


Table 3-5 ALU Signal Definition

Signal	Input/Output	Description
I0	I	Arithmetic logic unit operand input
I1	I	Arithmetic logic unit operand input
I3	I	Arithmetic logic unit select input
CIN	I	Arithmetic logic unit operand input
SUM	O	Arithmetic logic unit operation result output
COUT	O	Arithmetic logic unit operand output

ALU_MODE is used to define the ALU operation modes. Table 3-6 lists the ALU operations of the different working modes.

Table 3-6 ALU Operation Modes

Attribute ALU_MODE	Operation Modes
ADD 0	Add two operands
SUB 1	Subtract two operands
ADDSUB 2	Add and Subtract two operands, selected by I3. 1: addition; 0: subtraction
NE 3	Not equal to comparison of two operands
GE 4	Greater than or equal to comparison of two operands
LE 5	Less than or equal to comparison of two operands
CUP 6	Accumulator of single operand
CDN 7	Continuous subtraction of single operand
CUPCDN 8	Accumulator and continuous subtraction of single operand, selected by I3. 1: Accumulator; 0: Continuous subtraction
MULT 9	Multiplication of two operands

3.6 RAM16S1/RAM16S2/RAM16S4

Shadow single-port SRAM can be configured as single-port RAM with a depth of 16 and data width of 1/2/4. Figure 3-6 and Table 3-7 show the basic structure and signal definition.

Figure 3-6 Shadow Single-port SRAM Structure View

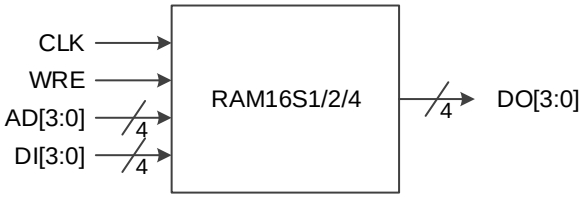


Table 3-7 Shadow Single-port SRAM Signal Definition

Signal	Input/Output	Description
CLK	I	Clock pulse input
WRE	I	Read/write enable control, 1 means "write", and 0 means "read"
AD[3:0]	I	4-bit address input
DI[3:0]	I	1/2/4-bit write data input
DO[3:0]	O	1/2/4-bit read data output

INIT_0/INIT_1/INIT_2/INIT_3 is used to assign the initialization file of shadow SRAM.

3.7 RAM16SDP1/RAM16SDP2/RAM16SDP4

The shadow semi dual port SRAM can be configured as a semi dual port RAM with a depth of 16 and data width of 1/2/4. Figure 3-7 and Table 3-8 show the basic structure and signal definition.

Figure 3-7 Shadow Semi Dual port SRAM Structure View

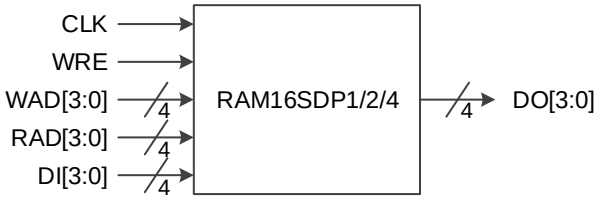


Table 3-8 Shadow Semi Dual port SRAM Signal Definition

Signal	Input/Output	Description
CLK	I	Clock pulse input
WRE	I	Read/write enable control, 1 means "write", and 0 means "read"
WAD[3:0]	I	4bit write address Input
DI[3:0]	I	1/2/4bit write data input
RAD[3:0]	I	4bit read address input
DO[3:0]	O	1/2/4bit read data output

INIT_0/1/2/3 is used to assign the initialization file of shadow SRAM.

3.8 ROM16

A single four-input LUT can be configured as ROM with the depth of 16 and data width of 1. Figure 3-8 and Table 3-9 shows the basic structure and signal definition.

Figure 3-8 Shadow ROM Structure View

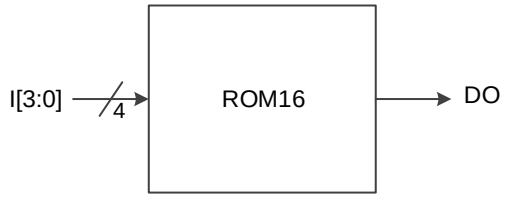


Table 3-9 Shadow ROM Signal Definition

Signal	Input/Output	Description
DO	O	1-bit data output
I[3:0]	I	4-bit address input

INIT_0 is used to assign the initialization file to the shadow SRAM.

4Shadow SRAM Initialization

4.1 Initialization File Format

The initialization file is used to initialize the memory space array for the shadow memory. The initialization is predominantly in the binary, hex, and hex including address information format.

4.2 Binary File

The binary file contains data only, which is arranged in row order in binary format. The binary file does not contain address information. An example of a binary initialization file with a depth of 16 and data width of 8 is as follows:

01010101
10101010
01010101
10101010
01010101
10101010
01010101
10101010
01010101
10101010
01010101
10101010
01010101
10101010
01010101
10101010

4.3 Hex File

The hex file contains data only, which is arranged in row order in hex format. The hex file does not contain address information. An example of a hex initialization file with a depth of 16 and data width of 8 is as follows:

```
55
AA
55
AA
55
AA
55
AA
55
AA
55
AA
55
AA
55
AA
```

4.4 Hex File with Address

The hex file with address arranges the address information and data in hex format. An example of an address hex initialization file with a depth of 16 and data width of 8 is as follows:

```
0:55
1:AA
2:55
3:AA
4:55
5:AA
6:55
7:AA
8:55
9:AA
A:55
```

B:AA

C:55

D:AA

E:55

F:AA

5 Design Considerations and Usage

5.1 Generic Attributes of the CFU

- You can use the physical constraints editor that is integrated in the Gowin Yunyuan software to lock LUT, ALU, registers, shadow RAM, or shadow ROM to the specified CFU or CLS. Syntax:

  INS_LOC "xxx" R2C2[0][A]

  NET_LOC "xxx" R8C8

- Define CFU usage rate using the physical constraints editor integrated in Gowin Yunyuan software. Syntax:

  UTIL R[2:5]C[3:8] 80%

- Define CFU with specified location using the physical constraints editor integrated in Gowin Yunyuan software. Syntax:

  LOC_RESERVE R6C6

5.2 Dedicated Attributes of the CFU

- Various devices have different matrix arrays of different sizes; for example:
  - The array size of GW1N-1 is 8 x 18;
  - The array size of GW1N-2 is 8 x 36;
  - The array size of GW1N-4 is 16 x 36;
  - The array size of GW2A-18 is 56 x 58;
  - The array size of GW2A-55 is 76 x 90;
  - The array size of GW2AR-18 is 56 x 58.
- GW2A-18, GW2A-55, GW2AR-18, GW1N-6, and GW1N-9 support shadow RAM and ROM.
- Registers can be placed in the CFU or IO cell.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